

TOSHIBA Field Effect Transistor Silicon P, N Channel MOS Type (U-MOS IV / U-MOS III)

TPCF8402

Portable Equipment Applications
 Motor Drive Applications
 DC-DC Converter Applications

- Low drain-source ON resistance : P Channel $R_{DS(ON)} = 60 \text{ m}\Omega$ (typ.)
 N Channel $R_{DS(ON)} = 38 \text{ m}\Omega$ (typ.)
- High forward transfer admittance : P Channel $|Y_{fs}| = 5.9 \text{ S}$ (typ.)
 N Channel $|Y_{fs}| = 6.8 \text{ S}$ (typ.)
- Low leakage current : P Channel $I_{DSS} = -10 \text{ }\mu\text{A}$ ($V_{DS} = -30 \text{ V}$)
 N Channel $I_{DSS} = 10 \text{ }\mu\text{A}$ ($V_{DS} = 30 \text{ V}$)
- Enhancement-mode
 : P Channel $V_{th} = -0.8 \text{ to } -2.0 \text{ V}$ ($V_{DS} = -10 \text{ V}$, $I_D = -1\text{mA}$)
 N Channel $V_{th} = 1.3 \text{ to } 2.5 \text{ V}$ ($V_{DS} = 10 \text{ V}$, $I_D = 1\text{mA}$)

Absolute Maximum Ratings ($T_a = 25^\circ\text{C}$)

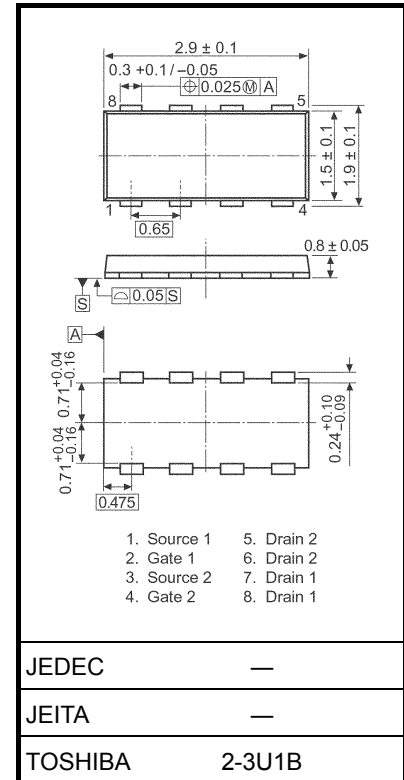
Characteristics		Symbol	Rating		Unit
Drain-source voltage		V_{DSS}	-30	30	V
Drain-gate voltage ($R_{GS} = 20 \text{ k}\Omega$)		V_{DGR}	-30	30	V
Gate-source voltage		V_{GSS}	± 20	± 20	V
Drain current	DC (Note 1)	I_D	-3.2	4.0	A
	Pulse (Note 1)	I_{DP}	-12.8	16.0	
Drain power dissipation ($t = 5 \text{ s}$) (Note 2a)	Single-device operation (Note 3a)	$P_D(1)$	1.35	1.35	W
	Single-device value at dual operation (Note 3b)	$P_D(2)$	1.12	1.12	
Drain power dissipation ($t = 5 \text{ s}$) (Note 2b)	Single-device operation (Note 3a)	$P_D(1)$	0.53	0.53	W
	Single-device value at dual operation (Note 3b)	$P_D(2)$	0.33	0.33	
Single pulse avalanche energy (Note 4)		E_{AS}	0.67	2.6	mJ
Avalanche current		I_{AR}	-1.6	2.0	A
Repetitive avalanche energy Single-device value at dual operation (Note 2a, 3b, 5)		E_{AR}	0.11		mJ
Channel temperature		T_{ch}	150		$^\circ\text{C}$
Storage temperature range		T_{stg}	-55 to 150		$^\circ\text{C}$

Note: For Notes 1 to 5, refer to the next page.

Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings. Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

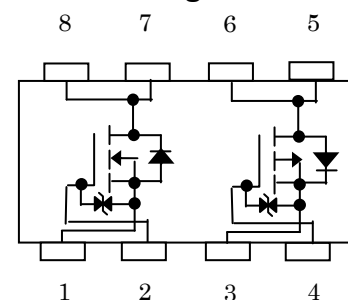
This transistor is an electrostatic-sensitive device. Handle with caution.

Unit: mm



Weight: 0.011 g (typ.)

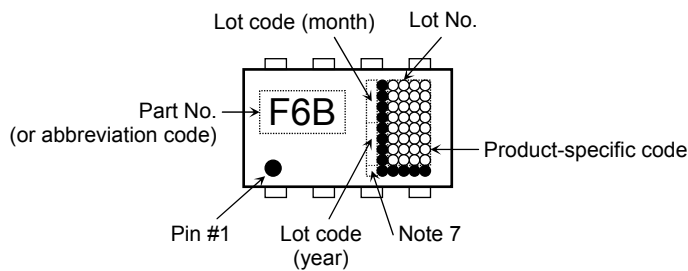
Circuit Configuration



Thermal Characteristics

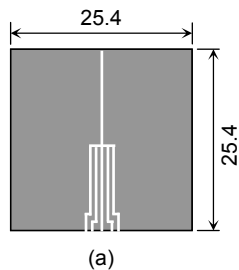
Characteristics		Symbol	Max	Unit
Thermal resistance, channel to ambient (t = 5 s) (Note 2a)	Single-device operation (Note 3a)	R _{th} (ch-a) (1)	92.6	°C/W
	Single-device value at dual operation (Note 3b)	R _{th} (ch-a) (2)	111.6	
Thermal resistance, channel to ambient (t = 5 s) (Note 2b)	Single-device operation (Note 3a)	R _{th} (ch-a) (1)	235.8	°C/W
	Single-device value at dual operation (Note 3b)	R _{th} (ch-a) (2)	378.8	

Marking (Note 6)

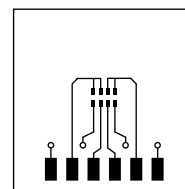


Note 1: Ensure that the channel temperature does not exceed 150°C.

Note 2: (a) Device mounted on a glass-epoxy board (a) (b) Device mounted on a glass-epoxy board (b)



FR-4
25.4 × 25.4 × 0.8
(Unit: mm)



FR-4
25.4 × 25.4 × 0.8
(Unit: mm)

Note 3: a) The power dissipation and thermal resistance values are shown for a single device. (During single-device operation, power is only applied to one device.)

b) The power dissipation and thermal resistance values are shown for a single device. (During dual operation, power is evenly applied to both devices.)

Note 4: P Channel: V_{DD} = -24 V, T_{ch} = 25°C (initial), L = 0.2 mH, R_G = 25 Ω, I_{AR} = -1.6 A
N Channel: V_{DD} = 24 V, T_{ch} = 25°C (initial), L = 0.5 mH, R_G = 25 Ω, I_{AR} = 2.0 A

Note 5: Repetitive rating: Pulse width limited by maximum channel temperature.

Note 6: “●” on the lower left of the marking indicates Pin 1.

Note 7 A dot marking identifies the indication of product Labels.
Without a dot: [[Pb]]/INCLUDES > MCV
With a dot: [[G]]/RoHS COMPATIBLE or [[G]]/RoHS [[Pb]]

Please contact your TOSHIBA sales representative for details as to environmental matters such as the RoHS compatibility of Product. The RoHS is the Directive 2002/95/EC of the European Parliament and of the Council of 27 January 2003 on the restriction of the use of certain hazardous substances in electrical and electronic equipment.

P-channel

Electrical Characteristics (Ta = 25°C)

Characteristics		Symbol	Test Condition	Min	Typ.	Max	Unit
Gate leakage current		I_{GSS}	$V_{GS} = \pm 16 \text{ V}, V_{DS} = 0 \text{ V}$	—	—	± 10	μA
Drain cut-off current		I_{DSS}	$V_{DS} = -30 \text{ V}, V_{GS} = 0 \text{ V}$	—	—	-10	μA
Drain-source breakdown voltage		$V_{(BR)DSS}$	$I_D = -10 \text{ mA}, V_{GS} = 0 \text{ V}$	-30	—	—	V
		$V_{(BR)DSX}$	$I_D = -10 \text{ mA}, V_{GS} = 20 \text{ V}$	-15	—	—	
Gate threshold voltage		V_{th}	$V_{DS} = -10 \text{ V}, I_D = -1 \text{ mA}$	-0.8	—	-2.0	V
Drain-source ON resistance		$R_{DS(ON)}$	$V_{GS} = -4.5 \text{ V}, I_D = -1.6 \text{ A}$	—	80	105	m Ω
			$V_{GS} = -10 \text{ V}, I_D = -1.6 \text{ A}$	—	60	72	
Forward transfer admittance		$ Y_{fs} $	$V_{DS} = -10 \text{ V}, I_D = -1.6 \text{ A}$	2.9	5.9	—	S
Input capacitance		C_{iss}	$V_{DS} = -10 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$	—	600	—	pF
Reverse transfer capacitance		C_{rss}		—	60	—	
Output capacitance		C_{oss}		—	70	—	
Switching time	Rise time	t_r		—	5.3	—	ns
	Turn-on time	t_{on}		—	12	—	
	Fall time	t_f		—	8.4	—	
	Turn-off time	t_{off}		—	34	—	
Total gate charge (gate-source plus gate-drain)		Q_g	$V_{DD} \approx -24 \text{ V}, V_{GS} = -10 \text{ V}, I_D = -3.2 \text{ A}$	—	14	—	nC
Gate-source charge 1		Q_{gs1}		—	1.4	—	
Gate-drain ("miller") charge		Q_{gd}		—	2.7	—	

Source-Drain Ratings and Characteristics (Ta = 25°C)

Characteristics		Symbol	Test Condition	Min	Typ.	Max	Unit
Drain reverse current	Pulse (Note 1)	I_{DRP}	—	—	—	-12.8	A
Forward voltage (diode)		V_{DSF}	$I_{DR} = -3.2 \text{ A}, V_{GS} = 0 \text{ V}$	—	—	1.2	V

N-channel

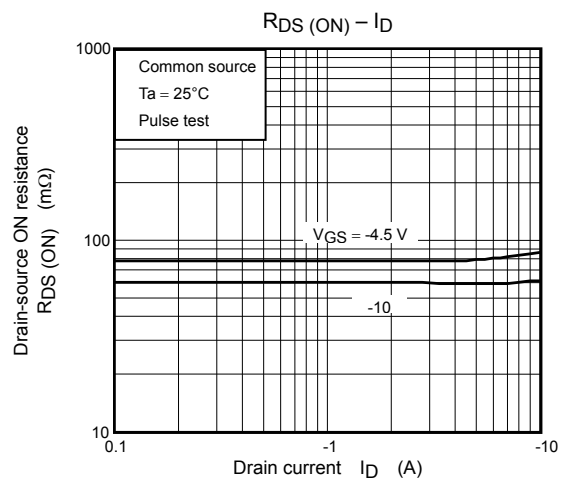
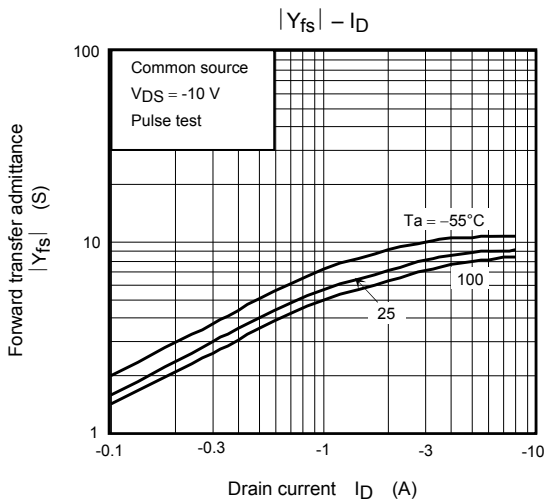
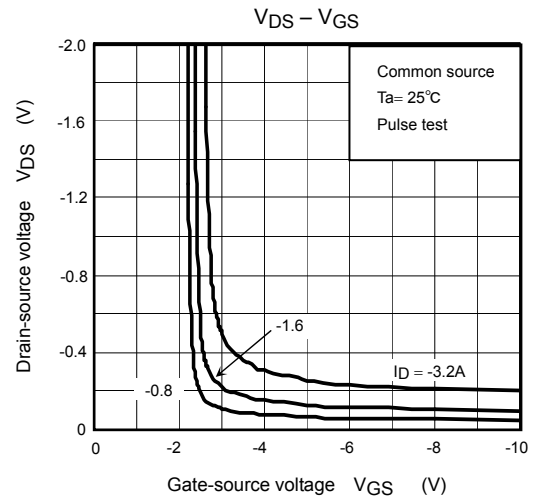
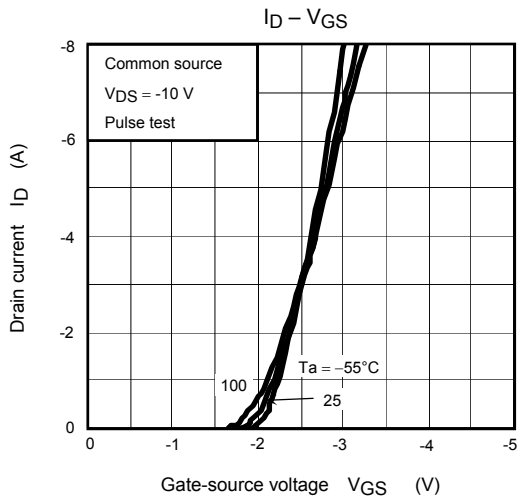
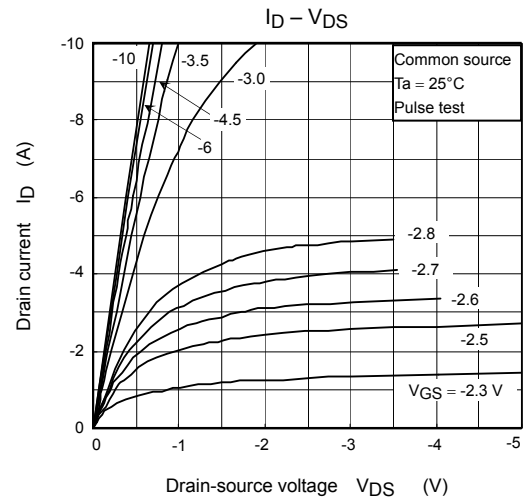
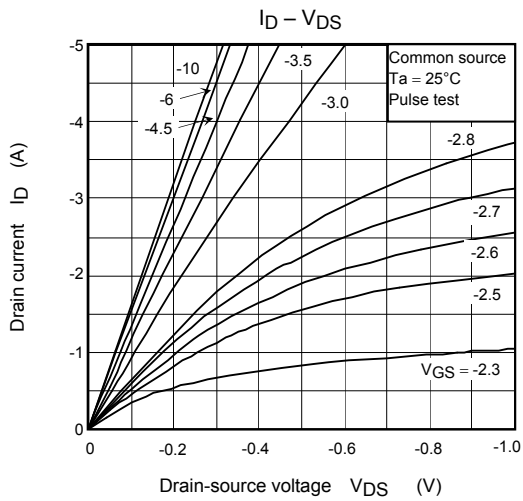
Electrical Characteristics (Ta = 25°C)

Characteristics		Symbol	Test Condition	Min	Typ.	Max	Unit
Gate leakage current		I_{GSS}	$V_{GS} = \pm 16\text{ V}, V_{DS} = 0\text{ V}$	—	—	± 10	μA
Drain cut-off current		I_{DSS}	$V_{DS} = 30\text{ V}, V_{GS} = 0\text{ V}$	—	—	10	μA
Drain-source breakdown voltage		$V_{(BR)DSS}$	$I_D = 10\text{ mA}, V_{GS} = 0\text{ V}$	30	—	—	V
		$V_{(BR)DSX}$	$I_D = 10\text{ mA}, V_{GS} = -20\text{ V}$	15	—	—	
Gate threshold voltage		V_{th}	$V_{DS} = 10\text{ V}, I_D = 1\text{ mA}$	1.3	—	2.5	V
Drain-source ON resistance		$R_{DS(ON)}$	$V_{GS} = 4.5\text{ V}, I_D = 2.0\text{ A}$	—	58	77	m Ω
			$V_{GS} = 10\text{ V}, I_D = 2.0\text{ A}$	—	38	50	
Forward transfer admittance		$ Y_{fs} $	$V_{DS} = 10\text{ V}, I_D = 2.0\text{ A}$	3.4	6.8	—	S
Input capacitance		C_{iss}	$V_{DS} = 10\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$	—	470	—	pF
Reverse transfer capacitance		C_{rss}		—	60	—	
Output capacitance		C_{oss}		—	80	—	
Switching time	Rise time	t_r		—	5.2	—	ns
	Turn-on time	t_{on}		—	8.3	—	
	Fall time	t_f		—	4.0	—	
	Turn-off time	t_{off}		Duty $\leq 1\%$, $t_w = 10\ \mu\text{s}$	—	22	
Total gate charge (gate-source plus gate-drain)		Q_g	$V_{DD} \approx 24\text{ V}, V_{GS} = 10\text{ V}, I_D = 4\text{ A}$	—	10	—	nC
Gate-source charge 1		Q_{gs1}		—	1.7	—	
Gate-drain ("miller") charge		Q_{gd}		—	2.4	—	

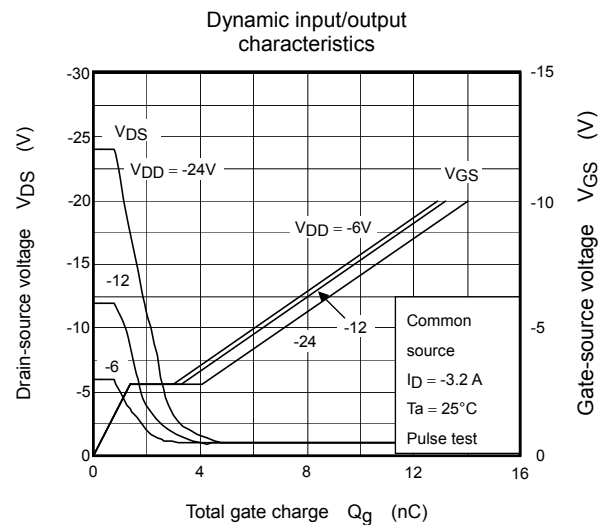
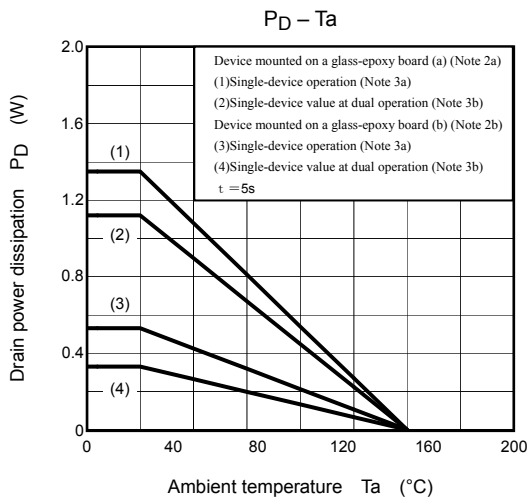
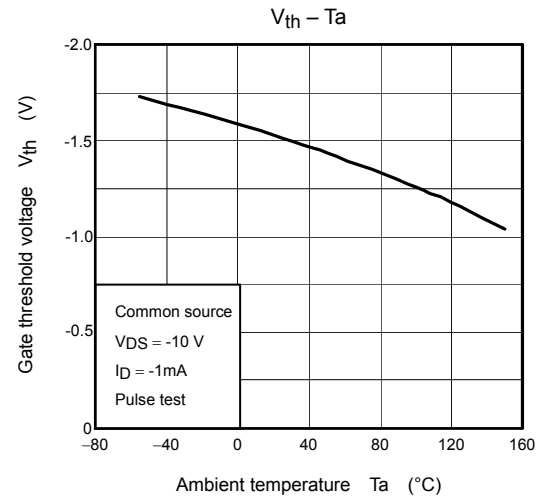
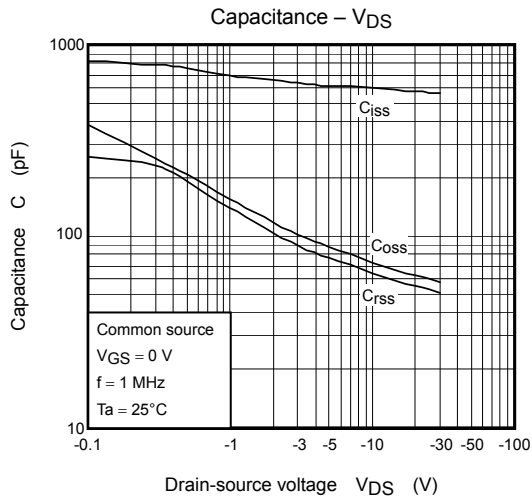
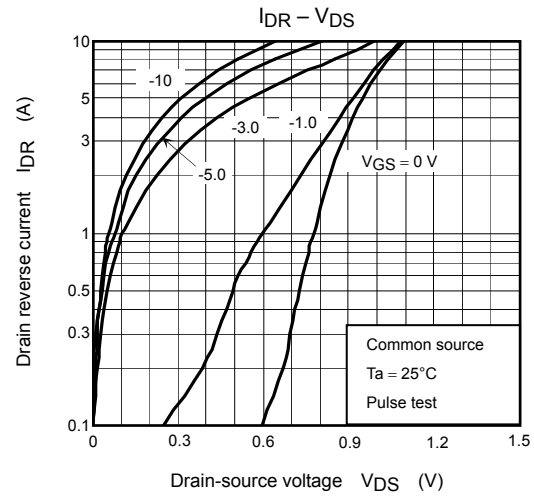
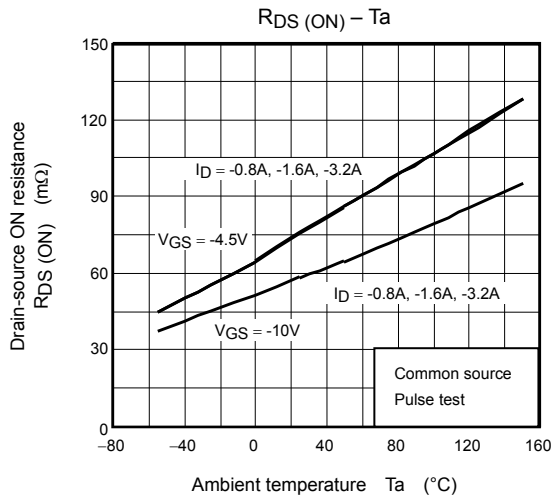
Source-Drain Ratings and Characteristics (Ta = 25°C)

Characteristics		Symbol	Test Condition	Min	Typ.	Max	Unit
Drain reverse current	Pulse (Note 1)	I_{DRP}	—	—	—	16.0	A
Forward voltage (diode)		V_{DSF}	$I_{DR} = 4.0\text{ A}, V_{GS} = 0\text{ V}$	—	—	-1.2	V

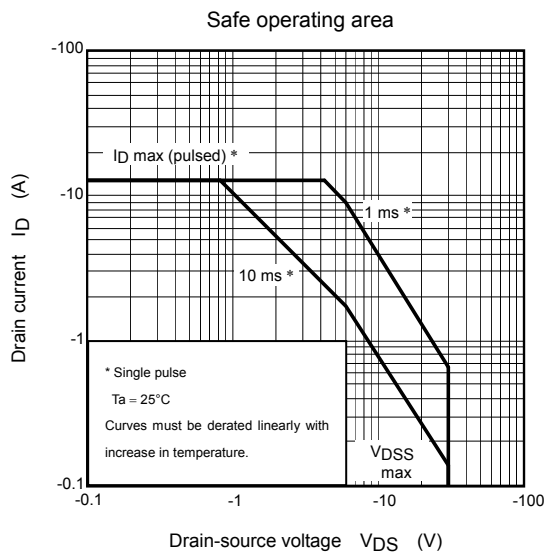
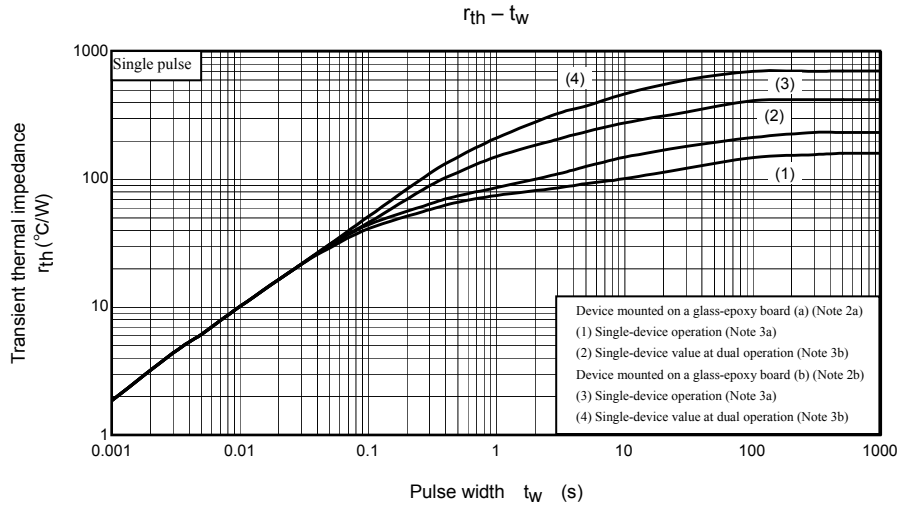
P-channel



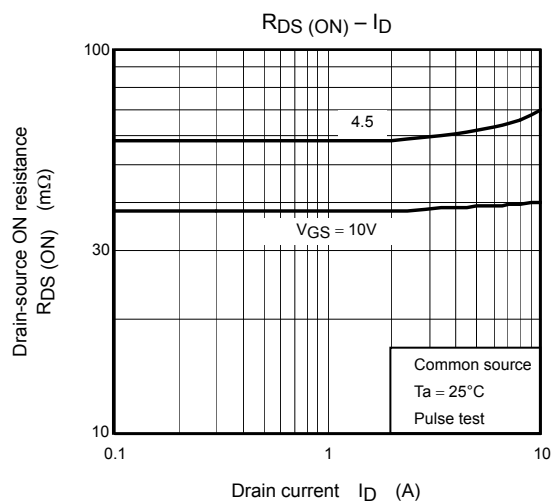
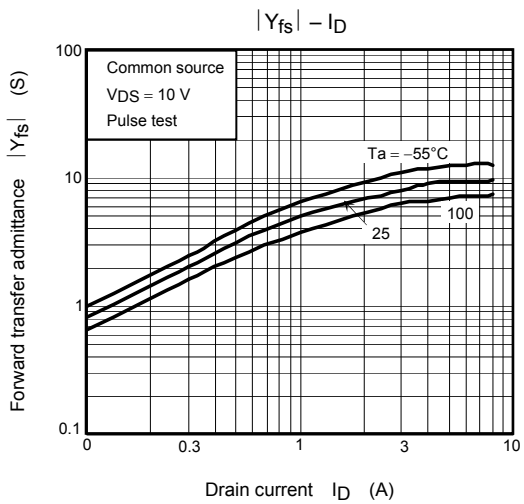
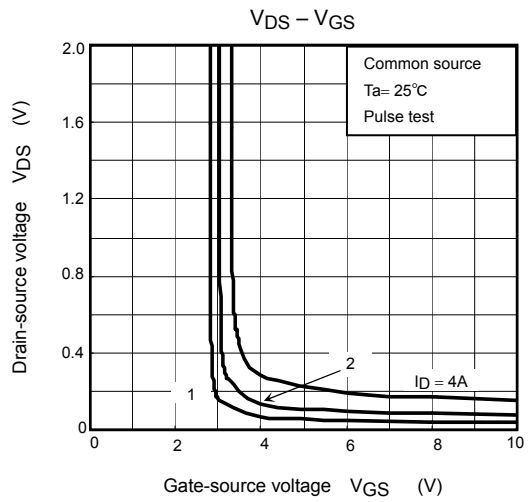
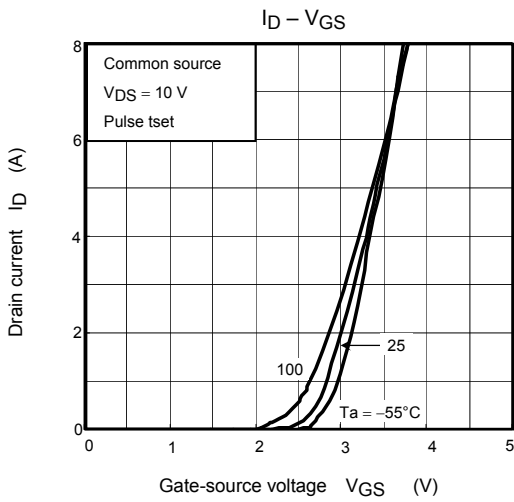
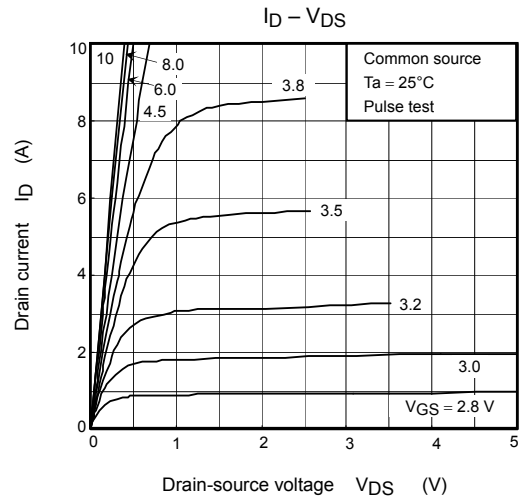
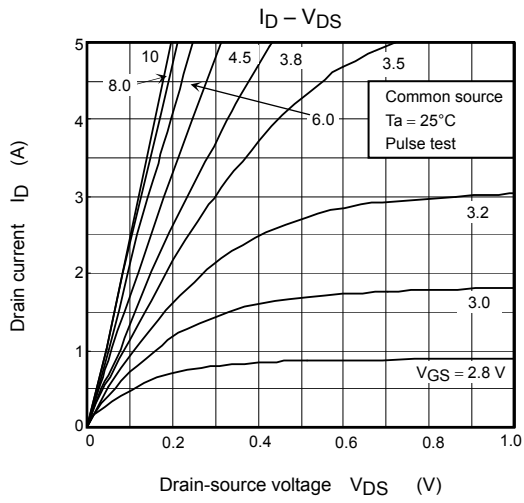
P-channel



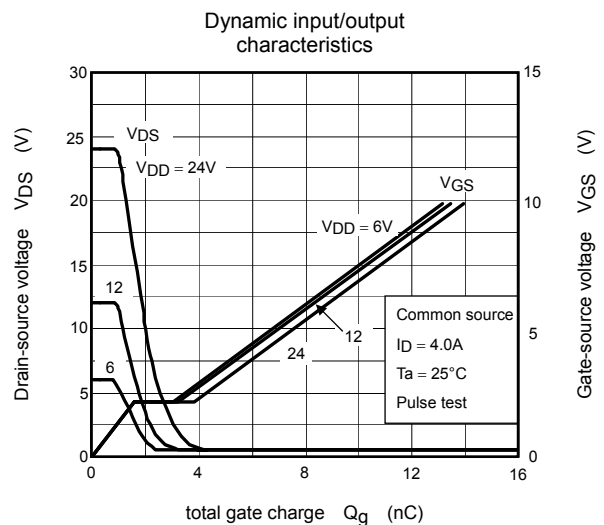
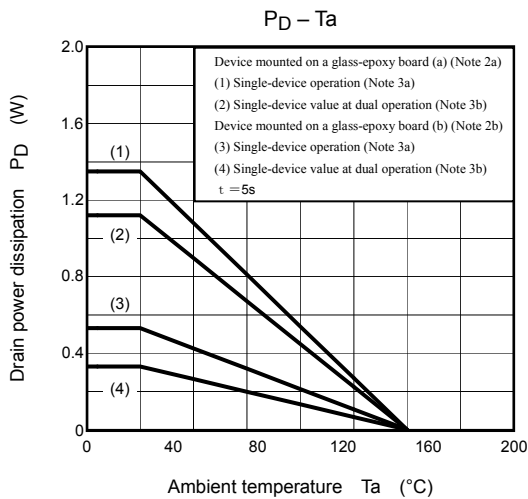
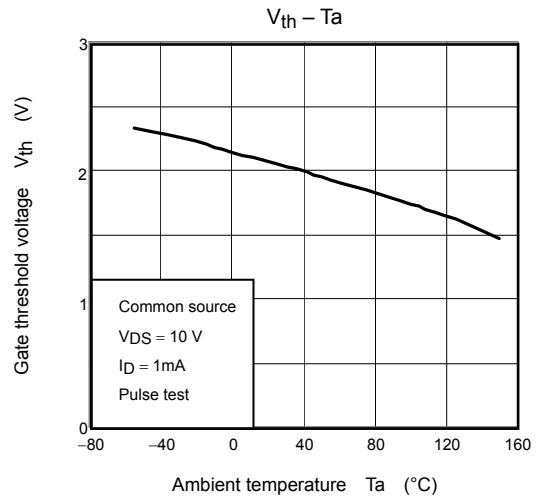
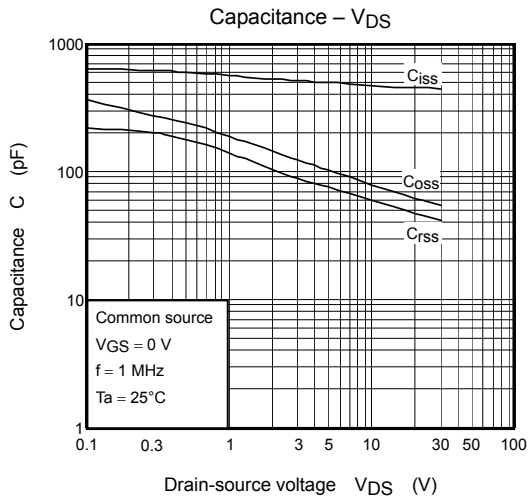
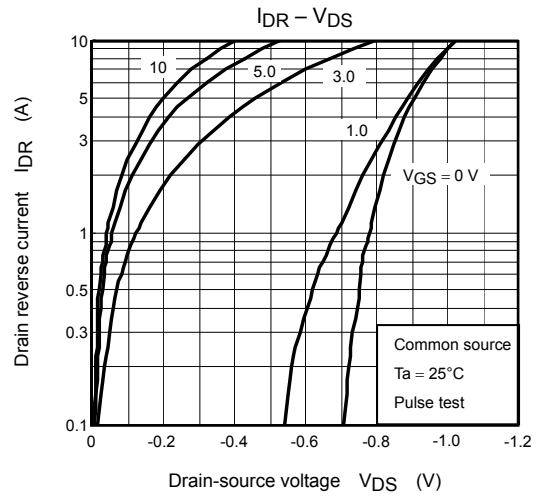
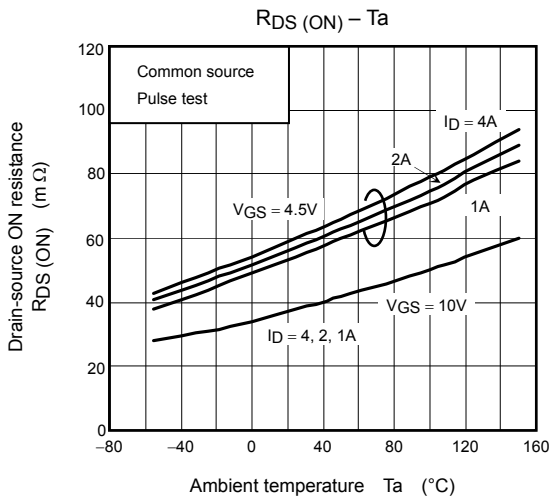
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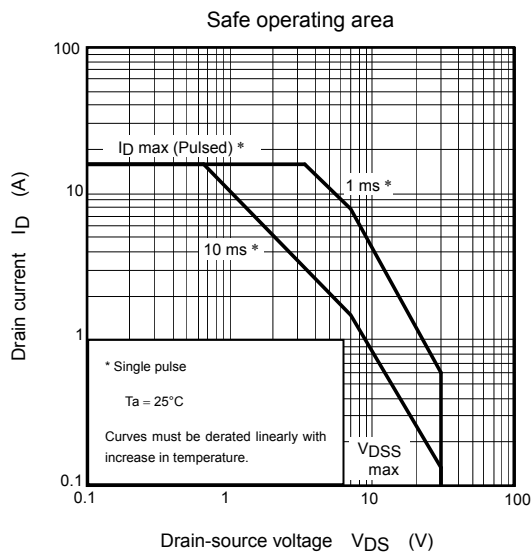
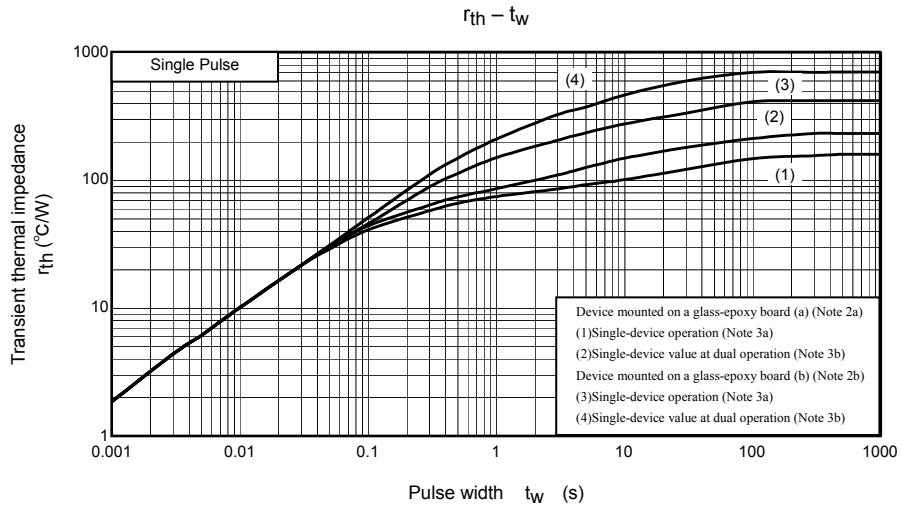
N-channel



N-channel



N-channel



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