Stereo 2.6W Audio Power Amplifier

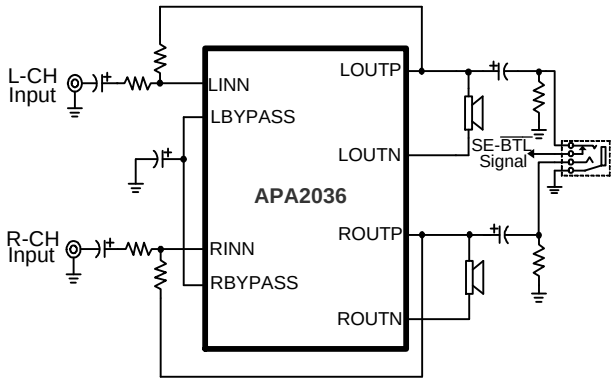
Features

- **Operating Voltage: 3.0 ~ 5.5V**
- **Low Shutdown Current**
  - **– I_{DD}= 0.5μA (typical) at V_{DD}= 5V**
- **Selectable Bridge-Tied Load (BTL) or Singled-Ended (SE) Operation**
- **Output Power (BTL) at 1% THD+N, V_{DD}= 5V**
  - **– 2.4W at R_L = 3Ω**
  - **– 2.0W at R_L = 4Ω**
  - **– 1.3W at R_L = 8Ω**
- **Output Power (SE) at 1% THD+N, V_{DD}= 5V**
  - **– 160mW at R_L = 16Ω**
  - **– 85mW at R_L = 32Ω**
- **Depop Circuitry Integrated**
- **Thermal and Over-Current Protections**
- **Short Circuit Protection**
- **Space Saving Packaging**
  - **– 4mmx4mm 16-Lead Thin QFN Package (TQFN4X4-16)**
- **Lead Free Available (RoHS Compliant)**

Applications

- **Handsets**
- **Portable multimedia devices**
- **Notebooks**

Simplified Application Circuit

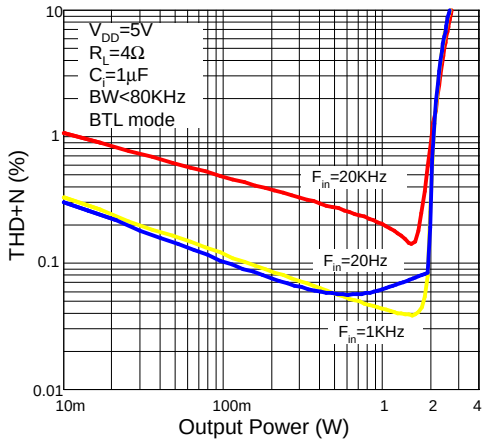


General Description

The APA2036 is a stereo audio power amplifier in a TQFN4x4-16 package. To simplify the audio system design in notebook computer applications, the APA2036 combines a stereo bridge-tied mode for speaker drive and a stereo single-end mode for headphone drive into a single chip, where both modes are easily switched by the SE/$\overline{\text{BTL}}$ input control pin signal. When the APA2036 is in the BTL mode with 5V supply voltage, it is capable of delivering 2.4W/2.0W/1.3W of continuous output power per channel into 3Ω/4Ω/8Ω load (Speaker) with less than 1% THD+N respectively. When the APA2036 operates in the single-ended mode, it is capable of delivering 160mW/85mW of continuous output power per channel into 16Ω/32Ω load (Headphone).

The APA2036 also serves low-voltage applications well. The APA2036, with 3.3V supply voltage, provides 900mW (at 1% THD+N) per channel into 4Ω load. Both of the depop circuitry and the thermal shutdown protection circuitry are integrated in the APA2036. The depop function reduces pops and clicks noise during power on/off and enable/shutdown processes. The thermal protection protects the chip from being destroyed by over-temperature failure. For power sensitive applications, the APA2036 also features a shutdown function which reduces the supply current only 0.5μA (typical).

THD+N vs. Output Power



Ordering and Marking Information

APA2036 □□-□□□

- Lead Free Code
- Handling Code
- Temperature Range
- Package Code

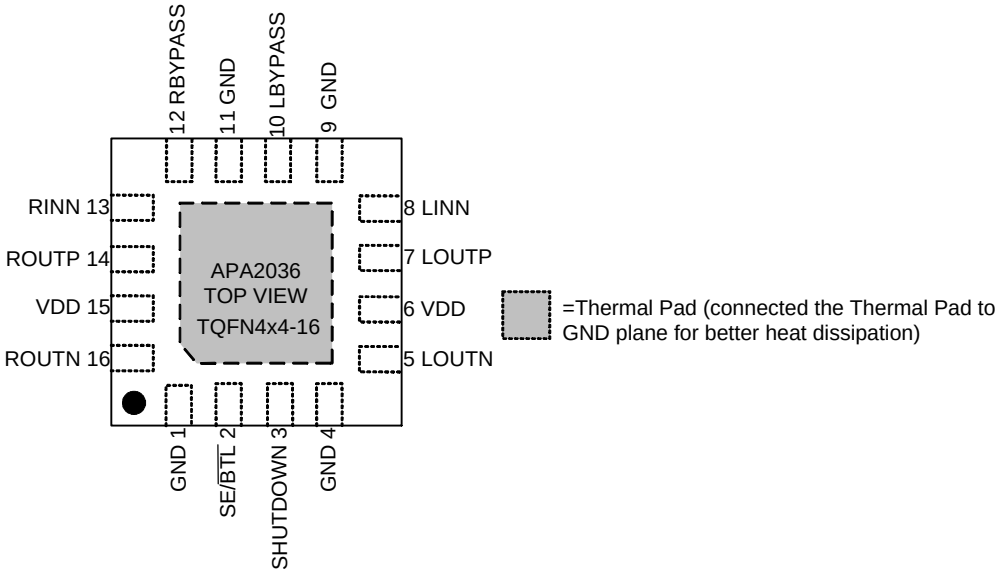
Package Code
QB : TQFN4x4-16
Operating Ambient Temperature Range
I : - 40 to 85 °C
Handling Code
TR : Tape & Reel
Lead Free Code
L : Lead Free Device

APA2036 QB :

XXXXX - Date Code

Note: ANPEC lead-free products contain molding compounds/die attach materials and 100% matte tin plate termination finish; which are fully compliant with RoHS and compatible with both SnPb and lead-free soldering operations. ANPEC lead-free products meet or exceed the lead-free requirements of IPC/JEDEC J STD-020C for MSL classification at lead-free peak reflow temperature.

Pin Configuration



Absolute Maximum Ratings (Note 1)

Symbol	Parameter	Rating	Unit
V_{DD}	Supply Voltage	-0.3 to 6	V
	Input Voltage (SE/$\overline{BTL}$, SHUTDOWN, RINN, LINN, RBYPASS, LBYPASS)	-0.3 to V_{DD}+0.3	V
	Output Voltage (ROUTP, ROUTN, LOUTP, LOUTN)	-0.3 to V_{DD}+0.3	V
T_A	Operating Ambient Temperature Range	-40 to 85	°C
T_J	Maximum Junction Temperature	150	°C
T_{STG}	Storage Temperature Range	-65 to +150	°C
T_{SDR}	Maximum Lead Soldering Temperature, 10 seconds	260	°C
P_D	Power Dissipation	Internally Limited	W

Note 1 : Absolute Maximum Ratings are those values beyond which the life of a device may be impaired. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Thermal Characteristics (Note 2,3)

Symbol	Parameter	Value	Unit
θ_{JA}	Thermal Resistance - Junction to Ambient (Note 2)	41	°C/W
θ_{JC}	Junction-to-Case Resistance in free air (Note 3)	9	

Note 2: θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. The thermal pad of TQFN4x4-16 is soldered directly on the PCB.

Note 3: The case temperature is measured at the center of the thermal pad on the underside of the TQFN4x4-16 package.

Recommended Operating Conditions

Symbol	Parameter		Range	Unit
V_{DD}	Supply Voltage		3.0 ~ 5.5	V
V_{IH}	High level threshold voltage	SHUTDOWN	0.4 V_{DD} ~ V_{DD}	V
		SE/$\overline{BTL}$	0.8 V_{DD} ~ V_{DD}	V
V_{IL}	Low level threshold voltage	SHUTDOWN	0 ~ 1.0	V
		SE/$\overline{BTL}$	0 ~ 0.6V_{DD}	V
V_{IC}	Common mode input voltage		~ V_{DD}-0.5	V
T_A	Ambient Temperature Range		-40 ~ 85	°C
T_J	Junction Temperature Range		-40 ~ 125	°C
R_L	Speaker Resistance		3 ~	Ω
R_L	Headphone Resistance		16 ~	Ω

Electrical Characteristics

Unless otherwise noted, these specifications apply over V_{DD}=5V, V_{GND}=0V, T_A= -40 ~ 85°C, Typical values are at T_A= 25°C

Symbol	Parameter	Test Condition		APA2036			Unit
				Min.	Typ.	Max.	
V_{DD}	Supply Voltage			3		5.5	V
I_{DD}	Supply Current	$V_{SE/\overline{BTL}}$=0V			5.5	13.5	mA
		$V_{SE/\overline{BTL}}$=5V			3	7.5	
I_{SD}	Shutdown Current	$V_{SHUTDOWN}$=5V			0.5	5	µA
$T_{START-UP}$	Start-Up time from shutdown	C_B=2.2µF			700		ms
BTL mode, V_{DD}=5V							
P_O	Output Power	THD+N=1%, F_{in}=1KHz	R_L=3Ω		2.4		W
			R_L=4Ω		2.0		
			R_L=8Ω	1.1	1.3		
		THD+N=10%, F_{in}=1KHz	R_L=3Ω		3.0		
			R_L=4Ω		2.6		
			R_L=8Ω		1.6		
THD+N	Total Harmonic Distortion Pulse Noise	F_{in}=1KHz	R_L=4Ω P_O=1.3W		0.06		%
			R_L=8Ω P_O=0.9W		0.03		

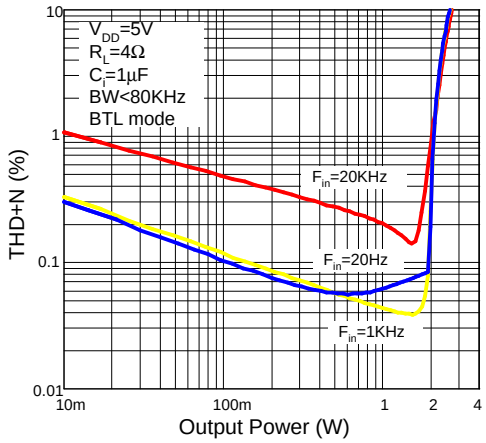
Electrical Characteristics (Cont.)

Unless otherwise noted, these specifications apply over V_{DD}=5V, V_{GND}=0V, T_A= -40 ~ 85°C, Typical values are at T_A=25°C

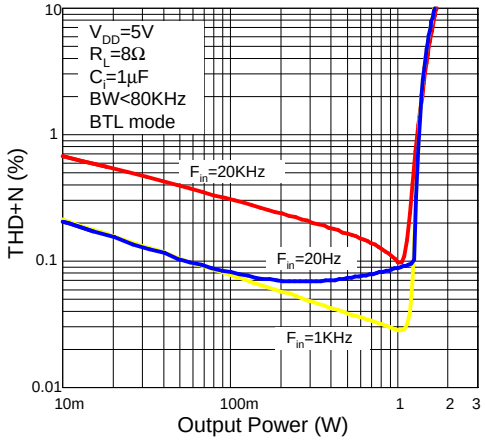
Symbol	Parameter	Test Condition		APA2036			Unit
				Min.	Typ.	Max.	
PSRR	Power Supply Rejection Ratio	R_L=8Ω, F_{in}=217Hz			61		dB
V_{OS}	Output Offset Voltage	V_{IN}=0V			10		mV
Crosstalk	Channel separation	R_L=8Ω, P_O=0.9W, F_{in}=1KHz			100		dB
S/N	Signal to Noise Ratio	R_L=8Ω, P_O=1.1W, A_weighting			93		dB
Vn	Noise Output Voltage	R_L=8Ω			22		μV(rms)
SE mode, V_{DD}=5V							
P_O	Output Power	THD+N=1%, F_{in}=1KHz	R_L=16Ω		160		mW
			R_L=32Ω	70	85		
		THD+N=10%, F_{in}=1KHz	R_L=16Ω		210		
			R_L=32Ω		110		
THD+N	Total Harmonic Distortion Pulse Noise	F_{in}=1KHz	R_L=32Ω P_O=60mW		0.02		%
PSRR	Power Supply Rejection Ratio	R_L=32Ω, F_{in}=217Hz			60		dB
V_{OS}	Output Offset Voltage	V_{IN}=0V			10		mV
Crosstalk	Channel separation	R_L=32Ω, P_O=60mW, F_{in}=1KHz			85		dB
S/N	Signal to Noise Ratio	R_L=32Ω, P_O=65mW, A_weighting			100		dB
Vn	Noise Output Voltage	R_L=32Ω			8		μV(rms)

Typical Operating Characteristics

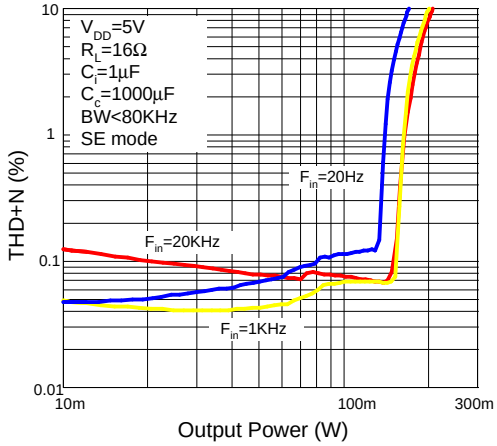
THD+N vs. Output Power



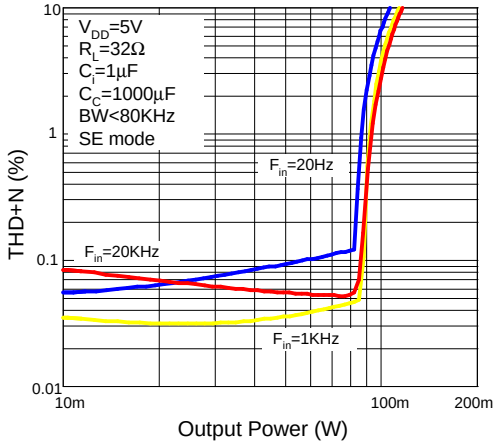
THD+N vs. Output Power



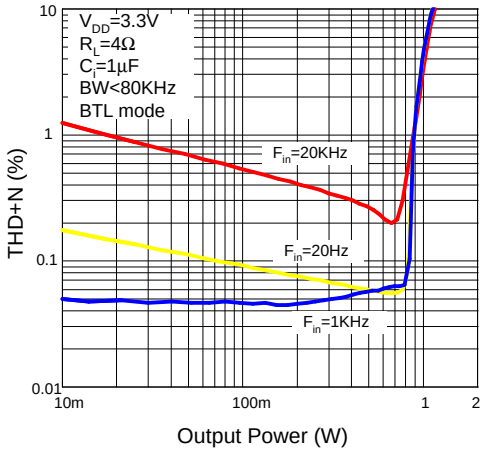
THD+N vs. Output Power



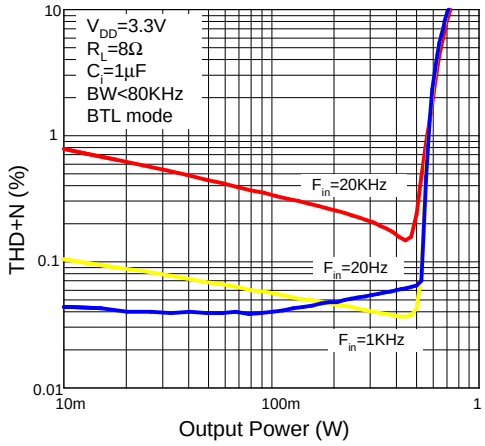
THD+N vs. Output Power



THD+N vs. Output Power

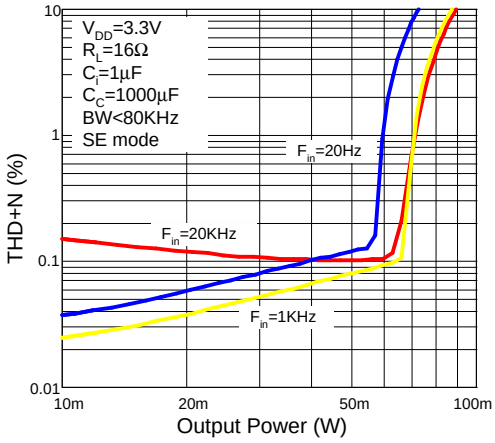


THD+N vs. Output Power

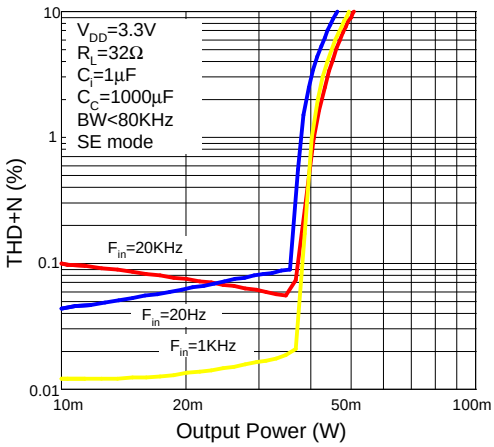


Typical Operating Characteristics (Cont.)

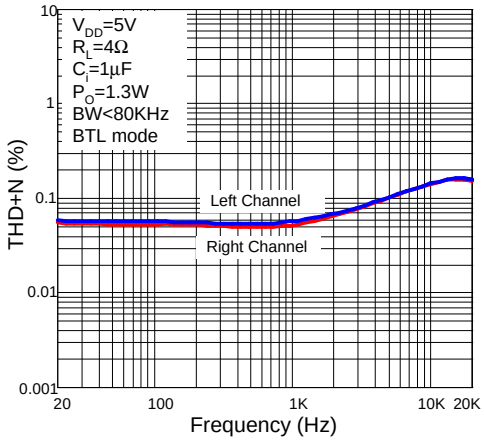
THD+N vs. Output Power



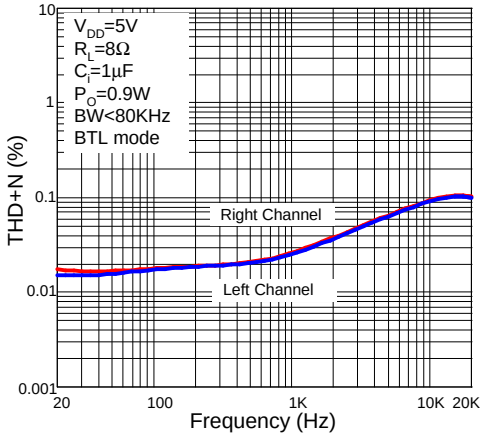
THD+N vs. Output Power



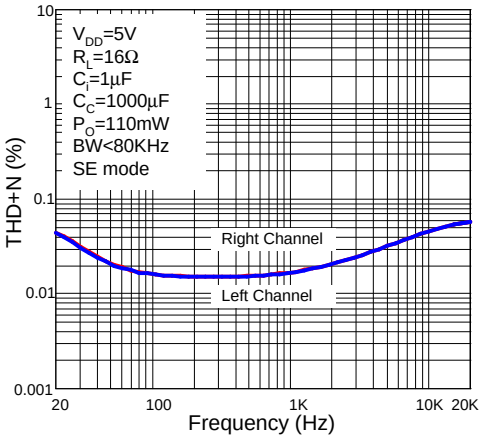
THD+N vs. Frequency



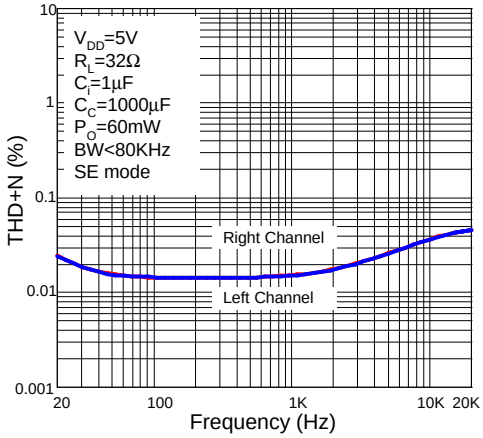
THD+N vs. Frequency



THD+N vs. Frequency

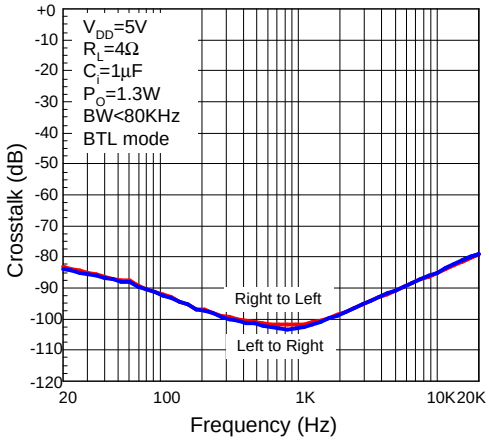


THD+N vs. Frequency

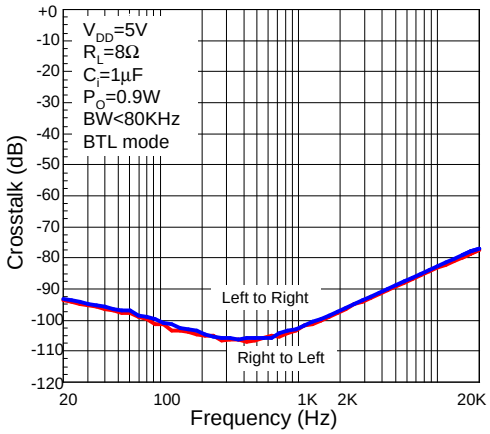


Typical Operating Characteristics (Cont.)

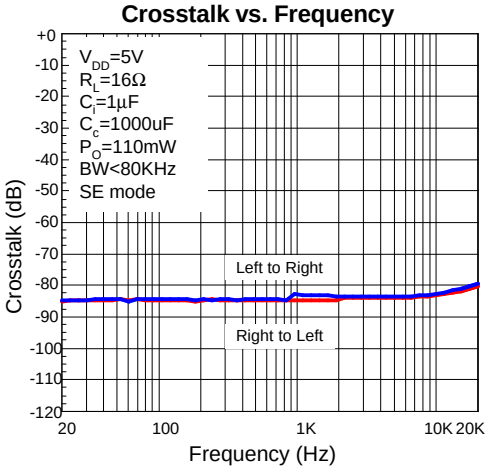
Crosstalk vs. Frequency



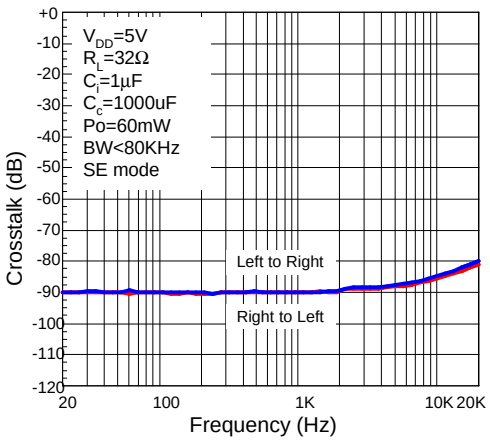
Crosstalk vs. Frequency



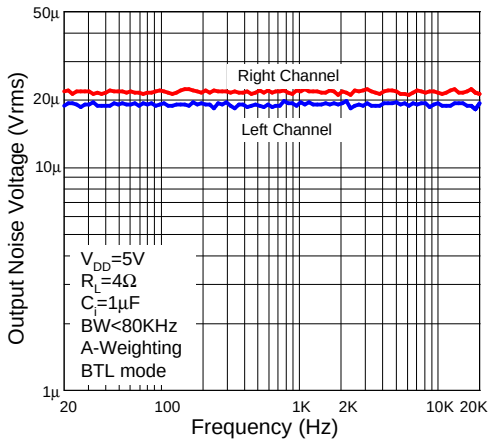
Crosstalk vs. Frequency



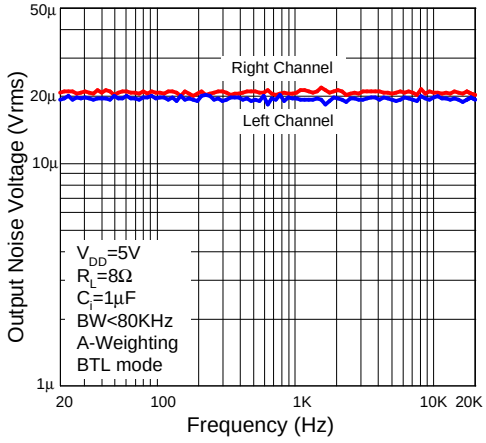
Crosstalk vs. Frequency



Output Noise Voltage vs. Frequency

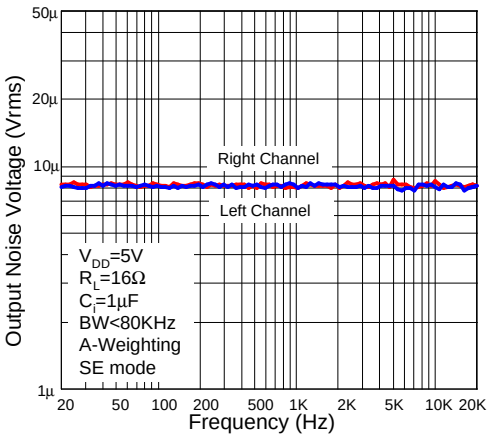


Output Noise Voltage vs. Frequency

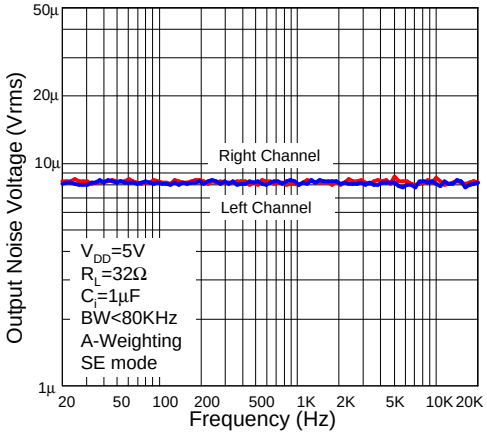


Typical Operating Characteristics (Cont.)

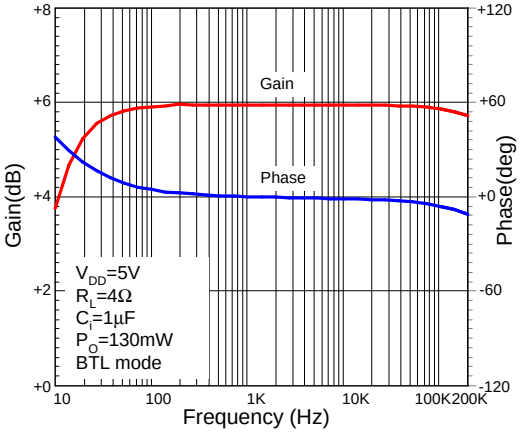
Output Noise Voltage vs. Frequency



Output Noise Voltage vs. Frequency



Frequency Response



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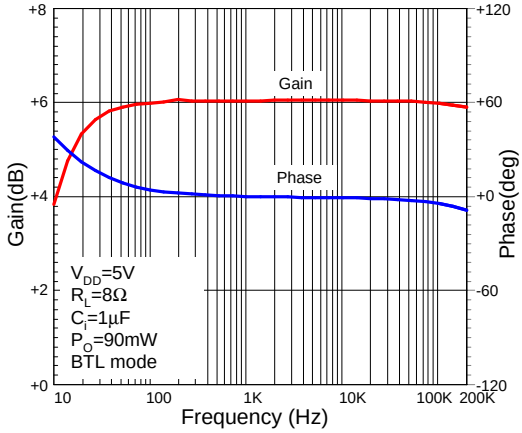
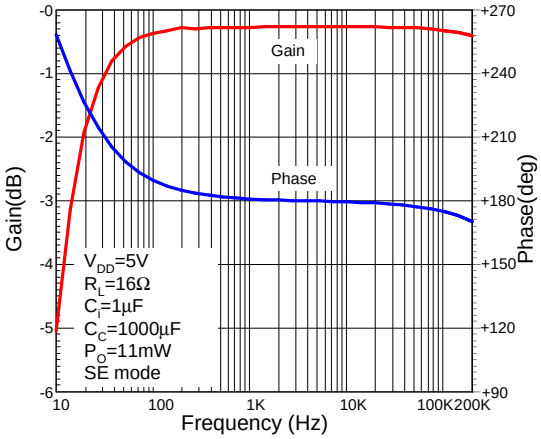
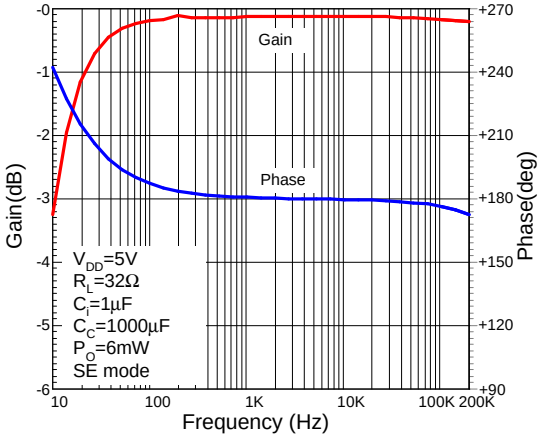


Frequency Response

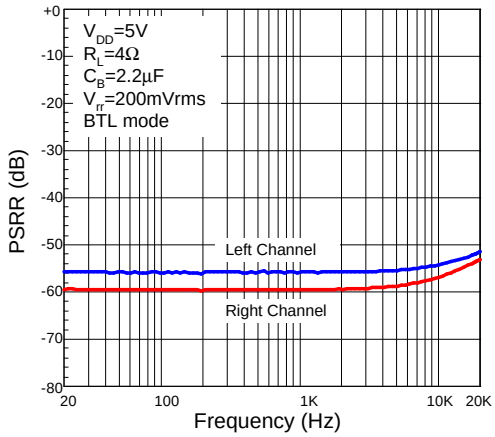


Frequency Response

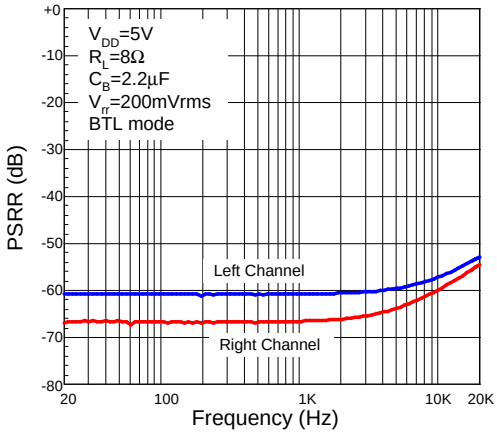


Typical Operating Characteristics (Cont.)

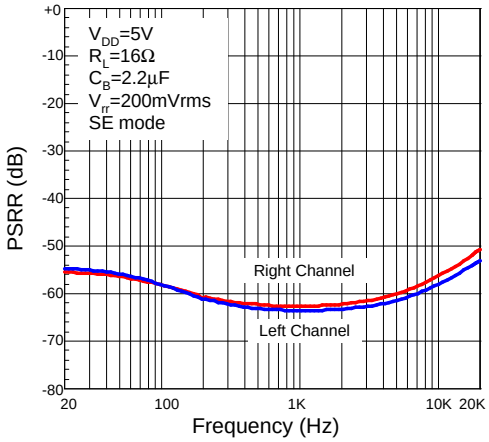
PSRR vs. Frequency



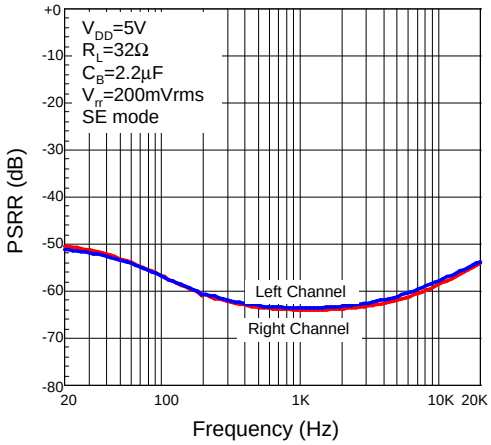
PSRR vs. Frequency



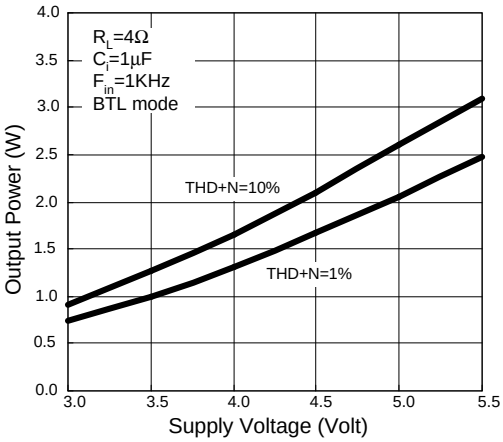
PSRR vs. Frequency



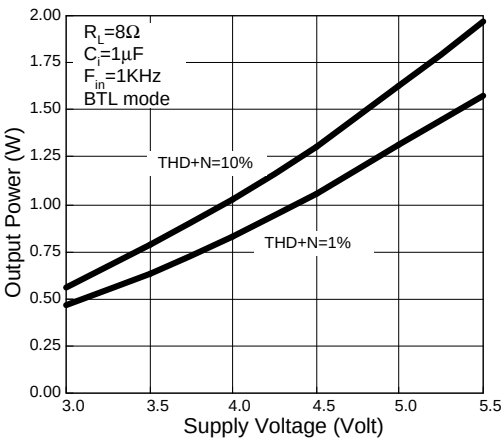
PSRR vs. Frequency



Output Power vs. Supply Voltage

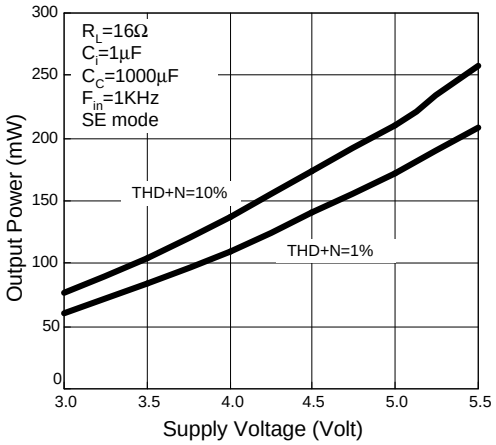


Output Power vs. Supply Voltage

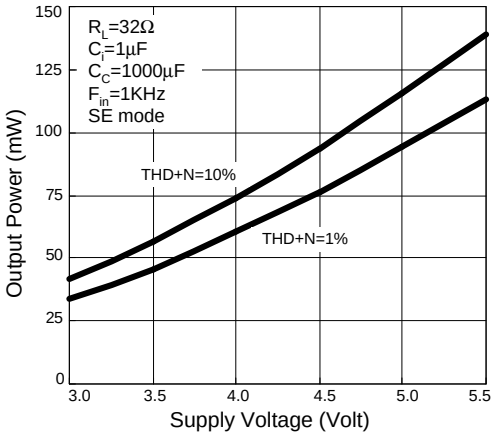


Typical Operating Characteristics (Cont.)

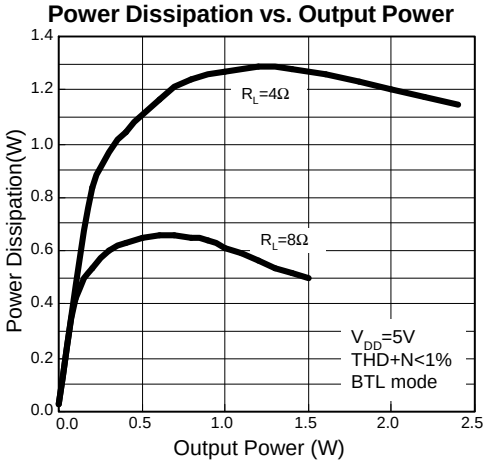
Output Power vs. Supply Voltage



Output Power vs. Supply Voltage



Power Dissipation vs. Output Power



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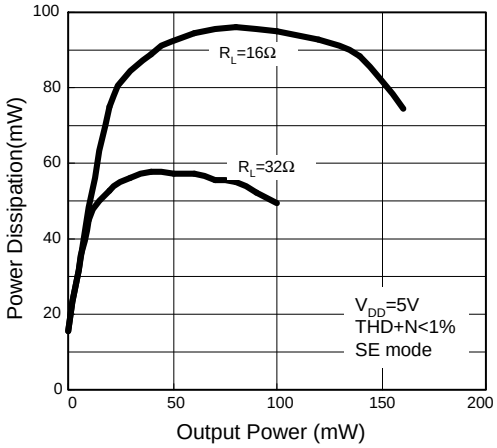
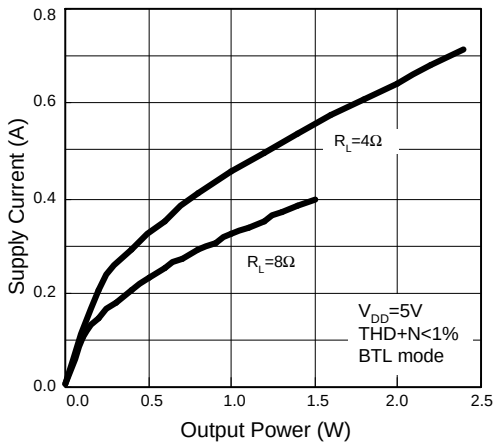
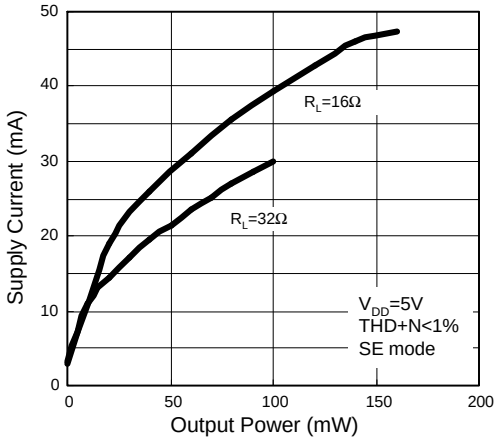


Supply Current vs. Output Power

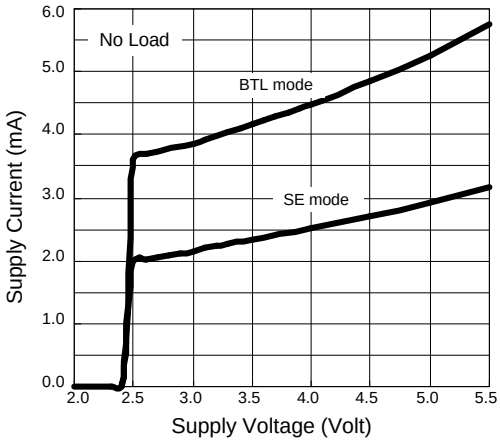


Supply Current vs. Output Power

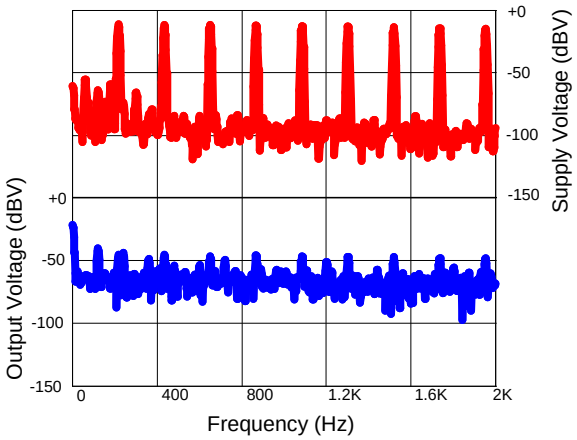


Typical Operating Characteristics (Cont.)

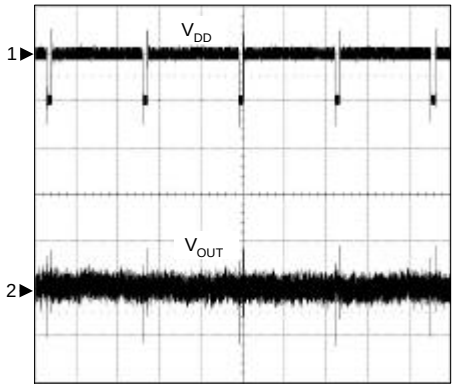
Supply Current vs. Supply Voltage



GSM Power Supply Rejection vs. Frequency

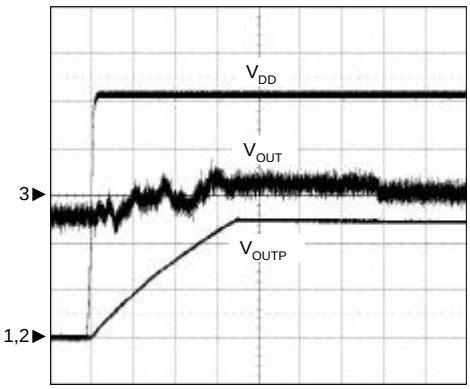


GSM Power Supply Rejection vs. Time



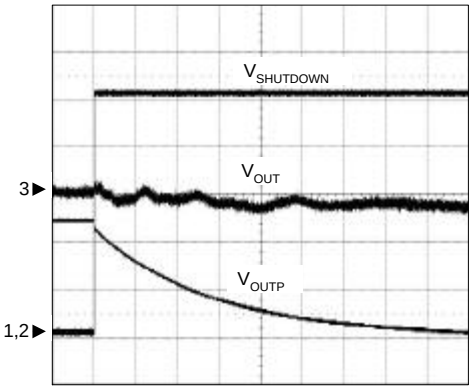
CH1: V_{DD}, 500mV/Div, DC
Voltage Offset = 5.0V
CH2: V_{OUT} (V_{OUTP}-V_{OUTN}), 20mV/Div, DC
TIME: 20ms/Div

Output Transient at Power-On



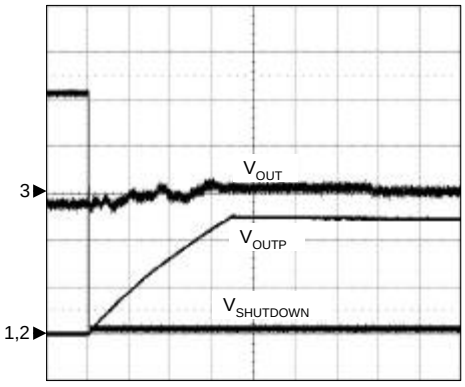
CH1: V_{DD}, 1V/Div, DC
CH2: V_{OUTP}, 1V/Div, DC
CH3: V_{OUT} (V_{OUTP}-V_{OUTN}), 50mV/Div, DC
TIME: 100ms/Div

Output Transient at Shutdown Active



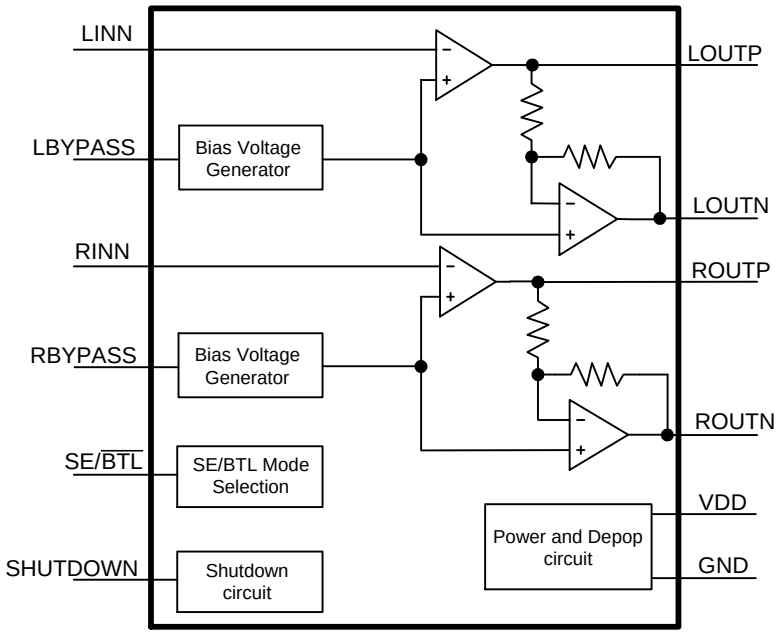
CH1: $V_{SHUTDOWN}$, 1V/Div, DC
CH2: V_{OUTP}, 1V/Div, DC
CH3: V_{OUT}(V_{OUTP}-V_{OUTN}), 50mV/Div, DC
TIME: 500ms/Div

Output Transient at Shutdown Release



CH1: $V_{SHUTDOWN}$, 1V/Div, DC
CH2: V_{OUTP}, 1V/Div, DC
CH3: V_{OUT}(V_{OUTP}-V_{OUTN}), 50mV/Div, DC
TIME: 100ms/Div

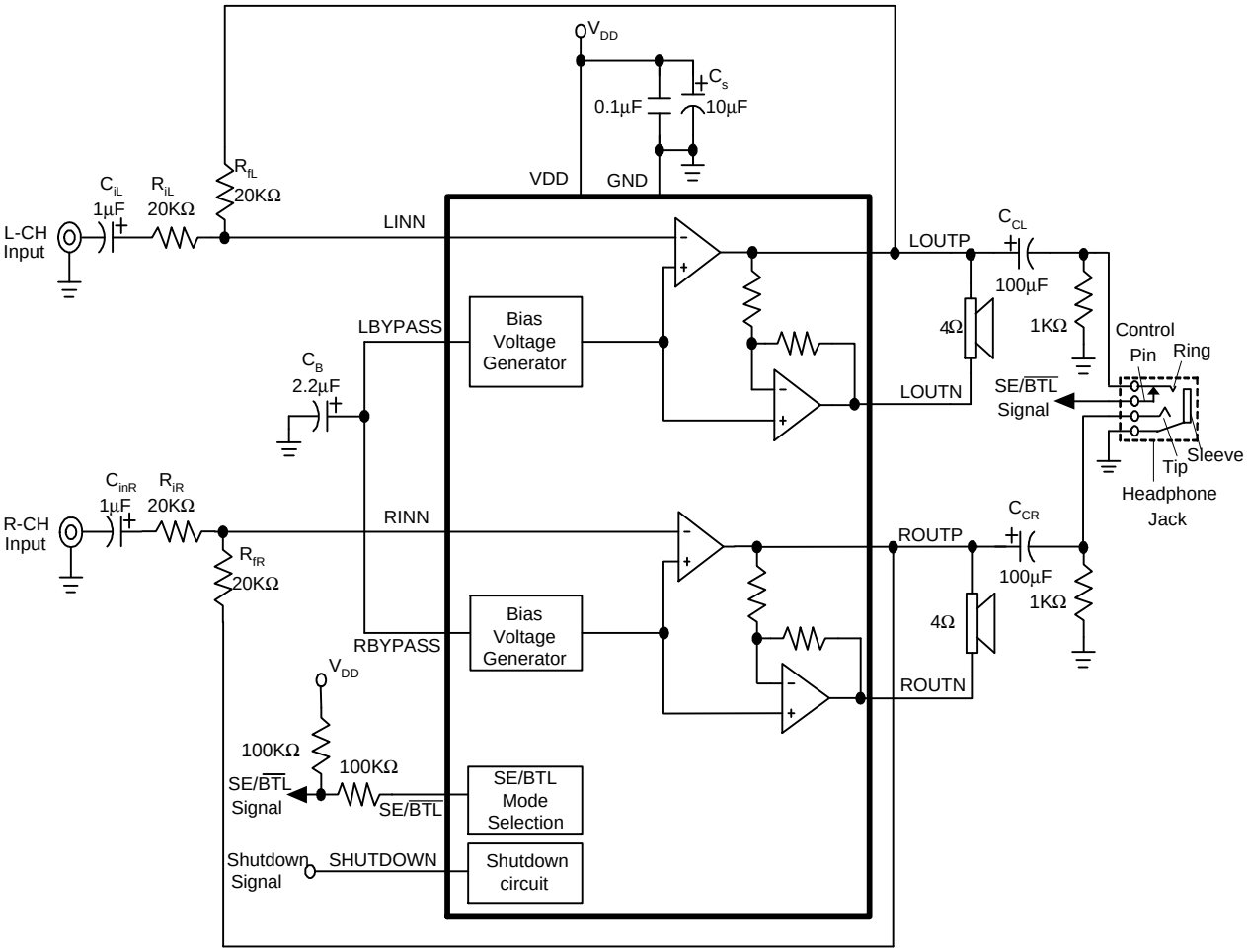
Block Diagram



Pin Description

Pin		Function Description
NO.	Name	
1,4,9,11	GND	Ground connection of circuitry. Connect all GND pins to the thermal pad and system ground plane.
2	SE/$\overline{BTL}$	Output Mode control pin, high for SE output mode and low for BTL mode.
3	SHUTDOWN	Shutdown mode control pin. Pulling high the voltage on this pin shuts off the IC. In shutdown mode, the IC only draws 0.5μA (typical) of supply current.
5	LOUTN	Left channel output in BTL mode, high impedance in SE mode.
6,15	VDD	Supply voltage input pin. Connect all of the VDD pins to supply voltage.
7	LOUTP	Left channel output in BTL mode and SE mode. As “Typical Application Circuit” shown, this pin’s output signal is inverted against LINN input signal.
8	LINN	Left channel input terminal.
10	LBYPASS	Bypass capacitor connection pin for the bias voltage generator.
12	RBYPASS	Bypass capacitor connection pin for the bias voltage generator.
13	RINN	Right channel input terminal.
14	ROUTP	Right channel output in BTL mode and SE mode. As “Typical Application Circuit” shown, this pin’s output signal is inverted against RINN input signal.
16	ROUTN	Right channel output in BTL mode, high impedance in SE mode.

Typical Application Circuit



Function Description

Bridge-Tied Load (BTL) Operation

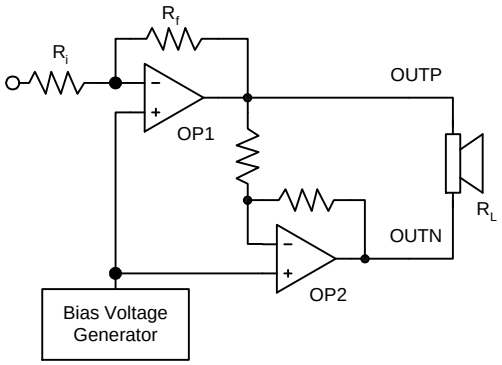


Figure 1: APA2036 internal configuration (each channel)

The power amplifier's (OP1) gain is set by external resistance R_i and R_f, while the second amplifier (OP2) is internally fixed in a unity-gain and inverting configuration. Figure 1 shows that the output of OP1 is connected to the input of OP2, which results in the output signals of both amplifiers with identical in magnitude, but out of phase 180°. Consequently, the differential gain for each channel is 2X (Gain of SE mode).

By driving the load differentially through outputs OUTP and OUTN, an amplifier configuration is commonly referred to established bridged mode. BTL mode operation is different from the classical single-ended SE amplifier configuration where one side of its load is connected to ground.

A BTL amplifier design has a few distinct advantages over the SE configuration, as it provides differential drive to the load, thus doubles the output swing for a specified supply voltage.

Four times the output power is possible as compared with a SE amplifier in the same conditions. A BTL configuration, such as the one used in the APA2036, also creates a second advantage over SE amplifiers. Since the differential outputs, ROUTP, ROUTN, LOUTP, and LOUTN, are biased at half-supply, DC voltage doesn't have to exist across the load. This eliminates the need for an output coupling capacitor which is required in a single supply, SE configuration.

Single-Ended (SE) Operation

To consider the single-supply SE configuration shown in Typical Application Circuit, a coupling capacitor is required to block the DC offset voltage from reaching the load. These capacitors can be quite large (approximately 33µF to 1000µF) so they tend to be expensive, occupy valuable PCB area, and have the additional drawback of limiting low-frequency performance of the system (refer to the Output Coupling Capacitor).

SE/BTL Mode Selection Function

Eazy switch between BTL and SE modes is one of its most important costs saving features for the APA2036. This feature eliminates the requirement for an additional headphone amplifier in applications where internal stereo speakers are driven in BTL mode but external headphone or speakers must be accommodated.

Inside of the APA2036, two separate amplifiers drive OUTP and OUTN (see Figure 1). The SE/$\overline{\text{BTL}}$ input controls the operation of the follower amplifier that drives LOUTP and ROUTN.

- When SE/$\overline{\text{BTL}}$ keeps low, the OP2 turns on and the APA2036 is in the BTL mode.
- When SE/$\overline{\text{BTL}}$ keeps high, the OP2 is in a high output impedance state, which configures the APA2036 as SE driver from OUTP. I_{DD} is reduced by approximately one-half in SE mode.

Control of the SE/$\overline{\text{BTL}}$ input can be a logic-level TTL source or a resistor divider network or the stereo headphone jack with switch pin as shown in Typical Application Circuit.

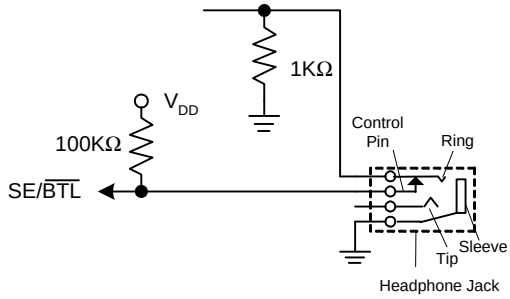


Figure 2: SE/$\overline{\text{BTL}}$ input selection by phonejack plug

Function Description (Cont.)

SE/BTL Mode Selection Function (Cont.)

In Figure 2, input SE/$\overline{\text{BTL}}$ operates as below:
When the phonejack plug is inserted, the 1KΩ resistor is disconnected and the SE/$\overline{\text{BTL}}$ input is pulled high to enable the SE mode. Meanwhile, the OUTN amplifier is shut down which turns the speaker to be mute. The OUTP amplifier then drives through the output capacitor into the headphone jack. When there is no headphone plugged into the system, the contact pin of the headphone jack is connected from the signal pin, and the voltage divider is set up by resistors 100KΩ and 1KΩ. Resistor 1KΩ then is pulled low the SE/$\overline{\text{BTL}}$ pin, enabling the BTL function.

Shutdown Function

In order to reduce power consumption while not in use, the APA2036 with shutdown function externally turns off the amplifier bias circuitry. This shutdown feature turns the amplifier off when logic high is placed on the SHUTDOWN pin for the APA2036. The trigger point between a logic high and logic low level is typical $0.4V_{DD}$. It would be better to switch between ground and the supply voltage V_{DD} to provide maximum device performance. By switching the SHUTDOWN pin to high level, the amplifier enters a low consumption current state; I_{DD} for the APA2036 is in shutdown mode. In normal operation, the APA2036's SHUTDOWN pin should be pulled to low level to keep the IC out of the shutdown mode. The SHUTDOWN pin should be tied to a definite voltage to avoid unwanted state changes.

Thermal Protection

The over-temperature circuit limits the junction temperature of the APA2036. When the junction temperature exceeds T_J = +150°C, a thermal sensor turns off the amplifier, allowing the devices to cool. The thermal sensor allows the amplifier to start up after the junction temperature cools down about 125°C. The thermal protection designed with a 25°C hysteresis lowers the average T_J during continuous thermal overload conditions, which is increasing lifetime of the IC.

Over-Current Protection

The APA2036 monitors the output current. When the current exceeds the current-limit threshold, the APA2036 turns off the output to prevent the IC damages from over-current or short-circuits condition. When the over-current occurs in power amplifier, the output buffer's current will be foldbacked to a low setting level, and it will release when over-current situation is no long existence. On the contrary, if the over-current period is long enough and the IC's junction temperature reaches the thermal protection threshold, the IC will enter thermal protection mode.

Application Information

Input Resistance (R_i)

The gain of the APA2036 is set by the external resistors (R_i and R_f).

$$\text{BTL Gain} = -2 \times \frac{R_f}{R_i} \quad (1)$$

$$\text{SE Gain} = -\frac{R_f}{R_i} \quad (2)$$

BTL mode operation brings the factor of 2 in the gain equation due to the inverting amplifier mirroring the voltage swing across the load. The input resistance will affect the low frequency performance of audio signal.

Input Capacitor (C_i)

In the typical application, an input capacitor (C_i) is required to allow the amplifier to bias the input signal to the proper DC level for optimum operation. In this case, C_i and the minimum input impedance R_i from a high-pass filter with the corner frequency are determined in the following equation:

$$F_{C(\text{highpass})} = \frac{1}{2\pi R_i C_i} \quad (3)$$

The value of C_i is important to consider as it directly affects the low frequency performance of the circuit. Consider the example where R_i is 20KΩ and the specification calls for a flat bass response down to 40Hz. Equation is reconfigured as followed:

$$C_i = \frac{1}{2\pi R_i F_C} \quad (4)$$

Consider to input resistance variation, the C_i is 0.2µF, so one would likely choose a value in the range of 0.22µF to 1.0µF. A further consideration for this capacitor is the leakage path from the input source through the input network (R_i +R_f, C_i) to the load.

This leakage current creates a DC offset voltage at the input to the amplifier that reduces useful headroom, especially in high gain applications. For this reason, a low-leakage tantalum or ceramic capacitor is the best choice. When polarized capacitors are used, the positive side of the capacitor should face the amplifier input in most applications as the DC level is held at V_{DD}/2, which is likely higher than the source DC level. Please note that it is important to confirm the capacitor polarity in the application.

Effective Bypass Capacitor (C_B)

As other power amplifiers, proper supply bypassing is critical for low noise performance and high power supply rejection. The capacitors located on the bypass and power supply pins should be as close to the device as possible. The effect of a larger half-supply bypass capacitor will improve PSRR due to increased half-supply stability. Typical application employs a 5V regulator with 1.0µF and a 0.1µF bypass as supply filtering. This does not eliminate the need for bypassing the supply nodes of the APA2036. The selection of bypass capacitors, especially C_B, thus depends upon desired PSRR requirements, click-and-pop performance.

To avoid start-up pop noise occurred, the bypass voltage should rise slower than the input bias voltage and the relationship shown in equation (5) should be maintained.

$$C_B \frac{V_B}{20\mu} + 0.4 > 3R_iC_i \quad (5)$$

The bypass capacitor is fed from a 160KΩ resistor inside the amplifier. Bypass capacitor, C_B, values of 1µF to 2.2µF ceramic or tantalum low-ESR capacitors are recommended for the best THD+N and noise performance. The bypass capacitance also effects the start up time. It is determined in the following equation:

$$T_{\text{start-up}} = C_B \frac{V_B}{20\mu} + 0.4 \quad (6)$$

$$\text{Note}: V_B = \frac{1}{2} V_{DD}$$

For example, if C_B=2.2µF, V_{DD}=5V, then the start-up time is 0.68s.

Output Coupling Capcaitor (C_C)

In the typical single-supply SE configuration, an output coupling capacitor (C_C) is required to block the DC bias at the output of the amplifier thus preventing DC currents in the load. As with the input coupling capacitor, the output coupling capacitor and impedance of the load form a high-pass filter governed by following equation:

$$F_{C(\text{highpass})} = \frac{1}{2\pi R_L C_C} \quad (7)$$

For example, a 330µF capacitor with an 8Ω speaker would attenuate low frequencies below 60.6Hz. The main disadvantage, from a performance standpoint, is typically small load impedance, which drives the low-frequency corner higher degrading the bass response. Large values of C_C are required to pass low frequencies into the load.

Application Information (Cont.)

Power Supply Decoupling (C_S)

The APA2036 is a high-performance CMOS audio amplifier that requires adequate power supply decoupling to ensure the output total harmonic distortion (THD+N) is as low as possible. Power supply decoupling also prevents the oscillations causing by long lead length between the amplifier and the speaker.

The optimum decoupling is achieved by using two different capacitors that target on different types of noise on the power supply leads. For higher frequency transients, spikes, or digital hash on the line, a good low equivalent-series-resistance (ESR) ceramic capacitor, typically 0.1µF is placed as close as possible to the device VDD lead works best. For filtering lower frequency noise signals, a large aluminum electrolytic capacitor of 10µF or greater placed near the audio power amplifier is recommended.

Optimizing Depop Circuitry

Circuitry has been included in the APA2036 to minimize the amount of popping noise at power-up while not in shutdown mode. Popping occurs whenever a voltage step is applied to the speaker. In order to eliminate click-and-pop, all capacitors must be fully discharged before turn-on.

Rapid on/off switching of the device or the shutdown function will cause the click-and-pop circuitry. The value of C_i will also affect turn-on pops (refer to Effective Bypass Capacitance). The bypass voltage rises up but should be slower than input bias voltage. Although the bypass pin current source cannot be modified, the size of C_B can be changed to alter the device turn-on time and the amount of click-and-pops. By increasing the value of C_B, turn-on pop can be reduced. However, the tradeoff for using a larger bypass capacitor is to increase the turn-on time for this device. There is a linear relationship between the size of C_B and the turn-on time.

In a SE configuration, the output coupling capacitor (C_C) is the particular concern. This capacitor discharges through the internal 10KΩ resistors. Depending on the size of C_C, the time constant can be relatively large. To reduce transients in SE mode, an external 1KΩ resistor can be placed in parallel with the internal 10KΩ resistor. The tradeoff for using this resistor is an increase in quiescent current.

In the most cases, choosing a small value of C_i in the range of 0.22µF to 1µF and C_B being equal to 2.2µF should cause a virtually click-less and pop-less turn-on.

A high gain amplifier intensifies the problem as the small delta in voltage is multiplied by the gain. Therefore it is advantageous to use low-gain configurations.

BTL Amplifier Efficiency

An easy-to-use equation to calculate efficiency starts out as being equal to the ratio of power from the power supply to the power is delivered to the load. The following equations are the basis for calculating amplifier efficiency.

$$\text{Efficiency} = \frac{P_O}{P_{SUP}} \quad (8)$$

where:

$$P_O = \frac{V_{O.RMS}^2}{R_L} = \frac{V_P^2}{2R_L} \quad (9)$$

$$V_{O.RMS} = \frac{V_P}{\sqrt{2}} \quad (10)$$

$$P_{SUP} = V_{DD} \times I_{DD.AVG} = V_{DD} \frac{2V_P}{\pi R_L} \quad (11)$$

Efficiency of a BTL configuration:

$$\frac{P_O}{P_{SUP}} = \frac{\frac{V_P^2}{2R_L}}{V_{DD} \times \frac{2V_P}{\pi R_L}} = \frac{\pi V_P}{4V_{DD}} \quad (12)$$

Table 1 is for calculating efficiency for four different output power levels.

Note that the efficiency of the amplifier is quite low for lower power levels and rises sharply as power to the load is increased resulting in nearly flat internal power dissipation over the normal operating range. In addition, the internal dissipation at full output power is less than in the half power range. Calculating the efficiency for a specific system is the key to proper power supply design. For a stereo 1W audio system with 8Ω loads and a 5V supply, the maximum draw on the power supply is almost 3W. In the equation, V_{DD} is in the denominator. One last key point to remember about linear amplifiers (either SE or BTL) is how to manipulate the terms in the efficiency equation to utmost advantage when possible. Note that in equation (12), V_{DD} is in the denominator. This indicates that as V_{DD} goes down, and efficiency goes up. In other words, choosing the correct supply voltage and speaker impedance for the application by using the efficiency analysis.

Application Information (Cont.)

BTL Amplifier Efficiency (Cont.)

P_O (W)	Efficiency (%)	I_{DD} (A)	V_{PP} (V)	P_O (W)
0.25	30.37	0.16	2.00	0.57
0.50	43.37	0.23	2.83	0.65
1.00	61.65	0.32	4.00	0.62
1.25	69.03	0.36	4.47	0.56

* *High peak voltages cause increasing of the THD+N.

Table 1. Efficiency vs. Output Power in 5-V/8Ω Differential Amplifier Systems

Power Dissipation

Whether the power amplifier is operated in BTL or SE modes, power dissipation is a major concern. Equation (13) states the maximum power dissipation point for a SE mode operating at a given supply voltage and driving a specified load.

$$\text{SE mode}: P_{D,MAX} = \frac{V_{DD}^2}{2\pi^2 R_L} \quad (13)$$

In BTL mode operation, the output voltage swing is doubled in SE mode. Thus the maximum power dissipation point for a BTL mode operated at the same given conditions is 4 times in SE mode.

$$\text{BTL mode}: P_{D,MAX} = 2\frac{V_{DD}^2}{\pi^2 R_L} \quad (14)$$

Even with this substantial increase in power dissipation, the APA2036 does not require extra heatsinking. The power dissipation from equation (14), assuming a 5V power supply and an 8Ω load, must not be greater than the power dissipation that results from the equation (15):

$$P_{D,MAX} = \frac{T_{J,MAX} - T_A}{\theta_{JA}} \quad (15)$$

Since the maximum junction temperature ($T_{J.MAX}$) of the APA2036 is 150°C and the ambient temperature (T_A) is defined by the power system design, the maximum power dissipation, which the IC package is able to handle, can be obtained from equation (15). Once the power dissipation is greater than the maximum limit ($P_{D,Max}$), the supply voltage (V_{DD}) must be decreased, the load impedance (R_L) must be increased or the ambient temperature should be reduced.

Thermal Consideration

Linear power amplifiers dissipates a significant amount of heat in the package in normal operating condition. The first consideration to calculate maximum ambient temperatures is the numbers from the Power Dissipation vs. Output Power graphs are per channel values, so the dissipation of the IC heat needs to be doubled for two-channel operation. Given θ_{JA}, the maximum allowable junction temperature (T_{JMax}), the total internal dissipation (P_D), and the maximum ambient temperature can be calculated with the following equation. The maximum recommended junction temperature for the APA2036 is 150°C. The internal dissipation figures are taken from the Power Dissipation vs. Output Power graphs.

$$T_{AMax} = T_{JMax} - \theta_{JA} \times P_D \quad (16)$$

$$150 - 45\ (0.8 \times 2) = 78°C$$

The APA2036 is designed with a thermal shutdown protection that turns the device off when the junction temperature surpasses 150°C to prevent damaging the IC.

Layout Consideration

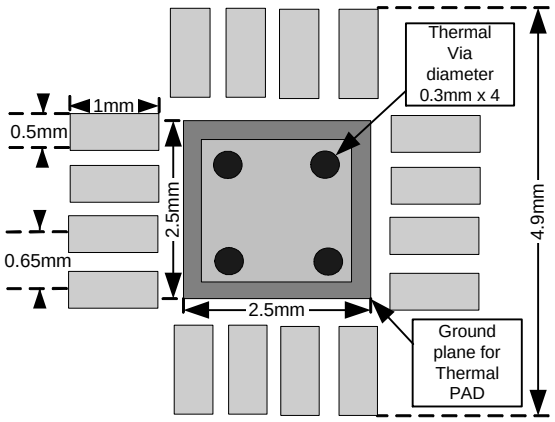


Figure 3: TQFN4x4-16 Land Pattern Recommendation

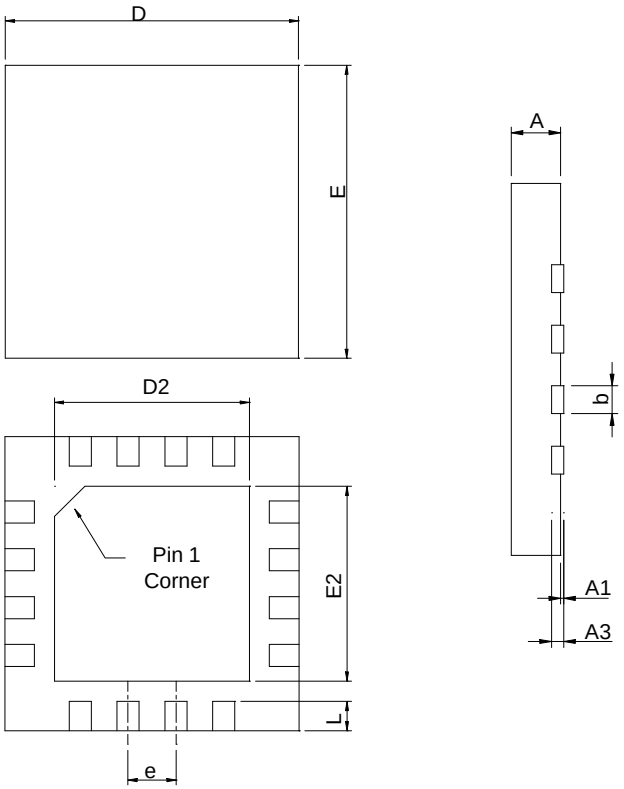
Application Information (Cont.)

Layout Consideration (Cont.)

1. All components should be placed close to the APA2036. For example, the input capacitor (C_i) should be close to APA2036's input pins to avoid causing noise coupling to APA2036's high impedance inputs; the decoupling capacitor (C_S) should be placed by the APA2036's power pin to decouple the power rail noise.
2. The output traces should be short, wide (>50mil) and symmetric.
3. The input trace should be short and symmetric.
4. The power trace width should be greater than 50mil.
5. The TQFN4X4-16 Thermal PAD should be soldered on PCB, and the ground plane needs soldered mask (to avoid short circuit) except the Thermal PAD area.

Package Information

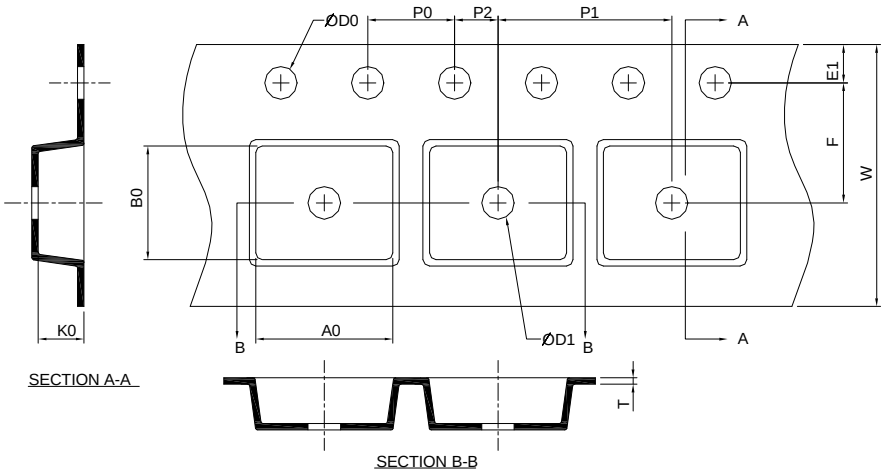
TQFN4x4-20

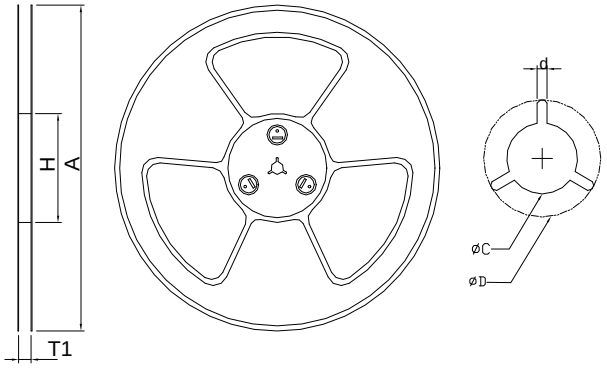


SYMBOL	TQFN4x4-16			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	0.70	0.80	0.028	0.031
A1	0.00	0.05	0.000	0.002
A3	0.20 REF		0.008 REF	
b	0.25	0.35	0.010	0.014
D	4.00 BSC		0.157 BSC	
D2	2.50	2.80	0.098	0.110
E	4.00 BSC		0.157 BSC	
E2	2.50	2.80	0.098	0.110
e	0.65 BSC		0.026 BSC	
L	0.30	0.50	0.012	0.020

Note : Follow JEDEC MO-220 WGGC-3.

Carrier Tape & Reel Dimensions





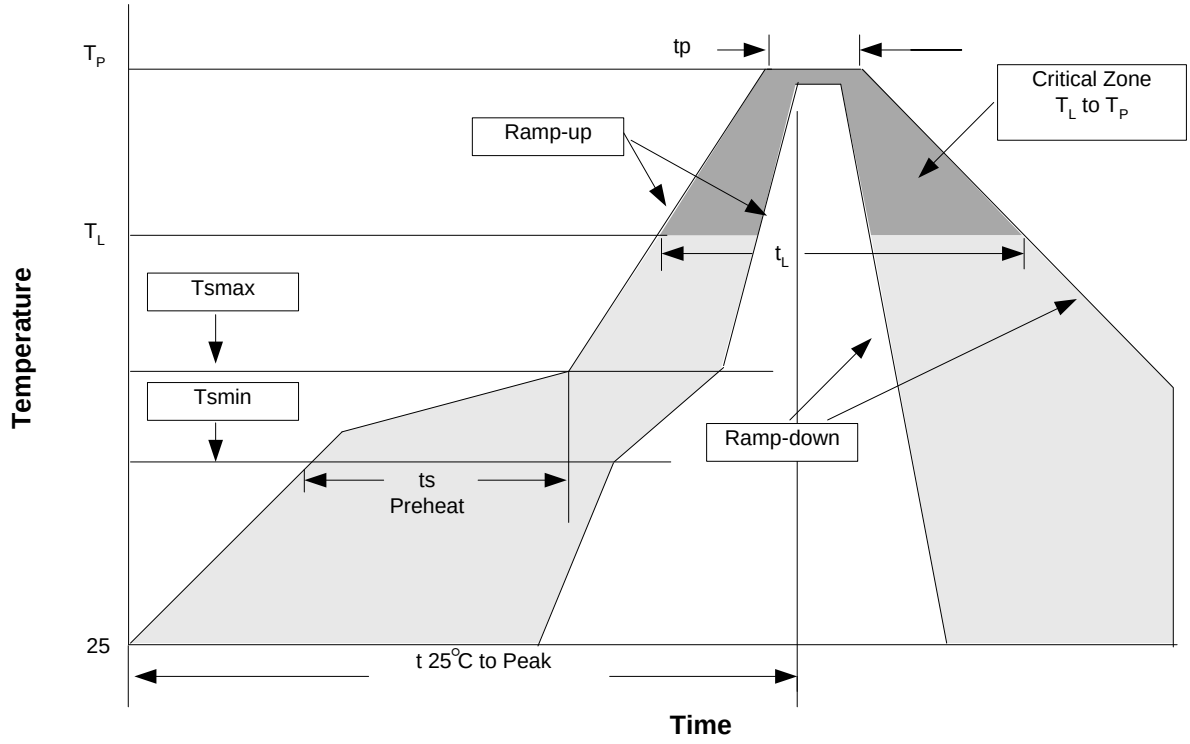
Application	A	H	T1	C	d	D	W	E1	F
TQFN 4x4-16	330.0±2.00	50 MIN.	12.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	12.0±0.30	1.75±0.10	5.5±0.10
	P0	**P1**	**P2**	**D0**	**D1**	**T**	**A0**	**B0**	**K0**
	4.0±0.10	8.0±0.10	2.0±0.10	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.40	4.30±0.20	4.30±0.20	1.30±0.20

(mm)

Devices Per Unit

Package Type	Unit	Quantity
TQFN4x4-16	Tape & Reel	3000

Reflow Condition (IR/Convection or VPR Reflow)



Reliability Test Program

Test item	Method	Description
SOLDERABILITY	MIL-STD-883D-2003	245°C, 5 sec
HOLT	MIL-STD-883D-1005.7	1000 Hrs Bias @125°C
PCT	JESD-22-B,A102	168 Hrs, 100%RH, 121°C
TST	MIL-STD-883D-1011.9	-65°C~150°C, 200 Cycles
ESD	MIL-STD-883D-3015.7	VHBM > 2KV, VMM > 200V
Latch-Up	JESD 78	10ms, 1_{tr} > 100mA

Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Average ramp-up rate (T_L to T_P)	3°C/second max.	3°C/second max.
Preheat - Temperature Min (Tsmin) - Temperature Max (Tsmax) - Time (min to max) (ts)	100°C 150°C 60-120 seconds	150°C 200°C 60-180 seconds
Time maintained above: - Temperature (T_L) - Time (t_L)	183°C 60-150 seconds	217°C 60-150 seconds
Peak/Classification Temperature (Tp)	See table 1	See table 2
Time within 5°C of actual Peak Temperature (tp)	10-30 seconds	20-40 seconds
Ramp-down Rate	6°C/second max.	6°C/second max.
Time 25°C to Peak Temperature	6 minutes max.	8 minutes max.

Note: All temperatures refer to topside of the package. Measured on the body surface.

Classification Reflow Profiles (Cont.)

Table 1. SnPb Eutectic Process – Package Peak Reflow Temperatures

Package Thickness	Volume mm^3 <350	Volume mm^3 ³350
<2.5 mm	240 +0/-5°C	225 +0/-5°C
≥2.5 mm	225 +0/-5°C	225 +0/-5°C

Table 2. Pb-free Process – Package Classification Reflow Temperatures

Package Thickness	Volume mm^3 <350	Volume mm^3 350-2000	Volume mm^3 >2000
<1.6 mm	260 +0°C*	260 +0°C*	260 +0°C*
1.6 mm – 2.5 mm	260 +0°C*	250 +0°C*	245 +0°C*
≥2.5 mm	250 +0°C*	245 +0°C*	245 +0°C*
* Tolerance: The device manufacturer/supplier **shall** assure process compatibility up to and including the stated classification temperature (this means Peak reflow temperature +0°C. For example 260°C+0°C) at the rated MSL level.			

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