MVS Series

9x14 mm, 5.0 Volt, HCMOS/TTL, VCXO









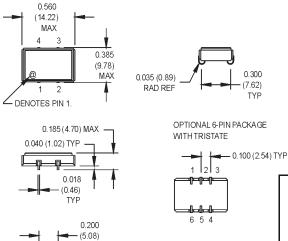
 General purpose VCXO for Phase Lock Loops (PLL), Clock Recovery, Reference Signal Tracking and Synthesizers

0.100 (2.54)

 \mathbf{H} \mathbf{H}

HHH

• Frequencies up to 160 MHz and tri-state option



All dimensions in inches (mm).

SUGGESTED SOLDER PAD LAYOUT

0.118 (3.00)

FUNCTION

Tristate

Output

N/C

+Vdd

Control Voltage

Circuit/Case Ground

-0.200 (5.08)

Pin Connections

0.346 (8.80)

4 Pin

Pkg.

2

3

6 Pin

Pkg.

1

3

4

5

6

	MVS 1	3 V	2	С	J	00.00 MH
Product Series ————————————————————————————————————					***************************************	
Stability		1				
1: ±1000 ppm 3: ±100 ppm 5: ±35 ppm	4: ±50 ppm					
*8: ±20 ppm						
Output Type ———						
V: Voltage Controlled						
Pull Range (Vc = .5 to	0 4.5 V) ————					
1: ±50 ppm min.	- 1 - 70 000 MILL-)					
2: ±100 ppm min. (U						
Symmetry/Logic Con A: 40/60 CMOS/TTL						
Package/Lead Config						
J: J Lead	,					
RoHS Compliance -						
Blank: non-RoHS co						

*Contact factory for availability.
M3001Sxxx - Contact factory for datasheet.

	PARAMETER	Symbol	Min.	Тур.	Max.	Units	Condition/Notes	
Specifications	Frequency Range	F	1.544	тур.	160	MHz	See Note 1	
	Operating Temperature	T _A	(See ordering information)			000 11010 1		
	Storage Temperature	Ts	-55	(000 0.40.	+125	·c		
	Frequency Stability	ΔF/F		(See orde	ing inform			
	Aging	2171		(000 0140	nig miorini	I		
	1 st Year		-3/-5		+3/+5	ppm	<52 MHz / >=52MHz	
	Thereafter (per year)		-1/-2		+1/+2	ppm	<52 MHz / >=52MHz	
	Pullability/APR		(See ordering information)			Over Control Voltage		
	Control Voltage	Vc	0.5	2.5	4.5	Ιν	i	
	Linearity				10	%	Positive Monotonic Slope	
	Modulation Bandwidth	Fm	10			kHz	İ	
	Input Impedance	Zin	50k			Ohms		
	Input Voltage	Vdd	4.75	5.0	5.25	V		
	Input Current	ldd		25	35	mA	1.544 to 24.999 MHz	
				35	60	mA	25 to 9 9.999 MHz	
				55	90	mA	70 to 160 MHz	
	Output Type						HCMOS/TTL	
ectrical	Load	See No					See Note 2	
E E	1.544 to 45 MHz	10 TTL or 50 pF						
l ä	45.001 to 160 MHz		5 TTL or 30 pF					
	Symmetry (Duty Cycle)		(See ordering information)			See Note 3		
	Logic "1" Level	Voh	90% Vdd			V	HCMOS Load	
			Vdd -0.5			V	TTL Load	
	Logic "0" Level	Vol			10%	V	HCMOS Load	
					Vdd	1,,	l	
	Rise/Fall Time	T 71	<u> </u>		0.5	V	TTL Load	
		Tr/Tf	Januari I. aan	3	10	ns	See Note 4	
	Tristate Function		Input Logic "1" or floating: output active Input Logic "0": output disables to high-Z					
	Start up Time		10 ms				-	
	Phase Jitter @ 155.52 MHz	φJ		10	15	ps RMS	Integrated 12 kHz – 20 MHz	
	Phase Noise (Typical)	φ3 10 Hz	100 Hz	1 kHz	10 kH		Offset from carrier	
	@155.52 MHz	-62	-93	-113	-115	-114	dBc/Hz	
\vdash	@ <u>.</u>	<u> </u>	00	110	110	1	450,112	
tal	Mechanical Shock	Per MIL-STD-202, Method 213, Condition C (100 g's, 6 mS duration, ½ sinewave)						
Environmental	Vibration	Per MIL-STD-202, Method 201 & 204 (10 g's from 10-2000 Hz)						
E	Hermeticity	Per MIL-STD-202, Method 112, (1x10-8 atm. cc/s of Helium)						
ੂੰ	Solderability	Per EIAJ-STD-002						
[2	Max Soldering Conditions	See solder profile, Figure 1						
1"	ÿ							

- 1. Frequencies above 90 MHz utilize a PLL design. Fundamental and PLL designs are available at other frequencies.
- Contact factory for availability.
 2. TTL load see load circuit diagram #1. HCMOS load see load circuit diagram #2.
- 3. Symmetry is measured at 1.4 V with TTL load, and at 50% Vdd with HCMOS load.
- 4. Rise/Fall times are measured between 0.5 V and 2.4 V with TTL load, and between 10% Vdd and 90% Vdd with HCMOS load.

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tasheets. Contact us for your application specific requirements: MtronPTI 1-800-762-8800.





