CMOS LDO Regulator Series for Portable Equipments

CMOS LDO Regulators with Auto Power Saving Function

BH□□PB1WHFV Series

No.09020EAT05

●Description

The BH□□PB1WHFV regulator series can respond to changes in output current by switching to a state in which regulator characteristics are ideal. The regulators cut power consumption by lowering their own current consumption to approximately 2 μA when the application is operating in the standby state. During normal-current operation it will automatically switch to high-speed operating mode. The IC's soft start function reduce the rush current that flows to the output capacitors during startup. The HVSOF5 package, which features excellent heat dissipation, contributes to space-saving application designs.

●Features

1) Automatic switching between low-consumption and high-speed modes
2) Built-in rush current prevention circuit
3) Low-voltage 1.7 V operation
4) High accuracy output voltage: ± 1%
5) Circuit current during low-consumption operation: 2 μA
6) Stable with a ceramic capacitor (0.47 μF)
7) Built-in temperature and overcurrent protection circuits
8) Built-in output discharge during standby operation function
9) Ultra-small HVSOF5 power package

●Applications

Battery-driven portable devices, etc.

●Product lineup

■150 mA BH□□PB1WHFV Series

Product name	1.2	1.5	1.8	2.5	2.8	2.9	3.0	3.1	3.3	Package
BH□□PB1WHFV	√	√	√	√	√	√	√	√	√	HVSOF5

Model name: BH□□PB1W□
a b

Symbol	Description			
a	Output voltage specification			
	□□	Output voltage (V)	□□	Output voltage (V)
	12	1.2 V (Typ.)	29	2.9 V (Typ.)
	15	1.5 V (Typ.)	30	3.0 V (Typ.)
	18	1.8 V (Typ.)	31	3.1 V (Typ.)
	25	2.5 V (Typ.)	33	3.3 V (Typ.)
	28	2.8 V (Typ.)		
b	Package HFV: HVSOF5			

●**Absolute maximum ratings (Ta = 25°C)**

Parameter	Symbol	Limits	Unit
Power supply voltage	VMAX	−0.3 to +6.5	V
Power dissipation	Pd	410 *1	mW
Operating temperature range	Topr	−40 to +85	°C
Storage temperature range	Tslg	−55 to +125	°C
Junction temperature	Tjmax	125	°C

*1: Reduced by 4.1 mW/°C over 25°C, when mounted on a glass epoxy board (70 mm × 70 mm × 1.6 mm)

●**Recommended operating ranges (not to exceed Pd)**

Parameter	Symbol	Limits	Unit
Power supply voltage	V_{IN}	1.7 to 5.5	V
Output MAX current	IMAX	0 to 150	mA

●**Recommended operating conditions**

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Input capacitor	C_{IN}	0.33 *2	0.47	−	μF	The use of ceramic capacitors is recommended.
Output capacitor	C_O	0.33 *2	0.47	−	μF	The use of ceramic capacitors is recommended.

*2: Make sure that the output capacitor value is not kept lower than this specified level across a variety of temperature, DC bias characteristic.
And also make sure that the capacitor value can not change as time progresses.

●**Electrical characteristics**

(Unless otherwise specified, Ta = 25°C, V_{IN} = V_{OUT} + 1.0 V, STBY = 1.5 V, SEL = 0 V, C_{IN} = 0.47 µF, C_O = 0.47 µF)

PARAMETER		Symbol	Limit MIN.	Limit TYP.	Limit MAX.	Unit	Conditions
【Regulator】							
Output voltage (high-speed mode)		$V_{OUT}1$	VOUT1×0.99	-	VOUT1×1.01	V	V_{OUT}≧2.5V,I_{OUT}=0.1mA,SEL=1.5V
			VOUT1-0.025	-	VOUT1+0.025	V	V_{OUT}≦1.8V,I_{OUT}=0.1mA,SEL=1.5V
Output voltage (low-consumption mode)		$V_{OUT}2$	VOUT2×0.97	-	VOUT2×1.038	V	V_{OUT}≧2.5V,I_{OUT}=0.1mA,SEL=0V
			VOUT2×0.967	-	VOUT2×1.043	V	V_{OUT}≦1.8V,I_{OUT}=0.1mA,SEL=0V
Circuit current (high-speed mode)		ICC1	-	20	40	µA	I_{OUT}=0mA, V_{IN} pin monitor,SEL=1.5V
Circuit current (low-consumption mode)		ICC2	-	2	4	µA	I_{OUT}=0mA, V_{IN} pin monitor, SEL=0V
Circuit current (STBY)		ISTBY	-	-	1.0	µA	STBY=0V
Ripple rejection ratio (high-speed mode)		RR1	42	60	-	dB	VRR=-20dBv, fRR=1kHz, I_{OUT}=10mA, SEL=1.5V
Dropout voltage 1 *1		VSAT1	-	100	200	mV	V_{IN}=VOUT×0.98,IOUT=50mA
Dropout voltage 2 *1		VSAT2	-	210	400	mV	V_{IN}=VOUT×0.98,I_{OUT}=100mA
Dropout voltage 3 *1		VSAT3	-	315	600	mV	V_{IN}=VOUT×0.98,I_{OUT}=150mA
Line regulation 1 (high-speed mode)		VDL1	-	2	20	mV	V_{IN}=VOUT+1V to 5.5V,I_{OUT}=10mA
Line regulation 2 (low-consumption mode)		VDL2	-	2	20	mV	V_{IN}=V_{OUT}+1V to 5.5V,I_{OUT}=100µA
Load regulation		VDLO	-	10	40	mV	I_{OUT}=10mA to 100mA
【Mode switch】							
Current threshold (low-consumption mode)		ITH1	0.09	0.3	-	mA	SEL=0V I_{OUT}=3mA⇒0mA sweep
Current threshold (high-speed mode)		ITH2	-	1.2	2.2	mA	SEL=0V I_{OUT}=0mA⇒3mA sweep
【Over Current Protection 1】							
Limit Current		ILMAX	160	300	500	mA	Vo=V_{OUT}×0.90
Short current		ISHORT	20	50	100	mA	Vo=0V
【Stand-by block】							
STBY pin sink current		ISTB	-	2	4	µA	STBY=1.5V
STBY control voltage	ON	VSTBH	1.5	-	V_{IN}	V	
	OFF	VSTBL	-0.3	-	0.3	V	
Discharge resistance at standby		RDCG	1.5	2.2	3.0	kΩ	STBY=0V
【SEL PIN】							
Pull-down resistance of SEL pin		RSEL	0.5	1.0	2.0	MΩ	
SEL control voltage	ON	VSELH	1.5	-	V_{IN}	V	Fixed high speed mode
	OFF	VSELL	-0.3	-	0.3	V	Automatic switch mode

* Note: This IC is not designed to be radiation-resistant. *3: Except at VOUT ≤ 1.5 V.

●**Electrical characteristics of each output voltage**

Output Voltage	Parameter	Min.	Typ.	Max.	Unit	Conditions
1.2 V	Max. output current	70	120	−	mA	VCC = 1.7 V
		150	−	−		VCC = 2.0 V
1.5 V		50	100	−		VCC = 1.8 V
		150	−	−		VCC = 2.2 V
1.8 V ≤ V_{OUT}		75	143	−		VCC = V_{OUT} + 0.3 V
		150	−	−		VCC = V_{OUT} + 0.6 V

●**Typical characteristics**

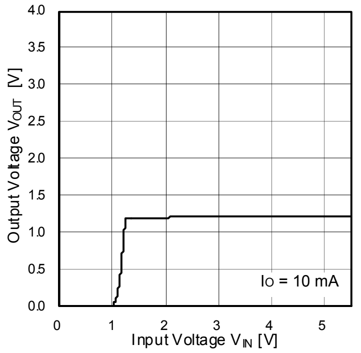


Fig. 1 Output Voltage vs Input Voltage (BH12PB1WHFV)

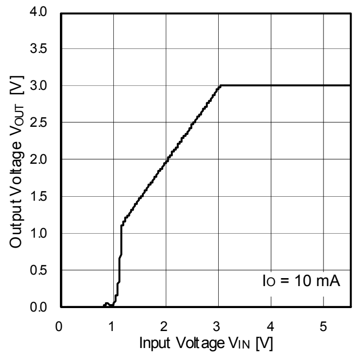


Fig. 2 Output Voltage vs Input Voltage (BH30PB1WHFV)

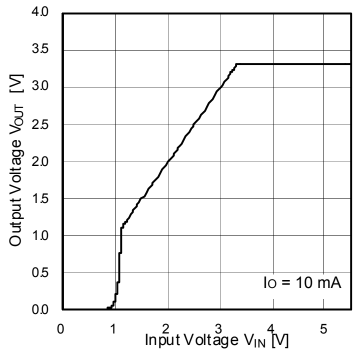


Fig. 3 Output Voltage vs Input Voltage (BH33PB1WHFV)

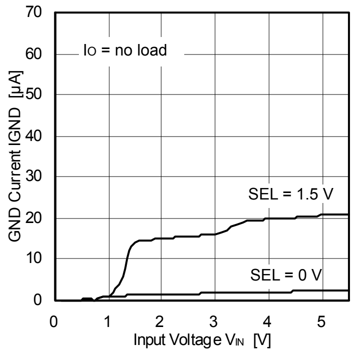
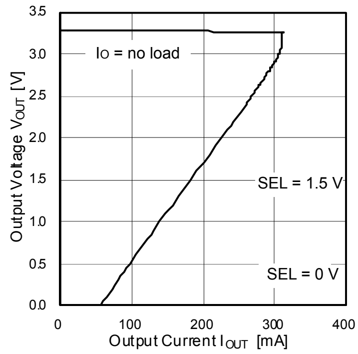


Fig.4 GND Current vs Input Voltage (BH12PB1WHFV)



(BH33PB1WHFV)

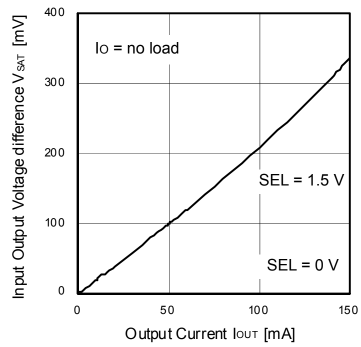


Fig.6 GND Current vs
─Input Voltage
(BH33PB1WHFV)

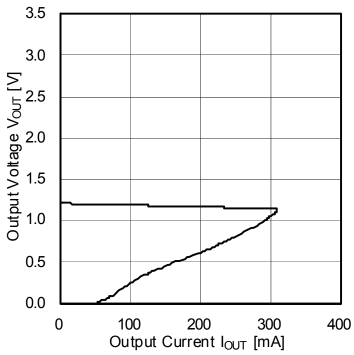


Fig. 7 Output Voltage vs Outout Current (BH12PB1WHFV)

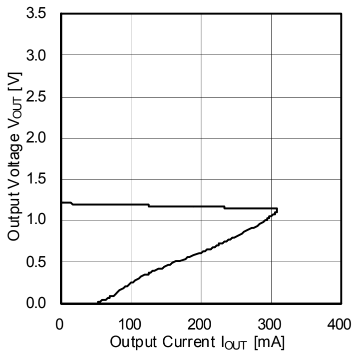
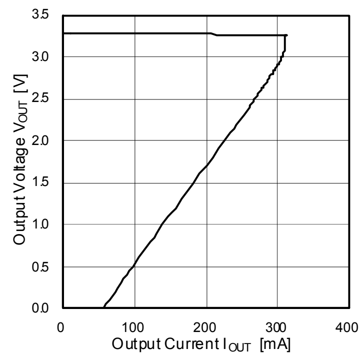


Fig.8 Output Voltage vs Output Current (BH30PB1WHFV)



(BH30PB1WHFV)
Output Current
(BH33PB1WHFV)

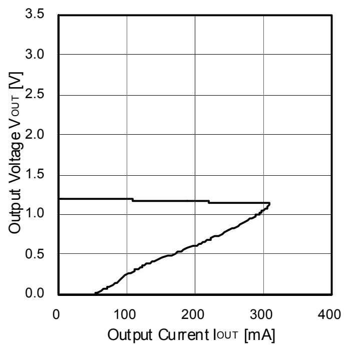


Fig. 10 Dropout voltage vs Output Current (BH18PB1WHFV)

Fig. 11 Dropout voltage vs Output Current (BH30PB1WHFV)

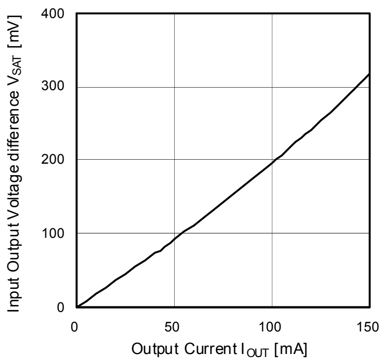


Fig. 12 Dropout voltage vs Output Current (BH33PB1WHFV)

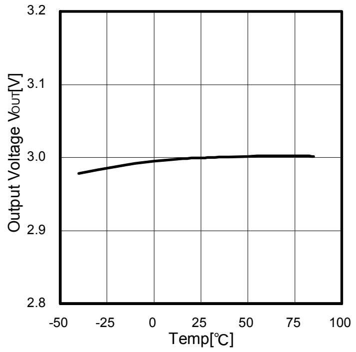


Fig. 13 Output Voltage vs Temperature (BH30PB1WHFV)

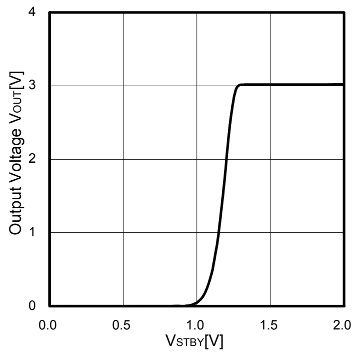


Fig. 14 Standby Pin Threshold (BH30PB1WHFV)

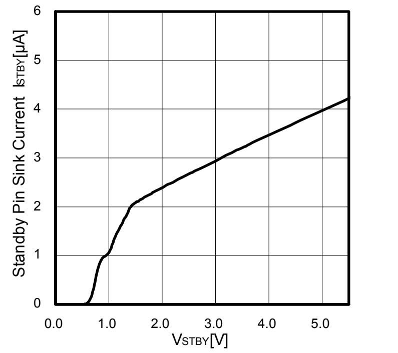


Fig. 15 Standby Pin Sink Current (BH30PB1WHFV)

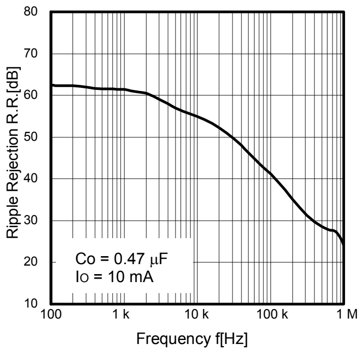


Fig. 16 Ripple Rejection (BH12PB1WHFV)

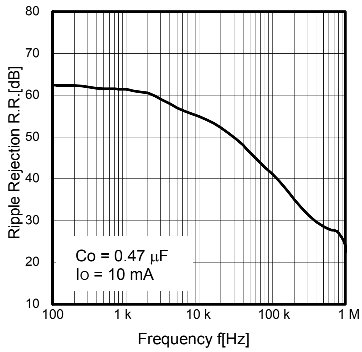


Fig. 17 Ripple Rejection (BH30PB1WHFV)

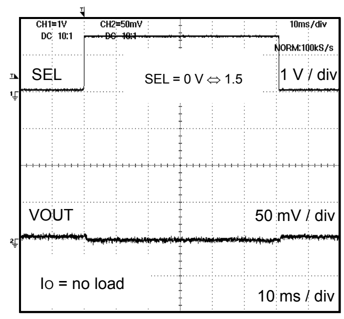


Fig. 18 Output Voltage Waveform During SEL Switching (BH30PB1WHFV)

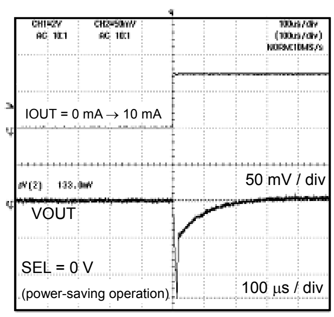


Fig. 19 Load Response (Co = 1.0 µF) (BH30PB1WHFV)

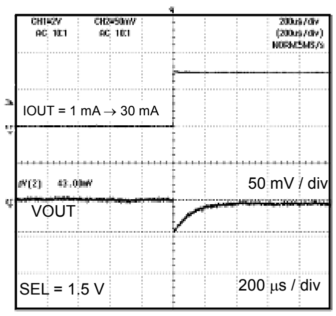


Fig. 20 Load Response (Co = 1.0 µF) (BH30PB1WHFV)

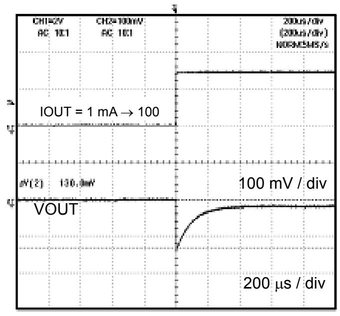


Fig. 21 Load Response (Co = 1.0 µF) (BH30PB1WHFV)

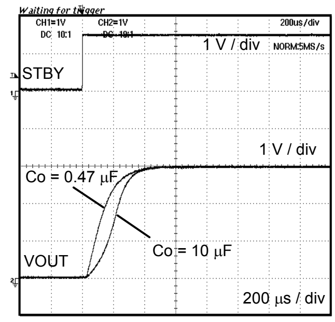


Fig. 22 Output Voltage Rise Time (BH30PB1WHFV)

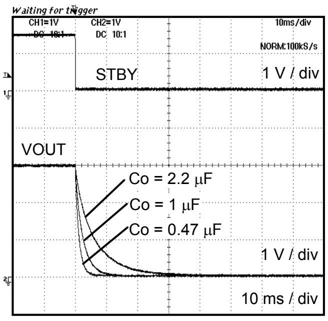


Fig. 23 Output Voltage Fall Time (BH30PB1WHFV)

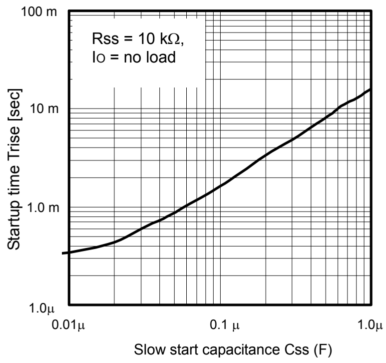
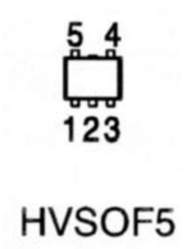


Fig. 24 Soft Start Rise Time (BH30PB1WHFV)

●Block diagram, recommended circuit diagram, and pin assignment table

BH□□PB1WHFV



PIN No.	Symbol	Function
1	STBY	Output voltage on/off control(High: ON, Low: OFF)
2	GND	Ground
3	VIN	Power supply input
4	VOUT	Voltage output
5	SEL	Mode switching (High: Fix in high-speed mode Low: Automatic low-consumption mode switching)

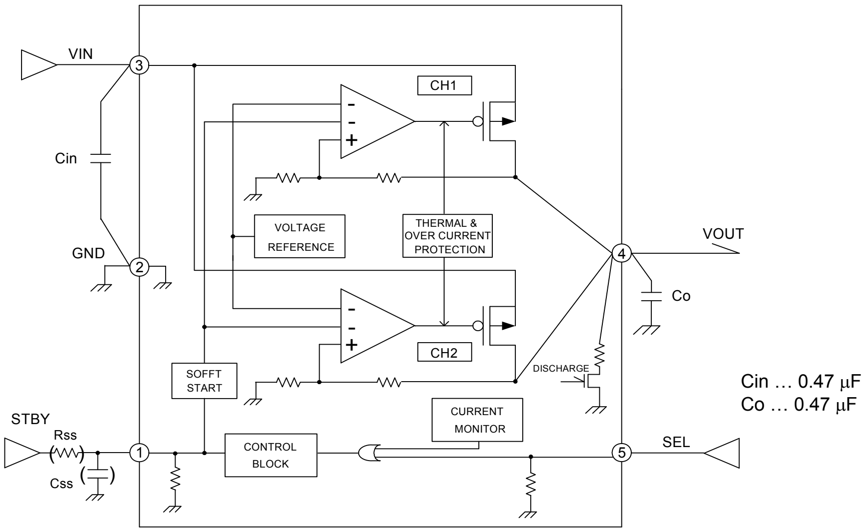


Fig. 25

●Auto Power-saving Function

The IC incorporates a built-in auto power-saving function that continuously monitors the output current and switches automatically between a low current consumption regulator and a high-speed operation regulator. This function reduces the regulator's own current consumption to approximately 1/10 or lower of normal levels when the output current falls below approximately 300 µA.
To operate only the high-speed operation regulator without using the auto power-saving function, fix the SEL pin to high.

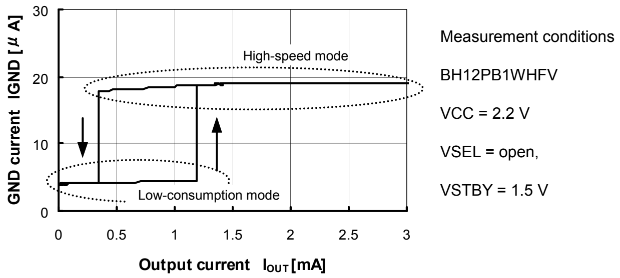


Fig. 26 Auto Power-Saving Function (Example)

●Power Dissipation (Pd)

1. Power Dissipation (Pd)

Power dissipation calculations include estimates of power dissipation characteristics and internal IC power consumption, and should be treated as guidelines. In the event that the IC is used in an environment where this power dissipation is exceeded, the attendant rise in the junction temperature will trigger the thermal shutdown circuit, reducing the current capacity and otherwise degrading the IC's design performance. Allow for sufficient margins so that this power dissipation is not exceeded during IC operation.

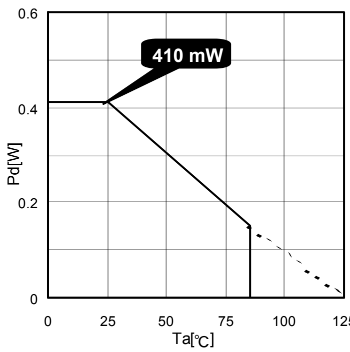
Calculating the maximum internal IC power consumption (PMAX)

$P_{MAX} = (V_{IN} - V_{OUT}) \times I_{OUT}$ (MAX.)

- V_{IN} : Input voltage
- V_{OUT} : Output voltage
- I_{OUT} (MAX) : Max. output current

2. Power Dissipation/Heat Reduction (Pd)

HVSOF5



*Circuit design should allow a sufficient margin for the temperature range so that PMAX < Pd.

Fig. 27 HVSOF5 Power Dissipation vs Heat Reduction (Example)

●**Input Output capacitors**

It is recommended to insert bypass capacitors between input and GND pins, positioning them as close to the pins as possible. These capacitors will be used when the power supply impedance increases or when long wiring paths are used, so they should be checked once the IC has been mounted.

Ceramic capacitors generally have temperature and DC bias characteristics. When selecting ceramic capacitors, use X5R or X7R, or better models that offer good temperature and DC bias characteristics and high tolerant voltages.

Typical ceramic capacitor characteristics

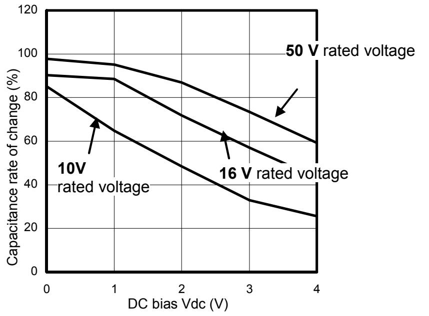


Fig. 28 Capacitance vs Bias (Y5V)

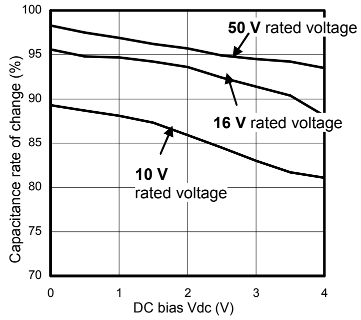


Fig. 29 Capacitance vs Bias (X5R, X7R)

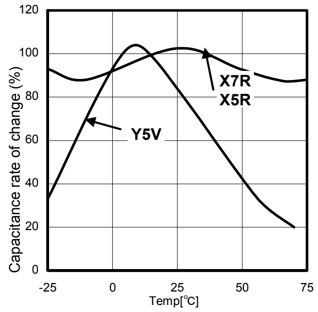


Fig. 30 Capacitance vs Temperature (X5R, X7R, Y5V)

●**Output capacitors**

Mounting input capacitor between input pin and GND(as close to pin as possible), and also output capacitor between output pin and GND(as close to pin as possible) is recommended.

The input capacitor reduces the output impedance of the voltage supply source connected to the VCC. The higher value the output capacitor goes, the more stable the whole operation becomes. This leads to high load transient response. Please confirm the whole operation on actual application board.

Generally, ceramic capacitor has wide range of tolerance, temperature coefficient, and DC bias characteristic. And also its value goes lower as time progresses. Please choose ceramic capacitors after obtaining more detailed data by asking capacitor makers.

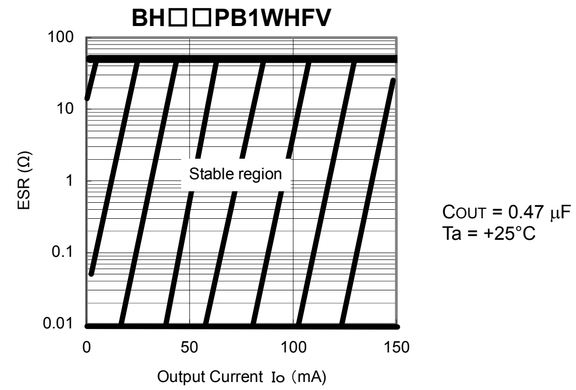


Fig. 31 Stable Operation Region (Example)

●**Operation Notes**

1. Absolute maximum ratings
   An excess in the absolute maximum ratings, such as supply voltage, temperature range of operating conditions, etc., can break down the devices, thus making impossible to identify breaking mode, such as a short circuit or an open circuit. If any over rated values will expect to exceed the absolute maximum ratings, consider adding circuit protection devices, such as fuses.
2. Thermal design
   Use a thermal design that allows for a sufficient margin in light of the power dissipation (Pd) in actual operating conditions.
3. Inter-pin shorts and mounting errors
   Use caution when positioning the IC for mounting on printed circuit boards. The IC may be damaged if there is any connection error or if pins are shorted together.
4. Thermal shutdown circuit (TSD)
   The IC incorporates a built-in thermal shutdown circuit (TSD circuit). The thermal shutdown circuit is designed only to shut the IC off to prevent runaway thermal operation. It is not designed to protect the IC or guarantee its operation. Do not continue to use the IC after operating this circuit or use the IC in an environment where the operation of this circuit is assumed.
5. Ground wiring patterns
   The power supply and ground lines must be as short and thick as possible to reduce line impedance. Fluctuating voltage on the power ground line may damage the device.

6. Overcurrent protection circuit
   The IC incorporates a built-in overcurrent protection circuit that operates according to the output current capacity. This circuit serves to protect the IC from damage when the load is shorted. The protection circuit is designed to limit current flow by not latching in the event of a large and instantaneous current flow originating from a large capacitor or other component. These protection circuits are effective in preventing damage due to sudden and unexpected accidents. However, the IC should not be used in applications characterized by the continuous operation or transitioning of the protection circuits. At the time of thermal designing, keep in mind that the current capability has negative characteristics to temperatures.
7. Actions in strong electromagnetic field
   Use caution when using the IC in the presence of a strong electromagnetic field as doing so may cause the IC to malfunction.
8. Back Current
   In applications where the IC may be exposed to back current flow, it is recommended to create a path to dissipate this current by inserting a bypass diode between the VIN and VOUT pins.

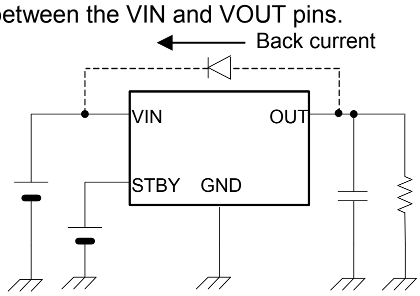


Fig. 32 Example Bypass Diode Connection

9. I/O voltage difference
   Using the IC in automatic switching mode when the I/O voltage differential becomes saturated (VIN - VOUT < 150 mV) may result in a large output noise level. If the noise level becomes problematic, use the IC with the SEL pin in the high state when the voltage differential is saturated.
10. GND Voltage
   The potential of GND pin must be minimum potential in all operating conditions.
11. Preventing Rush Current
   By attaching the Rss and Css time constants to the STBY pin, sudden rises in the regulator output voltage can be prevented, dampening the flow of rush current to the output capacitors. The larger the time constant used, the greater the resulting reduction. However, large time constants also result in longer startup times, so the constant should be selected after considering the conditions in which the IC is to be used.

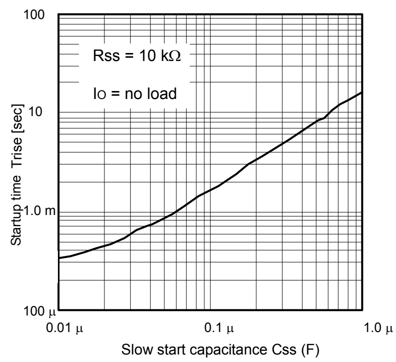


Fig. 33 VOUT Startup Time vs CSS Capacitance (Reference)

12. Regarding input Pin of the IC (Fig.34)
   This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of these P layers with the N layers of other elements, creating a parasitic diode or transistor. For example, the relation between each potential is as follows:
   When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
   When GND > Pin B, the P-N junction operates as a parasitic transistor.
   Parasitic diodes can occur inevitable in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Accordingly, methods by which parasitic diodes operate, such as applying a voltage that is lower than the GND (P substrate) voltage to an input pin, should not be used.

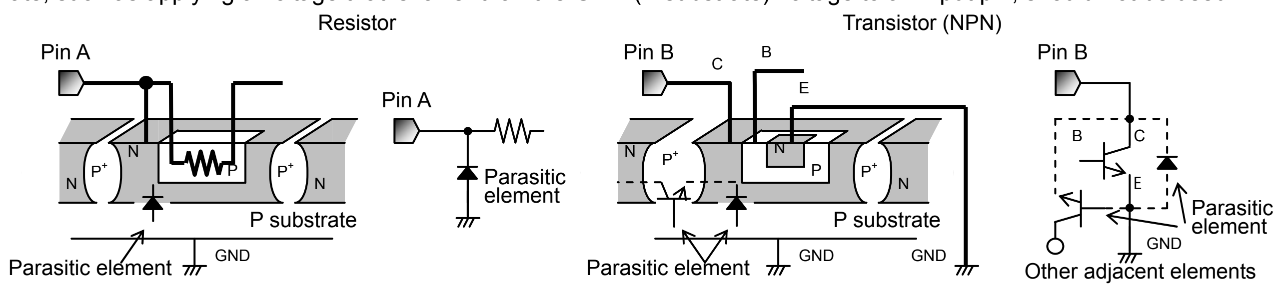
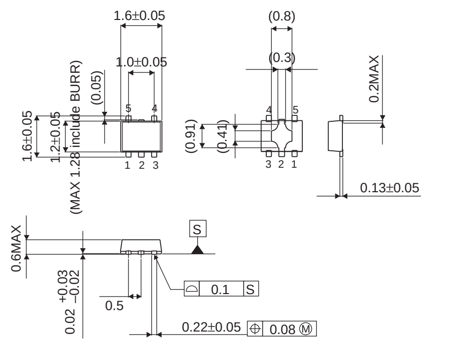


Fig.34

●Ordering part number

B H	3 0	P B 1	W	H F V	-	T R
Part No.	Output voltage	Series PB1:Auto power-saving type	Shutdown switch W : Includes switch	Package HFV : HVSOF5		Packaging and forming specification TR: Embossed tape and reel

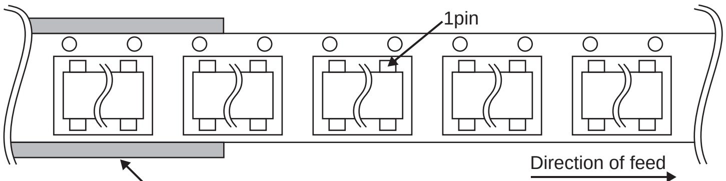
HVSOF5



(Unit : mm)

<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	3000pcs
Direction of feed	TR (The direction is the 1pin of product is at the upper right when you hold reel on the left hand and you pull out the tape on the right hand)



∗Order quantity needs to be multiple of the minimum quantity.

Notes

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