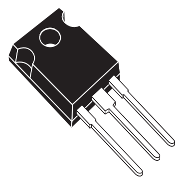
STGW30NC60WD

N-channel 30A - 600V - TO-247
Ultra fast switching PowerMESH™ IGBT

Features

Type	V_{CES}	$V_{CE(sat)}$Max @25°C	I_C @100°C
STGW30NC60WD	600V	< 2.5V	30A

- High frequency operation
- Lower C_{RES} / C_{IES} ratio (no cross-conduction susceptibility)
- Very soft ultra fast recovery antiparallel diode

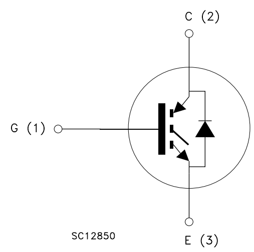


TO-247

Description

Using the latest high voltage technology based on a patented strip layout, STMicroelectronics has designed an advanced family of IGBTs, the PowerMESH™ IGBTs, with outstanding performances. The suffix “W” identifies a family optimized for very high frequency application.

Figure 1. Internal schematic diagram



Applications

- High frequency motor controls, inverters, ups
- HF, SMPS and PFC in both hard switch and resonant topologies

Table 1. Device summary

Order code	Marking	Package	Packaging
STGW30NC60WD	GW30NC60WD	TO-247	Tube

Contents

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CES}	Collector-emitter voltage (V_{GS} = 0)	600	V
I_C	Collector current (continuous) at 25°C	60	A
I_C	Collector current (continuous) at 100°C	30	A
I_{CM} (1)	Collector current (pulsed)	200	A
V_{GE}	Gate-emitter voltage	± 20	V
P_{TOT}	Total dissipation at T_C = 25°C	200	W
T_{stg}	Storage temperature	– 55 to 150	°C
T_j	Operating junction temperature		
T_L	Maximum lead temperature for soldering purpose (1.6mm from case, for 10 sec.)	300	°C

1. Pulse width limited by max junction temperature

Table 3. Thermal resistance

Symbol	Parameter	Min.	Typ.	Max.	Unit
Rthj-case	Thermal resistance junction-case			0.625	°C/W
Rthj-amb	Thermal resistance junction-ambient			62.5	°C/W

2 Electrical characteristics

(T_{CASE}=25°C unless otherwise specified)

Table 4. Static electrical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{BR(CES)}$	Collector-emitter breakdown voltage	I_C = 1mA, V_{GE} = 0	600			V
$V_{CE(SAT)}$	Collector-emitter saturation voltage	V_{GE}=15V, I_C= 20A, Tj= 25°C V_{GE}=15V, I_C= 20A,Tj= 125°C		2.1 1.8	2.5	V V
$V_{GE(th)}$	Gate threshold voltage	V_{CE}= V_{GE}, I_C= 250µA	3.75		5.75	V
I_{CES}	Collector-emitter leakage current (V_{GE} = 0)	V_{CE} = Max Rating,Tc=25°C V_{CE} = Max Rating, Tc=125°C			10 1	µA mA
I_{GES}	Gate-emitter leakage current (V_{CE} = 0)	V_{GE} = ±20V, V_{CE} = 0			± 100	nA
g_{fs}	Forward transconductance	V_{CE} = 15V, I_C= 20A		15		S

Table 5. Dynamic electrical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{ies} C_{oes} C_{res}	Input capacitance Output capacitance Reverse transfer capacitance	V_{CE} = 25V, f = 1MHz, V_{GE}=0		2080 175 52		pF pF pF
Q_g Q_{ge} Q_{gc}	Total gate charge Gate-emitter charge Gate-collector charge	V_{CE} = 390V, I_C = 20A, V_{GE} = 15V, *(see Figure 17)*		102 17.5 47	140	nC nC nC
I_{CL}	Turn-Off SOA minimum current	V_{clamp} = 480V , Tj = 150°C R_G = 10Ω, V_{GE}= 15V	200			A

Table 6. Switching on/off (inductive load)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r $(di/dt)_{on}$	Turn-on delay time Current rise time Turn-on current slope	V_{CC} = 390V, I_C = 20A R_G= 10Ω, V_{GE}= 15V, T_J= 25°C *(see Figure 17)*		29.5 12 1640		ns ns A/µs
$t_{d(on)}$ t_r $(di/dt)_{on}$	Turn-on delay time Current rise time Turn-on current slope	V_{CC} = 390V, I_C = 20A R_G= 10Ω, V_{GE}= 15V, T_J= 125°C *(see Figure 17)*		29 13.5 1600		ns ns A/µs
$t_r(V_{off})$ $t_d(_{off})$ t_f	Off voltage rise time Turn-off delay time Current fall time	V_{cc} = 390V, I_C = 20A, R_{GE} = 10Ω, V_{GE}=15V,T_J=25°C *(see Figure 19)*		19.5 118 27		ns ns ns
$t_r(V_{off})$ $t_d(_{off})$ t_f	Off voltage rise time Turn-off delay time Current fall time	V_{cc} = 390V, I_C = 20A, R_{GE}=10Ω, V_{GE} =15V, T_J=125°C *(see Figure 19)*		46 151 38		ns ns ns

Table 7. Switching energy (inductive load)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
E_{on} (1) E_{off} (2) E_{ts}	Turn-on switching losses Turn-off switching losses Total switching losses	V_{CC} = 390V, I_C = 20A R_G= 10Ω, V_{GE}= 15V, Tj= 25°C *(see Figure 19)*		305 181 486		µJ µJ µJ
E_{on} (1) E_{off} (2) E_{ts}	Turn-on switching losses Turn-off switching losses Total switching losses	V_{CC} = 390V, I_C = 20A R_G= 10Ω, V_{GE}= 15V, Tj= 125°C *(see Figure 19)*		455 355 801		µJ µJ µJ

1. Eon is the tun-on losses when a typical diode is used in the test circuit in figure 2. If the IGBT is offered in a package with a co-pak diode, the co-pack diode is used as external diode. IGBTs & Diode are at the same temperature (25°C and 125°C)
2. Turn-off losses include also the tail of the collector current

Table 8. Collector-emitter diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_f	Forward on-voltage	If = 10A If = 10A, Tj = 125°C		1.5 1.1	2	V V
t_{rr} Q_{rr} I_{rrm} S	Reverse recovery time Reverse recovery charge Reverse recovery current Softness factor of the diode	If = 20A, V_R = 50V, di/dt=100A/µs, T_j=25°C *(see Figure 20)*		44 66 3 0.375		ns nC A
t_{rr} Q_{rr} I_{rrm} S	Reverse recovery time Reverse recovery charge Reverse recovery current Softness factor of the diode	If = 20A, V_R = 50V, di/dt=100A/µs, T_j=125°C *(see Figure 20)*		88 237 5.4 0.57		ns nC A

2.1 Electrical characteristics (curves)

Figure 2. Output characteristics

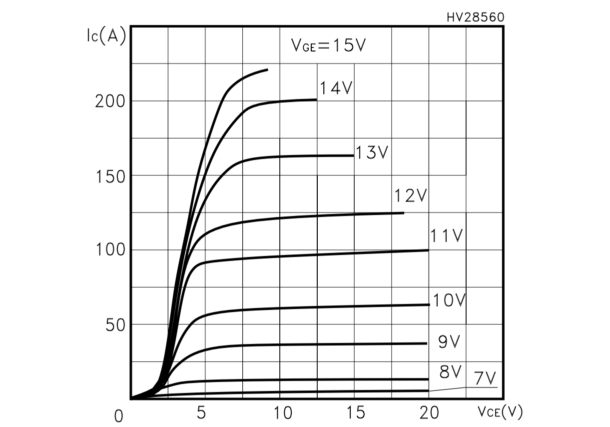


Figure 3. Transfer characteristics

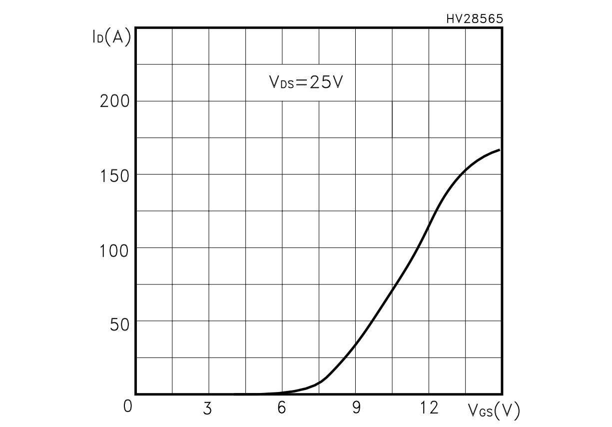


Figure 4. Transconductance

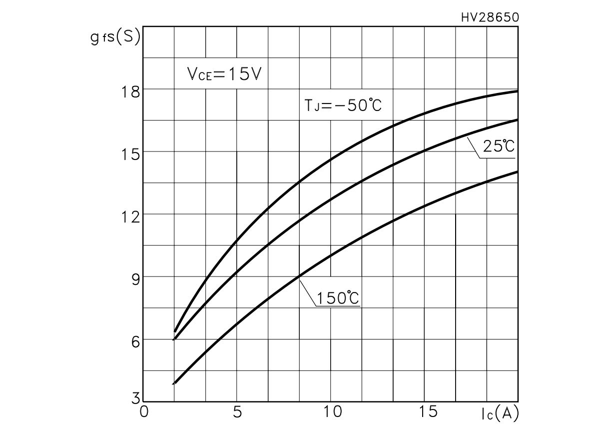


Figure 5. Collector-emitter on voltage vs temperature

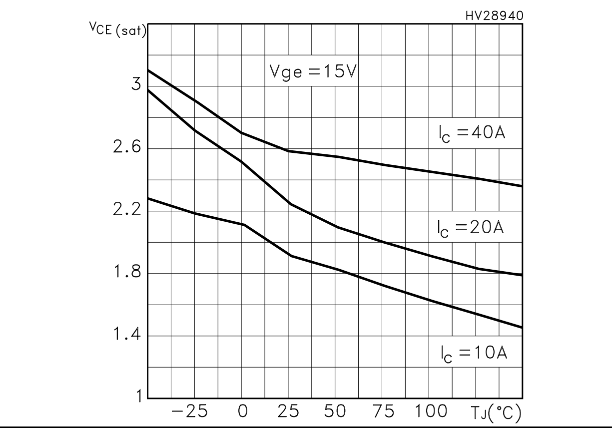


Figure 6. Gate charge vs gate-source voltage

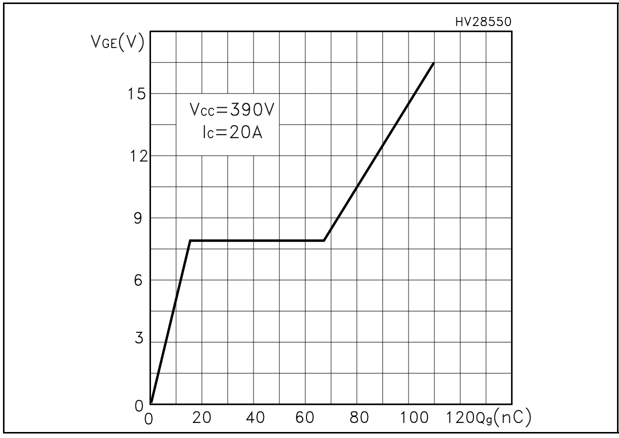


Figure 7. Capacitance variations

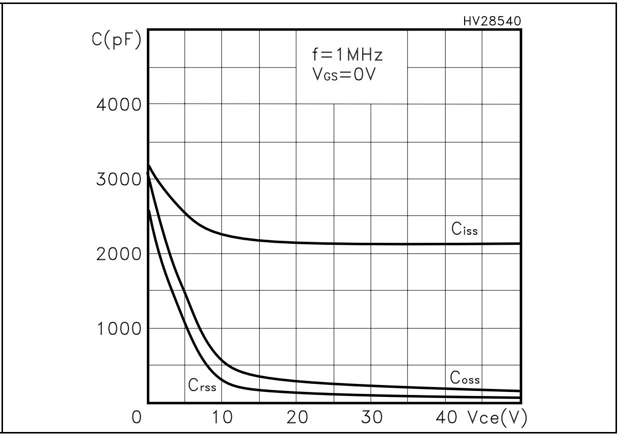


Figure 8. Normalized gate threshold voltage vs temperature

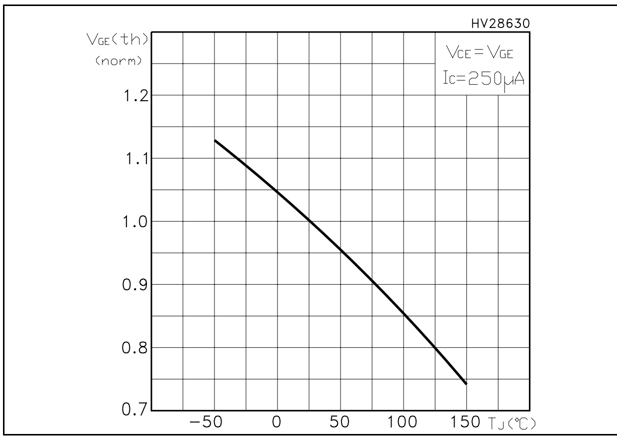


Figure 9. Collector-emitter on voltage vs collector current

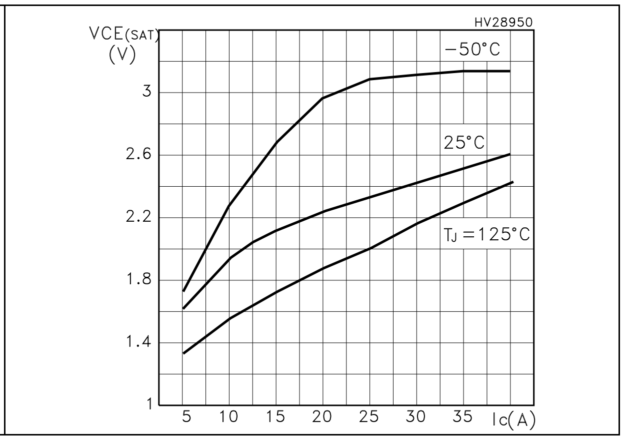


Figure 10. Normalized breakdown voltage vs temperature

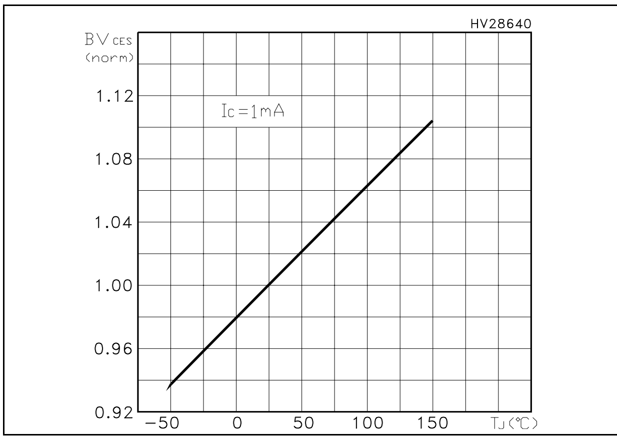


Figure 11. Switching losses vs temperature

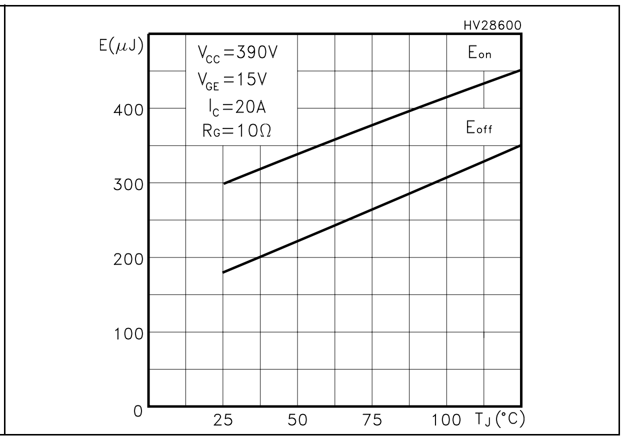


Figure 12. Switching losses vs gate resistance

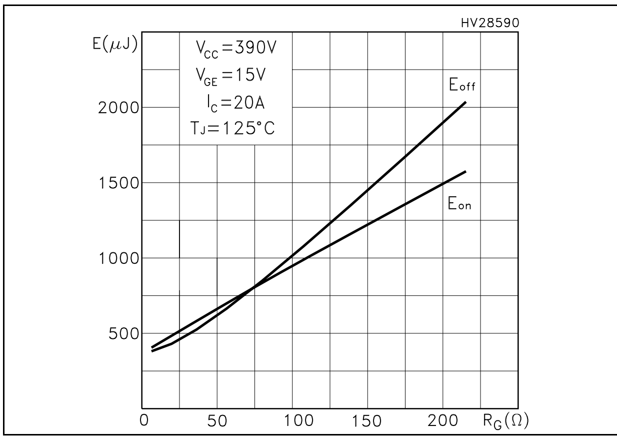


Figure 13. Switching losses vs collector current

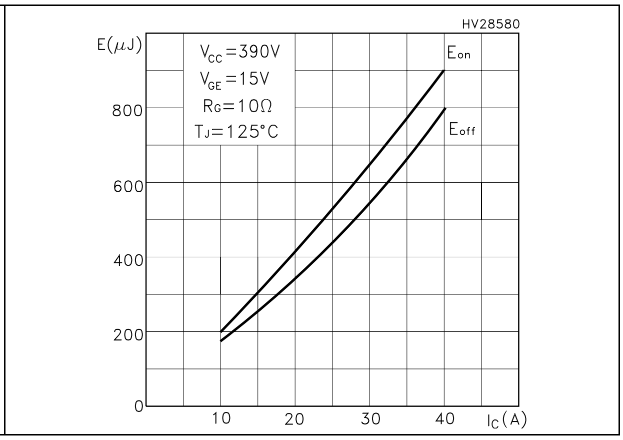


Figure 14. Thermal impedance

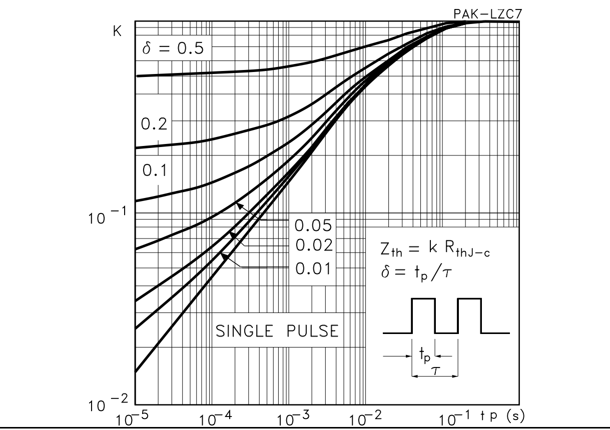


Figure 15. Turn-off SOA

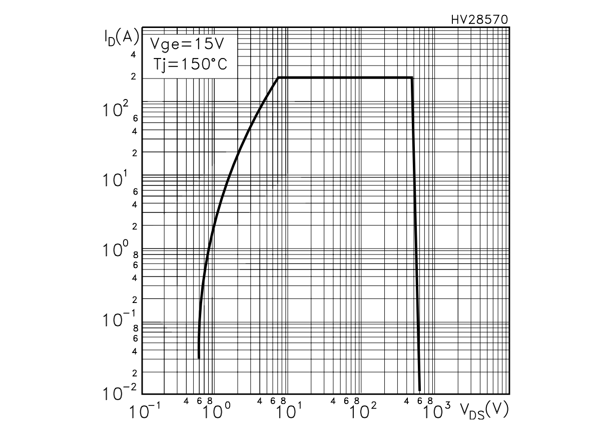
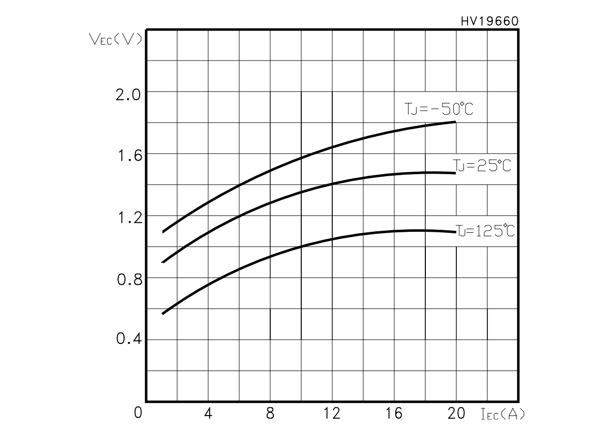


Figure 16. Emitter-collector diode characteristics



3 Test circuit

Figure 17. Test circuit for inductive load switching

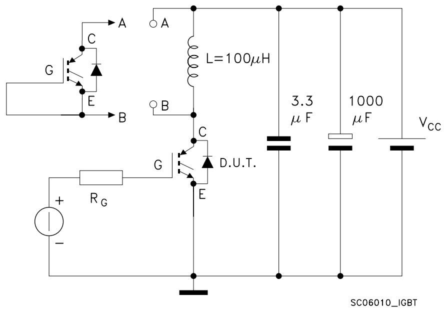


Figure 18. Gate charge test circuit

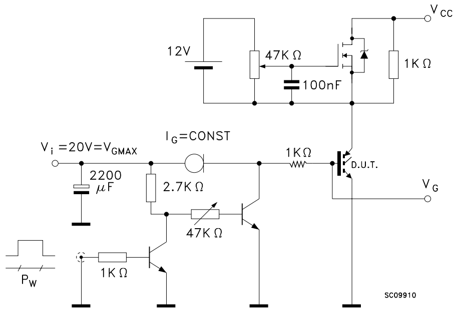


Figure 19. Switching waveform

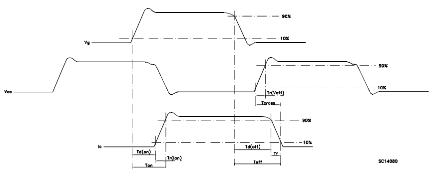
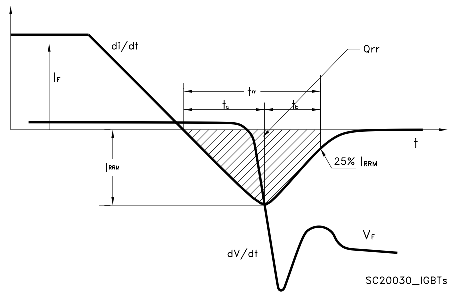


Figure 20. Diode recovery time waveform

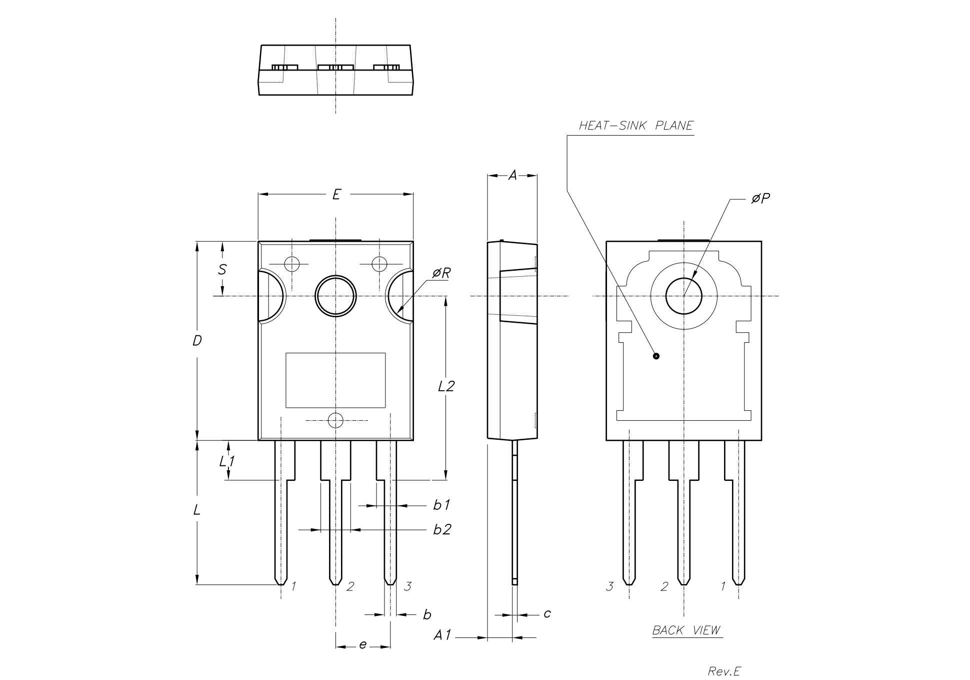


4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com

TO-247 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	4.85		5.15	0.19		0.20
A1	2.20		2.60	0.086		0.102
b	1.0		1.40	0.039		0.055
b1	2.0		2.40	0.079		0.094
b2	3.0		3.40	0.118		0.134
c	0.40		0.80	0.015		0.03
D	19.85		20.15	0.781		0.793
E	15.45		15.75	0.608		0.620
e		5.45			0.214	
L	14.20		14.80	0.560		0.582
L1	3.70		4.30	0.14		0.17
L2		18.50			0.728	
øP	3.55		3.65	0.140		0.143
øR	4.50		5.50	0.177		0.216
S		5.50			0.216	



5 Revision history

Table 9. Revision history

Date	Revision	Changes
21-Nov-2005	1	Initial release.
29-Nov-2005	2	Modified *Figure 5* and *Figure 6*
06-Mar-2006	3	New template
12-Jul-2007	4	Corrected *Figure 11*, *Figure 12*, *Figure 13*