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AK4683

Asynchronous Multi-Channel Audio CODEC with DIR/T

GENERAL DESCRIPTION

The AK4683 is a single chip CODEC that includes two channels of ADC and four channels of DAC. The ADC outputs 24bit data and the DAC accepts up to 24bit input data. The ADC has the Enhanced Dual Bit architecture with wide dynamic range. The DAC introduces the new developed Advanced Multi-Bit architecture, and achieves wider dynamic range and lower outband noise. The AK4683 also has digital audio receiver (DIR) and transmitter (DIT) compatible with 192kHz, 24bits. The DIR can automatically detect a Non-PCM bit stream such as Dolby Digital (AC-3)*. The AK4683 has a dynamic range of 100dB for ADC, 106dB for DAC and is well suited for digital TV and home theater system.

* Dolby Digital (AC-3) is a trademark of Dolby Laboratories.

FEATURES

- **ADC/DAC part**
  - **Asynchronous ADC/DAC Operation**
  - **6:1 Input Selector with Pre-amp**
  - **2ch 24bit ADC**
    - **64x Oversampling**
    - **Sampling Rate up to 96kHz**
    - **Linear Phase Digital Anti-Alias Filter**
    - **Single-Ended Input**
    - **S/(N+D): 90dB**
    - **Dynamic Range, S/N: 100dB**
    - **Digital HPF for Offset Cancellation**
    - **Channel Independent Digital Volume (+24/-103dB, 0.5dB/step)**
    - **Soft Mute**
    - **Overflow Flag**
  - **4ch 24bit DAC**
    - **128x Oversampling**
    - **Sampling Rate up to 192kHz**
    - **24bit 8 times Digital Filter**
    - **Single-Ended Outputs**
    - **S/(N+D): 90dB**
    - **Dynamic Range, S/N: 106dB**
    - **Channel Independent Digital Volume (+12/-115dB, 0.5dB/step)**
    - **Soft Mute**
    - **De-emphasis Filter (32kHz, 44.1kHz, 48kHz)**
    - **Zero Detect Function**
  - **Stereo Headphone Amp with Volume**
    - **50mW at 16ohm**
    - **Click-noise free at Power on/off**
  - **High Jitter Tolerance**

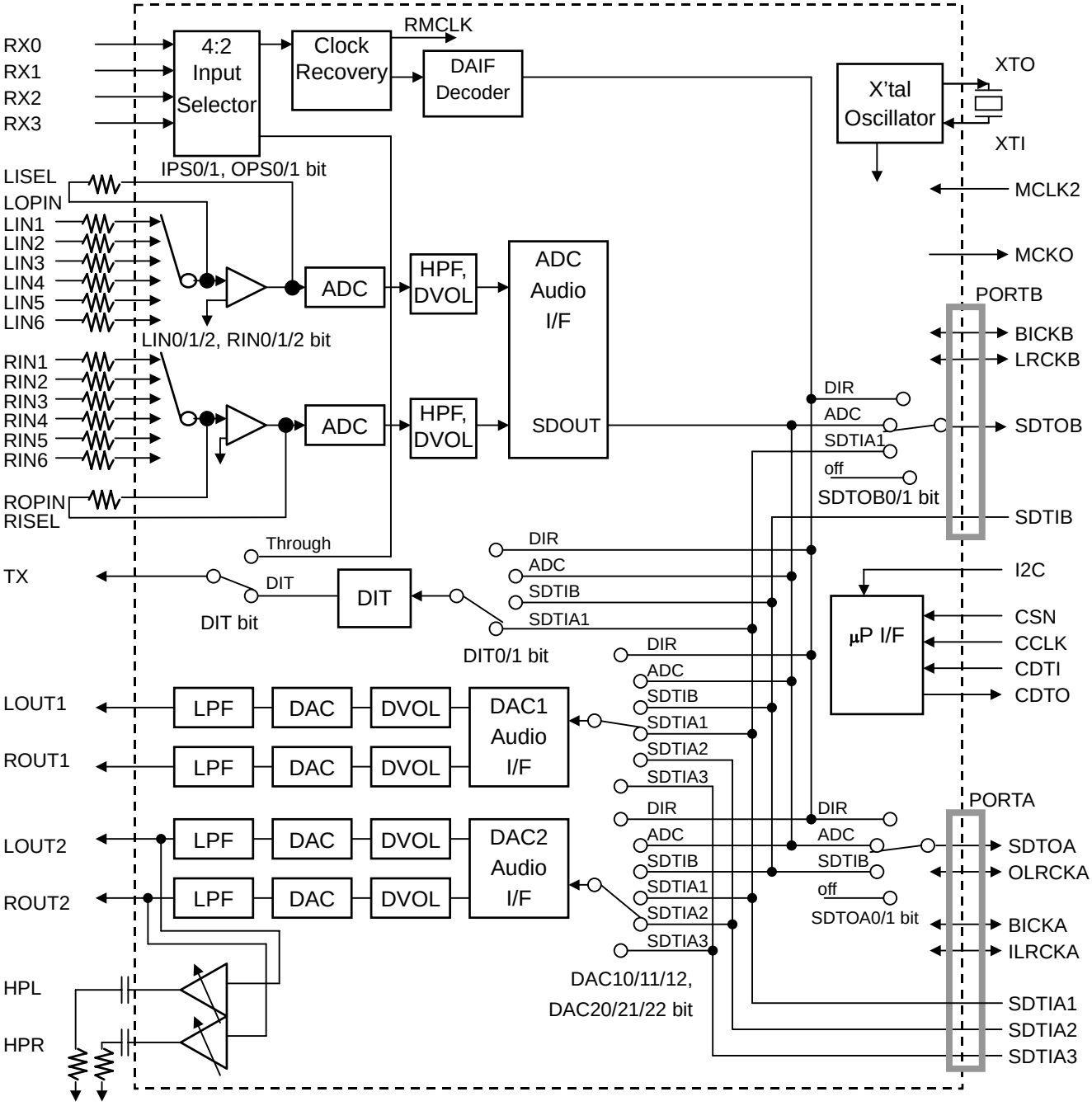
☐ **DIR/DIT Part**
- **AES3, IEC60958, S/PDIF, EIAJ CP1201 Compatible**
- **Low jitter Analog PLL**
- **PLL Lock Range : 32kHz to 192kHz**
- **Clock Source: PLL or X'tal**
- **4-channel Receiver input**
- **1-channel Transmission output (Through output or DIT)**
- **Auxiliary digital input**
- **De-emphasis for 32kHz, 44.1kHz, 48kHz and 96kHz**
- **Detection Functions**
  - **Non-PCM Bit Stream Detection**
  - **DTS-CD Bit Stream Detection**
  - **Sampling Frequency Detection (32kHz, 44.1kHz, 48kHz, 88.2kHz, 96kHz, 176.4kHz, 192kHz)**
  - **Unlock & Parity Error Detection**
  - **Validity Flag Detection**
- **Up to 24bit Audio Data Format**
- **40-bit Channel Status Buffer**
- **Burst Preamble bit Pc and Pd Buffer for Non-PCM bit stream**
- **Q-subcode Buffer for CD bit stream**

☐ **TTL Level Digital I/F**
☐ **External Master Clock Input:**
- **256fs, 384fs, 512fs (fs=32kHz ~ 48kHz)**
- **128fs, 192fs, 256fs (fs=64kHz ~ 96kHz)**
- **128fs (fs=120kHz ~ 192kHz)**

☐ **Master Clock Output: 128fs/256fs/384fs/512fs**
☐ **2 Audio Serial I/F (PORTA, PORTB)**
- **Master/Slave mode**
- **I/F format**
  PORTA: Left/Right(20/24 bit) justified, I^2S, TDM
  PORTB: Left/Right(20/24 bit) justified, I^2S

☐ **4-wire Serial and I^2C Bus μP I/F for mode setting**
☐ **Operating Voltage: 4.5 to 5.5V**
☐ **Power Supply for output buffer: 2.7 to 5.5V**
☐ **64pin LQFP Package (0.5mm pitch)**

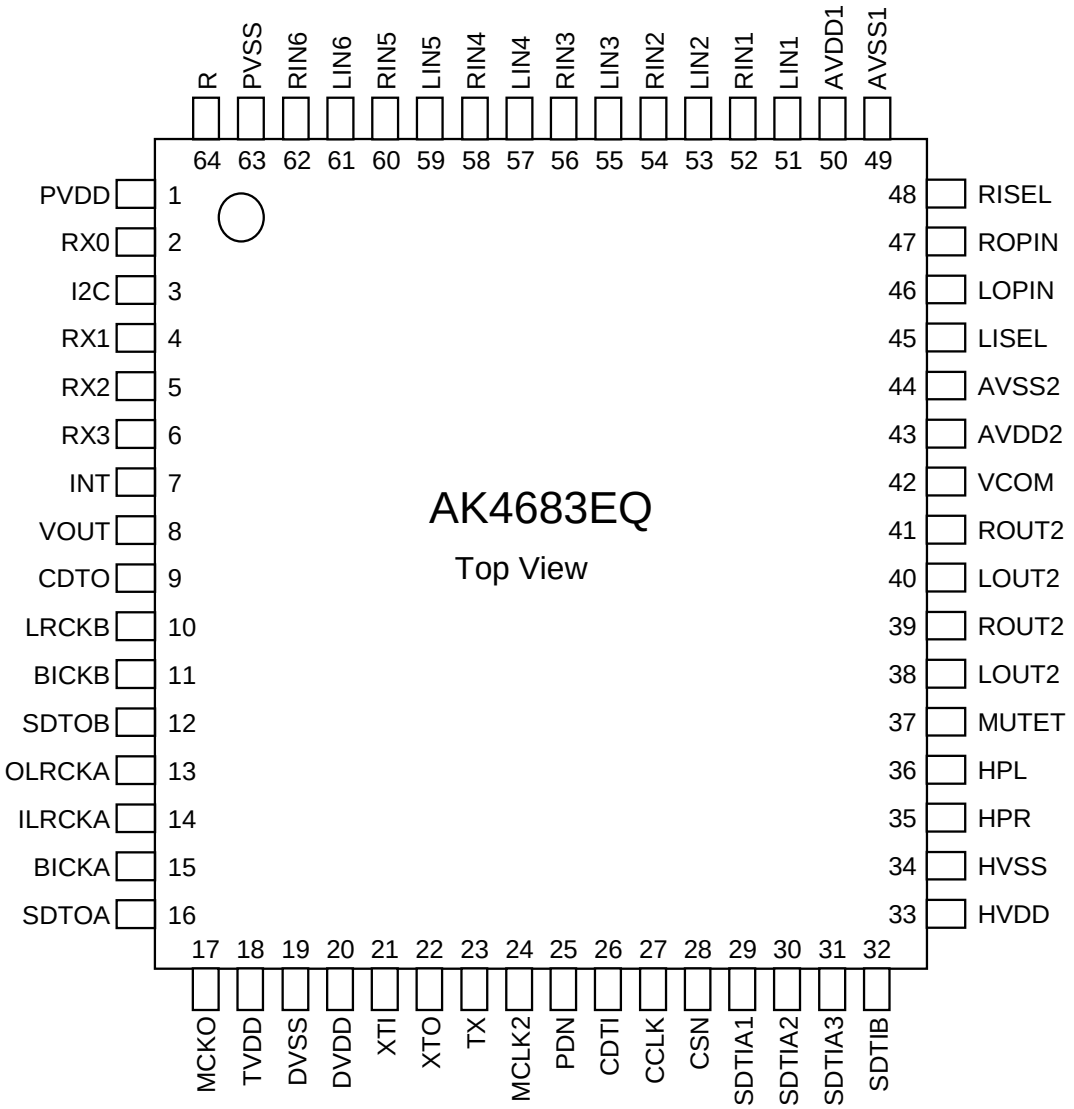
■ Block Diagram



■ Ordering Guide

AK4683EQ	-20 ~ +85°C	64pin LQFP (0.5mm pitch)
AKD4683	Evaluation Board for AK4683	

■ Pin Layout



■ Compatibility with AK4588

Functions	AK4588	AK4683
DAC, ADC Asynchronous operation	NOT Available	Available
DAC ch#	8ch	4ch
HP-Amp	-	2ch
ADC Input selector	-	6:1

PIN/FUNCTION

No.	Pin Name	I/O	Function
1	PVDD	-	PLL Power supply Pin, 4.5V~5.5V
2	RX0	I	Receiver Channel 0 Pin (Internal biased pin. Internally biased at PVDD/2)
3	I2C	I	Control Mode Select Pin. "L": 4-wire Serial, "H": I^2C Bus
4	RX1	I	Receiver Channel 1 Pin
5	RX2	I	Receiver Channel 2 Pin
6	RX3	I	Receiver Channel 3 Pin
7	INT	O	Interrupt Pin
8	VOUT	O	V-bit Output Pin for Receiver Input
	DZF	O	Zero Input Detect Pin When the input data of DAC follow total 8192 LRCK cycles with "0" input data, this pin goes to "H". And when RSTN1 bit is "0", PWDA bit is "0", this pin goes to "H".
	OVF	O	Analog Input Overflow Detect Pin This pin goes to "H" if the analog input of Lch or Rch overflows.
9	CDTO	O	Control Data Output Pin in Serial Mode and I2C pin = "L".
10	LRCKB	I/O	Channel Clock B Pin
11	BICKB	I/O	Audio Serial Data Clock B Pin
12	SDTOB	O	Audio Serial Data Output B Pin
13	OLRCKA	I/O	Output Channel Clock A Pin
14	ILRCKA	I/O	Input Channel Clock A Pin
15	BICKA	I/O	Audio Serial Data Clock A Pin
16	SDTOA	O	Audio Serial Data Output A Pin
17	MCKO	O	Master Clock Output Pin
18	TVDD	-	Output Buffer Power Supply Pin, 2.7V~5.5V
19	DVSS	-	Digital Ground Pin, 0V
20	DVDD	-	Digital Power Supply Pin, 4.5V~5.5V
21	XTI	I	X'tal Input Pin
22	XTO	O	X'tal Output Pin
23	TX	O	Transmit Channel Output pin When DIT bit = "0", RX0~3 Through. When DIT bit = "1", Internal DIT Output.
24	MCLK2	I	Master Clock Input Pin
25	PDN	I	Power-Down Mode & Reset Pin When "L", the AK4683 is powered-down, all registers are reset. And then all digital output pins go "L". The AK4683 must be reset once upon power-up.
26	CDTI	I	Control Data Input Pin in Serial Mode and I2C pin = "L".
	SDA	I/O	Control Data Pin in Serial Mode and I2C pin = "H".
27	CCLK	I	Control Data Clock Pin in Serial Mode and I2C pin = "L"
	SCL	I	Control Data Clock Pin in Serial Mode and I2C pin = "H"
28	CSN	I	Chip Select Pin in Serial Mode and I2C pin = "L".
	TEST	I	This pin should be connected to DVSS in Serial Mode and I2C pin = "H".
29	SDTIA1	I	Audio Serial Data Input A1 Pin
30	SDTIA2	I	Audio Serial Data Input A2 Pin
31	SDTIA3	I	Audio Serial Data Input A3 Pin
32	SDTIB	I	Audio Serial Data Input B Pin
33	HVDD	-	HP Power Supply Pin, 4.5V~5.5V
34	HVSS	-	HP Ground Pin, 0V
35	HPR	O	HP Rch Output Pin
36	HPL	O	HP Lch Output Pin
37	MUTET	-	HP Common Voltage Output Pin 1μF capacitor should be connected to HVSS externally.

No.	Pin Name	I/O	Function
38	LOUT2	O	DAC2 Lch Positive Analog Output Pin
39	ROUT2	O	DAC2 Rch Positive Analog Output Pin
40	LOUT1	O	DAC1 Lch Positive Analog Output Pin
41	ROUT1	O	DAC1 Rch Positive Analog Output Pin
42	VCOM	-	DAC/ADC Common Voltage Output Pin 2.2μF capacitor should be connected to AVSS2 externally.
43	AVDD2	-	DAC Power Supply Pin, 4.5V~5.5V
44	AVSS2	-	DAC Ground Pin, 0V
45	LISEL	O	Lch Feedback Resistor Output Pin
46	LOPIN	O	Lch Feedback Resistor Input Pin. 0.5 x AVDD1.
47	ROPIN	O	Rch Feedback Resistor Input Pin. 0.5 x AVDD1.
48	RISEL	O	Rch Feedback Resistor Output Pin
49	AVSS1	-	ADC Ground Pin, 0V
50	AVDD1	-	ADC Power Supply Pin, 4.5V~5.5V
51	LIN1	I	Lch Input 1 Pin
52	RIN1	I	Rch Input 1 Pin
53	LIN2	I	Lch Input 2 Pin
54	RIN2	I	Rch Input 2 Pin
55	LIN3	I	Lch Input 3 Pin
56	RIN3	I	Rch Input 3 Pin
57	LIN4	I	Lch Input 4 Pin
58	RIN4	I	Rch Input 4 Pin
59	LIN5	I	Lch Input 5 Pin
60	RIN5	I	Rch Input 5 Pin
61	LIN6	I	Lch Input 6 Pin
62	RIN6	I	Rch Input 6 Pin
63	PVSS	-	PLL Ground pin
64	R	-	External Resistor Pin 12kΩ +/-1% resistor should be connected to PVSS externally.

Note: All input pins except internal biased pin (RX0) and analog input pins (LIN1-6, RIN1-6) should not be left floating.

■ Handling of Unused Pin

The unused I/O pins should be processed appropriately as below.

Classification	Pin Name	Setting
Analog	RX0, LOUT1-2, ROUT1-2, LIN1-6, RIN1-6	These pins should be open.
Digital	INT, XTO, MCKO, VOUT/DZF/OVF, SDTOA-B, CDTO, TX	These pins should be open.
	RX1-3, CSN, CCLK, CDTI, XTI, MCLK2, OLRCKA, ILRCKA, BICKA, SDTIA1-3, LRCKB, BICKB, SDTIB	These pins should be connected to DVSS.

ABSOLUTE MAXIMUM RATINGS

(AVSS1, AVSS2, DVSS, PVSS, HVSS=0V; Note 1)

Parameter		Symbol	min	max	Units
Power Supplies	ADC Analog	AVDD1	-0.3	6.0	V
	DAC Analog	AVDD2	-0.3	6.0	V
	Headphone Analog	HVDD	-0.3	6.0	V
	Digital	DVDD	-0.3	6.0	V
	PLL	PVDD	-0.3	6.0	V
	Output buffer	TVDD	-0.3	6.0	V
	|AVSS2-AVSS1| (Note 2)	ΔGND1	-	0.3	V
	|AVSS2-DVSS| (Note 2)	ΔGND2	-	0.3	V
	|AVSS2-PVSS| (Note 2)	ΔGND3	-	0.3	V
	|AVSS2-HVSS| (Note 2)	ΔGND4	-	0.3	V
Input Current (any pins except for supplies)		IIN	-	±10	mA
Analog Input Voltage (LIN, RIN pins)		VINA	-0.3	AVDD1+0.3	V
Digital Input Voltage					
	Except for ILRCKA, OLRCKA, LRCKB, BICKA-B, RX0, I2C pins	VIND1	-0.3	DVDD+0.3	V
	ILRCKA, OLRCKA, LRCKB, BICKA-B pins	VIND2	-0.3	TVDD+0.3	V
	RX0, I2Cpins	VIND3	-0.3	PVDD+0.3	V
Ambient Temperature (power applied)		Ta	-20	85	°C
Storage Temperature		Tstg	-65	150	°C

Note 1. All voltages with respect to ground.
Note 2. AVSS, DVSS and PVSS must be connected to the same analog ground plane.

WARNING: Operation at or beyond these limits may result in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

RECOMMENDED OPERATING CONDITIONS

(AVSS, DVSS, PVSS=0V; Note 3)

Parameter		Symbol	min	typ	max	Units
Power Supplies (Note 4)	ADC Analog	AVDD1	4.5	5.0	5.5	V
	DAC Analog	AVDD2	4.5	5.0	5.5	V
	Headphone Analog	HVDD	AVDD2	5.0	5.5	V
	Digital	DVDD	4.5	5.0	5.5	V
	PLL	PVDD	4.5	5.0	5.5	V
	Output buffer	TVDD	2.7	5.0	DVDD	V
	|DVDD - AVDD1|	ΔVDD1	-0.3	0	+0.3	V
	|DVDD - AVDD2|	ΔVDD2	-0.3	0	+0.3	V
	|DVDD - HVDD|	ΔVDD3	-0.3	0	+0.3	V
	|DVDD - PVDD|	ΔVDD4	-0.3	0	+0.3	V
	|AVDD1 – AVDD2|	ΔVDD5	-0.1	0	+0.1	V

Note 3. All voltages with respect to ground.
Note 4. The power up sequences among AVDD1, AVDD2, DVDD, PVDD, HVDD and TVDD are not critical.

WARNING: EMD assumes no responsibility for the usage beyond the conditions in this datasheet.

ANALOG CHARACTERISTICS

(Ta=25°C; AVDD1, AVDD2, HVDD, DVDD, PVDD, TVDD=5V; AVSS1, AVSS2, HVSS, DVSS, PVSS=0V; fs=48kHz; BICK=64fs; Signal Frequency=1kHz; 24bit Data; Measurement Frequency=20Hz~20kHz at fs=48kHz, 20Hz~40kHz at fs=96kHz; 20Hz~40kHz at fs=192kHz, all blocks are synchronized, unless otherwise specified)

Parameter		min	typ	max	Units
Pre-Amp Characteristics:					
Feedback Resistance		10		50	kΩ
S/(N+D) (Note 5)		-	100		dB
S/N (A-weighted) (Note 5)		-	108		dB
Load Capacitance				20	pF
ADC Analog Input Characteristics (Note 6)					
Resolution				24	Bits
S/(N+D) (-0.5dBFS)	fs=48kHz	84	92		dB
	fs=96kHz	-	86		dB
DR (-60dBFS)	fs=48kHz, A-weighted	92	100		dB
	fs=96kHz	-	96		dB
	fs=96kHz, A-weighted	-	100		dB
S/N (Note 7)	fs=48kHz, A-weighted	92	100		dB
	fs=96kHz	-	96		dB
	fs=96kHz, A-weighted	-	100		dB
Interchannel Isolation (Note 8)		90	105		dB
Interchannel Gain Mismatch			0.2	0.5	dB
Gain Drift			50	-	ppm/°C
Input Voltage (Note 6)	AIN=1.22xAVDD1	5.7	6.1	6.5	Vpp
Power Supply Rejection (Note 9)			50		dB
DAC Analog Output Characteristics					
Resolution				24	Bits
S/(N+D)	fs=48kHz	80	90		dB
	fs=96kHz	-	88		dB
	fs=192kHz	-	88		dB
DR (-60dBFS)	fs=48kHz, A-weighted	95	106		dB
	fs=96kHz	-	100		dB
	fs=96kHz, A-weighted	-	106		dB
	fs=192kHz	-	100		dB
	fs=192kHz, A-weighted	-	106		dB
S/N (Note 10)	fs=48kHz, A-weighted	95	106		dB
	fs=96kHz	-	100		dB
	fs=96kHz, A-weighted	-	106		dB
	fs=192kHz	-	100		dB
	fs=192kHz, A-weighted	-	106		dB
Interchannel Isolation		90	110		dB
Interchannel Gain Mismatch			0.2	0.5	dB
Gain Drift			50	-	ppm/°C
Output Voltage	AOUT=0.6xAVDD2	2.75	3.0	3.25	Vpp
Load Resistance	(AC Load)	5			kΩ
Load Capacitance				30	pF
Power Supply Rejection (Note 9)			50		dB

Analog Volume Characteristics (OPGA):					
Step Size:	+0dB ~ -16dB	0.1	1	-	dB
	-16dB ~ -38dB	0.1	2	-	dB
	-38dB ~ -50dB	-	4	-	dB
Headphone-Amp Characteristics: DAC → HPL/HPR pins, RL=16Ω					
Output Voltage	(0.506xHVDD)	1.94	2.43	2.92	Vpp
S/(N+D)	(–3dBFS)	-	70	-	dBFS
S/N	(A-weighted)	-	90	-	dB
Interchannel Isolation		-	80	-	dB
Interchannel Gain Mismatch		-	0.1	0.5	dB
Load Resistance		16	-	-	Ω
Load Capacitance	C1 in Figure 1	-	-	30	pF
	C2 in Figure 1	-	-	300	pF
Power Supplies					
Power Supply Current					
Normal Operation (PDN pin = "H")	(Note 11)				
AVDD1+ AVDD2	fs=48kHz, fs=96kHz		37	52	mA
	fs=192kHz		19	27	mA
HVDD			7	10	mA
PVDD			8	11	mA
DVDD+TVDD	fs=48kHz (Note 12)		35	49	mA
	fs=96kHz		45	63	mA
	fs=192kHz		55	77	mA
Power-down mode (PDN pin = "L")	(Note 13)		80	200	μA

Note 5. Measured at LISEL/RISEL pins when the input resistor=47kohm, the feedback resistor=24kohm and input level =2Vrms.
Note 6. Measured through Pre-Amp -> ADC. Input resistor=47kohm, feedback resistor=24kohm.
Note 7. S/N measured by CCIR-ARM is 96dB(@fs=48kHz).
Note 8. This value is the interchannel isolation between all the channels of the LIN1-6 and RIN1-6.
Note 9. PSR is applied to AVDD, DVDD, PVDD and TVDD with 1kHz, 50mVpp.
Note 10. S/N measured by CCIR-ARM is 102dB(@fs=48kHz).
Note 11. C_L=20pF, X'tal=24.576MHz, CM1-0="10", CM1-0="10", OCKS1-0="10"@48kHz,"00"@96kHz, "11"@192kHz. Headphone = No output. The resister network is attached to TX pin.
Note 12. TVDD=6mA(typ@fs=48kHz), 7mA(typ@fs=96kHz), 10mA(typ@fs=192kHz).
Note 13. In the power-down mode. RX0 input is open and all digital input pins including clock pins (MCLK2, BICKA, BICKB, ILRCKA, OLRCKA, BICKB pins) and RX1-3 pins are held DVSS

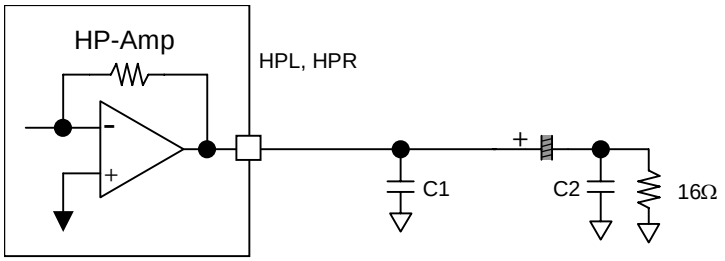


Figure 1. Headphone Amplifier output circuit

FILTER CHARACTERISTICS

(Ta=25°C; AVDD1, AVDD2, DVDD, PVDD, HVDD=4.5~5.5V; TVDD=2.7~5.5V; fs=48kHz)

Parameter		Symbol	min	typ	max	Units
ADC Digital Filter (Decimation LPF):						
Passband (Note 14)	±0.1dB	PB	0		18.9	kHz
	-0.2dB		-	20.0	-	kHz
	-3.0dB		-	23.0	-	kHz
Stopband		SB	28.0			kHz
Passband Ripple		PR			±0.04	dB
Stopband Attenuation		SA	68			dB
Group Delay (Note 15)		GD		19		1/fs
Group Delay Distortion		ΔGD		0		μs
ADC Digital Filter (HPF):						
Frequency Response (Note 14)	-3dB	FR		1.0		Hz
	-0.1dB			6.5		Hz
DAC Digital Filter:						
Passband (Note 14)	-0.1dB	PB	0		21.8	kHz
	-6.0dB		-	24.0	-	kHz
Stopband		SB	26.2			kHz
Passband Ripple		PR			±0.02	dB
Stopband Attenuation		SA	54			dB
Group Delay (Note 15)		GD		21		1/fs
DAC Digital Filter + Analog Filter:						
Frequency Response: 0 ~ 20.0kHz		FR		±0.2		dB
40.0kHz (Note 16)		FR		±0.3		dB
80.0kHz (Note 16)		FR		±1.0		dB

Note 14. The passband and stopband frequencies are proportional to fs.
For example, 21.8kHz at –0.1dB is 0.454 x fs (DAC). The reference frequency of these responses is 1kHz.

Note 15. The calculating delay time which occurred by digital filtering. This time is from setting the input of analog signal to setting the 24bit data of both channels to the output register of PORTA or PORTB.
For DAC, this time is from setting the 20/24bit data of both channels on input register of PORTA or PORTB to the output of analog signal.

Note 16. 40kHz@fs=96kHz, 80kHz@fs=192kHz

DC CHARACTERISTICS

(Ta=25°C; AVDD1, AVDD2, DVDD, PVDD, HVDD=4.5~5.5V; TVDD=2.7~5.5V)

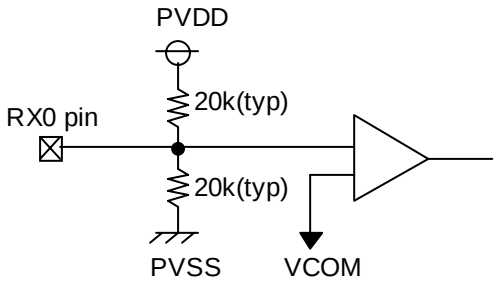
Parameter	Symbol	min	typ	max	Units
High-Level Input Voltage (Except XTI pin)	VIH	2.2	-	-	V
(XTI pin)	VIH	70%DVDD	-	-	V
Low-Level Input Voltage (Except XTI pin)	VIL	-	-	0.8	V
(XTI pin)	VIL	-	-	30%DVDD	V
Input Voltage at AC Coupling (XTI pin) (Note 17)	VAC	40%DVDD	-	-	Vpp
High-Level Output Voltage					
(Except TX pins: Iout=-400μA)	VOH	TVDD-0.4	-	-	V
(TX pin: Iout=-400μA)	VOH	DVDD-0.4	-	-	V
Low-Level Output Voltage (Iout=400μA)	VOL	-		0.4	V
Input Leakage Current (Except RX0 pin)	Iin	-	-	±10	μA

Note 17. In case of connecting capacitance to XTI pin.

S/PDIF RECEIVER CHARACTERISTICS (RX0)

(Ta=25°C; AVDD1, AVDD2, DVDD, PVDD, HVDD=4.5~5.5V; TVDD=2.7~5.5V)

Parameter	Symbol	min	typ	max	Units
Input Resistance	Zin		10		kΩ
Input Voltage (internally biased at PVDD/2)	VTH	200			mVpp
Input Hysteresis	VHY	-	50		mV
Input Sample Frequency	fs	32	-	192	kHz



Internal biased pin Circuit

S/PDIF RECEIVER CHARACTERISTICS (RX1-3)

(Ta=25°C; AVDD1, AVDD2, DVDD, PVDD, HVDD=4.5~5.5V;TVDD=2.7~5.5V)

Parameter	Symbol	min	typ	max	Units
High-Level Input Voltage	VIH	2.2	-		V
Low-Level Input Voltage	VIL	-	-	0.8	V
Input Sample Frequency	fs	32	-	192	kHz
Input Leakage Current	Iin	-	-	±10	μA

SWITCHING CHARACTERISTICS

(Ta=25°C; AVDD1, AVDD2, DVDD, PVDD, HVDD=4.5~5.5V; TVDD=2.7~5.5V; C_L=20pF; Note 18)

Parameter		Symbol	min	typ	max	Units
Master Clock Timing						
Crystal Resonator	Frequency	fXTAL	11.2896		24.576	MHz
External Clock	Frequency	fECLK	4.096		24.576	MHz
	Duty	dECLK	40	50	60	%
MCKO Output	Frequency	fMCK	4.096		24.576	MHz
	Duty (Note 19)	dMCLK	40	50	60	%
	(Note 20)	dMCK		33		%
PLL Clock Recover Frequency (RX0-3)		fpll	32	-	192	kHz
Master Clock						
256fsn, 128fsd:		fCLK	8.192		12.288	MHz
Pulse Width Low		tCLKL	27			ns
Pulse Width High		tCLKH	27			ns
384fsn, 192fsd:		fCLK	12.288		18.432	MHz
Pulse Width Low		tCLKL	20			ns
Pulse Width High		tCLKH	20			ns
512fsn, 256fsd, 128fsq:		fCLK	16.384		24.576	MHz
Pulse Width Low		tCLKL	15			ns
Pulse Width High		tCLKH	15			ns
LRCKA (LRCKB) Timing (Slave Mode)						
Normal mode						
Normal Speed Mode		fsn	32		48	kHz
Double Speed Mode		fsd	64		96	kHz
Quad Speed Mode		fsq	120		192	kHz
Duty Cycle		Duty	45		55	%
TDM 256 mode						
LRCKA frequency		fsd	32		48	kHz
"H" time		tLRH	1/256fs			ns
"L" time		tLRL	1/256fs			ns
TDM 128 mode						
LRCKA frequency		fsd	64		96	kHz
"H" time		tLRH	1/128fs			ns
"L" time		tLRL	1/128fs			ns
LRCKA (LRCKB) Timing (Master Mode)						
Normal mode						
Normal Speed Mode		fsn	32		48	kHz
Double Speed Mode		fsd	64		96	kHz
Quad Speed Mode		fsq	120		192	kHz
Duty Cycle		Duty		50		%
TDM 256 mode						
LRCKA frequency		fsn	32		48	kHz
"H" time	(Note 21)	tLRH		1/8fs		ns
TDM 128 mode						
LRCKA frequency		fsd	64		96	kHz
"H" time	(Note 21)	tLRH		1/4fs		ns
Power-down & Reset Timing						
PDN Pulse Width	(Note 22)	tPD	150			ns
PDN "↑" to SDTO valid	(Note 23)	tPDV		522		1/fs

Note 18. SDTOA is specified against OLRCKA, SDTIA1-3 are measured against ILRCKA.
Note 19. When MCKO1-0 bits = "01", "10" or MCKO1-0 bits = "00" and CKSDT bit = "0".
Note 20. When MCKO1-0 bits = "00" and CKSDT bit = "1" and the EXTCLK is selected by CM1-0 bits.
Duty = ("H" width) / (clock cycle) x 100
Note 21. "L" time at I^2S format
Note 22. The AK4683 can be reset by bringing PDN "L" to "H" upon power-up.
Note 23. These cycles are the number of LRCKA (LRCKB) rising from PDN rising.

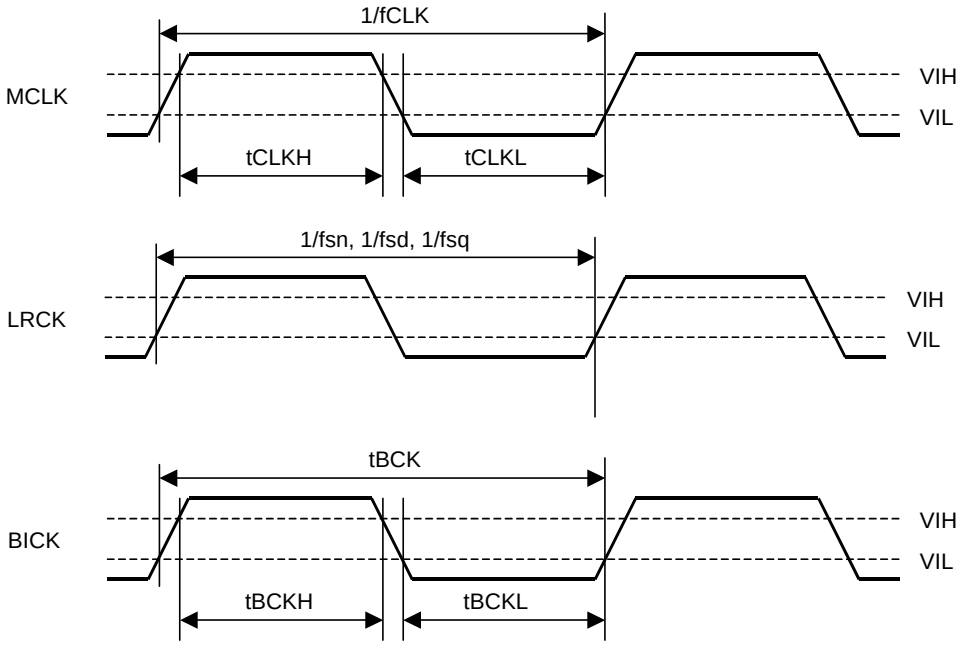
Parameter	Symbol	min	typ	max	Units
Audio Interface Timing (Slave Mode)					
Normal mode					
BICKA (BICKB) Period	tBCK	81			ns
BICKA (BICKB) Pulse Width Low	tBCKL	32			ns
Pulse Width High	tBCKH	32			ns
LRCKA (LRCKB) Edge to BICKA (BICKB) "↑" (Note 24)	tLRB	20			ns
BICKA (BICKB) "↑" to LRCKA (LRCKB) Edge (Note 24)	tBLR	20			ns
LRCKA (LRCKB) to SDTOA, SDTOB (MSB)	tLRS			20	ns
BICKA (BICKB) "↓" to SDTOA, SDTOB	tBSD			20	ns
SDTIA1-3, SDTIB Hold Time	tSDH	20			ns
SDTIA1-3, SDTIB Setup Time	tSDS	20			ns
TDM 256 mode					
BICKA Period	tBCK	81			ns
BICKA Pulse Width Low	tBCKL	32			ns
Pulse Width High	tBCKH	32			ns
LRCKA Edge to BICKA "↑" (Note 24)	tLRB	20			ns
BICKA "↑" to LRCKA Edge (Note 24)	tBLR	20			ns
BICKA "↓" to SDTOA	tBSD			20	ns
SDTIA1 Hold Time	tSDH	10			ns
SDTIA1 Setup Time	tSDS	10			ns
TDM 128 mode					
BICKA Period	tBCK	81			ns
BICKA Pulse Width Low	tBCKL	32			ns
Pulse Width High	tBCKH	32			ns
LRCKA Edge to BICKA "↑" (Note 24)	tLRB	20			ns
BICKA "↑" to LRCKA Edge (Note 24)	tBLR	20			ns
BICKA "↓" to SDTOA	tBSD			20	ns
SDTIA1-2 Hold Time	tSDH	10			ns
SDTIA1-2 Setup Time	tSDS	10			ns
Audio Interface Timing (Master Mode)					
Normal mode					
BICKA (BICKB) Frequency	fBCK		64fs		Hz
BICKA (BICKB) Duty	dBCK		50		%
BICKA (BICKB) "↓" to LRCKA (LRCKB) Edge	tMBLR	-20		20	ns
BICKA (BICKB)"↓" to SDTO	tBSD			20	ns
SDTIA1-3, B Hold Time	tSDH	20			ns
SDTIA1-3, B Setup Time	tSDS	20			ns
TDM 256 mode					
BICKA Frequency	fBCK		256fs		Hz
BICKA Duty (Note 25)	dBCK		50		%
BICKA "↓" to LRCKA Edge	tMBLR	-12		12	ns
BICKA "↓" to SDTOA	tBSD			20	ns
SDTIA1 Hold Time	tSDH	10			ns
SDTIA1 Setup Time	tSDS	10			ns
TDM 128 mode					
BICKA Frequency	fBCK		128fs		Hz
BICKA Duty (Note 26)	dBCK		50		%
BICKA "↓" to LRCKA Edge	tMBLR	-12		12	ns
BICKA "↓" to SDTOA	tBSD			20	ns
SDTIA1-2 Hold Time	tSDH	10			ns
SDTIA1-2 Setup Time	tSDS	10			ns

Note 24. BICK rising edge must not occur at the same time as LRCK edge.
Note 25. When MCLK2/XTI is 512fs, dBCK is guaranteed. When 384fs and 256fs, dBCK can not be guaranteed.
Note 26. When MCLK2/XTI is 256fs, dBCK is guaranteed. When 128fs, dBCK can not be guaranteed.

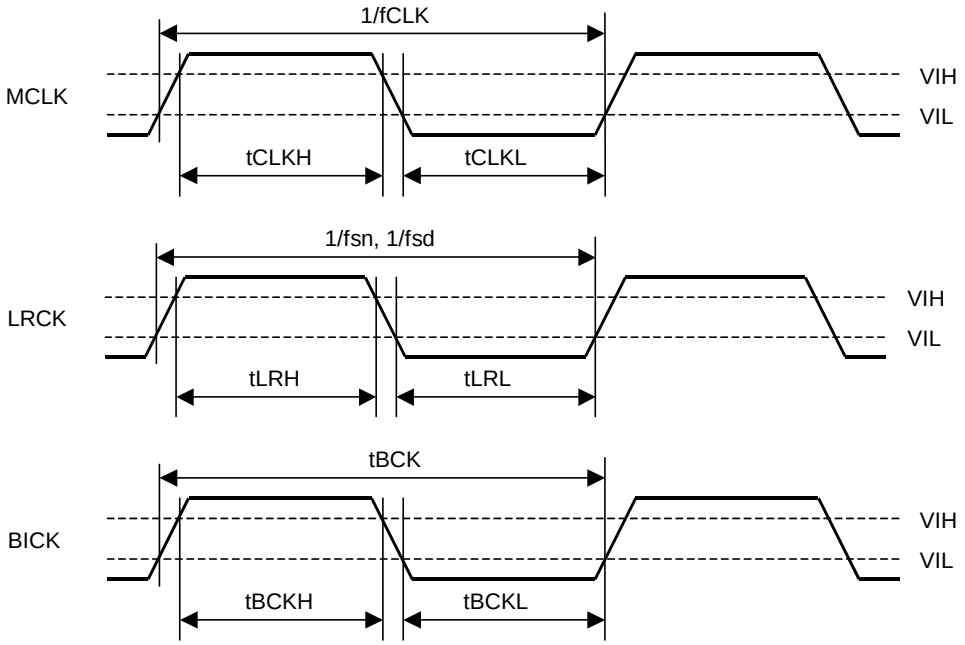
Parameter	Symbol	min	typ	max	Units
Control Interface Timing (4-wire serial mode)					
CCLK Period	tCCK	200			ns
CCLK Pulse Width Low	tCCKL	80			ns
Pulse Width High	tCCKH	80			ns
CDTI Setup Time	tCDS	50			ns
CDTI Hold Time	tCDH	50			ns
CSN "H" Time	tCSW	150			ns
CSN "↓" to CCLK "↑"	tCSS	50			ns
CCLK "↑" to CSN "↑"	tCSH	50			ns
CDTO Delay	tDCD			45	ns
CSN "↑" to CDTO Hi-Z	tCCZ			70	ns
Control Interface Timing (I^2C Bus mode)					
SCL Clock Frequency	fSCL	-		100	kHz
Bus Free Time Between Transmissions	tBUF	4.7		-	µs
Start Condition Hold Time (prior to first clock pulse)	tHD:STA	4.0		-	µs
Clock Low Time	tLOW	4.7		-	µs
Clock High Time	tHIGH	4.0		-	µs
Setup Time for Repeated Start Condition	tSU:STA	4.7		-	µs
SDA Hold Time from SCL Falling (Note 27)	tHD:DAT	0		-	µs
SDA Setup Time from SCL Rising	tSU:DAT	0.25		-	µs
Rise Time of Both SDA and SCL Lines	tR	-		1.0	µs
Fall Time of Both SDA and SCL Lines	tF	-		0.3	µs
Setup Time for Stop Condition	tSU:STO	4.0		-	µs
Pulse Width of Spike Noise Suppressed by Input Filter	tSP	0		50	ns
Capacitive load on bus	Cb	-		400	pF

Note 27. Data must be held for sufficient time to bridge the 300 ns transition time of SCL.
Note 28. I^2C is a registered trademark of Philips Semiconductors.

■ Timing Diagram

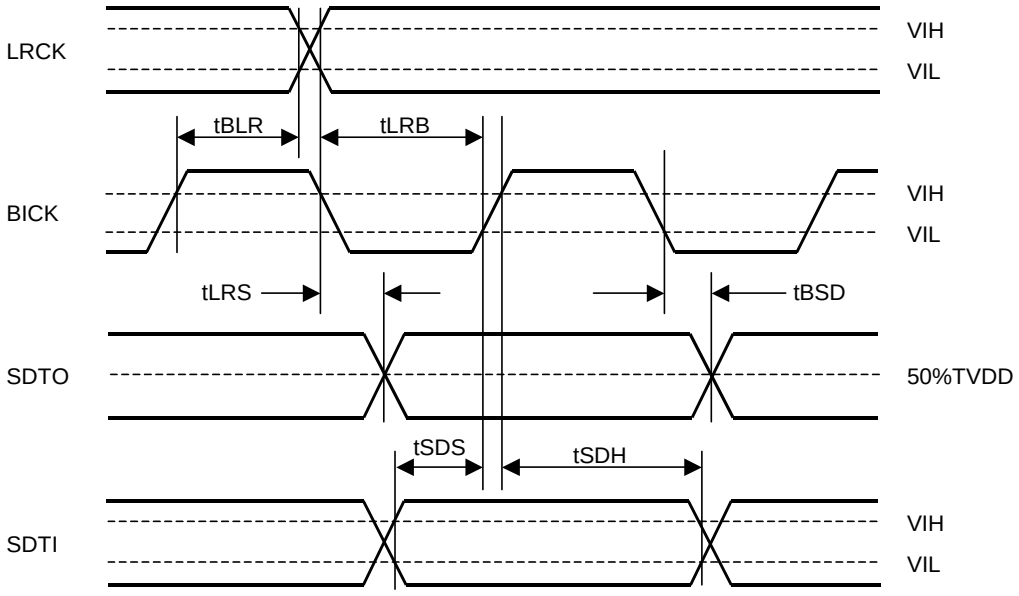


Clock Timing (Normal mode)

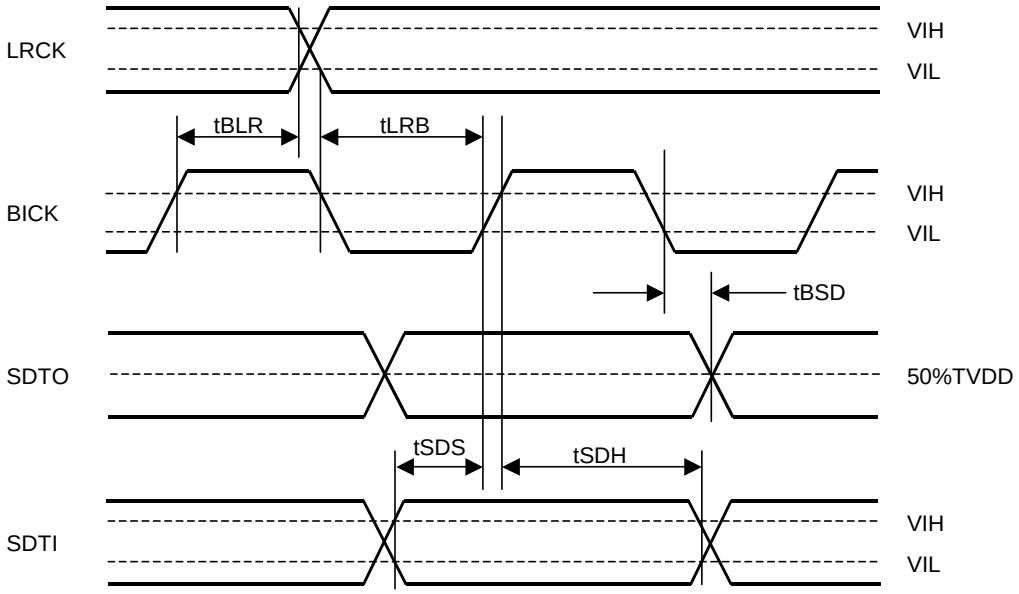


Clock Timing (TDM 256 mode, TDM 128 mode)

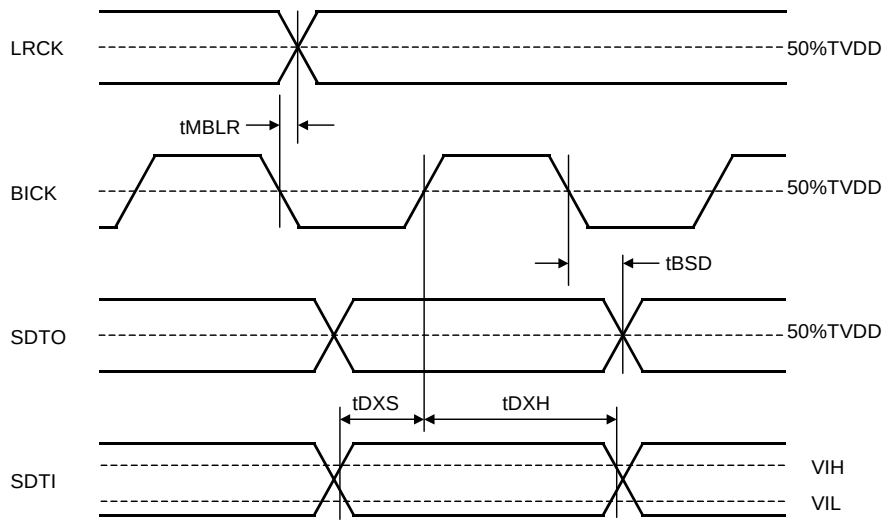
LRCK= LRCKB, ILRCKA, OLRCKA,
BICK= BICKA, BICKB,
SDTI= SDTIA, SDTIB,
SDTO= SDTOA, SDTOB.



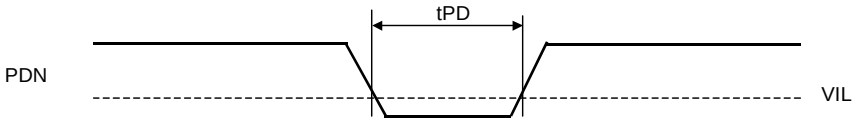
Audio Interface Timing (Normal mode)



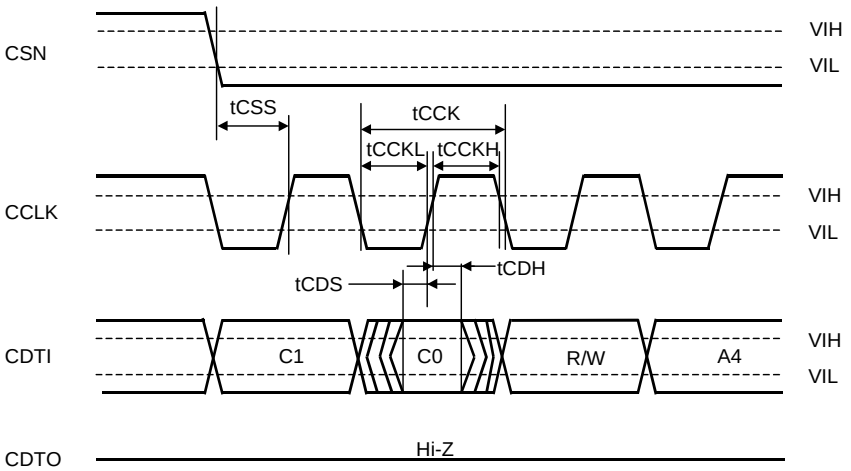
Audio Interface Timing (TDM 256 mode, TDM 128 mode)



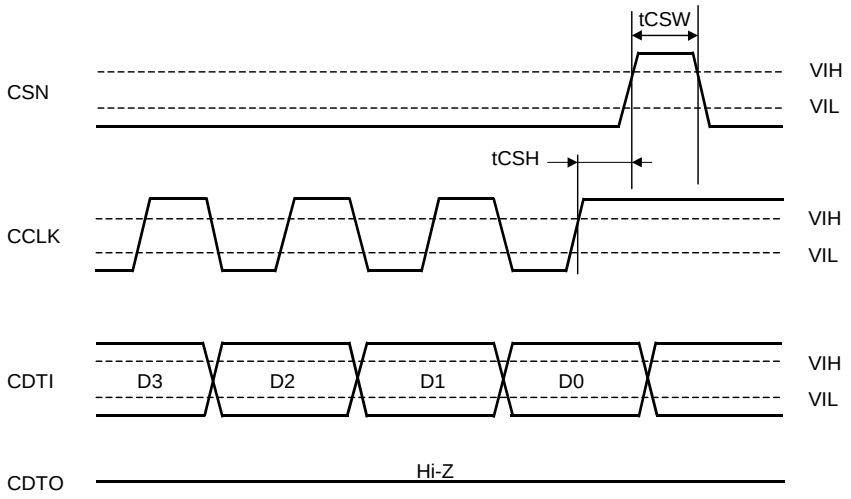
Audio Interface timing (Master Mode)



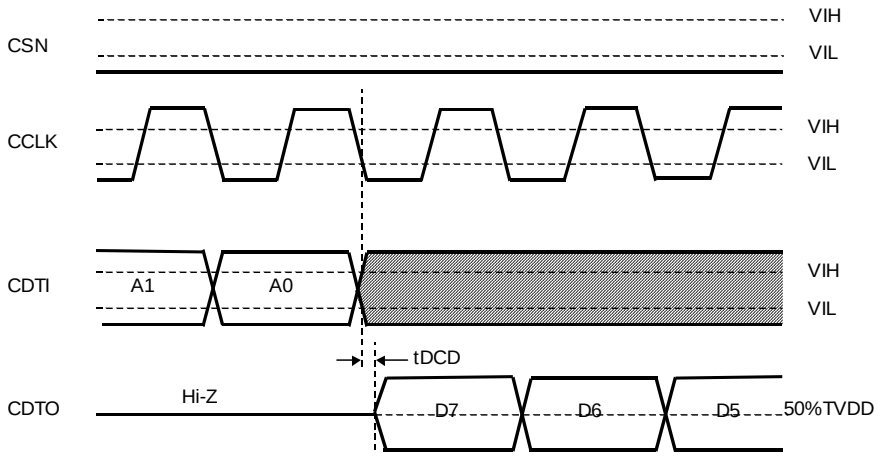
Power Down & Reset Timing



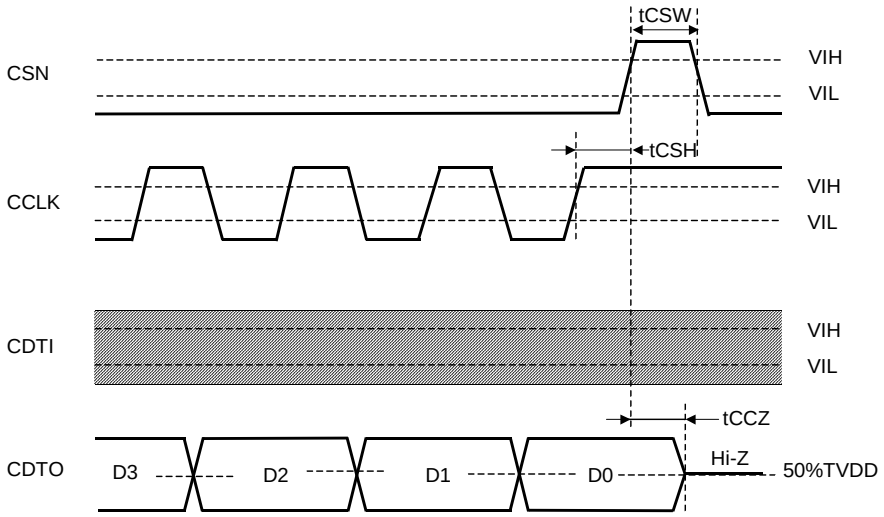
WRITE/READ Command Input Timing in 4-wire serial mode
The ADC/DAC part doesn't support READ command.



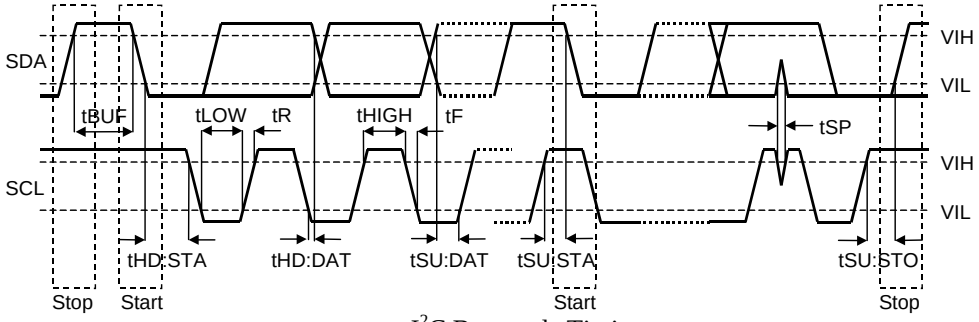
WRITE Data Input Timing in 4-wire serial mode



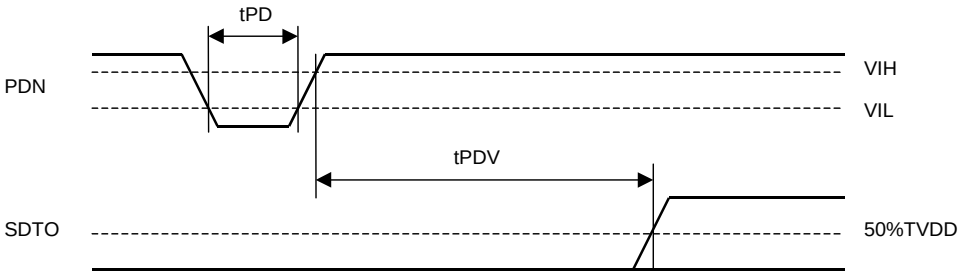
READ Data Output Timing 1 in 4-wire serial mode
The ADC/DAC part doesn't support READ command..



READ Data Input Timing 2 in 4-wire serial mode
The ADC/DAC part doesn't support READ command.



I^2C Bus mode Timing
The ADC/DAC part doesn't support READ command.



Power-down & Reset Timing

OPERATION OVERVIEW (General)

■ Device Configuration and System Clocks

The AK4683 integrates the stereo ADC with input selector, 4ch DAC with stereo HP amp, DIR and DIT. The AK4683 has two serial audio interfaces (PORTA, B) for two input/output dataset (Figure 2). Each block can independently select the operation clock from the three clock sources (recovered clock from DIR (RMCLK), X'tal clock (XTI) and external clock (MCLK2)) and also input data source/output data destination. By using the Clock Gen C, the loop-back such as AD-DA can operate even if the PORTA/B are powered down.

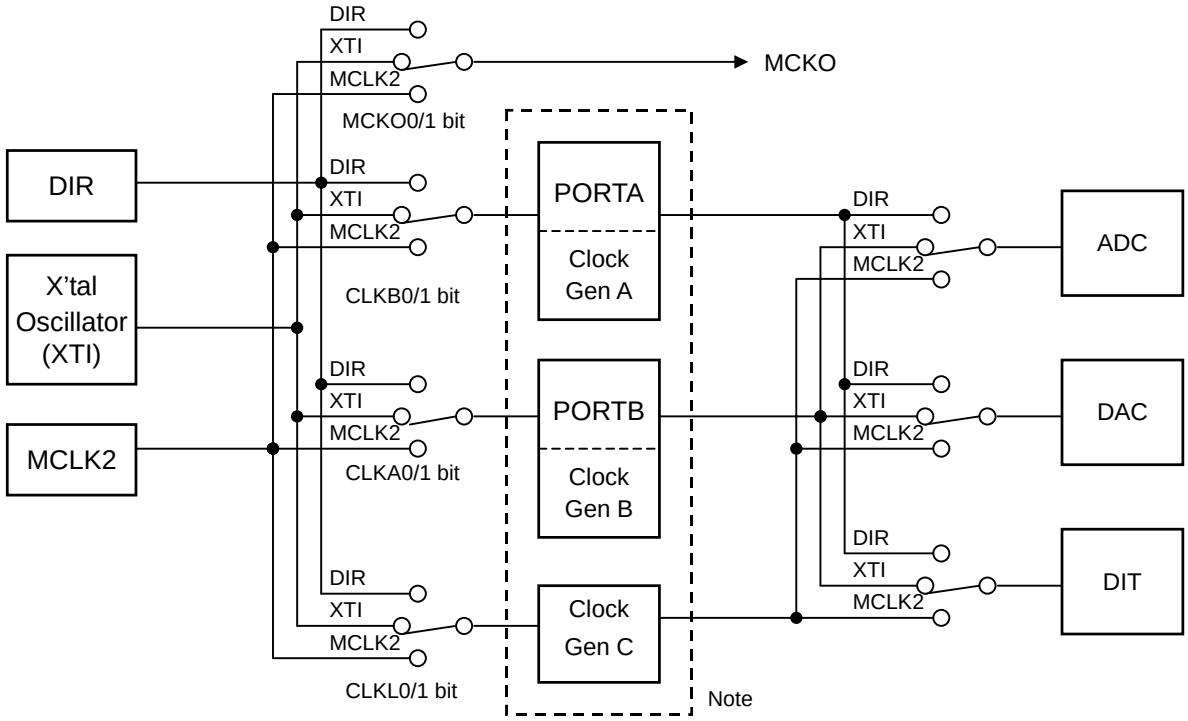


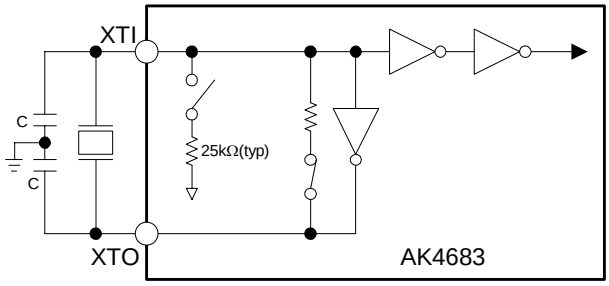
Figure 2 System Clock

Note: Each block must select the same clock source each other when connected. The operation will not be normal when the clock sources are not same among a connection. The ADC and DAC are synchronized to the clock source that the connected block uses. Even if the RMCLK is selected, the X'tal/MCLK2 may be chosen by the setting of CM1-0bits. DIR and DIT must be synchronized when these two blocks operates.

■ X'tal Oscillator

The following circuits are available to feed the clock to XTI pin of the AK4683.

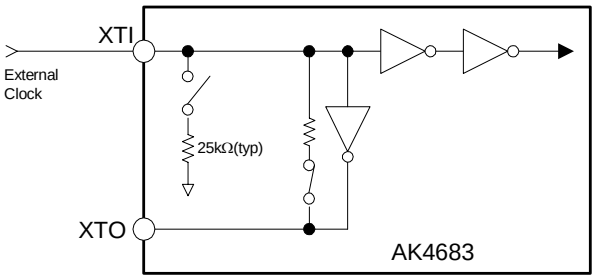
1) X'tal



Note: External capacitance depends on the crystal oscillator (Typ. 10-40pF)

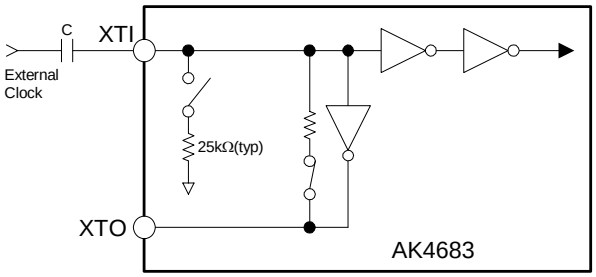
Figure 3. X'tal mode

2) External clock
- Note: Input clock must not exceed DVDD.



(Input: CMOS Level)

Figure 4 DC-coupled Input



(Input: ≥40%DVDD, C=0.1μF)

Figure 5 AC-coupled Input

3) XTI/XTO are not used

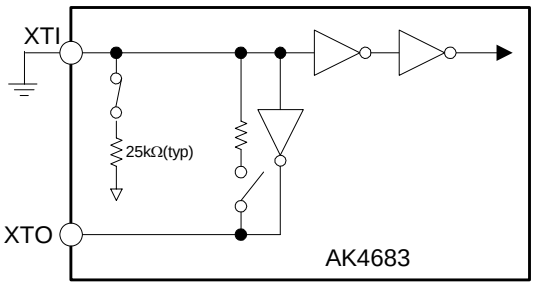


Figure 6. OFF mode

■ Master Clock Output

The AK4683 has one master clock output pin. The clock source can be selected from the three clocks (recovered clock from DIR (RMCLK), X'tal clock (XTI) and external clock (MCLK2)). When the DIR is powered-down or unlocked state at CM1/0 bit = "10", the CLKDT bit selects the clock source. The OCKS1/0 bits select the clock speed. The 512fs at fs=96kHz, 256fs/512fs at fs=192kHz are not available.

CM1 bit	CM0 bit	UNLOCK	Clock Source
0	0	-	RMCLK
0	1	-	EXTCLK
1	0	0	RMCLK
		1	EXTCLK
1	1	-	EXTCLK

Table 1. Clock Mode Control

CLKDT bit	Clock Source	
0	XTI	Default
1	MCLK2	

Table 2. EXTCLK Control

OCKS1 bit	OCKS0 bit	MCLKO(RMCLK)	fs (max)
0	0	256fs	96 kHz
0	1	256fs	96 kHz
1	0	512fs	48 kHz
1	1	128fs	192 kHz

Table 3. MCLKO Speed

MCKO1 bit	MCKO0 bit	MCKO Clock Source	
0	0	DIR	
0	1	X'tal(XTI)	default
1	0	MCLK2	
1	1	Reserved	

Table 4. MCKO Clock Source Control

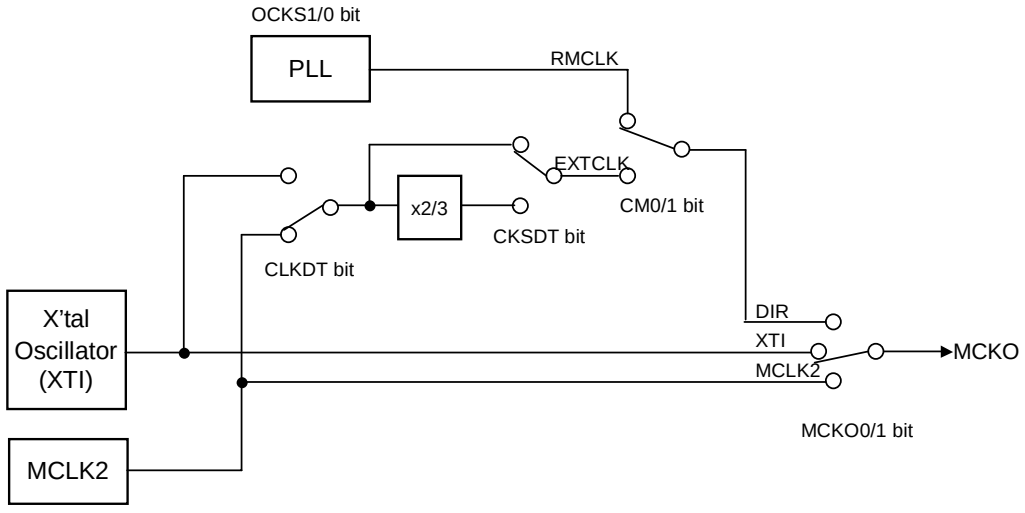


Figure 7. MCKO Clock

■ Master/Slave Mode Change

MSA and MSB bits control the master/slave mode of PORTA and PORTB respectively. The "1" is for master mode, "0" is for slave mode. The AK4683 is slave mode at power-down (PDN pin = "L"). To change to the master mode, write "1" to MSA/MSB bit. The ACKSAI, ACKSAO and ACKSB bits are ignored in master mode. Until when writing "1" to MSA/MSB bit, the ILRCKA, OLRCKA, BICKA, LRCKB and BICKB pin are input pins. Pull-up(or down) resistor with around 100kohm is required to prevent the floating of these input pins.

MSA, MSB bit	Mode	
0	Slave Mode	(default)
1	Master Mode	

Table 5. Select Master/Salve Mode

Note: When PORTA and PORTB operate synchronously, PORTB must not be the Master Mode. In that case the PORTA must be the Master Mode, or both PORTA and PORTB must be the Slave Mode with supplying the same BICK and LRCK.

■ Other Detection Function

The FUNC1-0 bit selects the function of VOUT / DZF / OVF pin.

Mode	FUNC1	FUNC0	Mode	
0	0	0	OFF ("L")	Default
1	0	1	ADC Overflow Detection	
2	1	0	DAC Zero Detection	
3	1	1	V bit output	

Table 6. Detection Function Control

1. Overflow Detection

The AK4683 has overflow detect function for analog input. OVF pin goes to "H" if analog input of Lch or Rch overflows (more than -0.3dBFS). OVF output for overflowed analog input has the same group delay as ADC (GD = 16/fs = 333μs @fs=48kHz). OVF pin is "L" for 522/fs (=10.9ms @fs=48kHz) after PDN = "↑", and then overflow detection is enabled. The overflow detection is applied to the data between the digital HPF and the DATT.

2. Zero Detection

The AK4683 has one pin for zero detect flag output. The DZFM1-0 bits select the channel grouping (Table 7). The DZF pin goes "H" when all of the enabled channels are continuously zeros for 8192 LRCK cycles. DZF pin immediately goes to "L" if input data of any enabled channel is not zero after going DZF "H".

Mode	DZFM1 bit	DZFM0 bit	AOUT				
			L1	R1	L2	R2	
0	0	0	Enable	Enable	Enable	Enable	(default)
1	0	1	Enable	Enable	-	-	
2	1	0	-	-	Enable	Enable	
3	1	1	-	-	-	-	

Table 7. Zero Detection Control

3. Validity Detection

The AK4683 has Validity Detection function. DIR decodes the V bit and output "H" via pin. When unlocked, "L" is output.

OPERATION OVERVIEW (ADC/DAC/PORTA, B part)

■ System Clock

The AK4683 has two audio serial interface (PORTA, B), can operate these PORTs with asynchronous. At each PORT, the external clocks, which are required to operate the AK4683, are MCLK, LRCK and BICK. The MCLK should be synchronized with LRCK but the phase is not critical.

The CLKA1-0, CLKB1-0bits select the clock sources for each PORT (Table 8, Table 9). The MSA and MSB bits select the master/slave mode (Table 16, Table 17).

The block that is connected to PORTA/B and the block that is connected to the PORT indirectly operate at the same clock as the PORTA/B selects. e. g. When the DAC selects the ADC data while the PORTB selects the ADC data also, the DAC operates same clock as the PORTB selects. The block that isn't connected to PORTA/B is automatically connected to the Clock Gen C and operates the same clock as the Clock Gen C selects with the CLKL1-0 bits (Table 10).

In master mode, the CKSIA2-0, OLRA1-0, BICKAF, CKSB2-0 bits select the clock frequency (Table 11, Table 12 , Table 13, Table 14). In master mode, external clock (MCLK) should always be supplied except in the power-down mode. The AK4683 is in power-down mode until MCLK will be supplied, when reset was canceled by Power-ON and so on. At PORTA, the input/output data has independent LRCK (ILRCKA/OLRCKA) and common BICK (BICKA). The ILRCK and OLRCK can operate at different sample rate but synchronized each other (Table 12).

In slave mode, external clocks (MCLK, BICK, LRCK) should always be present whenever the AK4683 is in normal operation mode (PDN pin = "H"). The master clock (MCLK) should be synchronized with LRCK but the phase is not critical. If these clocks are not provided, the AK4683 may draw excess current because the device utilizes dynamic refreshed logic internally. If the external clocks are not present, the AK4683 should be in the power-down mode (PDN pin = "L") or in the reset mode (RSTN1 bit = "0"). After exiting reset at power-up etc., the AK4683 is in the power-down mode until MCLK and LRCK are input.

When the block selects RMCLK as clock source, the sample rate of the PORT in the master mode or ADC/DAC connecting to the Clock Gen C is forced to the same rate as DIR. The DFSAD, DFSDA1-0 bits should be controlled properly.

Note: When PORTA and PORTB operate synchronously, PORTB must not be the in Master Mode. In that case the PORTA must be in the Master Mode, or both PORTA and PORTB must be in the Slave Mode with supplying the same BICK and LRCK.

CLKA1 bit	CLKA0 bit	PORTA Clock Source	
0	0	DIR	
0	1	X'tal(XTI)	(default)
1	0	MCLK2	
1	1	Reserved	

Table 8. PORTA Clock Source Control

CLKB1 bit	CLKB0 bit	PORTB Clock Source	
0	0	DIR	
0	1	X'tal(XTI)	(default)
1	0	MCLK2	
1	1	Reserved	

Table 9. PORTB Clock Source Control

CLKL1 bit	CLKL0 bit	Clock Gen C Clock Source	
0	0	DIR	
0	1	X'tal (XTI)	(default)
1	0	MCLK2	
1	1	Reserved	

Table 10. Clock Gen C Clock Source Control

CKSAI2	CKSAI1	CKSAI0	Clock Speed	
0	0	0	128fs	
0	0	1	192fs	
0	1	0	256fs	(default)
0	1	1	384fs	
1	0	0	512fs	
1	0	1	Reserved	
1	1	0	Reserved	
1	1	1	Reserved	

Table 11. PORTA Input Data Clock Control (Master Mode)

OLRA1 bit	OLRA0 bit	OLRCKA Clock Freq	
0	0	ILRCKA x 1	(default)
0	1	ILRCKA x 1/2	
1	0	ILRCKA x 2	
1	1	Reserved	

Note: Select OLRA1-0 bits = "00" in TDM mode.

Table 12. PORTA Output Data Control (Master Mode)

BCAF bit	PORTA BICK Frequency Mode	
0	ILRCK x 64	(default)
1	ILRCK x128	

Note: ILRCK x 128 is available when the MCLK=ILRCK x 256 or higher.
BCAF bit is ignored in TDM mode.

Table 13. PORTA BICK Control (Master Mode)

CKSB2	CKSB1	CKSB0	Clock Speed	
0	0	0	128fs	
0	0	1	192fs	
0	1	0	256fs	(default)
0	1	1	384fs	
1	0	0	512fs	
1	0	1	Reserved	
1	1	0	Reserved	
1	1	1	Reserved	

Table 14. PORTB Data Clock Control (Master Mode)

CKSL2	CKSL1	CKSL0	Clock Speed	
0	0	0	128fs	
0	0	1	192fs	
0	1	0	256fs	(default)
0	1	1	384fs	
1	0	0	512fs	
1	0	1	Reserved	
1	1	0	Reserved	
1	1	1	Reserved	

Table 15. Clock Gen C Clock Control

In master mode, LRCKA (LRCKB) pin, BICKA (BICKB) pin are output pins. In slave mode, these are input pins (Table 18).

MSA bit	PORTA Master/Slave Mode	
0	Slave	(default)
1	Master	

Table 16. PORTA Master/Slave Control

MSB bit	PORTB Master/Slave Mode	
0	Slave	(default)
1	Master	

Table 17. PORTB Master/Slave Control

PDN pin	PWPOA(PWPOB) bit	Master/Slave	LRCKA (LRCKB) pin	BICKA (BICKB) pin
L	-	Slave	Input	Input
H	"0"	Slave	Input (*)	Input (*)
		Master	"L" output	" L" output
H	"1"	Slave	Input	Input
		Master	Output	Output

(*): These are input pins, but input signals are ignored internally.

Table 18. LRCKA (LRCKB) pin, BICKA (BICKB) pin

The SDTOB1-0, SDTOA1-0 bits select the output data source of each PORT.

SDTOA1 bit	SDTOA0 bit	SDTOA Source	
0	0	DIR	
0	1	ADC	(default)
1	0	SDTIB	
1	1	Off ("L" Output)	

Table 19. SDTOA Source Control

SDTOB1 bit	SDTOB0 bit	SDTOB Source	
0	0	DIR	
0	1	ADC	(default)
1	0	Off	
1	1	SDTIA1	

Table 20. SDTOB Source Control

■ ADC, DAC Control

There are two modes for controlling the sampling speed for ADC and DAC. One is the Manual Setting Mode using the DFSAD1-0, DFSDA1-0 bits, and the other is Auto Setting Mode. When the block connects to both PORTA and PORTB, the PORTA setting is used.

1. Manual Setting Mode (ACSKAD / ACSKDA bit = "0": Default)

When the ADC and DAC are connected to each PORT placed in Manual Setting Mode, the sampling speed are selected by DFSAD, DFSDA1-0 bits (Table 21, Table 22). The frequencies and the duties of the clocks (ILRCKA, OLRCKA, LRCKB, BICKA, BICKB) may be unstable for the moment when changing the sampling speed mode.

DFSAD0	Sampling Speed (fs)		
0	Normal Speed Mode	32kHz~48kHz	(default)
1	Double Speed Mode	64kHz~96kHz	

Table 21.ADC sampling speed (Manual Setting Mode)

DFSDA1	DFSDA0	Sampling Speed (fs)		
0	0	Normal Speed Mode	32kHz~48kHz	(default)
0	1	Double Speed Mode	64kHz~96kHz	
1	0	Quad Speed Mode	120kHz~192kHz	
1	1	Not Available	-	

Table 22.DAC sampling speed (Manual Setting Mode)

LRCKA (LRCKB)	MCLK (MHz)			BICKA (BICKB) (MHz)
fs	256fs	384fs	512fs	64fs
32.0kHz	8.1920	12.2880	16.3840	2.0480
44.1kHz	11.2896	16.9344	22.5792	2.8224
48.0kHz	12.2880	18.4320	24.5760	3.0720

(Normal Speed Mode @Manual Setting Mode)

Table 23. System clock example

LRCKA (LRCKB)	MCLK (MHz)			BICKA (BICKB) (MHz)
fs	128fs	192fs	256fs	64fs
88.2kHz	11.2896	16.9344	22.5792	5.6448
96.0kHz	12.2880	18.4320	24.5760	6.1440

(Double Speed Mode @Manual Setting Mode)

(Note: ADC is not available for 128fs and 192fs at Double Speed Mode (DFSAD="1"))

Table 24. System clock example

LRCKA (LRCKB)	MCLK (MHz)			BICKA (BICKB) (MHz)
Fs	128fs	192fs	256fs	64fs
176.4kHz	22.5792	-	-	11.2896
192.0kHz	24.5760	-	-	12.2880

(Quad Speed Mode @Manual Setting Mode)
(Note: ADC is not available at the Quad Speed Mode)

Table 25. System clock example

2. Auto Setting Mode (ACSKAD/ACSKDA bit = "1")

When the ADC and DACs are connected to each PORT placed in Auto Setting Mode, MCLK frequency is detected automatically (Table 26) and the internal master clock is set to the appropriate frequency (Table 27). In this mode, the setting of DFSAD, DFSDA1-0 bits are ignored.

MCLK	Sampling Speed
512fs	Normal
256fs	Double
128fs	Quad

Table 26. Sampling Speed (Auto Setting Mode)

LRCKA (LRCKB)	MCLK (MHz)			Sampling Speed
fs	128fs	256fs	512fs	
32.0kHz	-	-	16.3840	Normal
44.1kHz	-	-	22.5792	
48.0kHz	-	-	24.5760	
88.2kHz	-	22.5792	-	Double
96.0kHz	-	24.5760	-	
176.4kHz	22.5792	-	-	Quad
192.0kHz	24.5760	-	-	

Table 27. System clock example (Auto Setting Mode)

The DAC12-10, DAC22-20 bits select the output data for each DAC. DAC1 and DAC2 must be connected to the same PORT.

DAC12 bit	DAC11 bit	DAC10 bit	DAC1 Source	
0	0	0	DIR	
0	0	1	ADC	
0	1	0	SDTIB	
0	1	1	SDTIA1	(default)
1	0	0	SDTIA2	
1	0	1	SDTIA3	
1	1	0	Reserved	
1	1	1	Reserved	

Table 28. DAC1 Source Control

DAC22 bit	DAC21 bit	DAC20 bit	DAC2 Source	
0	0	0	DIR	
0	0	1	ADC	
0	1	0	SDTIB	
0	1	1	SDTIA1	
1	0	0	SDTIA2	(default)
1	0	1	SDTIA3	
1	1	0	Reserved	
1	1	1	Reserved	

Table 29. DAC2 Source Control

■ De-emphasis Filter

The AK4683 includes the digital de-emphasis filter (tc=50/15μs) by IIR filter. De-emphasis filter is not available in Double Speed Mode and Quad Speed Mode. This filter corresponds to three sampling frequencies (32kHz, 44.1kHz, 48kHz). De-emphasis of each DAC can be set individually by register.

Mode	Sampling Speed	DEM1	DEM0	DEM
0	Normal Speed	0	0	44.1kHz
1	Normal Speed	0	1	OFF
2	Normal Speed	1	0	48kHz
3	Normal Speed	1	1	32kHz

(default)

Table 30. De-emphasis control

■ Digital High Pass Filter

The ADC has a digital high pass filter for DC offset cancel. The cut-off frequency of the HPF is 1.0Hz at fs=48kHz and scales with sampling rate (fs).

■ Audio Serial Interface Format

Each PORTA/B can select independent audio interface format. The TDMA1-0, DIFA1-0 bits control the audio format for PORTA and support normal mode, TDM256 mode and TDM128 mode. The DIFB1-0 bits control the audio format for PORTB and support only normal mode. The default is mode 2. In all modes the serial data is MSB-first, 2's complement format. The SDTO pins are clocked out on the falling edge of BICK pins and the SDTI pins are latched on the rising edge of BICK pins.

1. Setting for the PORTA

1-1. Normal mode: TDMA1-0 bit = "00"

The TDMA1-0 bits = "00" set the AK4683 audio serial interface format to the normal mode. The DIFA1-0 bits select following eight serial data format (Table 31).

Mode	Master /slave	DIFA1	DIFA0	SDTOA	SDTIA1-3	LRCKA		BICKA		
							I/O		I/O	
0	Slave	0	0	24bit, L J	20bit, R J	H/L	I	≥ 48fs	I	
1	Slave	0	1	24bit, L J	24bit, R J	H/L	I	≥ 48fs	I	
2	Slave	1	0	24bit, L J	24bit, L J	H/L	I	≥ 48fs	I	(default)
3	Slave	1	1	24bit, I^2S	24bit, I^2S	L/H	I	≥ 48fs	I	
4	Master	0	0	24bit, L J	20bit, R J	H/L	O	64fs	O	
5	Master	0	1	24bit, L J	24bit, R J	H/L	O	64fs	O	
6	Master	1	0	24bit, L J	24bit, L J	H/L	O	64fs	O	
7	Master	1	1	24bit, I^2S	24bit, I^2S	L/H	O	64fs	O	

Table 31 Audio Interface Format (Normal mode, L J: Left justified, R J: Right justified.)

1-2. TDM 256 mode: TDMA1-0 bit = “01”

The TDMA1-0 bits = “01” set the AK4683 audio serial interface format to the TDM 256 mode. The serial data of all SDTIA (1,2,3) is input to the SDTIA1 pin. The input data to SDTIA2-3 pins is ignored. BICKA should be fixed to 256fs. “H” time and “L” time of I/OLRCKA pin should be 1/256fs at least. The DIFA1-0 bits select eight modes.

Mode	Master /slave	DIFA1	DIFA0	SDTOA	SDTIA1-3	LRCKA		BICKA		
							I/O		I/O	
8	Slave	0	0	24bit, L J	20bit, R J	↑	I	256fs	I	
9	Slave	0	1	24bit, L J	24bit, R J	↑	I	256fs	I	
10	Slave	1	0	24bit, L J	24bit, L J	↑	I	256fs	I	(default)
11	Slave	1	1	24bit, I^2S	24bit, I^2S	↓	I	256fs	I	
12	Master	0	0	24bit, L J	20bit, R J	↑	O	256fs	O	
13	Master	0	1	24bit, L J	24bit, R J	↑	O	256fs	O	
14	Master	1	0	24bit, L J	24bit, L J	↑	O	256fs	O	
15	Master	1	1	24bit, I^2S	24bit, I^2S	↓	O	256fs	O	

Table 32. Audio Interface Format (TDM 256 mode, L J: Left justified, R J: Right justified.)

1-3. TDM 128 mode: TDMA1-0 bit = “11”

The TDMA1-0 bits = “11” set the AK4683 audio serial interface format to the TDM 1286 mode. The four channel serial data (SDTIA1, 2) is input to the SDTIA1 pin. Other two channel data (SDTIA3) is input to the SDTIA2 pin.

Mode	Master /slave	DIFA1	DIFA0	SDTOA	SDTIA1-3	LRCKA		BICKA		
							I/O		I/O	
16	Slave	0	0	24bit, L J	20bit, R J	↑	I	128fs	I	
17	Slave	0	1	24bit, L J	24bit, R J	↑	I	128fs	I	
18	Slave	1	0	24bit, L J	24bit, L J	↑	I	128fs	I	(default)
19	Slave	1	1	24bit, I^2S	24bit, I^2S	↓	I	128fs	I	
20	Master	0	0	24bit, L J	20bit, R J	↑	O	128fs	O	
21	Master	0	1	24bit, L J	24bit, R J	↑	O	128fs	O	
22	Master	1	0	24bit, L J	24bit, L J	↑	O	128fs	O	
23	Master	1	1	24bit, I^2S	24bit, I^2S	↓	O	128fs	O	

Table 33. Audio Interface Format (TDM 128 mode, L J: Left justified, R J: Right justified.)

2. Setting for the PORTB

2-1: Normal mode:

The PORTB supports only the normal mode. The DIFB1-0 bits select following eight serial data format (Table 34).

Mode	Master /slave	DIFB1	DIFB0	SDTOB	SDTIB	LRCKB		BICKB		
							I/O		I/O	
0	Slave	0	0	24bit, L J	20bit, R J	H/L	I	≥ 48fs	I	
1	Slave	0	1	24bit, L J	24bit, R J	H/L	I	≥ 48fs	I	
2	Slave	1	0	24bit, L J	24bit, L J	H/L	I	≥ 48fs	I	(default)
3	Slave	1	1	24bit, I^2S	24bit, I^2S	L/H	I	≥ 48fs	I	
4	Master	0	0	24bit, L J	20bit, R J	H/L	O	64fs	O	
5	Master	0	1	24bit, L J	24bit, R J	H/L	O	64fs	O	
6	Master	1	0	24bit, L J	24bit, L J	H/L	O	64fs	O	
7	Master	1	1	24bit, I^2S	24bit, I^2S	L/H	O	64fs	O	

Table 34. Audio Interface Format (Normal mode, L J: Left justified, R J: Right justified.)

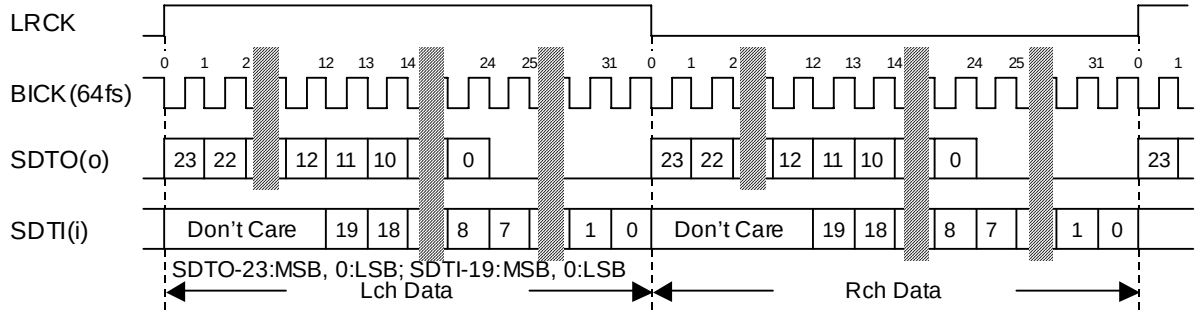


Figure 8. Mode 0,4 Timing

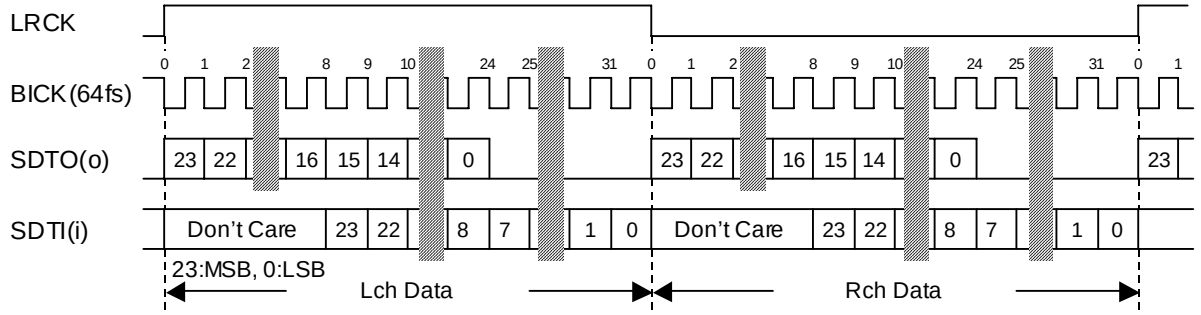


Figure 9. Mode 1 ,5 Timing

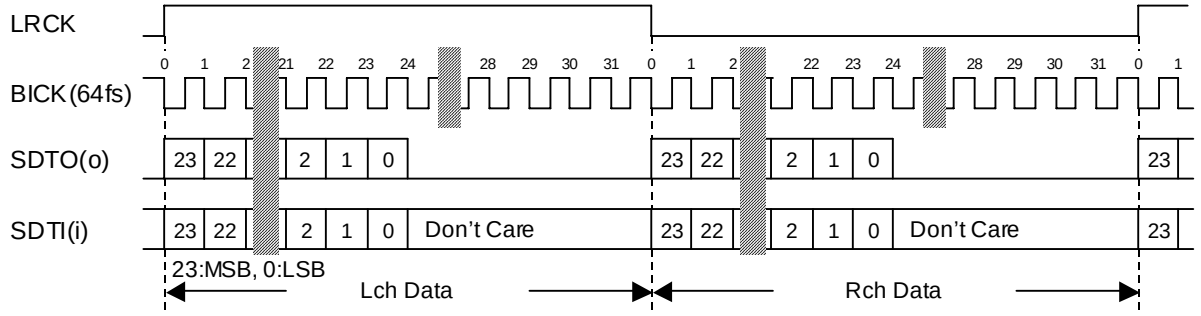


Figure 10.Mode 2,6 Timing

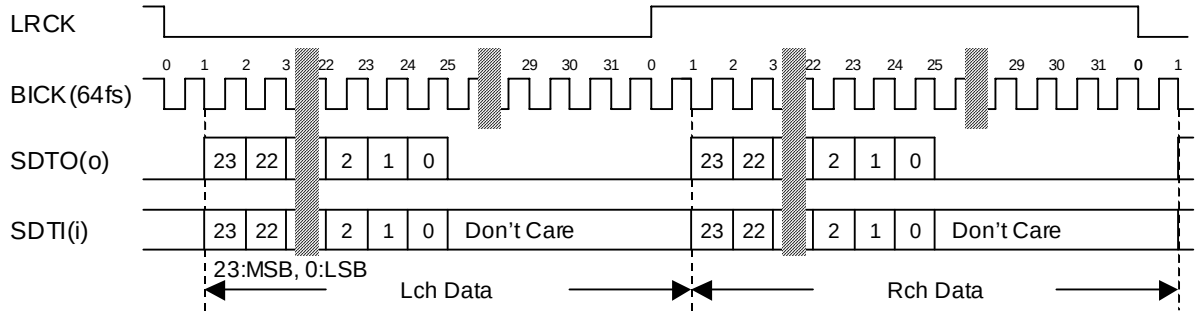


Figure 11. Mode 3 ,7 Timing

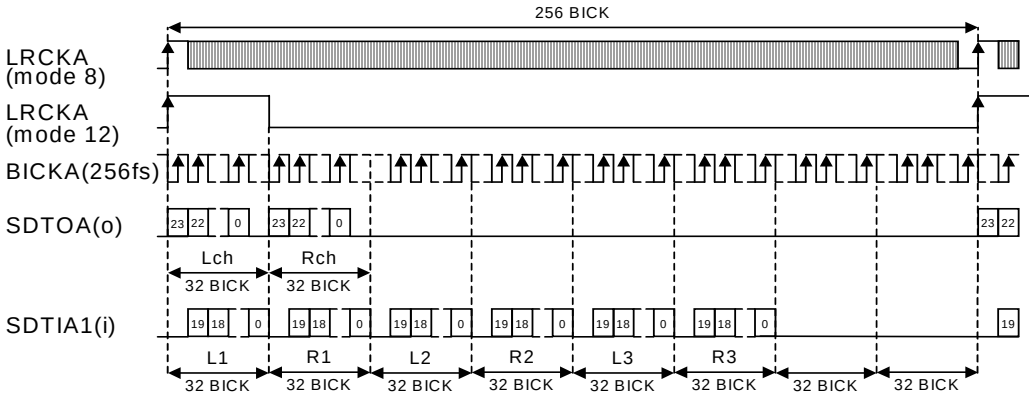


Figure 12. Mode 8 ,12 Timing

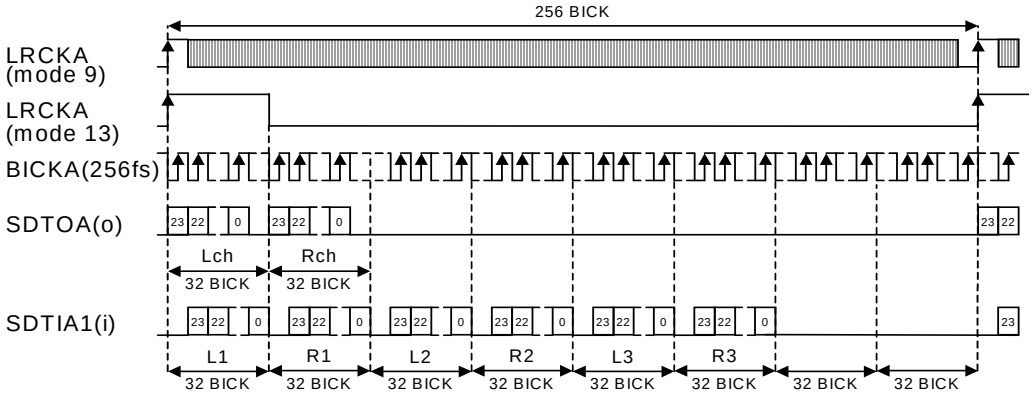


Figure 13. Mode 9 ,13 Timing

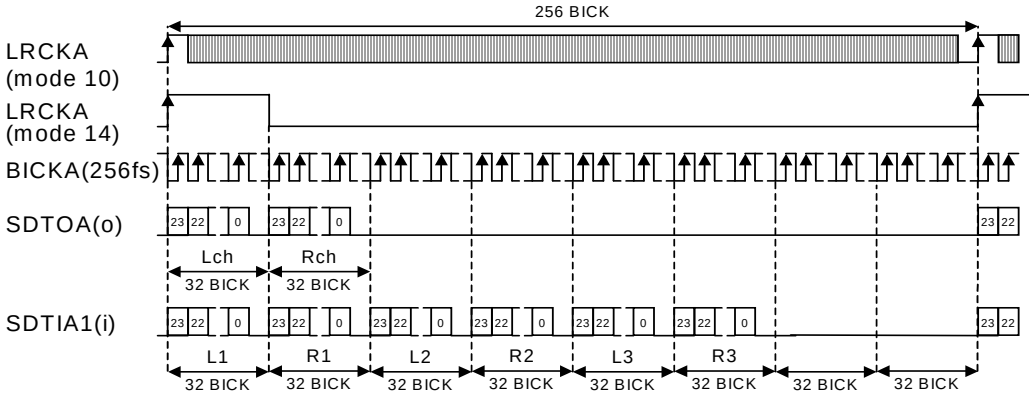


Figure 14. Mode 10 ,14 Timinig

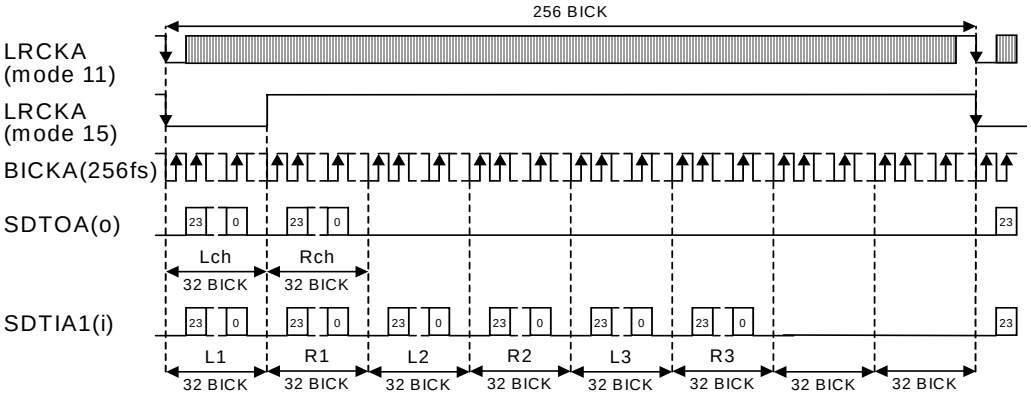


Figure 15. Mode 11 ,15 Timing

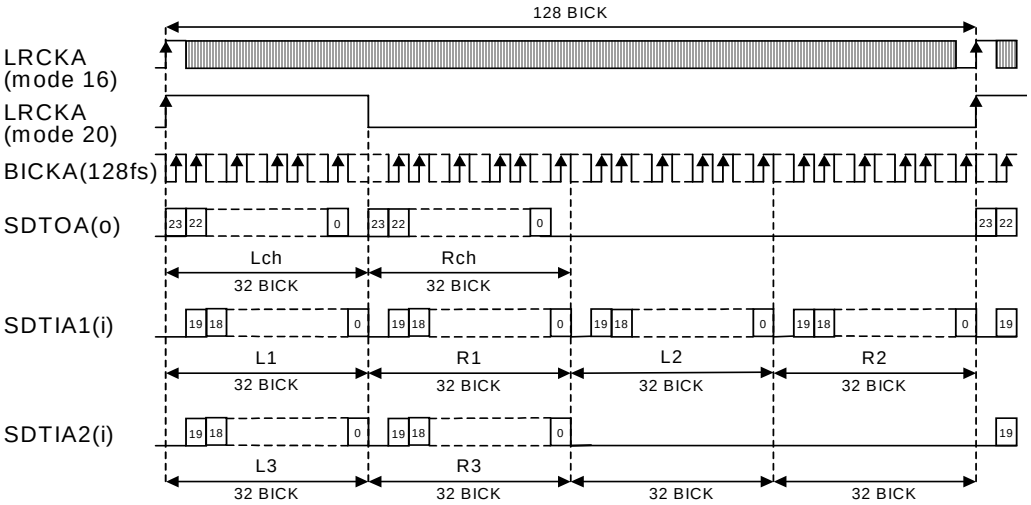


Figure 16. Mode 16 ,20 Timing

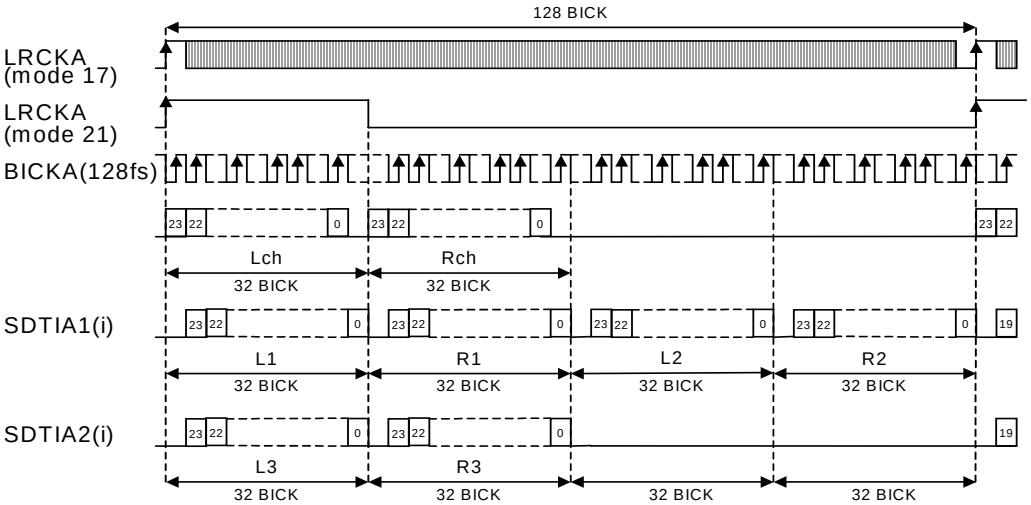


Figure 17. Mode 17 ,21 TIming

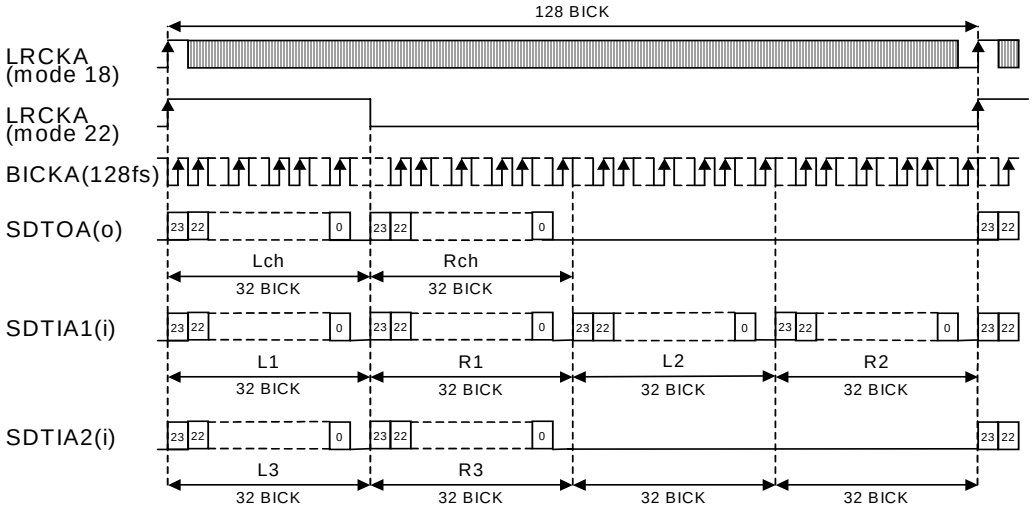


Figure 18. Mode 18 ,22 Timing

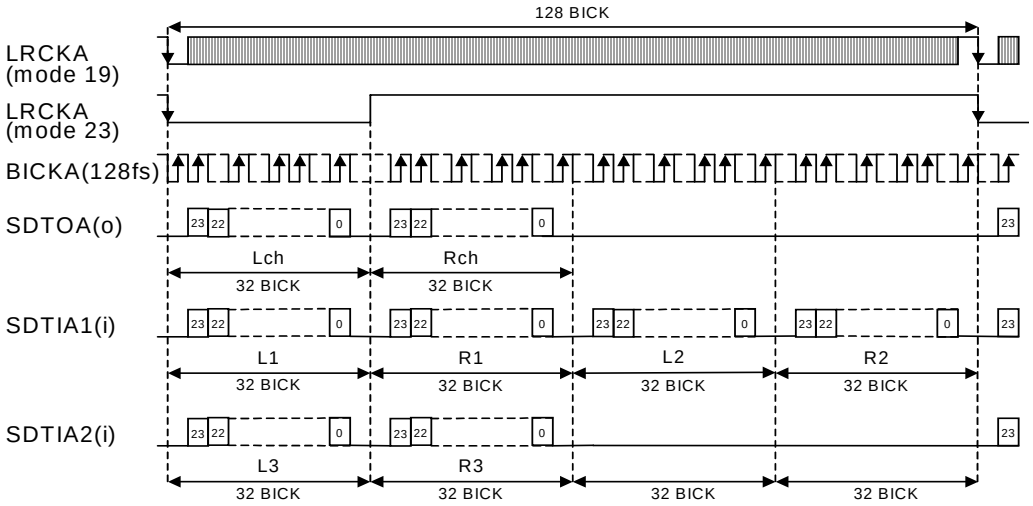


Figure 19. Mode 19 ,23 Timing

■ Digital Volume Control

The AK4683 has channel-independent digital volume control (256 levels, 0.5dB step). The ATTAD7-0 bit set the volume level of each ADC channel (Table 35), ATTDA7-0 set each DAC channel (Table 36).

ATTAD7-0	Attenuation Level	
00H	+24dB	
01H	+23.5dB	
02H	+22.0dB	
:	:	
2FH	+0.5dB	
30H	0dB	(default)
31H	-0.5dB	
	:	
FEH	-103dB	
FFH	MUTE (-∞)	

Table 35.ADC Digital Volume

ATTDA7-0	Attenuation Level	
00H	+12dB	
01H	+11.5dB	
02H	+11.0dB	
:	:	
17H	+0.5dB	
18H	0dB	(default)
19H	-0.5dB	
	:	
FEH	-115dB	
FFH	MUTE (-∞)	

Table 36.DAC Digital Volume

Transition time between set values of ATTAD7-0 (ATTDA7-0) bits can be selected by ATSAD (ATSDA) bits (Table 37, Table 38). Transition between set values of Mode 0 and Mode 1is the soft transition. Therefore, the switching noise does not occur in the transition.

Mode	ATSAD	ATT speed	
0	0	1061/fs	(default)
1	1	256/fs	

Table 37. Transition time between set values of ATTAD7-0 bits (ADC)

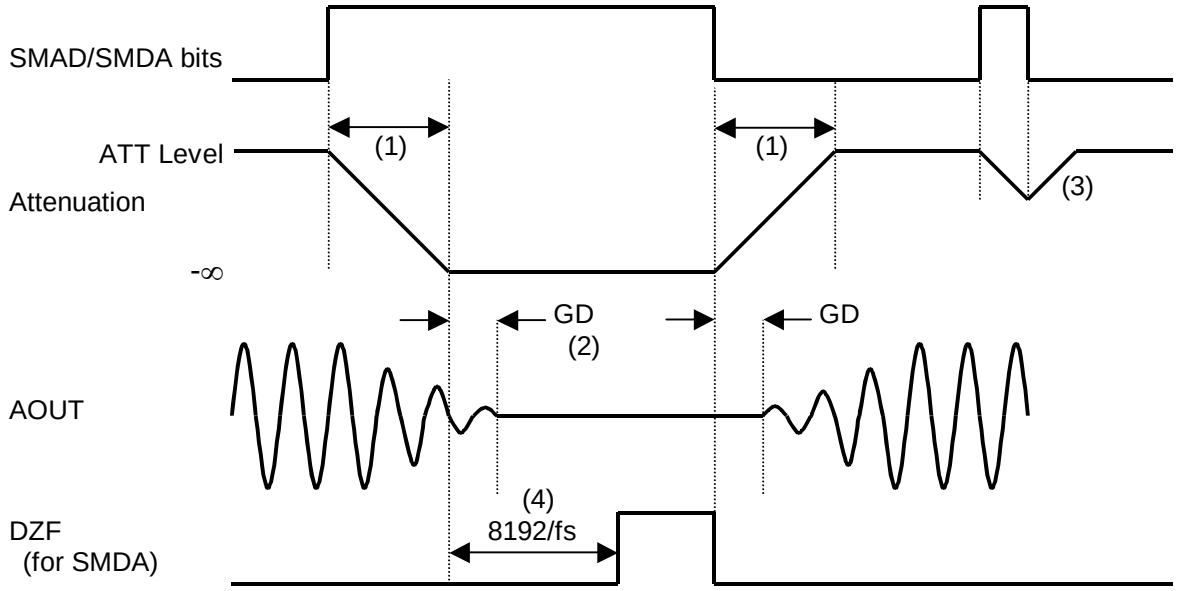
Mode	ATSDA	ATT speed	
0	0	1061/fs	(default)
1	1	256/fs	

Table 38. Transition time between set values of ATTDA7-0 bits (DAC)

The transition between set values is soft transition of 1061 levels in Mode 0. It takes 1061/fs (24ms@fs=48kHz) from 00H to FFH(MUTE) in Mode 0. If PDN pin goes to “L”, the ATTAD7-0(ATTDA7-0) bits are initialized to 30H(18H). The ATTs goes to their default value when RSTN1 bit = “0”. When RSTN1 bit return to “1”, the ATTs fade to their current value.

■ Soft mute operation

The ADC and DAC have the soft mute function. The soft mute operation is performed at digital domain. When the SMAD/SMDA bits go to "1", the output signal is attenuated by -∞ during ATT_DATA×ATT transition time (Table 37, Table 38) from the current ATT level. When the SMAD/SMDA bits are returned to "0", the mute is cancelled and the output attenuation gradually changes to the ATT level during ATT_DATA×ATT transition time. If the soft mute is cancelled before attenuating to -∞ after starting the operation, the attenuation is discontinued and returned to ATT level by the same cycle. The soft mute is effective for changing the signal source without stopping the signal transmission.



Notes:

(1) ATT_DATA×ATT transition time (Table 37, Table 38). For example, in Normal Speed Mode, this time is 1061/fs cycles (1792/fs) at ATT_DATA=00H. ATT transition of the soft-mute is from 00H to FFH

(2) The analog output corresponding to the digital input has a group delay, GD.

(3) If the soft mute is cancelled before attenuating to -∞ after starting the operation, the attenuation is discontinued and returned to ATT level by the same cycle.

(4) When the input data at all the channels of the group are continuously zeros for 8192 cycles, DZF pin of each channel goes to "H". DZF pin immediately goes to "L" if the input data of either channel of the group are not zero after going DZF "H".

Figure 20. Soft mute and zero detection

■ Input Selector, Input Attenuator

The AK4683 includes 6ch stereo input selectors (Figure 21). The input selector is 6 to 1 selector. The AIN2-0 bits set the input channel (Table 39).

AIN2 bit	AIN1 bit	AIN0 bit	Input Selector	
0	0	0	LIN1 / RIN1	Default
0	0	1	LIN2 / RIN2	
0	1	0	LIN3 / RIN3	
0	1	1	LIN4 / RIN4	
1	0	0	LIN5 / RIN5	
1	0	1	LIN6 / RIN6	
1	1	0	None	
1	1	1	None	

Table 39. Input Selector

The input ATTs are constructed by adding the input resistor (Ri) for LIN1-6/RIN1-6 pins and the feedback resistor (Rf) between LOPIN (ROPIN) pin and LISEL (RISEL) pin (Figure 21). The voltage range of the LISEL(RISEL) pin should be less than typ. 0.62 x AVDD1 (Vpp). If the input voltage of the input selector exceeds typ. 0.62 x AVDD, the input voltage of the LISEL(RISEL) pins must be attenuated to typ. 0.62 x AVDD1 (Vpp) by the input ATTs. The Table 40 shows the example of Ri and Rf.

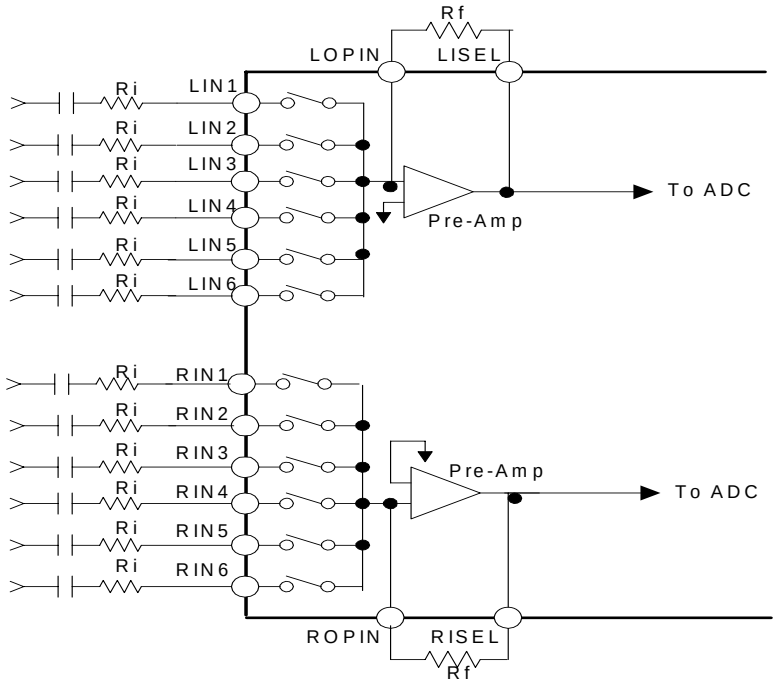


Figure 21. Input ATT

Input Range	Ri [kΩ]	Rf [kΩ]	ATT Gain [dB]	LISEL/R pin
4Vrms	47	12	–11.86	1.02Vrms (2.88Vpp)
2Vrms	47	24	–5.84	1.02Vrms (2.88Vpp)
1Vrms	47	47	0	1Vrms (2.82Vpp)

Note: Input range of internal ADC is 0.62 x AVDD1 (5V) = 3.1Vpp typ.

Table 40. Input ATT example

[Input selector switching sequence]

The input selector should be changed after soft mute to avoid the switching noise of the input selector (Figure 22).

1. Enable the soft mute before changing channel.
2. Change channel.
3. Disable the soft mute.

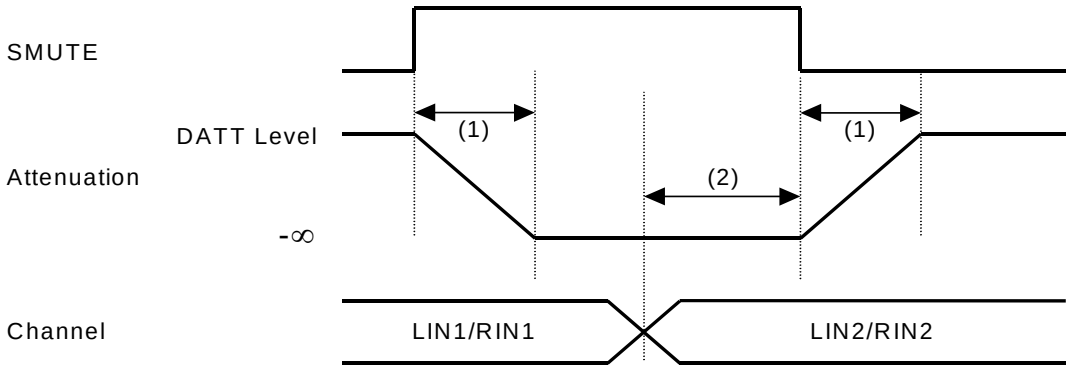


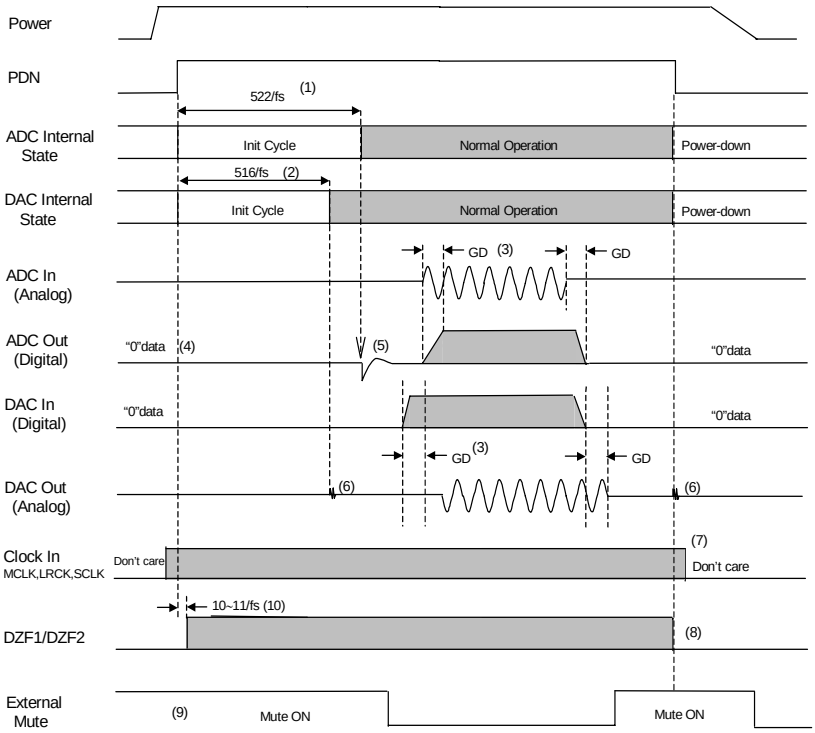
Figure 22. Input channel switching sequence example

The period of (1) varies in the setting value of DATT. It takes 1028/fs to mute when DATT value is +24dB.

When changing channels, the input channel should be changed during (2). The period of (2) should be around 200ms because there is some DC difference between the channels.

■ Power ON/OFF Sequence

The each block of the AK4683 are placed in the power-down mode by bringing PDN pin "L" and both digital filters are reset at the same time. PDN pin "L" also reset the control registers to their default values. In the power-down mode, the analog outputs go to VCOM voltage and SDTOA,B, DZF/OVF pin go to "L". This reset should always be done after power-up.
In slave mode, after exiting reset at power-up etc., the AK4683 starts to operate from the rising edge of LRCK after MLCK, then the device is in the power-down mode until MCLK and LRCK are input. In slave mode or Internal Loop Mode, the AK4683 starts to operate by the input of MLCK after exiting reset.
The analog initialization cycle of ADC starts after exiting the power-down mode. Therefore, the output data, SDTO becomes available after 522/fs cycles of LRCK clock. In case of the DAC, an analog initialization cycle starts after exiting the power-down mode. The analog outputs are VCOM voltage during the initialization. Figure 23 hows the sequences of the power-down and the power-up.
The ADC and all DACs can be powered-down individually by PWAD bit , PWDA bit and PWDA2-1 bits. These bits don't initialize the internal register values. When PWAD bit = "0" and selecting ADC, the SDTOA(SDTOB) pin goes to "L". When PWDA bit and PWDA1-2 bits = "0", the analog outputs go to VCOM voltage and DZF/OVF pin go to "H". Since some click noise may occur, the analog output should muted externally if the click noise influences system application.



Notes:
(1) The analog part of ADC is initialized after exiting the power-down state.
(2) The analog part of DAC is initialized after exiting the power-down state.
(3) Digital output corresponding to analog input and analog output corresponding to digital input have the group delay (GD).
(4) ADC output is "0" data at the power-down state.
(5) Click noise occurs at the end of initialization of the analog part. Please mute the digital output externally if the click noise influences system application.
(6) Click noise occurs at the falling edge of PDN and at 512/fs(DAC1) and 512/fs +96ms(DAC2) after the rising edge of PDN.
(7) When the external clocks (MCLK, BICKA (BICKB), LRCKA (LRCKB)) are stopped, the AK4683 should be in the power-down mode.
(8) DZF/OVF pin is "L" in the power-down mode (PDN pin = "L").
(9) Please mute the analog output externally if the click noise (6) influences system application.
(10) DZF pin = "L" for 10~11/fs after PDN= "↑".

Figure 23. Power-down/up sequence example

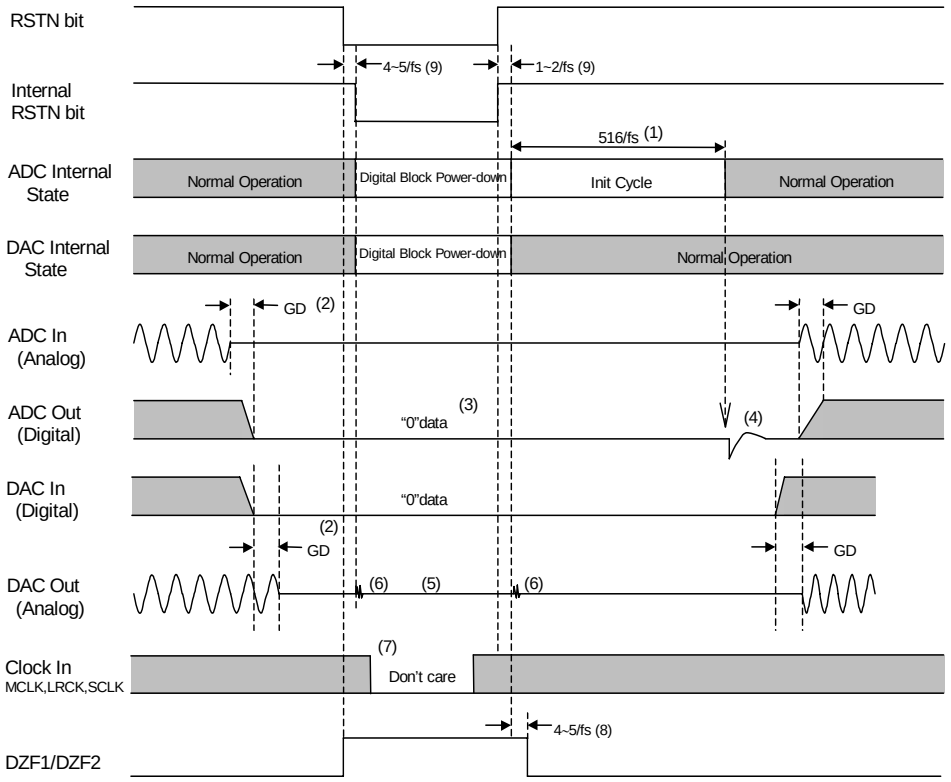
■ Status of analog output pins during power-down (PDN pin ="L")

The status of analog output pins is as follows.

Pin Name	
HPL/HPR	HVSS
LOUT1/ROUT1/LOUT2/ROUT2	VCOM
LISEL/RISEL	Hi-Z

■ Reset Function

When RSTN1 bit = "0", ADC and DACs are powered-down but the internal register are not initialized. The analog outputs go to VCOM voltage, DZF/OVF pin goes to "H" and SDTOA/B pins go to "L". Because some click noise occurs, the analog output should be muted externally if the click noise influences system application. The Figure 24 shows the power-up sequence.



Notes:

(1) The analog part of ADC is initialized after exiting the reset state.

(2) Digital output corresponding to analog input and analog output corresponding to digital input have the group delay (GD).

(3) ADC output is "0" data at the power-down state.

(4) Click noise occurs when the internal RSTN bit becomes "1". Please mute the digital output externally if the click noise influences system application.

(5) When RSTN1 bit = "0", the analog outputs go to VCOM voltage.

(6) Click noise occurs at 4~5/fs after RSTN1 bit becomes "0", and occurs at 1~2/fs after RSTN1 bit becomes "1". This noise is output even if "0" data is input.

(7) The external clocks (MCLK, BICKA (BICKB), LRCKA (LRCKB)) can be stopped in the reset mode. When exiting the reset mode, "1" should be written to RSTN1 bit after the external clocks (MCLK, BICKA (BICKB), LRCKA (LRCKB)) are fed.

(8) DZF pins go to "H" when the RSTN1 bit becomes "0", and go to "L" at 6~7/fs after RSTN1 bit becomes "1".

(9) There is a delay, 4~5/fs from RSTN1 bit "0" to the internal RSTN bit "0".

Figure 24. Reset sequence example

■ Headphone Output

Power supply voltage for the Headphone-Amp is supplied from the HVDD pin and centered on the HVDD/2 voltage. When the MUTEN bit is "0", the common voltage of Headphone-Amp falls and the outputs (HPL and HPR pins) go to "L" (HVSS). When the MUTEN bit is "1", the common voltage rises to HVDD/2. A capacitor between the MUTET pin and ground reduces click noise at power-up. Rise/Fall time constant is proportional to HVDD voltage and the capacitor at MUTET pin.

[Example]: A capacitor between the MUTET pin and ground = 1.0μF, HVDD=5V:
Rise/fall time constant: τ = 120ms(typ)

When PWHP bit is "0", the Headphone-Amp is powered-down, and the outputs (HPL and HPR pins) go to "L" (HVSS).

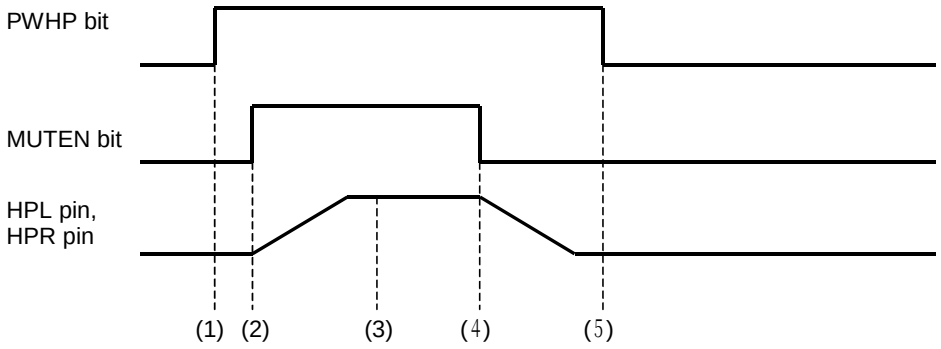


Figure 25. Power-up/Power-down Timing for Headphone-Amp

(1) Headphone-Amp power-up (PWHP bit = "1"). The outputs are still HVSS.
(2) Headphone-Amp common voltage rises up (MUTEN bit = "1"). Common voltage of Headphone-Amp is rising.
(3) Start the audio output after finishing the setup pf common voltage to prevent the clipping.
(4) Headphone-Amp common voltage falls down (MUTEN bit = "0"). Common voltage of Headphone-Amp is falling.
(5) Headphone-Amp power-down (PWHP bit = "0"). The outputs are HVSS. If the power supply is switched off or Headphone-Amp is powered-down before the common voltage goes to HVSS, some CLICK noise occurs.

The cut-off frequency (fc) of Headphone-Amp depends on the external resistor and capacitor. Table 41 shows the cut off frequency and the output power for various resistor/capacitor combinations. The headphone impedance R_L is 16Ω. Output powers are shown at HVDD = 5V.

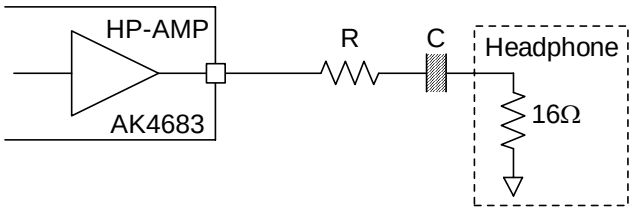


Figure 26. External Circuit Example of Headphone

R [Ω]	C [μF]	fc [Hz]	Output Power [mW]@0dBFS
0	220	45	50
	100	100	
6.8	100	70	25
	47	149	
16	100	50	12.5
	47	106	

Table 41. External Circuit Example

■ Output Analog Volume (OPGA)

Volume range of the output analog volume is 0dB to -50dB and MUTE with by zero crossing detection. The OPGA is operated by the clock for DAC. The zero crossing detection of Lch and Rch is worked independently. If there are no zero-crossings, the level will then change after a timeout period; the timeout period scales with fs. When ZCE is "0", it is changed immediately without zero crossing detection.

When writing to OPGA4-0 bits continually, it should take an interval of zero crossing timeout period or more. If the OPGA4-0 bits are changed before zero crossing, the volume of Lch and Rch may differ. When the volume that is same as the present is set, the zero crossing counter isn't reset and timeout according to the previous writing timing.

OPGA4-0	GAIN(dB)	STEP	LEVEL	
1FH	+0	1dB	17	
1EH	-1			
1DH	-2			
:	:			
10H	-15			
0FH	-16			
0EH	-18	2dB	11	
0DH	-20			
:	:			
05H	-36			
04H	-38			
03H	-42	4dB	3	
02H	-46			
01H	-50			
00H	MUTE		1	(default)

Table 42. Output Analog Volume Setting

When ZCE bit is "1", the Lch/Rch volume level are changed independently by zero crossing detection or zero crossing timeout operation. The count of timer is doubled when DAC double speed mode, four times when DAC quad speed mode.

DAC2 Sampling Speed	Zero crossing timeout
Normal Speed Mode	768/fs (16ms @fs=48kHz)
Double Speed Mode	1536/fs (16ms @fs=96kHz)
Quad Speed Mode	3072/fs (16ms @fs=192kHz)

Table 43. Zero crossing timeout

The OPGA is enable at PWDA bit = PWDA2 bit = "1". The initializing of OPGA starts when DAC is powered up. This initializing cycle is 96ms(@fs=48kHz). Writing to the OPGA4-0 during the initialization is ignored. The default volume value is mute after power up. Initialization time is 512/fs+96ms(@fs=48kHz) after PDN pin = "H".

DAC2 Sampling Speed	OPGA Initialization Time
Normal Speed Mode	4608/fs (96ms @fs=48kHz)
Double Speed Mode	9216/fs (96ms @fs=96kHz)
Quad Speed Mode	18432/fs (96ms @fs=192kHz)

Table 44. OPGA Initialization Time

OPERATION OVERVIEW (DIR/DIT part)

■ 192kHz Clock Recovery

On chip low jitter PLL has a wide lock range with 32kHz to 192kHz and the lock time is less than 20ms. The AK4683 has the sampling frequency detect function. By either the clock comparison against X'tal oscillator or using the channel status, the AK4683 detects the sampling frequency (32kHz, 44.1kHz, 48kHz, 88.2kHz, 96kHz, 176.4kHz and 192kHz). The PLL loses lock when the received sync interval is incorrect.

■ Clock Operation Mode

When DIR is selected. the CM0/CM1 bits select the clock source and the data source of SDTO. In Mode 2, the clock source is automatically switched from PLL to XTI/MCLK2 when PLL goes unlock state. In Mode 3, the clock source is fixed to XTI/MCLK2, but PLL is also operating and the recovered data such as C bits can be monitored. For Mode 2 and 3, it is recommended that the frequency of XTI/MCLK2 is different from the recovered frequency from PLL.

Mode	CM1	CM0	UNLOCK	PLL	Clock source	SDTO	
0	0	0	-	ON	PLL	RX	(default)
1	0	1	-	OFF	EXTCLK	DIT source	
2	1	0	0	ON	PLL	RX	
			1	ON	EXTCLK	DIT source	
3	1	1	-	ON	EXTCLK	DIT source	

ON: Oscillation (Power-up), OFF: STOP (Power-down)

Table 45. Clock Operation Mode select

When 384fs of XTI/MCLK2 is supplied to DIR/DIT, CKSDT bit should be set to "1".

CKSDT bit	Clock Speed	
0	x 1	(default)
1	x 2/3	

Table 46. XTI/MCLK2 speed

■ Sampling Frequency and Pre-emphasis Detection

The AK4683 has two methods for detecting the sampling frequency as follows.

1. Clock comparison between recovered clock and XTI/MCLK2
2. Sampling frequency information on channel status

Those could be selected by XTL1, 0 bits. And the detected frequency is reported on FS3-0 bits.

XTL1	XTL0	XTI/MCLK2 Frequency	
0	0	11.2896MHz	(default)
0	1	12.288MHz	
1	0	24.576MHz	
1	1	(Use channel status)	

Table 47. Reference XTI/MCLK2 frequency

Register output				fs	Except XTL1,0= "1,1"	XTL1,0= "1,1"		
					Clock comparison (Note 1)	Consumer mode (Note 2)	Professional mode	
FS3	FS2	FS1	FS0			Byte3 Bit3,2,1,0	Byte0 Bit7,6	Byte4 Bit6,5,4,3
0	0	0	0	44.1kHz	44.1kHz	0 0 0 0	0 1	0 0 0 0
0	0	0	1	Reserved	Reserved	0 0 0 1	(Others)	
0	0	1	0	48kHz	48kHz	0 0 1 0	1 0	0 0 0 0
0	0	1	1	32kHz	32kHz	0 0 1 1	1 1	0 0 0 0
1	0	0	0	88.2kHz	88.2kHz	(1 0 0 0)	0 0	1 0 1 0
1	0	1	0	96kHz	96kHz	(1 0 1 0)	0 0	0 0 1 0
1	1	0	0	176.4kHz	176.4kHz	(1 1 0 0)	0 0	1 0 1 1
1	1	1	0	192kHz	192kHz	(1 1 1 0)	0 0	0 0 1 1

Note1: At least ±3% range is identified as the value in the Table 48. In case of intermediate frequency of those two, FS3-0 bits indicate nearer value. When the frequency is much bigger than 192kHz or much smaller than 32kHz, FS3-0 bits may indicate "0001".

Note2: When consumer mode, Byte3 Bit3-0 are copied to FS3-0 bits.

Table 48. fs Information

The pre-emphasis information is detected and reported on PEM bit. This information is extracted from channel 1 at default. It can be switched to channel 2 by CS12 bit in control register.

PEM	Pre-emphasis	Byte 0 Bits 3-5
0	OFF	≠ 0X100
1	ON	0X100

Table 49. PEM in Consumer Mode

PEM	Pre-emphasis	Byte 0 Bits 2-4
0	OFF	≠110
1	ON	110

Table 50. PEM in Professional Mode

■ De-emphasis Filter Control

The AK4683 includes the digital de-emphasis filter (tc=50/15μs) by IIR filter corresponding to four sampling frequencies (32kHz, 44.1kHz, 48kHz and 96kHz). When DEAU bit="1", the de-emphasis filter is enabled automatically by sampling frequency and pre-emphasis information in the channel status. The AK4683 goes this mode at default. Therefore, in Parallel Mode, the AK4683 is always placed in this mode and the status bits in channel 1 control the de-emphasis filter. In Serial Mode, DEM0/1 and DFS bits can control the de-emphasis filter when DEAU bit is "0". The internal de-emphasis filter is bypassed and the recovered data is output without any change if either pre-emphasis or de-emphasis Mode is OFF.

PEM	FS3	FS2	FS1	FS0	Mode
1	0	0	0	0	44.1kHz
1	0	0	1	0	48kHz
1	0	0	1	1	32kHz
1	1	0	1	0	96kHz
1	(Others)				OFF
0	x	x	x	x	OFF

Table 51. De-emphasis Auto Control at DEAU bit = "1" (default)

PEM	DFS	DEM1	DEM0	Mode	
1	0	0	0	44.1kHz	
1	0	0	1	OFF	(default)
1	0	1	0	48kHz	
1	0	1	1	32kHz	
1	1	0	0	OFF	
1	1	0	1	OFF	
1	1	1	0	96kHz	
1	1	1	1	OFF	
0	x	x	x	OFF	

Table 52. De-emphasis Manual Control at DEAU bit = "0"

■ System Reset and Power-Down

The AK4683 has a power-down mode for all circuits by PDN pin can be partially powerd-down by PWN bit. The RSTN2 bit initializes the register and resets the internal timing. The AK4683 should be reset once by bringing PDN pin = "L" upon power-up.

PDN pin: All analog and digital circuit are placed in the power-down and reset mode by bringing PDN pin = "L". All the registers are initialized, and clocks are stopped. Reading/Witting to the register are disabled.

RSTN2 bit: All the registers except PWN and RSTN2 bits are initialized by bringing RSTN2 bit = "0". The internal timings are also initialized. When RSTN2 bit = "0", the clock are output but SDTO pin is hold to "L". Witting to the register is not available except PWN and RSTN2 bits. Reading to the register is disabled.

PWN bit: The clock recovery part is initialized by bringing PWN bit = "0". In this case, clocks from PLL are stopped. The registers are not initialized and the mode settings are kept. Writing and Reading to the registers are enabled.

■ Biphase Input and Through Output

Eight receiver inputs (RX0-3) are available in Serial Control Mode. Only the RX0 input includes amplifier corresponding to unbalance mode and can accept the signal of 200mV or more. IPS1-0 bits select the receiver channel. The V bit can be output via pin.

IPS1 bit	IPS0 bit	DIR Source	
0	0	RX0	(default)
0	1	RX1	
1	0	RX2	
1	1	RX3	

Table 53. Recovery Data Select

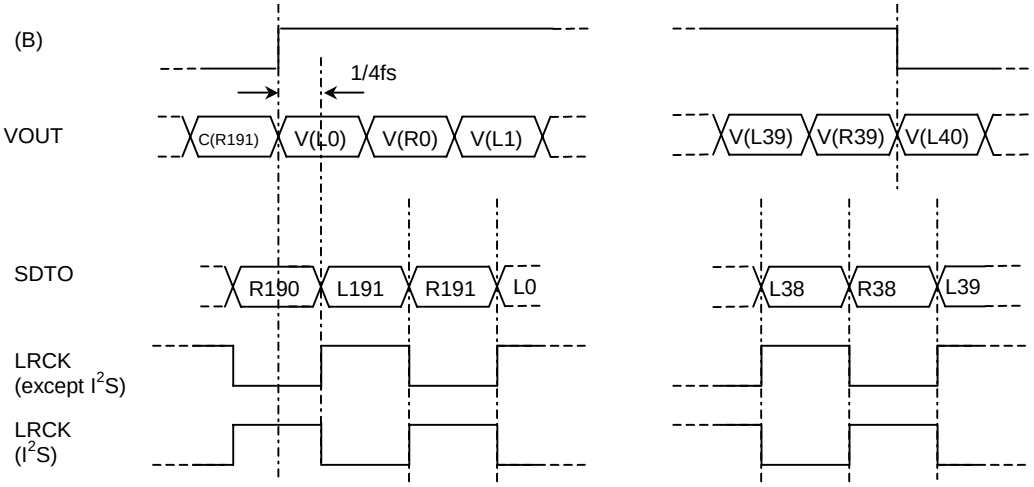


Figure 27. V output timings

■ Biphase Output

The AK4683 can output either the through output (from RX) or transmitter output (DIT) via TX pin. Those could be selected by DIT bit. The source of the through output from TX0 could be selected among RX0-3 by OPS0, 1 bits. When output DIT data, V bit could be controlled by VIN bit and first 5 bytes of C bit could be controlled by CT39-CT0 bits in control registers. When bit0= "0"(consumer mode), bit20-23 (Audio channel) could not be controlled directly but be controlled by CT20 bit. When the CT20 bit is "1", the AK4683 outputs "1000" as C20-23 for left channel and outputs "0100" at C20-23 for right channel automatically. When CT20 bit is "0", the AK4683 outputs "0000" set as "1000" for sub frame 1, and "0100" for sub frame 2. U bits are fixed to "0".

DIT bit	OPS1 bit	OPS0 bit	TX Source	
0	0	0	RX0	(default)
0	0	1	RX1	
0	1	0	RX2	
0	1	1	RX3	
1	*	*	DIT	

Table 54. TX Source Control

CM1-0 bit, CLKDT bit, CKSDT bit and OCKS1-0 select the clock source of DIT. This clock must be the same clock as the clock sources of PORT connecting to DIT.

CM1	CM0	UNLOCK	Clock Source	
0	0	-	RMCK	(default)
0	1	-	EXTCLK	
1	0	0	RMCK	
		1	EXTCLK	
1	1	-	EXTCLK	

Table 55. Clock Mode Control

CLKDT bit	Clock Source
0	XTI
1	MCLK2

Table 56. EXTCLK Control

CKSDT	OCKS1	OCKS0	EXTCLK	fs(max)
0	0	0	256fs	96kHz
0	0	1	256fs	96kHz
0	1	0	512fs	48kHz
0	1	1	128fs	192kHz
1	0	0	384fs	48kHz
1	0	1	384fs	48kHz
1	1	0	768fs	32kHz
1	1	1	192fs	96kHz

Table 57. MCLKO Speed

The DITD1-0 bits control the data source of DIT.

DITD1 bit	DITD0 bit	DIT Source
0	0	DIR
0	1	ADC
1	0	SDTIB
1	1	SDTIA1(default)

Table 58. DIT Source Control

■ Biphase signal input/output circuit (RX0, TX)

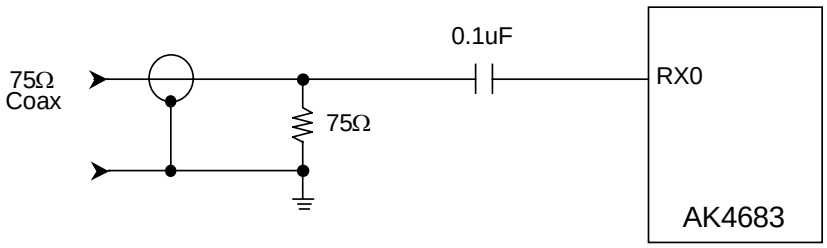


Figure 28. Consumer Input Circuit (Coaxial Input)

Note: In case of coaxial input, if a coupling level to this input from the next RX input line pattern exceeds 50mV, there is a possibility to occur an incorrect operation. In this case, it is possible to lower the coupling level by adding this decoupling capacitor.

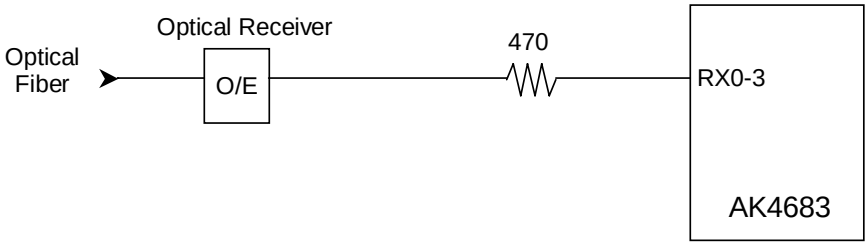


Figure 29. Consumer Input Circuit (Optical Input)

In case of coaxial input, as the input level of RX0 line is small, be careful not to crosstalk among RX input lines. For example, by inserting the shield pattern among them.

The AK4683 includes the TX output buffer. The output level meets combination 0.5V+/-20% using the external resistor network. The T1 in Figure 30 is a transformer of 1:1.

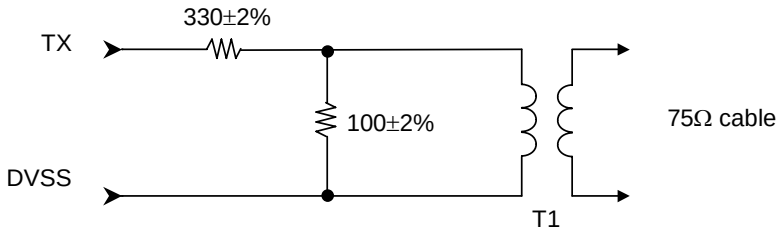


Figure 30. TX External Resistor Network

■ Q-subcode buffers

The AK4683 has Q-subcode buffer for CD application. The AK4683 takes Q-subcode into registers by following conditions.

1. The sync word (S0,S1) is constructed at least 16 "0"s.
2. The start bit is "1".
3. Those 7bits Q-W follows to the start bit.
4. The distance between two start bits are 8-16 bits.

The QINT bit in the control register goes "1" when the new Q-subcode differs from old one, and goes "0" when QINT bit is read.

	1	2	3	4	5	6	7	8	*
S0	0	0	0	0	0	0	0	0	0…
S1	0	0	0	0	0	0	0	0	0…
S2	1	Q2	R2	S2	T2	U2	V2	W2	0…
S3	1	Q3	R3	S3	T3	U3	V3	W3	0…
:	:	:	:	:	:	:	:	:	:
S97	1	Q97	R97	S97	T97	U97	V97	W97	0…
S0	0	0	0	0	0	0	0	0	0…
S1	0	0	0	0	0	0	0	0	0…
S2	1	Q2	R2	S2	T2	U2	V2	W2	0…
S3	1	Q3	R3	S3	T3	U3	V3	W3	0…
:	:	:	:	:	:	:	:	:	:
		↑		(*) number of "0" : min=0; max=8.					
		Q							

Figure 31. Configuration of U-bit(CD)

Q2	Q3	Q4	Q5	Q6	Q7	Q8	Q9	Q10	Q11	Q12	Q13	Q14	Q15	Q16	Q17	Q18	Q19	Q20	Q21	Q22	Q23	Q24	Q25
CTRL				ADRS				TRACK NUMBER								INDEX							

Q26	Q27	Q28	Q29	Q30	Q31	Q32	Q33	Q34	Q35	Q36	Q37	Q38	Q39	Q40	Q41	Q42	Q43	Q44	Q45	Q46	Q47	Q48	Q49
MINUTE								SECOND								FRAME							

Q50	Q51	Q52	Q53	Q54	Q55	Q56	Q57	Q58	Q59	Q60	Q61	Q62	Q63	Q64	Q65	Q66	Q67	Q68	Q69	Q70	Q71	Q72	Q73
ZERO								ABSOLUTE MINUTE								ABSOLUTE SECOND							

Q74	Q75	Q76	Q77	Q78	Q79	Q80	Q81	Q82	Q83	Q84	Q85	Q86	Q87	Q88	Q89	Q90	Q91	Q92	Q93	Q94	Q95	Q96	Q97
ABSOLUTE FRAME								CRC															

$G(x)=x^{16}+x^{12}+x^5+1$

Figure 32. Q-subcode

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
16H	Q-subcode Address / Control	Q9	Q8	…	…	…	…	Q3	Q2
17H	Q-subcode Track	Q17	Q16	…	…	…	…	Q11	Q10
18H	Q-subcode Index	…	…	…	…	…	…	…	…
19H	Q-subcode Minute	…	…	…	…	…	…	…	…
1AH	Q-subcode Second	…	…	…	…	…	…	…	…
1BH	Q-subcode Frame	…	…	…	…	…	…	…	…
1CH	Q-subcode Zero	…	…	…	…	…	…	…	…
1DH	Q-subcode ABS Minute	…	…	…	…	…	…	…	…
1EH	Q-subcode ABS Second	…	…	…	…	…	…	…	…
1FH	Q-subcode ABS Frame	Q81	Q80	…	…	…	…	Q75	Q74

Figure 33. Q-subcode register

■ Error Handling

There are the following eight events that make INT pin "H". INT pin show the status of following conditions.

1. UNLOCK: "1" when the PLL loses lock.
   The AK4683 loses lock when the distance between two preambles is not correct or when those preambles are not correct.
2. PAR: "1" when parity error or biphase coding error is detected, and keeps "1" until this register is read.
   Updated every sub-frame cycle. Reading this register resets itself.
3. AUTO: "1" when Non-PCM bitstream is detected.
   Updated every 4096 frames cycle.
4. DTSCD: "1" when DTS-CD bitstream is detected.
   Updated every DTS-CD sync cycle.
5. AUDION: "1" when the "AUDIO" bit in recovered channel status indicates "1".
   Updated every block cycle.
6. PEM: "1" when "PEM" in recovered channel status indicates "1".
   Updated every block cycle.
7. QINT: "1" when Q-subcode differ from old one, and keeps "1" until this register is read.
   Updated every sync code cycle for Q-subcode. Reading this register resets itself.
8. CINT: "1" when received C bits differ from old one, and keeps "1" until this register is read.
   Updated every block cycle. Reading this register resets itself.

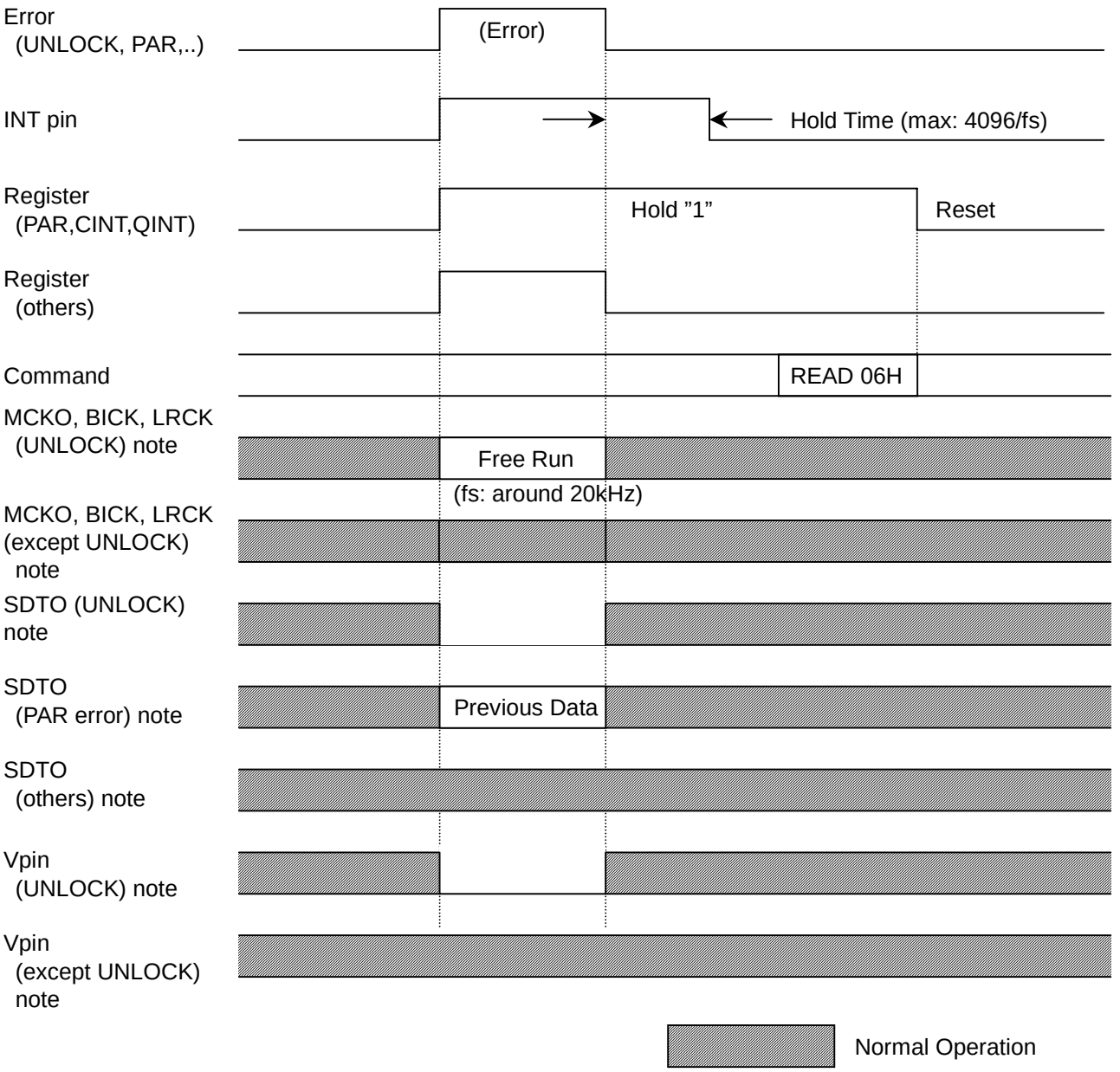
INT pin is fixed to "L" when the PLL is off (CM1,0= "01"). Once the INT pin goes to "H", this pin holds "H" for 1024/fs cycles (this value can be changed by EFH0/1 bits) after those events are removed. INT pin can mask those eight events individually. Once PAR, QINT and CINT bit goes to "1", those registers are held to "1" until those registers are read. While the AK4683 loses lock, registers regarding C-bit or U-bits are not initialized and keep previous value.

INT pin outputs the ORed signal among those eight events. However, each mask bits can mask each event. When each bit masks those events, the event does not affect INT pin operation (those mask do not affect those registers (UNLOCK, PAR, etc.) themselves. Once INT pin goes "H", it maintains "H" for 1024/fs cycles (this value can be changed by EFH0-1 bits) after the all events are removed. Once those PAR, QINT or CINT bit goes "1", it holds "1" until reading those registers. While the AK4683 loses lock, the channel status Q-subcode bits are not updated and hold the previous data. At initial state, INT outputs the ORed signal between UNLOCK and PAR.

Event								Pin		
UNLOCK	PAR	AUTO	DTSCD	AUDION	PEM	QINT	CINT	SDTO*	V*	TX*
1	x	x	x	x	x	x	x	"L"	"L"	Output
0	1	x	x	x	x	x	x	Previous Data	Output	Output
0	0	1	x	x	x	x	x	Output	Output	Output
0	0	x	1	x	x	x	x	Output	Output	Output
0	0	x	x	1	x	x	x	Output	Output	Output
0	0	x	x	x	1	x	x	Output	Output	Output
0	0	x	x	x	x	1	x	Output	Output	Output
0	0	x	x	x	x	x	1	Output	Output	Output

Note: when selected.

Table 59. Error Handling



Note: When DIR is selected as source.

Figure 34. INT0/1 pin timing

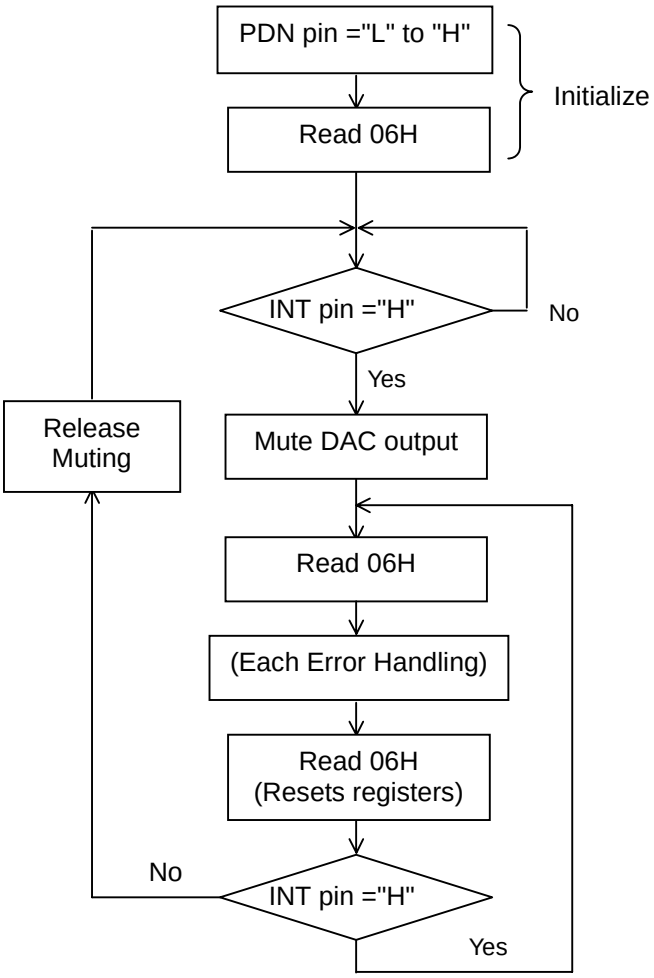


Figure 35. Error Handling Sequence Example 1

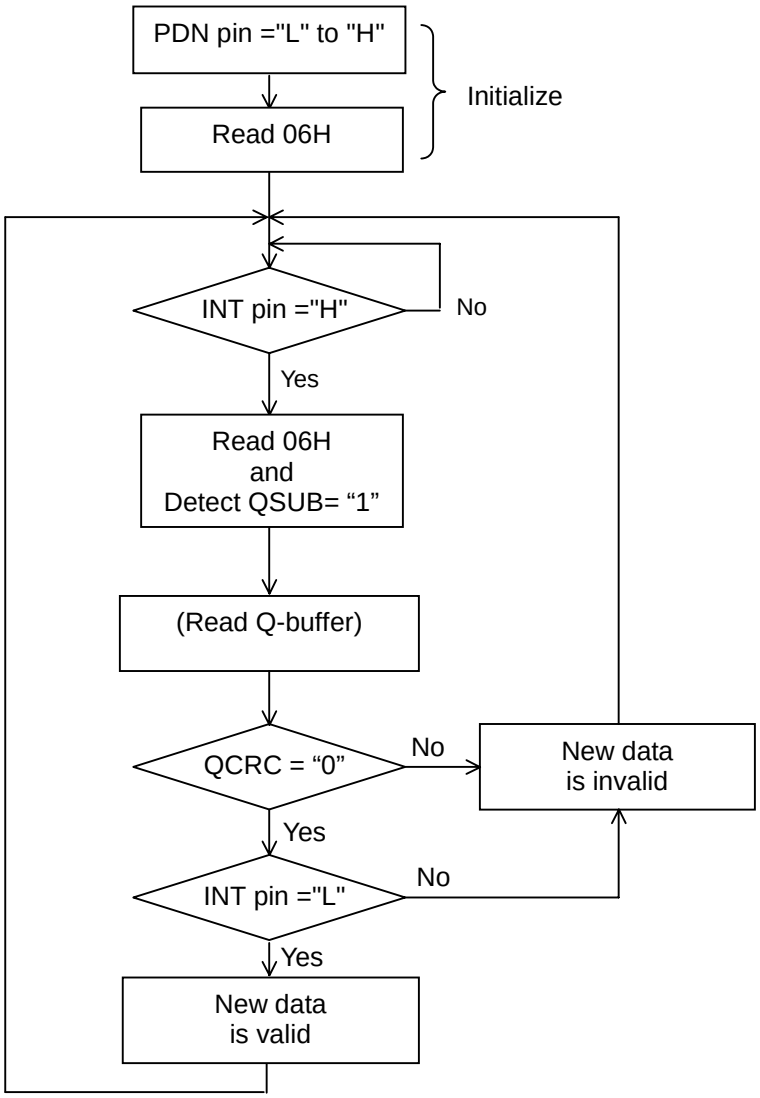


Figure 36. Error Handling Sequence Example 2 (for Q/CINT)

■ Non-PCM (AC-3, MPEG, etc.) and DTS-CD Bitstream Detection

The AK4683 has a Non-PCM steam auto-detection function. When the 32bit mode Non-PCM preamble based on Dolby "AC-3 Data Stream in IEC60958 Interface" is detected, the AUTO bit goes "1". The 96bit sync code consists of 0x0000, 0x0000, 0x0000, 0x0000, 0xF872 and 0x4E1F. Detection of this pattern will set the AUTO bit "1". Once the AUTO bit is set "1", it will remain "1" until 4096 frames pass through the chip without additional sync pattern being detected. When those preambles are detected, the burst preambles Pc and Pd that follow those sync codes are stored to registers. The AK4683 also has the DTS-CD bitstream auto-detection function. When The AK4683 detects DTS-CD bitstreams, DTSCD bit goes to "1". When the next sync code does not come within 4096 flames, DTSCD bit goes to "0" until when the AK4683 detects the stream again.

■ Burst Preambles in non-PCM Bitstreams

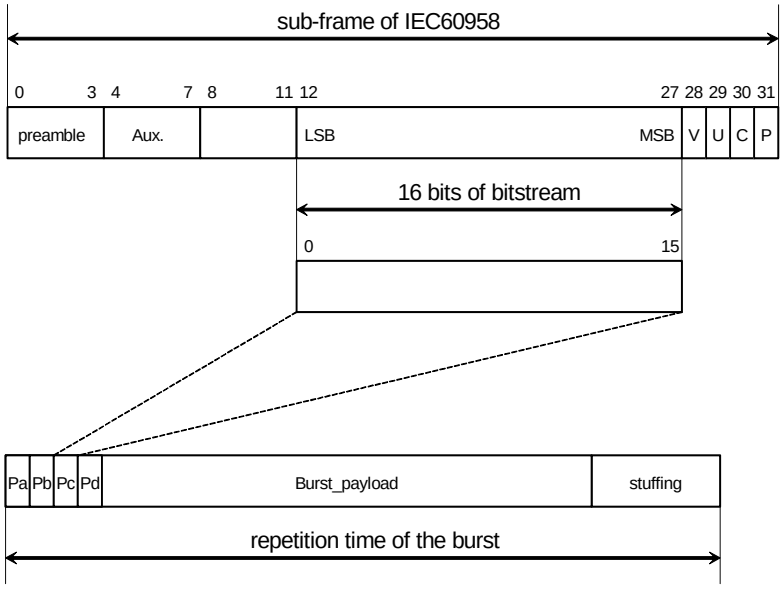


Figure 37. Data structure in IEC60958

Preamble word	Length of field	Contents	Value
Pa	16 bits	sync word 1	0xF872
Pb	16 bits	sync word 2	0x4E1F
Pc	16 bits	Burst info	see Table 61
Pd	16 bits	Length code	Numbers of bits

Table 60. Burst preamble words

Bits of Pc	Value	Contents	Repetition time of burst in IEC60958 frames
0-4		data type	
	0	NULL data	≤4096
	1	Dolby AC-3 data	1536
	2	reserved	
	3	PAUSE	
	4	MPEG-1 Layer1 data	384
	5	MPEG-1 Layer2 or 3 data or MPEG-2 without extension	1152
	6	MPEG-2 data with extension	1152
	7	MPEG-2 AAC ADTS	1024
	8	MPEG-2, Layer1 Low sample rate	384
	9	MPEG-2, Layer2 or 3 Low sample rate	1152
	10	reserved	
	11	DTS type I	512
	12	DTS type II	1024
	13	DTS type III	2048
	14	ATRAC	512
	15	ATRAC2/3	1024
	16-31	reserved	
5, 6	0	reserved, shall be set to “0”	
7	0	error-flag indicating a valid burst_payload	
	1	error-flag indicating that the burst_payload may contain errors	
8-12		data type dependent info	
13-15	0	bit stream number, shall be set to “0”	

(Refer the IEC standards.)

Table 61. Fields of burst info Pc

■ Non-PCM Bitstream timing

1) When Non-PCM preamble is not coming within 4096 frames,

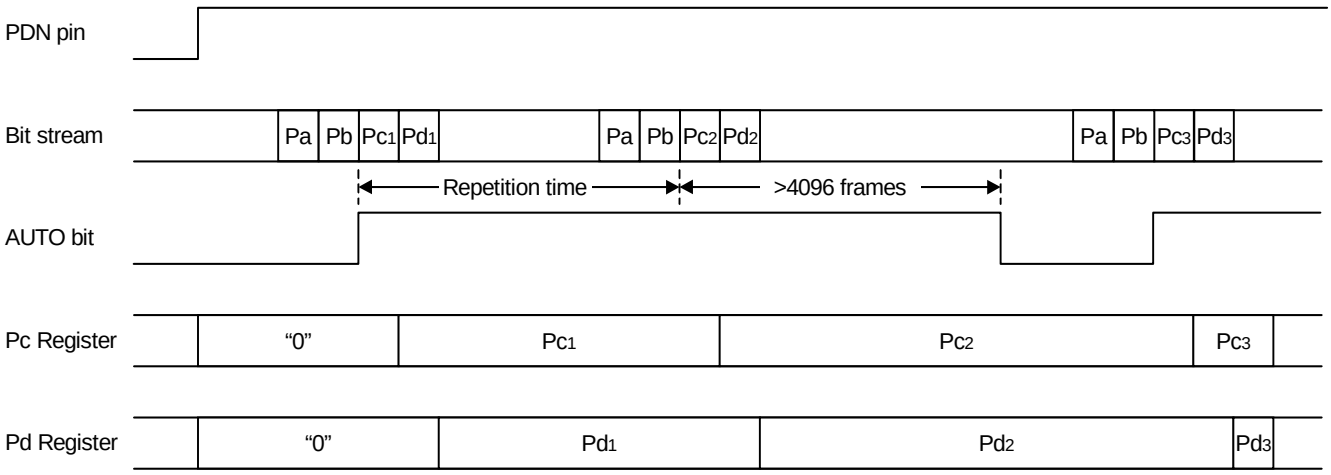


Figure 38. Timing example 1

2) When Non-PCM bitstream stops (when MULK0=0),

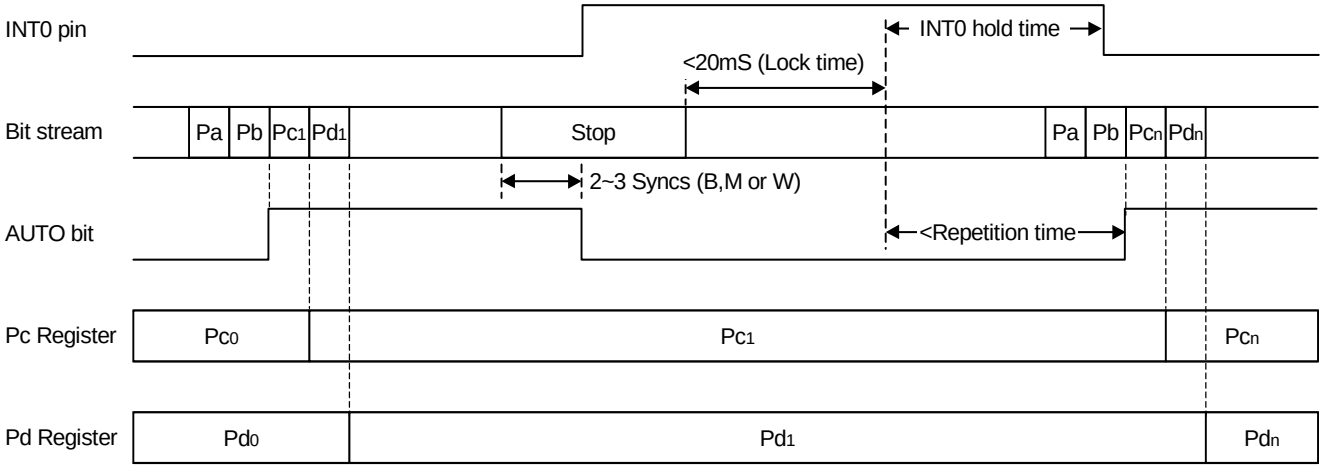


Figure 39. Timing example 2

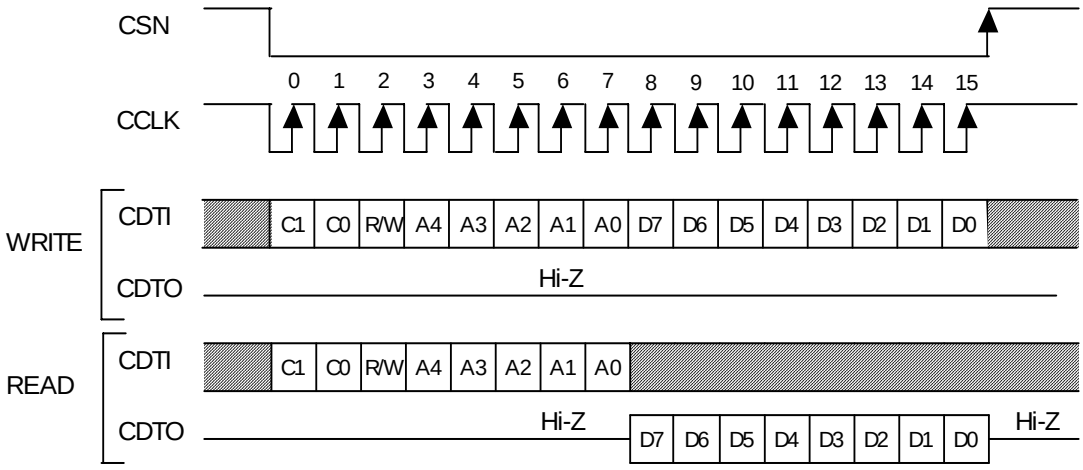
OPERATION OVERVIEW (ADC/DAC part, DIR/DIT part)

■ Serial Control Interface

The AK4683 has two registers, which are ADC/DAC part and DIR/DIT part. Each register is set by chip address pin.

(1). 4-wire serial control mode (I2C pin = "L")

The internal registers may be either written or read by the 4-wire μP interface pins: CSN, CCLK, CDTI & CDTO. The data on this interface consists of Chip address (2bits, C1-C0= ",10" for ADC/DAC part, "00" for DIR/DIT part), Read/Write (1bit), Register address (MSB first, 5bits) and Control data (MSB first, 8bits). Address and data is clocked in on the rising edge of CCLK and data is clocked out on the falling edge. For write operations, data is latched after the 16th rising edge of CCLK, after a high-to-low transition of CSN. For read operations, the CDTO output goes high impedance after a low-to-high transition of CSN. The maximum speed of CCLK is 5MHz. PDN pin = "L" resets the registers to their default values. When the state of P/S pin is changed, the AK4683 should be reset by PDN pin = "L". Register of ADC/DAC part can not read.



C1-C0: Chip Address: (Fixed to "10" for ADC/DAC part, "00" for DIR/DIT part)
R/W: READ/WRITE (0:READ, 1:WRITE)
A4-A0: Register Address
D7-D0: Control Data

Figure 40. 4-wire Serial Control I/F Timing

(2). I^2C bus control mode (I2C pin = "H")

AK4683 supports the standard-mode I^2C-bus (max: 100kHz). Then AK4683 does not support a fast-mode I^2C-bus system (max: 400kHz).

(2)-1. Data transfer

All commands are preceded by a START condition. After the START condition, a slave address is sent. After the AK4683 recognizes the START condition, the device interfaced to the bus waits for the slave address to be transmitted over the SDA line. If the transmitted slave address matches an address for one of the devices, the designated slave device pulls the SDA line to LOW (ACKNOWLEDGE). The data transfer is always terminated by a STOP condition generated by the master device.

(2)-1-1. Data validity

The data on the SDA line must be stable during the HIGH period of the clock. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW except for the START and the STOP condition.

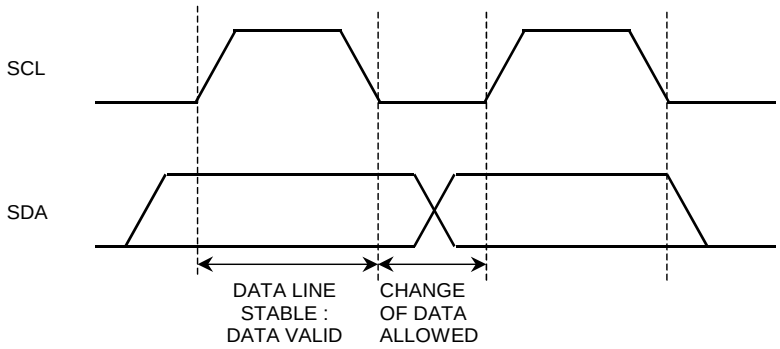


Figure 41. Data transfer

(2)-1-2. START and STOP condition

A HIGH to LOW transition on the SDA line while SCL is HIGH indicates a START condition. All sequences start from the START condition.
A LOW to HIGH transition on the SDA line while SCL is HIGH defines a STOP condition. All sequences end by the STOP condition.

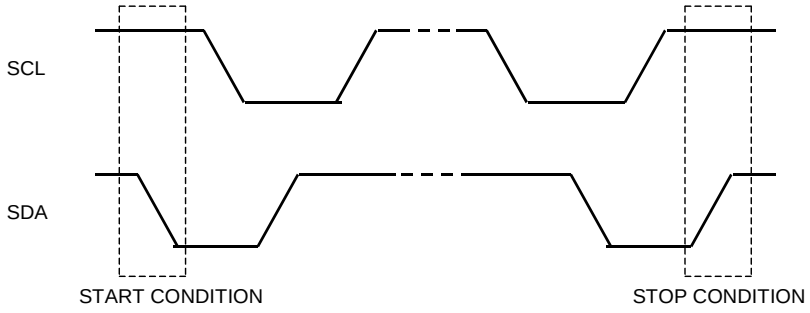


Figure 42. START and STOP conditions

(2)-1-3. ACKNOWLEDGE

ACKNOWLEDGE is a software convention used to indicate successful data transfers. The transmitting device will release the SDA line (HIGH) after transmitting eight bits. The receiver must pull down the SDA line during the acknowledge clock pulse so that that it remains stable "L" during "H" period of this clock pulse. The AK4683 will generates an acknowledge after each byte has been received.
In the read mode, the slave, the AK4683 will transmit eight bits of data, release the SDA line and monitor the line for an acknowledge. If an acknowledge is detected and no STOP condition is generated by the master, the slave will continue to transmit data. If an acknowledge is not detected, the slave will terminate further data transmissions and await the STOP condition.

The register of ADC/DAC part can not generate acknowledge for READ operations.

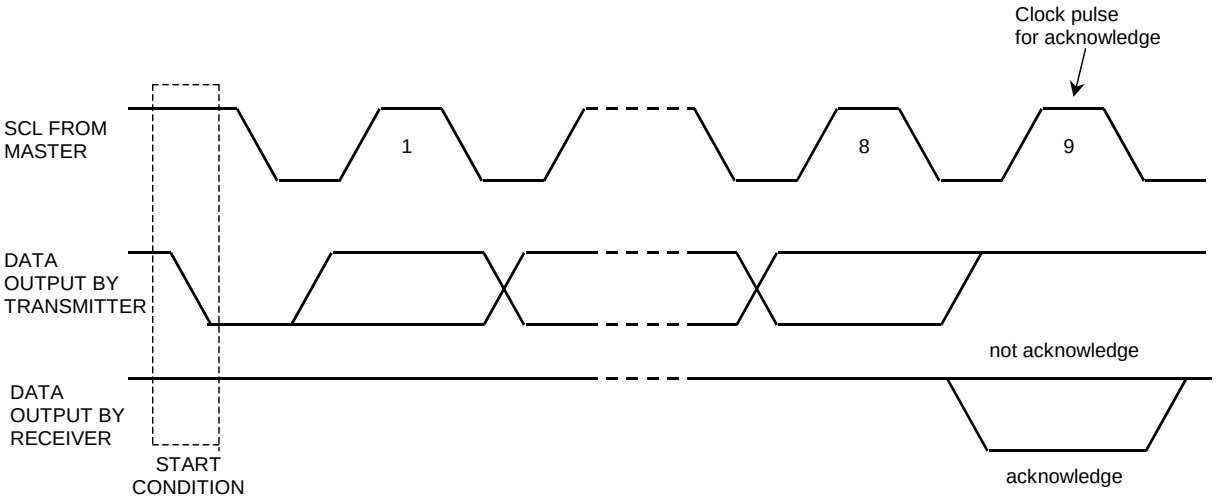


Figure 43. Acknowledge on the I^2C-bus

(2)-1-4. FIRST BYTE

The first byte, which includes seven bits of slave address and one bit of R/W bit, is sent after the START condition. If the transmitted slave address matches an address for one of the device, the receiver who has been addressed pulls down the SDA line.
The most significant five bits of the slave address are fixed as "00100". The next two bits are CAD1 and CAD0 (device address bits). These two bits identify the specific device on the bus. The eighth bit (LSB) of the first byte (R/W bit) defines whether a write or read condition is requested by the master. A "1" indicates that the read operation is to be executed. A "0" indicates that the write operation is to be executed.

0	0	1	0	0	CAD1	CAD0	R/W

(CAD1-CAD0 = fixed to "10" for ADC/DAC part, "00" for DIR/DIT part)

Figure 44. The First Byte

(2)-2. WRITE Operations

Set R/W bit = "0" for the WRITE operation of the AK4683.
After receipt the start condition and the first byte, the AK4683 generates an acknowledge, and awaits the second byte (register address). The second byte consists of the address for control registers of AK4683. The format is MSB first, and those most significant 3-bits are "Don't care".

*	*	*	A4	A3	A2	A1	A0

(*: Don't care)

Figure 45. The Second Byte

After receipt the second byte, the AK4683 generates an acknowledge, and awaits the third byte. Those data after the second byte contain control data. The format is MSB first, 8bits.

D7	D6	D5	D4	D3	D2	D1	D0

Figure 46. Byte structure after the second byte

The AK4683 is capable of more than one byte write operation by one sequence.
After receipt of the third byte, the AK4683 generates an acknowledge, and awaits the next data again. The master can transmit more than one words instead of terminating the write cycle after the first data word is transferred. After the receipt of each data, the internal 5bits address counter is incremented by one, and the next data is taken into next address automatically. If the address exceed 1FH prior to generating the stop condition, the address counter will "roll over" to 00H and the previous data will be overwritten.

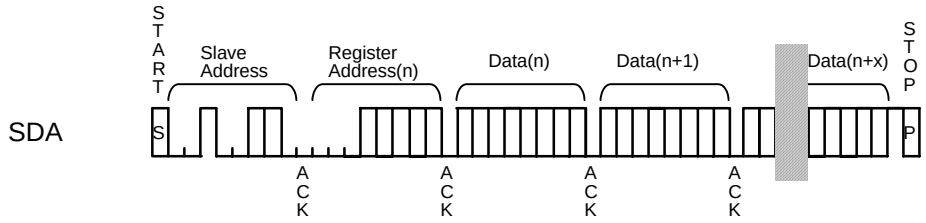


Figure 47. WRITE Operation

(2)-3. READ Operations

Set R/W bit = "1" for the READ operation of the AK4683.
After transmission of a data, the master can read next address's data by generating the acknowledge instead of terminating the write cycle after the receipt the first data word. After the receipt of each data, the internal 5bits address counter is incremented by one, and the next data is taken into next address automatically. If the address exceed 1FH prior to generating the stop condition, the address counter will "roll over" to 00H and the previous data will be overwritten.
The AK4683 supports two basic read operations: CURRENT ADDRESS READ and RANDOM READ.
ADC/DAC part register can not read.

(2)-3-1. CURRENT ADDRESS READ

The AK4683 contains an internal address counter that maintains the address of the last word accessed, incremented by one. Therefore, if the last access (either a read or write) was to address n, the next CURRENT READ operation would access data from the address n+1.
After receipt of the slave address with R/W bit set to "1", the AK4683 generates an acknowledge, transmits 1byte data which address is set by the internal address counter and increments the internal address counter by 1. If the master does not generate an acknowledge to the data but generate the stop condition, the AK4683 discontinues transmission

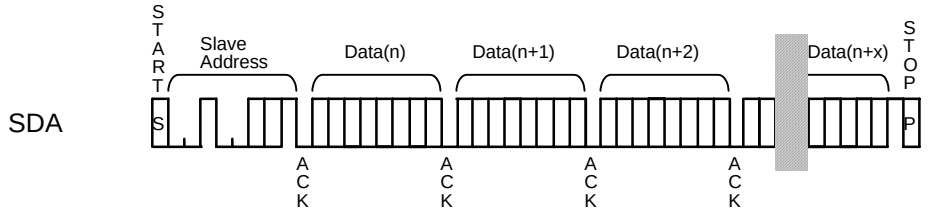


Figure 48. CURRENT ADDRESS READ

(2)-3-2. RANDOM READ

Random read operation allows the master to access any memory location at random. Prior to issuing the slave address with the R/W bit set to "1", the master must first perform a "dummy" write operation.
The master issues the start condition, slave address(R/W="0") and then the register address to read. After the register address's acknowledge, the master immediately reissues the start condition and the slave address with the R/W bit set to "1". Then the AK4683 generates an acknowledge, 1byte data and increments the internal address counter by 1. If the master does not generate an acknowledge to the data but generate the stop condition, the AK4683 discontinues transmission.

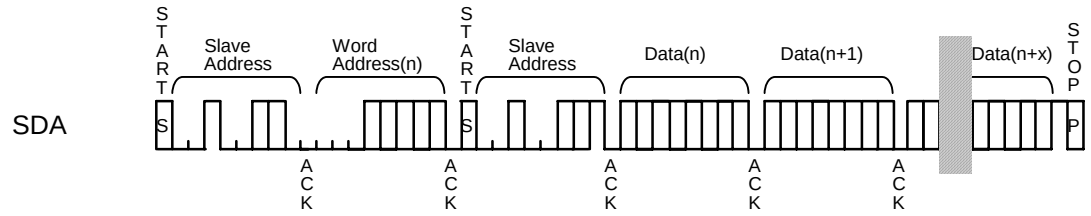


Figure 49. RANDOM READ

■ Register Map (ADC/DAC part)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	Powerdown 1	PWXTL	MUTEN	PWVR	PWHP	0	SMAD	SMDA	RSTN1
01H	Powerdown 2	PWPOB	PWPOA	PWDA	PWAD	0	0	PWDA2	PWDA1
02H	Clock Select 1	0	0	0	0	CLKB1	CLKB0	CLKA1	CLKA0
03H	Clock Select 2	CKSL2	CKSL1	CKSL0	CLKL1	CLKL0	MCKO1	MCKO0	CLKDT
04H	Clock Select 3	CKSAI2	CKSAI1	CKSAI0	0	OLRA1	OLRA0	BCAF	MSA
05H	Clock Select 4	0	XTL1	XTL0	CKSDT	CKSB2	CKSB1	CKSB0	MSB
06H	Sampling Speed	0	ACKSAI	ACKSAO	ACKSB	0	DFSAD	DFSDA1	DFSDA0
07H	Data Source Select 1	0	0	DITD1	DITD0	SDTOB1	SDTOB0	SDTOA1	SDTOA0
08H	Data Source Select 2	0	DAC22	DAC21	DAC20	0	DAC12	DAC11	DAC10
09H	Analog Input Control	0	0	0	0	0	AIN2	AIN1	AIN0
0AH	Audio Data Format	0	0	DIFB1	DIFB0	TDMA1	TDMA0	DIFA1	DIFA0
0BH	De-emphasis/ ATT speed	DEM11	DEM10	DEM21	DEM20	0	ATSAD	0	ATSDA
0CH	LIN Volume Control	ATTAD7	ATTAD6	ATTAD5	ATTAD4	ATTAD3	ATTAD2	ATTAD1	ATTAD0
0DH	RIN Volume Control	ATTAD7	ATTAD6	ATTAD5	ATTAD4	ATTAD3	ATTAD2	ATTAD1	ATTAD0
0EH	LOUT1 Volume Control	ATTDA7	ATTDA6	ATTDA5	ATTDA4	ATTDA3	ATTDA2	ATTDA1	ATTDA0
0FH	ROUT1 Volume Control	ATTDA7	ATTDA6	ATTDA5	ATTDA4	ATTDA3	ATTDA2	ATTDA1	ATTDA0
10H	LOUT2 Volume Control	ATTDA7	ATTDA6	ATTDA5	ATTDA4	ATTDA3	ATTDA2	ATTDA1	ATTDA0
11H	ROUT2 Volume Control	ATTDA7	ATTDA6	ATTDA5	ATTDA4	ATTDA3	ATTDA2	ATTDA1	ATTDA0
12H	HPL Volume Control	0	0	0	OPGA4	OPGA3	OPGA2	OPGA1	OPGA0
13H	OVF/DZF/V Control	0	0	ZCE	VIN	FUNC1	FUNC0	DZFM1	DZFM0

Note: For addresses from14H to 1FH, data must not be written.

When PDN pin goes to “L”, the registers are initialized to their default values.

When RSTN1 bit goes to “0”, the internal timing is reset and DZF pin goes to “H”, but registers are not initialized to their default values.

■ Register Definitions

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	Powerdown 1	PWXTL	MUTEN	PWVR	PWHP	0	SMAD	SMDA	RSTN1
Default		1	0	1	0	0	0	0	1

RSTN1: Internal timing reset
0: Reset. DZF pin go to “H”, but registers are not initialized.
1: Normal operation (default)

SMDA: DAC Soft Mute Enable
0: Normal operation (default)
1: All DAC outputs soft-muted

SMAD: ADC Soft Mute Enable
0: Normal operation (default)
1: ADC outputs soft-muted

PWHP: Power management for headphone amplifier
0: Power OFF (default)
1: Power ON

PWVR: Power management for reference voltage
0: Power OFF
1: Power ON (default)

MUTEN: Bias voltage control for headphone amp
0: bias = 0V (default).
1: Normal operation. Bias = 0.5xHVDD(typ).

PWXTL: Power management for X’tal oscillator
0: Power OFF
1: Power ON (default)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
01H	Powerdown 2	PWPOB	PWPOA	PWDA	PWAD	0	0	PWDA2	PWDA1
Default		1	1	1	1	0	0	1	1

PWDA1: Power-down control of DAC1 Analog
0: Power-down
1: Normal operation (default)

PWDA2: Power-down control of DAC2 Analog
0: Power-down
1: Normal operation (default)

PWAD: Power-down control of ADC
0: Power-down
1: Normal operation (default)

PWDA: Full-Power-down control of DAC1-2
0: Power-down
1: Normal operation (default)

PWPOA: Power-down control of PORTA
0: Power-down
1: Normal operation (default)

PWPOB: Power-down control of PORTB
0: Power-down
1: Normal operation (default)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
02H	Clock Select 1	0	0	0	0	CLKB1	CLKB0	CLKA1	CLKA0
Default		0	0	0	0	0	1	0	1

CLKA1-0: Clock source control for PORTA
00: DIR
01: X'tal(XTI) (default)
10: MCLK2
11: (Reserved)

CLKB1-0: Clock source control for PORTB
00: DIR
01: X'tal(XTI) (default)
10: MCLK2
11: (Reserved)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
03H	Clock Select 2	CKSL2	CKSL1	CKSL0	CLKL1	CLKL0	MCKO1	MCKO0	CLKDT
Default		0	1	0	0	1	0	1	0

CLKDT: Clock source control for DIT
Refer Table 56.

MCLKO1-0: Clock source control for MCLKO
Refer Table 4.

CLKL1-0: Clock source control for Clock Gen C
00: DIR
01: X'tal(XTI) (default)
10: MCLK2
11: (Reserved)

CLSL2-0: Clock control for Clock Gen C
Refer Table 15

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
04H	Clock Select 3	CKSAI2	CKSAI1	CKSAI0	SELAO	OLRA1	OLRA0	BCAF	MSA
Default		0	1	0	0	0	0	0	0

MSA: Master/Slave control for input data of PORTA.
Refer Table 16.

BCAF: Bit clock control for PORTA
Refer Table 13.

OLRA1-0: Clock control for PORTA OLRCKA.
Refer Table 12.

SELAO: Clock control for DIR/DIT
0: Except for the case at "1". (default)
1: Selects when the frequency of ILRCKA and OLRCKA are different, DITD[1:0]= "00" or "01" and both SDTOA[1:0] and DITD[1:0] select same data source.

CKSAI2-0: Clock control for PORTA Input Data.
Refer Table 11.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
05H	Clock Select 4	0	XTL1	XTL0	CKSDT	CKSB2	CKSB1	CKSB0	MSB
Default		0	0	0	0	0	1	0	0

MSB: Master/Slave control for input data of PORTB.
Refer Table 17.

CKSB2-0: Clock control for PORTB.
Refer Table 14.

CKSDT: Clock control for DIT.
Refer Table 57.

XTL1-0: X'tal Frequency control
00: 11.2896MHz (default)
01: 12.288MHz
10: 24.576MHz
11: (channel status)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
06H	Sampling Speed	0	ACKSAI	ACKSAO	ACKSB	0	DFSAD	DFSDA1	DFSDA0
Default		0	0	0	0	0	0	0	0

DFSDA1-0: DAC sampling speed control
These settings are ignored in Auto Setting Mode. Refer Table 22.

DFSAD: ADC sampling speed control
This setting is ignored in Auto Setting Mode. Refer Table 21.

ACSKB: Auto Setting Mode of PORTB
0: Disable, Manual Setting Mode (default)
1: Enable, Auto Setting Mode
Master clock frequency is detected automatically at ACKSB bit "1". In this case, the setting of DFSAD, DFSDA1-0 bits of the block connecting this PORT is ignored. When this bit is "0", DFSAD, DFSDA1-0 bits set the sampling speed mode.

ACSKAO: Auto Setting Mode of PORTA Output
0: Disable, Manual Setting Mode (default)
1: Enable, Auto Setting Mode
Master clock frequency is detected automatically at ACKSAO bit "1". In this case, the setting of DFSAD, DFSDA1-0 bits of the block connecting this PORT is ignored. When this bit is "0", DFSAD, DFSDA1-0 bits set the sampling speed mode.

ACSKAI: Auto Setting Mode of PORTA Input
0: Disable, Manual Setting Mode (default)
1: Enable, Auto Setting Mode
Master clock frequency is detected automatically at ACKSAI bit "1". In this case, the setting of DFSAD, DFSDA1-0 bits of the block connecting this PORT is ignored. When this bit is "0", DFSAD, DFSDA1-0 bits set the sampling speed mode.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
07H	Data Source Select 1	0	0	DITD1	DITD0	SDTOB1	SDTOB0	SDTOA1	SDTOA0
Default		0	0	1	1	0	1	0	1

SDTOA1-0: Data source control for PORTA
- 00: DIR
- 01: ADC (default)
- 10: SDTIB
- 11: off (“L” output)

SDTOB1-0: Data source control for PORTB
- 00: DIR
- 01: ADC (default)
- 10: off (“L” output)
- 11: SDTIA1

DITD1-0: Data source control for DIT
- 00: DIR
- 01: ADC
- 10: SDTIB
- 11: SDTIA1 (default)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
08H	Data Source Select 2	0	DAC22	DAC21	DAC20	0	DAC12	DAC11	DAC10
Default		0	1	0	0	0	0	1	1

DAC12-10: Data source control for DAC1
000: DIR
001: ADC
010: SDTIB
011: SDTIA1 (default)
100: SDTIA2
101: SDTIA3

DAC22-20: Data source control for DAC2
000: DIR
001: ADC
010: SDTIB
011: SDTIA1
100: SDTIA2 (default)
101: SDTIA3

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
09H	Analog Input Control	0	0	0	0	0	AIN2	AIN1	AIN0
Default		0	0	0	0	0	0	0	0

AIN2-0: ADC input selector control
000: LIN1/RIN1 (default)
001: LIN2/RIN2
010: LIN3/RIN3
011: LIN4/RIN4
100: LIN5/RIN5
101: LIN6/RIN6
110: None
111: None

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0AH	Audio Data Format	0	0	DIFB1	DIFB0	TDMA1	TDMA0	DIFA1	DIFA0
Default		0	0	1	0	0	0	1	0

DIFA1-0, TDMA1-0: Audio format control for PORTA
Refer Table 31, Table 32, Table 33.
DIFB1-0: Audio format control for PORTB
Refer Table 34.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0BH	De-emphasis/ ATT speed	DEM21	DEM20	DEM11	DEM10	0	ATSAD	0	ATSDA
Default		0	1	0	1	0	0	0	0

ATSDA: DAC digital Attenuator transition time control
ATSAD: ADC digital Attenuator transition time control
Refer Table 37, Table 38.

DEM11-10: DAC1 De-emphasis filter control
DEM21-20: DAC2 De-emphasis filter control
Refer Table 30. Default: “01”, OFF

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0CH	LIN Volume Control	ATTAD7	ATTAD6	ATTAD5	ATTAD4	ATTAD3	ATTAD2	ATTAD1	ATTAD0
0DH	RIN Volume Control	ATTAD7	ATTAD6	ATTAD5	ATTAD4	ATTAD3	ATTAD2	ATTAD1	ATTAD0
Default		0	0	1	1	0	0	0	0

ATTAD7-0: ADC Attenuation level control
Refer Table 35. Default: “30H”, 0bd

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0EH	LOUT1 Volume Control	ATTDA7	ATTDA6	ATTDA5	ATTDA4	ATTDA3	ATTDA2	ATTDA1	ATTDA0
0FH	ROUT1 Volume Control	ATTDA7	ATTDA6	ATTDA5	ATTDA4	ATTDA3	ATTDA2	ATTDA1	ATTDA0
10H	LOUT2 Volume Control	ATTDA7	ATTDA6	ATTDA5	ATTDA4	ATTDA3	ATTDA2	ATTDA1	ATTDA0
11H	ROUT2 Volume Control	ATTDA7	ATTDA6	ATTDA5	ATTDA4	ATTDA3	ATTDA2	ATTDA1	ATTDA0
Default		0	0	0	1	1	0	0	0

ATTDA7-0: DAC Attenuation level control
Refer Table 36. Default: “18H”, 0db

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
12H	HP Volume Control	0	0	0	OPGA4	OPGA3	OPGA2	OPGA1	OPGA0
Default		0	0	0	0	0	0	0	0

OPGA5-0: HP OPGA Attenuation level control
Refer Table 42. Default: “00H”, Mute

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
13H	OVF/DZF/V Control	0	0	ZCE	VIN	FUNC1	FUNC0	DZFM1	DZFM0
Default		0	0	1	0	0	0	0	0

DZFM1-0: DZF mode setting
Refer Table 7.

FUNC1-0: OVF/DZF/V mode control
00: off (“L” output. default)
01: ADC Overflow detection
10: DAC Zero data detection
11: V output

VIN: DIT V bit control
0: V bit = “0” (default)
1: V bit = “1”

ZCE: OPGA Zero-cross enable
0: Disable
1: Enable (default)

■ Register Map (DIR/DIT part)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	CLK & Power Down Control	CS12	1	CM1	CM0	OCKS1	OCKS0	PWN	RSTN2
01H	Format & De-em Control	0	1	1	0	DEAU	DEM1	DEM0	DFS
02H	Input/ Output Control 0	TXE	0	OPS1	OPS0	0	0	0	0
03H	Input/ Output Control 1	EFH1	EFH0	0	0	DIT	0	IPS1	IPS0
04H	INT MASK	MQIT0	MAUT0	MCIT0	MULK0	MDTS0	MPE0	MAUD0	MPAR0
05H	TEST	1	0	1	1	0	1	0	1
06H	Receiver status 0	QINT	AUTO	CINT	UNLCK	DTSCD	PEM	AUDION	PAR
07H	Receiver status 1	FS3	FS2	FS1	FS0	0	V	QCRC	CCRC
08H	RX Channel Status Byte 0	CR7	CR6	CR5	CR4	CR3	CR2	CR1	CR0
09H	RX Channel Status Byte 1	CR15	CR14	CR13	CR12	CR11	CR10	CR9	CR8
0AH	RX Channel Status Byte 2	CR23	CR22	CR21	CR20	CR19	CR18	CR17	CR16
0BH	RX Channel Status Byte 3	CR31	CR30	CR29	CR28	CR27	CR26	CR25	CR24
0CH	RX Channel Status Byte 4	CR39	CR38	CR37	CR36	CR35	CR34	CR33	CR32
0DH	TX Channel Status Byte 0	CT7	CT6	CT5	CT4	CT3	CT2	CT1	CT0
0EH	TX Channel Status Byte 1	CT15	CT14	CT13	CT12	CT11	CT10	CT9	CT8
0FH	TX Channel Status Byte 2	CT23	CT22	CT21	CT20	CT19	CT18	CT17	CT16
10H	TX Channel Status Byte 3	CT31	CT30	CT29	CT28	CT27	CT26	CT25	CT24
11H	TX Channel Status Byte 4	CT39	CT39	CT39	CT39	CT39	CT39	CT39	CT32
12H	Burst Preamble Pc Byte 0	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0
13H	Burst Preamble Pc Byte 1	PC15	PC14	PC13	PC12	PC11	PC10	PC9	PC8
14H	Burst Preamble Pd Byte 0	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
15H	Burst Preamble Pd Byte 1	PD15	PD14	PD13	PD12	PD11	PD10	PD9	PD8
16H	Q-subcode Address / Control	Q9	Q8	Q7	Q6	Q5	Q4	Q3	Q2
17H	Q-subcode Track	Q17	Q16	Q15	Q14	Q13	Q12	Q11	Q10
18H	Q-subcode Index	Q25	Q24	Q23	Q22	Q21	Q20	Q19	Q18
19H	Q-subcode Minute	Q33	Q32	Q31	Q30	Q29	Q28	Q27	Q26
1AH	Q-subcode Second	Q41	Q40	Q39	Q38	Q37	Q36	Q35	Q34
1BH	Q-subcode Frame	Q49	Q48	Q47	Q46	Q45	Q44	Q43	Q42
1CH	Q-subcode Zero	Q57	Q56	Q55	Q54	Q53	Q52	Q51	Q50
1DH	Q-subcode ABS Minute	Q65	Q64	Q63	Q62	Q61	Q60	Q59	Q58
1EH	Q-subcode ABS Second	Q73	Q72	Q71	Q70	Q69	Q68	Q67	Q66
1FH	Q-subcode ABS Frame	Q81	Q80	Q79	Q78	Q77	Q76	Q75	Q74

When PDN pin goes “L”, the registers are initialized to their default values.
When RSTN bit goes “0”, the internal timing is reset and the registers are initialized to their default values.
All data can be written to the register even if PWN bit is “0”.
The “0” register should be written “0”, the “1” register should be written “1” data.

■ Register Definitions

Reset & Initialize

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	CLK & Power Down Control	CS12	1	CM1	CM0	OCKS1	OCKS0	PWN	RSTN2
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	1	0	0	0	0	1	1

RSTN2: Timing Reset & Register Initialize
0: Reset & Initialize
1: Normal Operation (default)

PWN: Power Down
0: Power Down
1: Normal Operation (default)

OCKS1-0: Master Clock Frequency Select
Refer Table 3, Table 57.

CM1-0: Master Clock Operation Mode Select
Refer Table 1, Table 45, Table 55.

CS12: Channel Status Select
0: Channel 1 (default)
1: Channel 2
Selects which channel status is used to derive C-bit buffers, AUDION, PEM, FS3, FS2, FS1, FS0, Pc and Pd. The de-emphasis filter is controlled by channel 1 in the Parallel Mode.

Format & De-emphasis Control

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
01H	Format & De-em Control	0	1	1	0	DEAU	DEM1	DEM0	DFS
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	1	1	0	1	0	1	0

DFS: 96kHz De-emphasis Control
Refer Table 52.

DEM1-0: 32, 44.1, 48kHz De-emphasis Control
Refer Table 52.

DEAU: De-emphasis Auto Detect Enable
0: Disable
1: Enable (default)

Input/Output Control

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
02H	Input/ Output Control 0	TXE	0	OPS1	OPS0	0	0	0	0
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		1	0	0	0	0	0	0	0

OPS1-0: Output Through Data Select for TX pin
Refer Table 54.

TXE: TX Output Enable
0: Disable. TX0 pin outputs "L".
1: Enable (default)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
03H	Input/ Output Control 1	EFH1	EFH0	0	0	DIT	0	IPS1	IPS0
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	1	0	0	1	0	0	0

IPS1-0: Input Recovery Data Select
Refer Table 53.

DIT: Through data/Transmit data select for TX1 pin
0: Through data (RX data).
1: Transmit data (DAUX2 data. default.).
(U bit for DIT is fixed to "0")

EFH1-0: Interrupt 0 Pin Hold Count Select
00: 512 LRCK2
01: 1024 LRCK (default)
10: 2048 LRCK
11: 4096 LRCK

Mask Control for INT

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
04H	INT MASK	MQI0	MAT0	MCI0	MUL0	MDTS0	MPE0	MAN0	MPR0
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		1	1	1	0	1	1	1	0

MPR0: Mask Enable for PAR bit
MAN0: Mask Enable for AUDN bit
MPE0: Mask Enable for PEM bit
MDTS0: Mask Enable for DTSCD bit
MUL0: Mask Enable for UNLOCK bit
MCI0: Mask Enable for CINT bit
MAT0: Mask Enable for AUTO bit
MQI0: Mask Enable for QINT bit

0: Mask disable
1: Mask enable

Receiver Status 0

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
06H	Receiver status 0	QINT	AUTO	CINT	UNLCK	DTSCD	PEM	AUDION	PAR
R/W		RD	RD	RD	RD	RD	RD	RD	RD
Default		0	0	0	0	0	0	0	0

PAR: Parity Error or Biphase Error Status
- 0: No Error
- 1: Error
  It is "1" if Parity Error or Biphase Error is detected in the sub-frame.

AUDION: Audio Bit Output
- 0: Audio
- 1: Non Audio
  This bit is made by encoding channel status bits.

PEM: Pre-emphasis Detect.
- 0: OFF
- 1: ON
  This bit is made by encoding channel status bits.

DTSCD: DTS-CD Auto Detect
- 0: No detect
- 1: Detect

UNLCK: PLL Lock Status
- 0: Locked
- 1: Unlocked

CINT: Channel Status Buffer Interrupt
- 0: No change
- 1: Changed

AUTO: Non-PCM Auto Detect
- 0: No detect
- 1: Detect

QINT: Q-subcode Buffer Interrupt
- 0: No change
- 1: Changed

QINT, CINT and PAR bits are initialized when 06H is read.

Receiver Status 1

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
07H	Receiver status 1	FS3	FS2	FS1	FS0	0	V	QCRC	CCRC
R/W		RD	RD	RD	RD	RD	RD	RD	RD
Default		0	0	0	1	0	0	0	0

CCRC: Cyclic Redundancy Check for Channel Status
0:No Error
1:Error

QCRC: Cyclic Redundancy Check for Q-subcode
0:No Error
1:Error

V: Validity of channel status
0:Valid
1: Invalid

FS3-0: Sampling Frequency detection (refer Table 48.)

Receiver Channel Status

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
08H	RX Channel Status Byte 0	CR7	CR6	CR5	CR4	CR3	CR2	CR1	CR0
09H	RX Channel Status Byte 1	CR15	CR14	CR13	CR12	CR11	CR10	CR9	CR8
0AH	RX Channel Status Byte 2	CR23	CR22	CR21	CR20	CR19	CR18	CR17	CR16
0BH	RX Channel Status Byte 3	CR31	CR30	CR29	CR28	CR27	CR26	CR25	CR24
0CH	RX Channel Status Byte 4	CR39	CR38	CR37	CR36	CR35	CR34	CR33	CR32
R/W		RD							
Default		Not Initialized							

CR39-0: Receiver Channel Status Byte 4-0

Transmitter Channel Status

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0DH	TX Channel Status Byte 0	CT7	CT6	CT5	CT4	CT3	CT2	CT1	CT0
0EH	TX Channel Status Byte 1	CT15	CT14	CT13	CT12	CT11	CT10	CT9	CT8
0FH	TX Channel Status Byte 2	CT23	CT22	CT21	CT20	CT19	CT18	CT17	CT16
10H	TX Channel Status Byte 3	CT31	CT30	CT29	CT28	CT27	CT26	CT25	CT24
11H	TX Channel Status Byte 3	CT39	CT38	CT37	CT36	CT35	CT34	CT335	CT32
R/W		R/W							
Default		0							

CT39-0: Transmitter Channel Status Byte 4-0

Burst Preamble Pc/Pd in non-PCM encoded Audio Bitstreams

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
12H	Burst Preamble Pc Byte 0	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0
13H	Burst Preamble Pc Byte 1	PC15	PC14	PC13	PC12	PC11	PC10	PC9	PC8
14H	Burst Preamble Pd Byte 0	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
15H	Burst Preamble Pd Byte 1	PD15	PD14	PD13	PD12	PD11	PD10	PD9	PD8
R/W		RD							
Default		Not Initialized							

PC15-0: Burst Preamble Pc Byte 0 and 1
PD15-0: Burst Preamble Pd Byte 0 and 1

Q-subcode Buffer

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
16H	Q-subcode Address / Control	Q9	Q8	Q7	Q6	Q5	Q4	Q3	Q2
17H	Q-subcode Track	Q17	Q16	Q15	Q14	Q13	Q12	Q11	Q10
18H	Q-subcode Index	Q25	Q24	Q23	Q22	Q21	Q20	Q19	Q18
19H	Q-subcode Minute	Q33	Q32	Q31	Q30	Q29	Q28	Q27	Q26
1AH	Q-subcode Second	Q41	Q40	Q39	Q38	Q37	Q36	Q35	Q34
1BH	Q-subcode Frame	Q49	Q48	Q47	Q46	Q45	Q44	Q43	Q42
1CH	Q-subcode Zero	Q57	Q56	Q55	Q54	Q53	Q52	Q51	Q50
1DH	Q-subcode ABS Minute	Q65	Q64	Q63	Q62	Q61	Q60	Q59	Q58
1EH	Q-subcode ABS Second	Q73	Q72	Q71	Q70	Q69	Q68	Q67	Q66
1FH	Q-subcode ABS Frame	Q81	Q80	Q79	Q78	Q77	Q76	Q75	Q74
R/W		RD							
Default		Not Initialized							

SYSTEM DESIGN

Figure 50 shows the system connection diagram. The evaluation board is available which demonstrates application circuits, the optimum layout, power supply arrangements and measurement results.

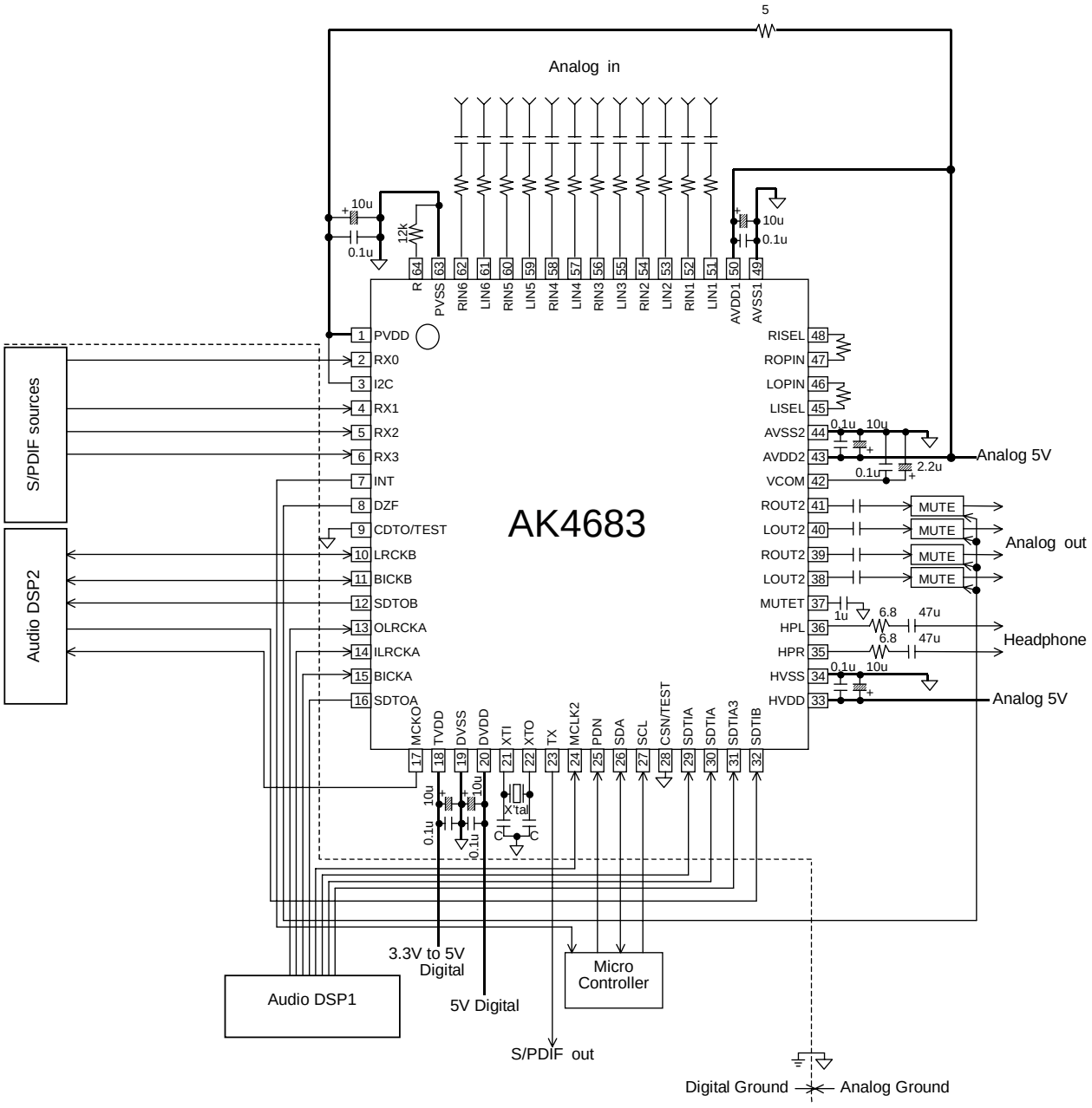


Figure 50. Typical Connection Diagram(I^2C serial control mode)

Notes:

- "C" depends on the crystal.
- AVSS, DVSS, PVSS and HVSS must be connected to the same analog ground plane.
- Digital signals, especially clocks, should be kept away from the R pin in order to avoid an effect to the clock jitter performance.
- In case of coaxial input, ground of RCA connector and terminator should be connected to PVSS of the AK4683 with low impedance on PC board.

1. Grounding and Power Supply Decoupling

The AK4683 requires careful attention to power supply and grounding arrangements. AVDD1, AVDD2, DVDD, PVDD and HVDD are usually supplied from analog supply in system. If AVDD1, AVDD2, DVDD, PVDD and HVDD are supplied separately, the power up sequence is not critical. **AVSS1, AVSS2, DVSS PVSS and HVSS of the AK4683 must be connected to analog ground plane.** System analog ground and digital ground should be connected together near to where the supplies are brought onto the printed circuit board. Decoupling capacitors should be as near to the AK4683 as possible, with the small value ceramic capacitor being the nearest.

2. Voltage Reference Inputs

The voltage of AVDD1, AVDD2 sets the analog input/output range. VCOM is a signal ground of this chip. An electrolytic capacitor 2.2μF parallel with a 0.1μF ceramic capacitor attached between VCOM pin and AVSS1 pin eliminates the effects of high frequency noise. No load current may be drawn from VCOM pin. All signals, especially clocks, should be kept away from the AVDD1, AVDD2 and VCOM pins in order to avoid unwanted coupling into the AK4683.

3. Analog Inputs

The AK4683 receives the analog input through the single-ended Pre-amp using external resistors. Adjust the input level/gain at Pre-amp to match the input range 1.22 x AVDD1 Vpp (typ. fs=48kHz, Ri =47kohm, Rf = 24kohm). Each input pins are biased internally. The ADC output data format is 2's complement. The internal digital HPF removes the DC offset.

The AK4683 samples the analog inputs at 64fs. The digital filter rejects noise above the stop band except for multiples of 64fs. The AK4683 includes an anti-aliasing filter (RC filter) to attenuate a noise around 64fs.

4. Analog Outputs

The analog outputs are also single-ended and centered around the VCOM voltage. The input signal range scales with the supply voltage and nominally 0.6 x AVDD2 Vpp. The DAC input data format is 2's complement. The output voltage is a positive full scale for 7FFFFFH(@24bit) and a negative full scale for 800000H(@24bit). The ideal output is VCOM voltage for 000000H(@24bit). The internal analog filters remove most of the noise generated by the delta-sigma modulator of DAC beyond the audio passband.

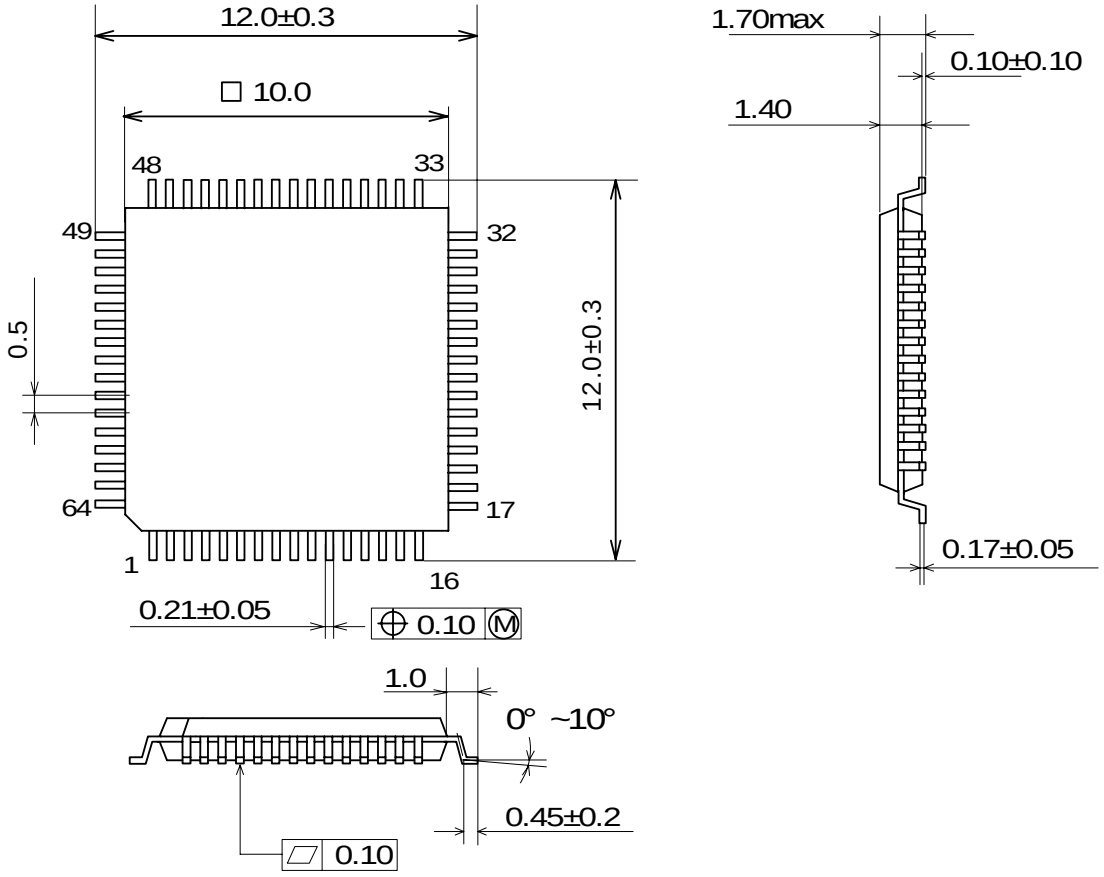
DC offsets on analog outputs are eliminated by AC coupling since DAC outputs have DC offsets of a few mV.

5. Attention to the PCB Wiring

LIN1-6 and RIN1-6 pins are the summing nodes of the Pre-Amp. Attention should be given to avoid coupling with other signals on those nodes. This can be accomplished by making the wire length of the input resistors as short as possible. The same theory also applies to the LOPIN/ROPIN pins and feedback resistors; keep the wire length to a minimum. Unused input pins among LIN1-6 and RIN1-6 pins should be left open.

PACKAGE

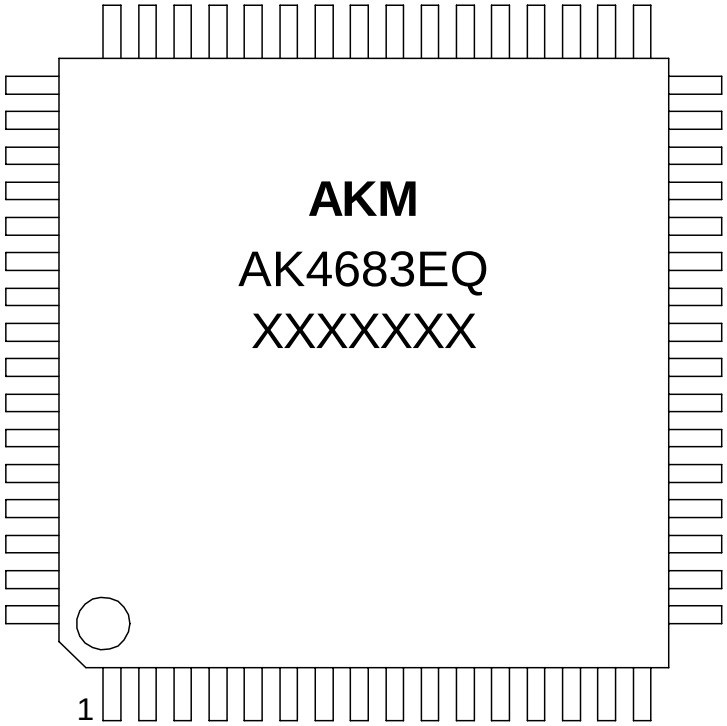
64pin LQFP(Unit:mm)



■ Package & Lead frame material

Package molding compound:	Epoxy
Lead frame material:	Cu
Lead frame surface treatment:	Solder (Pb free) plate

MARKING



1) Pin #1 indication
2) Asahi Kasei Logo
3) Marking Code: AK4683EQ
4) Date Code: XXXXXXX(7 digits)

REVISION HISTORY

Date (YY/MM/DD)	Revision	Reason	Page	Contents
05/09/30	00	First Edition		
05/11/15	01	Error Correction	30	Table 28, 29: “off” -> “SDTIB”
			38	“(Table 16)” -> “(Table 37, Table 38)”
			67	CLKDT: “Table 58” -> “Table 56” SELAO: “DIT[1:0]” -> “DITD[1:0]”
07/4/1	02	Comment Addition	23,25	Notes were added for the synchronous operation of PORTA and PORTB.

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