

# HD74LVCR2245A

## Octal Bidirectional Transceivers with 3-state Outputs

REJ03D0377-0400  
 (Previous ADE-205-235B (Z))  
 Rev.4.00  
 Aug. 20, 2004

### Description

The HD74LVCR2245A has eight buffers with three state outputs in a 20 pin package. When ( $T/\bar{R}$ ) is high, data flows from the A inputs to the B outputs, and when ( $T/\bar{R}$ ) is low, data flows from the B inputs to the A outputs. A and B bus are separated by making enable input ( $\overline{OE}$ ) high level.

All outputs, which are designed to sink up to 12mA, include equivalent 26  $\Omega$  resistors to reduce overshoot and undershoot.

Low voltage and high-speed operation is suitable at battery drive product (note type personal computer) and low power consumption extends the life of a battery for long time operation.

### Features

- $V_{CC} = 1.65$  to  $5.5$  V
- All inputs  $V_{IH} (\text{Max}) = 5.5$  V (@ $V_{CC} = 0$  to  $5.5$  V)
- All inputs / outputs  $V_{I/O} (\text{Max}) = 5.5$  V (@ $V_{CC} = 0$  V or output off state)
- Typical  $V_{OL}$  ground bounce  $< 0.8$  V (@ $V_{CC} = 3.3$  V,  $T_a = 25^\circ\text{C}$ )
- Typical  $V_{OH}$  undershoot  $> 2.0$  V (@ $V_{CC} = 3.3$  V,  $T_a = 25^\circ\text{C}$ )
- High output current  $\pm 12\text{mA}$  (@ $V_{CC} = 3.0$  to  $5.5$  V)
- All outputs have equivalent 26  $\Omega$  series resistors, so no external resistors are required
- Ordering Information

Part Name	Package Type	Package Code	Package Abbreviation	Taping Abbreviation (Quantity)
HD74LVCR2245AFPEL	SOP-20 pin (JEITA)	FP-20DAV	FP	EL (2,000 pcs/reel)
HD74LVCR2245ATELL	TSSOP-20 pin	TTP-20DAV	T	ELL (2,000 pcs/reel)

Note: Please consult the sales office for the above package availability.

### Function Table

#### Inputs

$\overline{OE}$	$T/\bar{R}$	Operation
L	L	B data to A bus
L	H	A data to B bus
H	X	Z

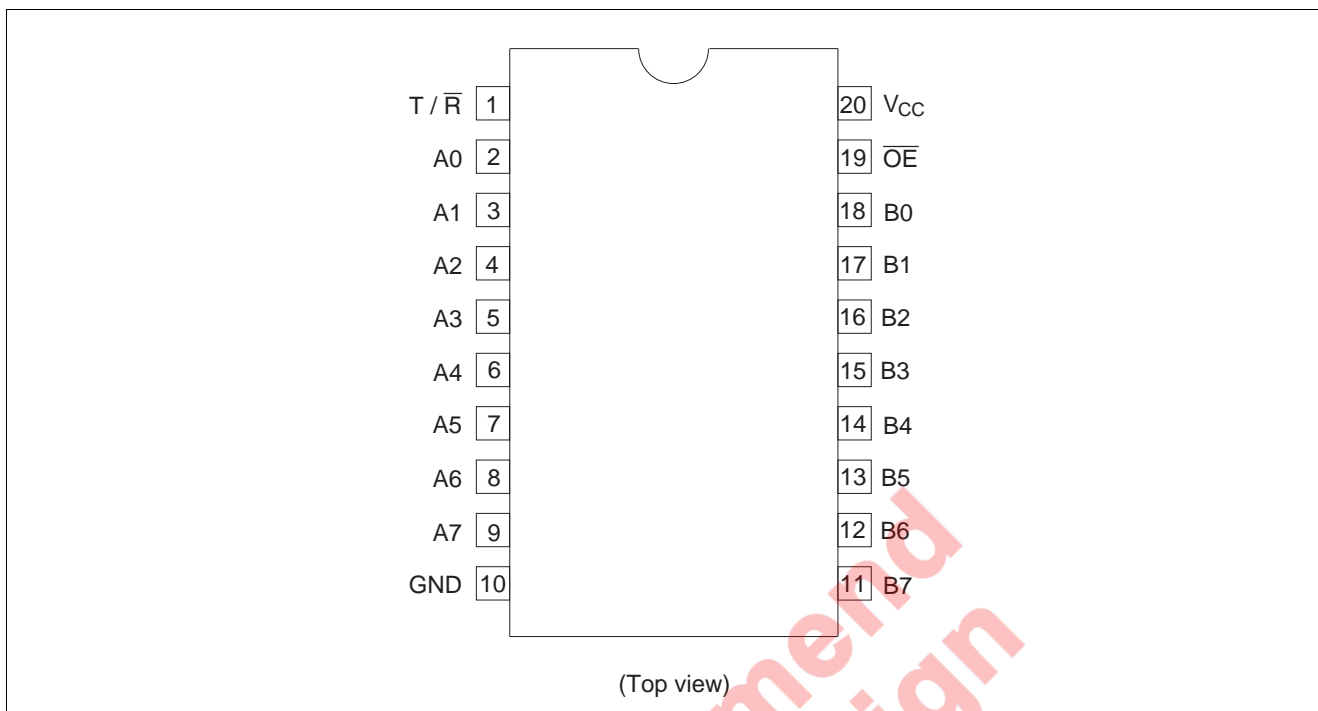
H: High level

L: Low level

X: Immaterial

Z: High impedance

**Pin Arrangement**



**Absolute Maximum Ratings**

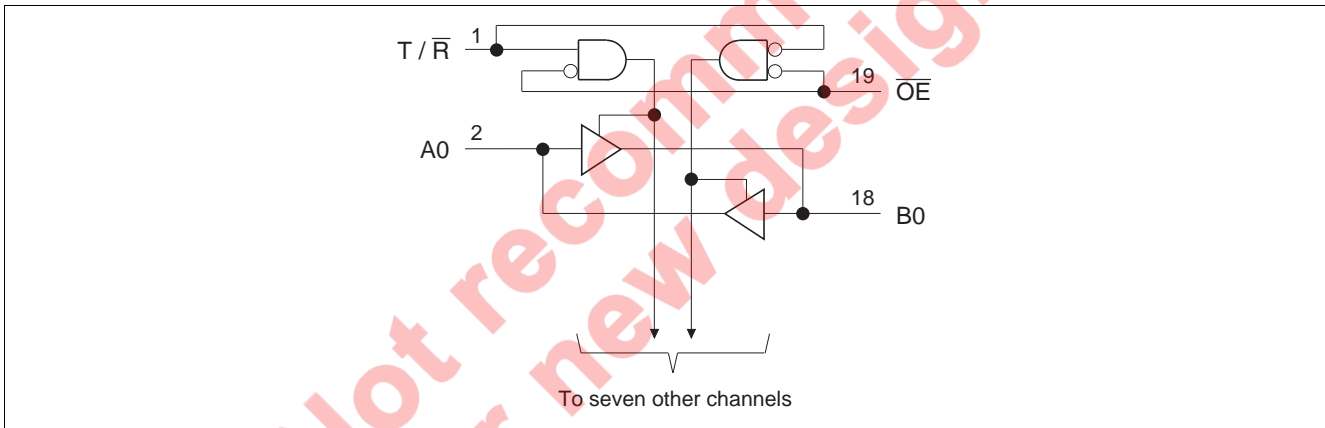
Item	Symbol	Ratings	Unit	Conditions
Supply voltage	$V_{CC}$	-0.5 to 7.0	V	
Input voltage	$V_I$	-0.5 to 7.0	V	
Output voltage	$V_O$	-0.5 to 7.0	V	Output "Z" or $V_{CC}$ : OFF
		-0.5 to $V_{CC}+0.5$		Output "H" or "L"
Input diode current	$I_{IK}$	-50	mA	$V_I < 0$
Output diode current	$I_{OK}$	-50	mA	$V_O < 0$
Output current	$I_O$	$\pm 50$	mA	
$V_{CC}$ , GND current	$I_{CC}$ or $I_{GND}$	$\pm 100$	mA	
Storage temperature	$T_{stg}$	-65 to 150	$^{\circ}C$	

Note: The absolute maximum ratings are values, which must not individually be exceeded, and furthermore no two of which may be realized at the same time.

**Recommended Operating Conditions**

Item	Symbol	Ratings	Unit	Conditions
Supply voltage	$V_{CC}$	1.65 to 5.5	V	At operation
		1.5 to 5.5		Data retention only
Input voltage	$V_I$	0 to 5.5	V	
Output voltage	$V_O$	0 to 5.5	V	Output "Z" or $V_{CC}$ : OFF
		0 to $V_{CC}$		Output "H" or "L"
Output current	$I_{OH}$	-2	mA	$V_{CC} = 1.65\text{ V}$
		-4		$V_{CC} = 2.3\text{ V}$
		-8		$V_{CC} = 2.7\text{ V}$
		-12		$V_{CC} = 3.0\text{ to }5.5\text{ V}$
	$I_{OL}$	2	mA	$V_{CC} = 1.65\text{ V}$
		4		$V_{CC} = 2.3\text{ V}$
		8		$V_{CC} = 2.7\text{ V}$
		12		$V_{CC} = 3.0\text{ to }5.5\text{ V}$
Input rise / fall time	$t_r, t_f$	0 to 6	ns / V	
Operating temperature	$T_a$	-40 to +85	°C	

**Logic Diagram**



Electrical Characteristics

(Ta = -40 to 85°C)

Item	Symbol	V <sub>CC</sub> (V)	Min	Typ	Max	Unit	Test Conditions
Input voltage	V <sub>IH</sub>	1.65 to 1.95	V <sub>CC</sub> ×0.65	—	—	V	
		2.3 to 2.7	1.7	—	—		
		2.7 to 3.6	2.0	—	—		
		4.5 to 5.5	V <sub>CC</sub> ×0.7	—	—		
	V <sub>IL</sub>	1.65 to 1.95	—	—	V <sub>CC</sub> ×0.35	V	
		2.3 to 2.7	—	—	0.7		
		2.7 to 3.6	—	—	0.8		
		4.5 to 5.5	—	—	V <sub>CC</sub> ×0.3		
Output voltage	V <sub>OH</sub>	1.65 to 5.5	V <sub>CC</sub> -0.2	—	—	V	I <sub>OH</sub> = -100 μA
		1.65	1.2	—	—		I <sub>OH</sub> = -2 mA
		2.3	1.7	—	—		I <sub>OH</sub> = -4 mA
		2.7	2.2	—	—		
		3.0	2.4	—	—		I <sub>OH</sub> = -6 mA
		2.7	2.0	—	—		I <sub>OH</sub> = -8 mA
		3.0	2.0	—	—		I <sub>OH</sub> = -12 mA
		4.5	3.6	—	—		
	V <sub>OL</sub>	1.65 to 5.5	—	—	0.2	V	I <sub>OL</sub> = 100 μA
		1.65	—	—	0.45		I <sub>OL</sub> = 2 mA
		2.3	—	—	0.7		I <sub>OL</sub> = 4 mA
		2.7	—	—	0.4		
		3.0	—	—	0.55		I <sub>OL</sub> = 6 mA
		2.7	—	—	0.6		I <sub>OL</sub> = 8 mA
3.0	—	—	0.8	I <sub>OL</sub> = 12 mA			
4.5	—	—	0.8				
Input current	I <sub>IN</sub>	0 to 5.5	—	—	±5	μA	V <sub>IN</sub> = 0 to 5.5 V
Off state output current	I <sub>OZ</sub>	1.65 to 5.5	—	—	±5	μA	V <sub>OUT</sub> = 0 to 5.5 V
Output leak current	I <sub>OFF</sub>	0	—	—	±5	μA	V <sub>IN</sub> or V <sub>O</sub> = 5.5 V
Quiescent supply current	I <sub>CC</sub>	1.65 to 3.6	—	—	10	μA	V <sub>IN</sub> = 3.6 to 5.5 V <sup>*1</sup> , I <sub>O</sub> = 0
		1.65 to 5.5	—	—	10		V <sub>IN</sub> = V <sub>CC</sub> or GND
	ΔI <sub>CC</sub>	2.7 to 3.6	—	—	500	μA	V <sub>IN</sub> = one input at (V <sub>CC</sub> -0.6)V, other inputs at V <sub>CC</sub> or GND
Input capacitance	C <sub>IN</sub>	3.3	—	3.4	—	pF	V <sub>IN</sub> = V <sub>CC</sub> or GND
Input output capacitance	C <sub>I/O</sub>	3.3	—	9.5	—	pF	V <sub>OUT</sub> = V <sub>CC</sub> or GND

Note: 1. This applies in the disabled state only.

Switching Characteristics

(Ta = -40 to 85°C)

Item	Symbol	V <sub>CC</sub> (V)	Min	Typ	Max	Unit	FROM (Input)	TO (Output)
Propagation delay time	t <sub>PLH</sub>	1.8±0.15	—	—	15.0	ns	A or B	B or A
	t <sub>PHL</sub>	2.5±0.2	—	—	9.0			
		2.7	—	—	7.3			
		3.3±0.3	1.5	—	6.3			
		5.0±0.5	—	—	4.8			
Output enable time	t <sub>ZH</sub>	1.8±0.15	—	—	18.0	ns	OE	A or B
	t <sub>ZL</sub>	2.5±0.2	—	—	11.0			
		2.7	—	—	9.5			
		3.3±0.3	1.5	—	8.2			
		5.0±0.5	—	—	6.8			
Output disable time	t <sub>HZ</sub>	1.8±0.15	—	—	16.0	ns	OE	A or B
	t <sub>LZ</sub>	2.5±0.2	—	—	10.0			
		2.7	—	—	8.5			
		3.3±0.3	1.7	—	7.8			
		5.0±0.5	—	—	6.6			
Between output pin skew <sup>*1</sup>	t <sub>OSLH</sub>	1.8±0.15	—	—	2.0	ns		
	t <sub>OSHL</sub>	2.5±0.2	—	—	2.0			
		2.7	—	—	1.5			
		3.3±0.3	—	—	1.0			
		5.0±0.5	—	—	1.0			

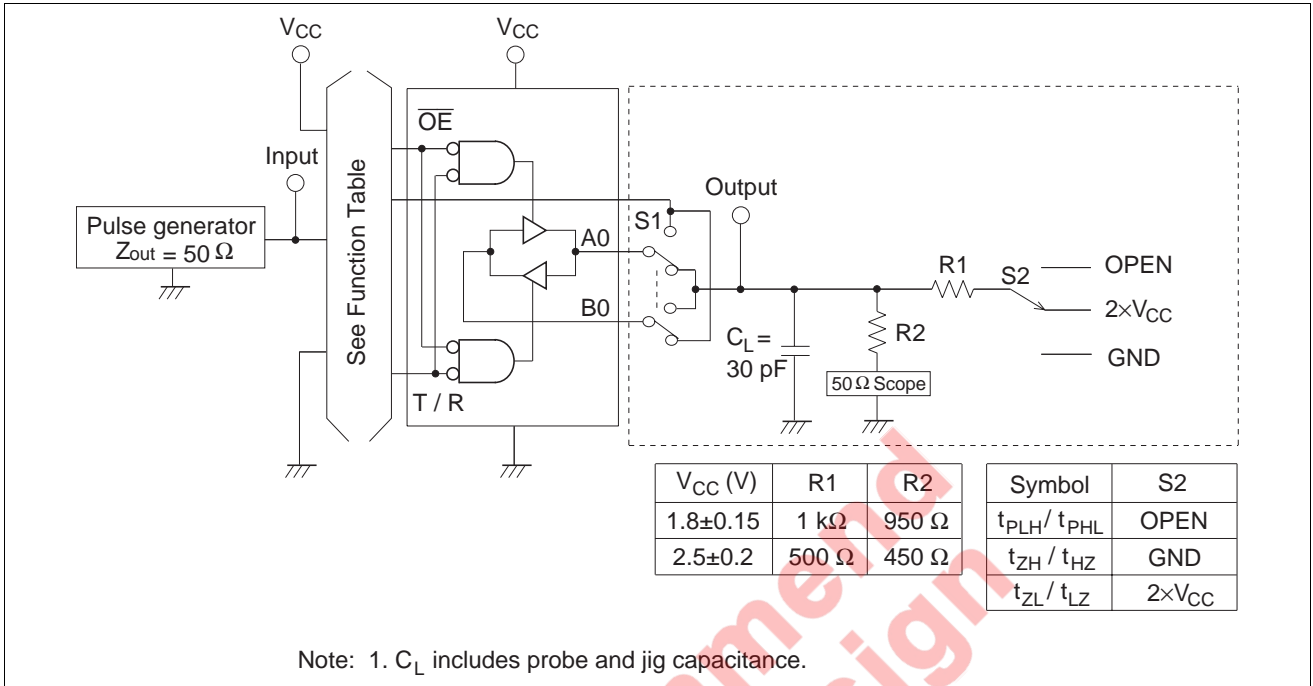
Note: 1. This parameter is characterized but not tested.

$$t_{OSLH} = |t_{PLHm} - t_{PLHn}|, t_{OSHL} = |t_{PHLm} - t_{PHLn}|$$

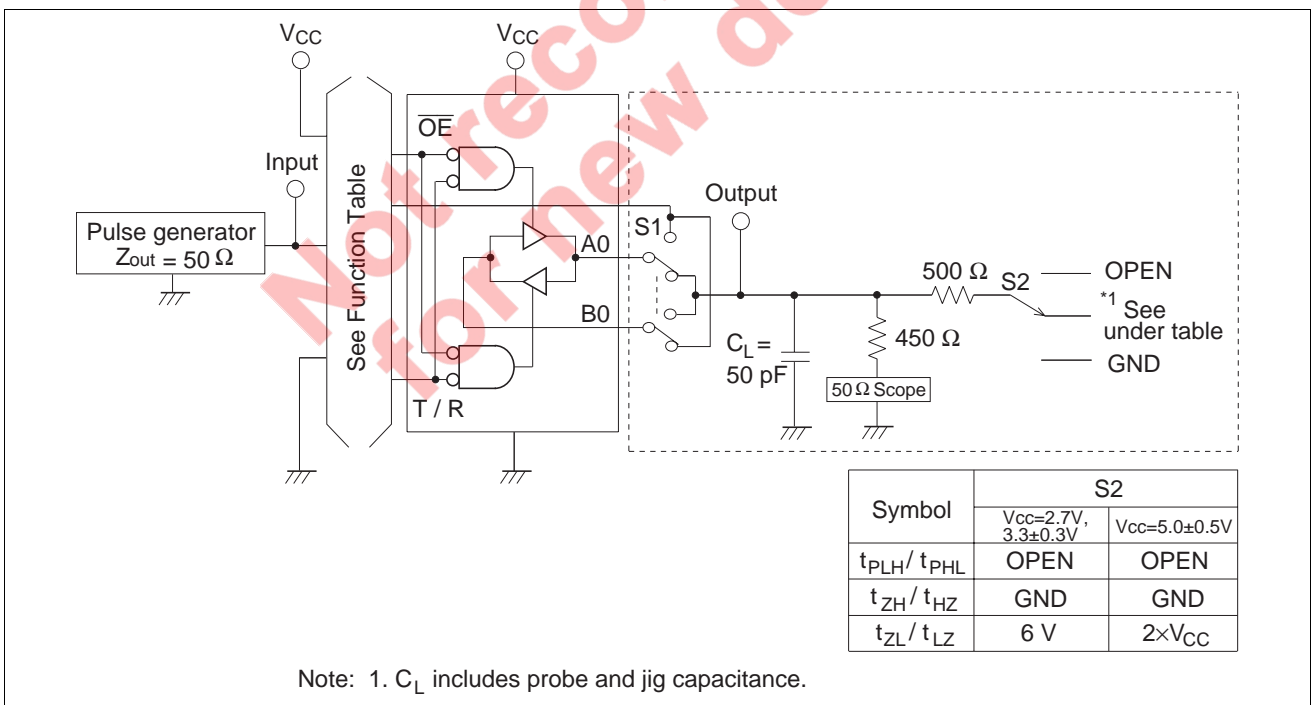
Not recommended for new design

Test Circuit

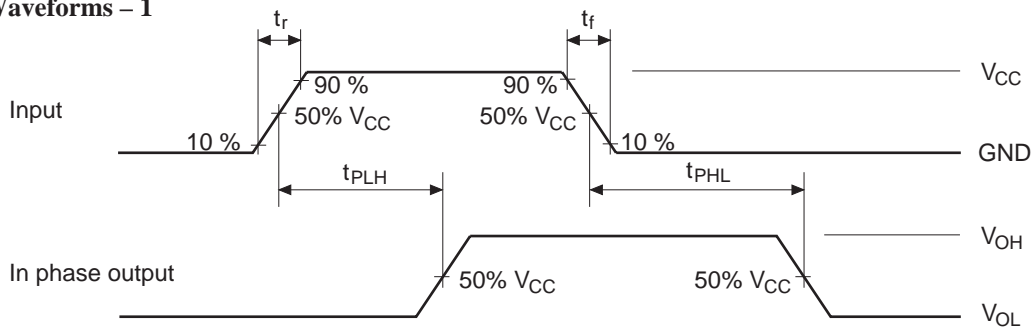
( $V_{CC} = 1.8 \pm 0.15 \text{ V}$ ,  $V_{CC} = 2.5 \pm 0.2 \text{ V}$ )



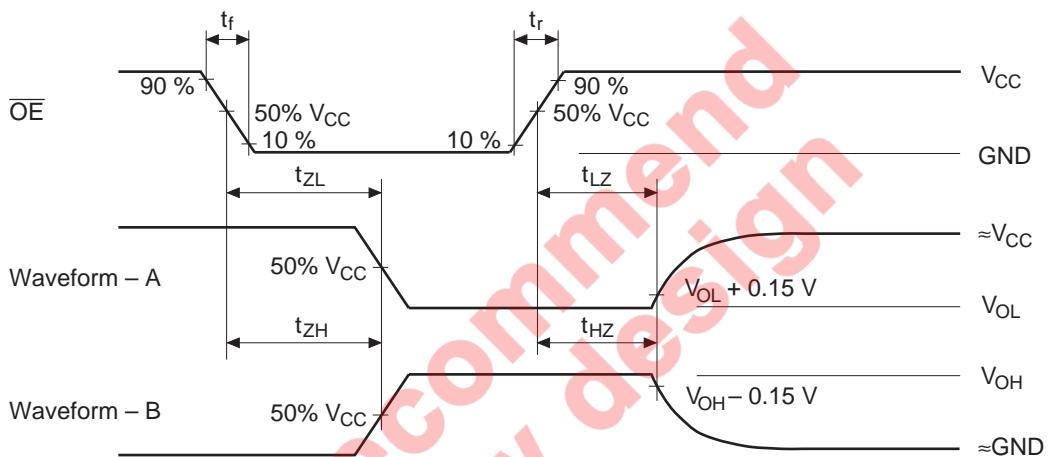
( $V_{CC} = 2.7 \text{ V}$ ,  $V_{CC} = 3.3 \pm 0.3 \text{ V}$ ,  $V_{CC} = 5.0 \pm 0.5 \text{ V}$ )



• Waveforms – 1

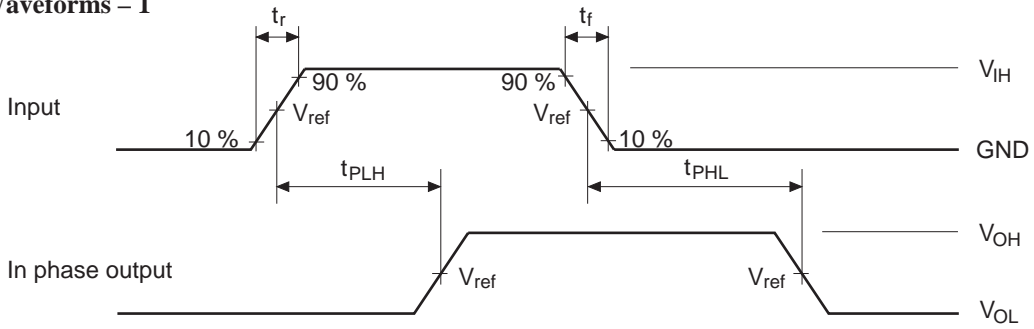


• Waveforms – 2

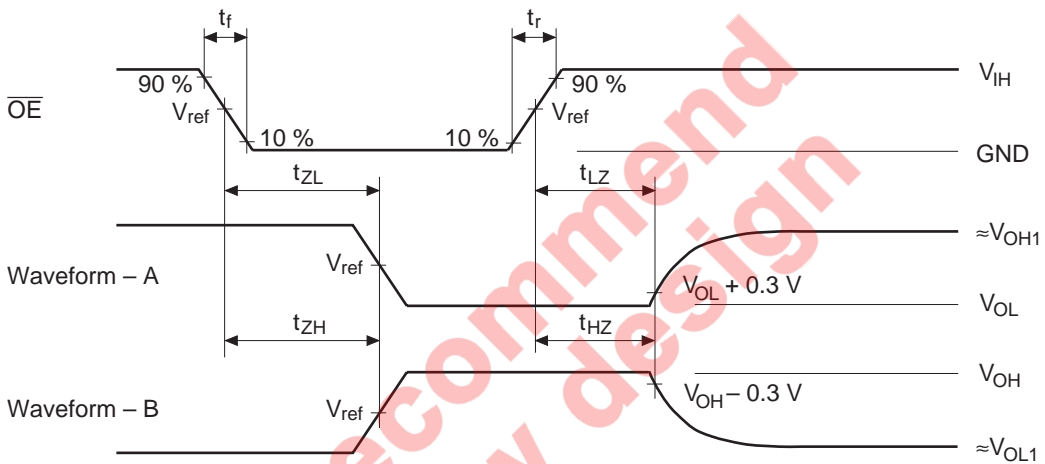


- Notes: 1. Input waveform : PRR = 10 MHz, duty cycle 50%,  $t_r = 2.0 \text{ ns}$ ,  $t_f = 2.0 \text{ ns}$   
 2. Waveform – A shows input conditions such that the output is "L" level when enabled by the output control.  
 3. Waveform – B shows input conditions such that the output is "H" level when enabled by the output control.

• Waveforms – 1



• Waveforms – 2

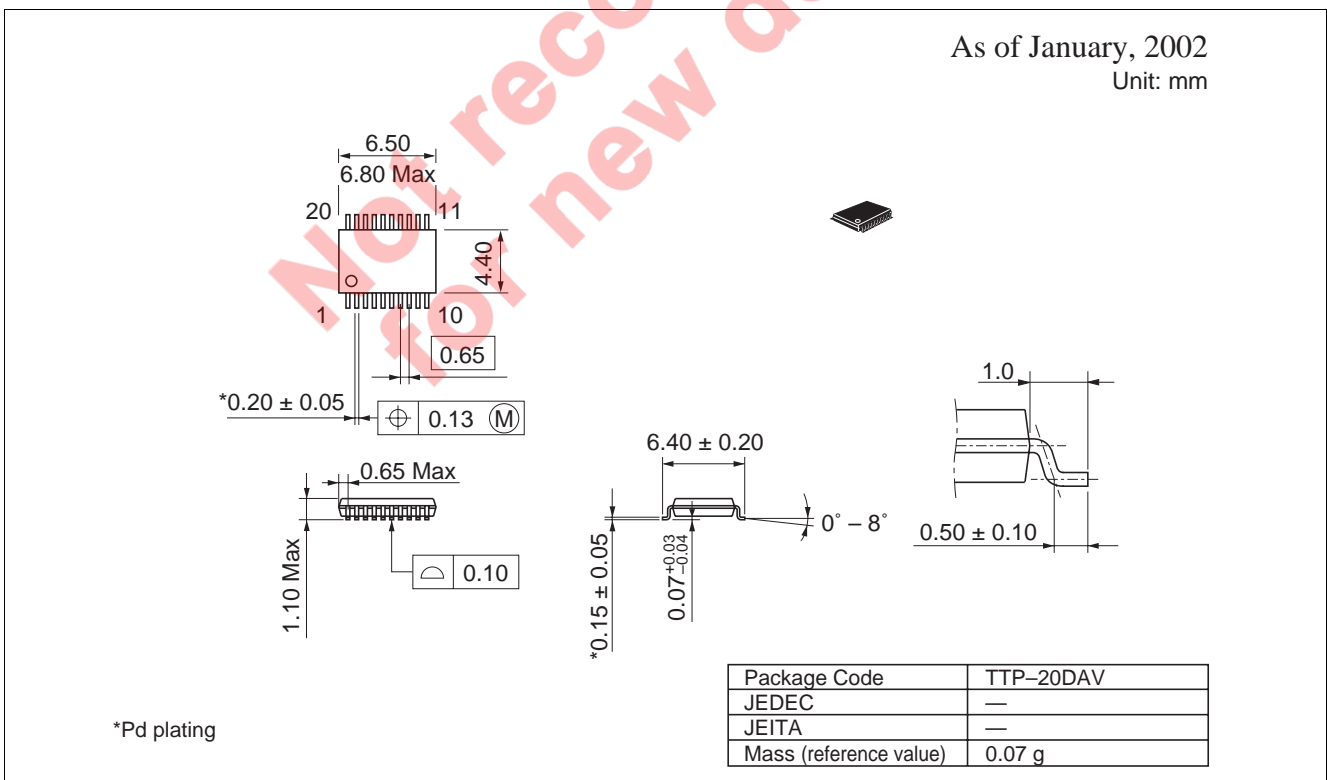
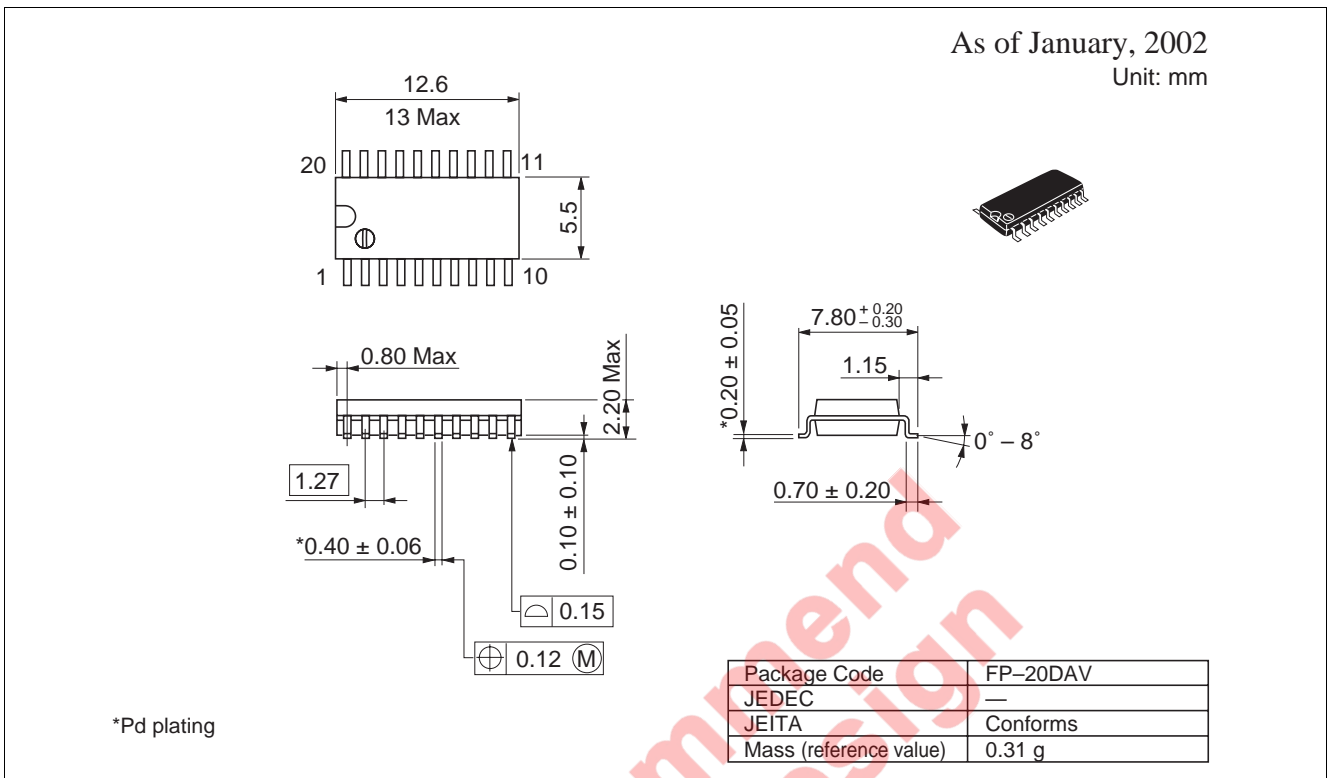


TEST	$V_{CC}=2.7\text{ V}$ $3.3 \pm 0.3\text{ V}$	$V_{CC}=5.0 \pm 0.5\text{ V}$
$V_{IH}$	2.7 V	$V_{CC}$
$V_{ref}$	1.5 V	$50\%V_{CC}$
$V_{OH1}$	3 V	$V_{CC}$
$V_{OL1}$	GND	GND

- Notes: 1. Input waveform : PRR = 10 MHz, duty cycle 50%,  $t_r = 2.5\text{ ns}$ ,  $t_f = 2.5\text{ ns}$   
 2. Waveform – A shows input conditions such that the output is "L" level when enabled by the output control.  
 3. Waveform – B shows input conditions such that the output is "H" level when enabled by the output control.



Package Dimensions



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