

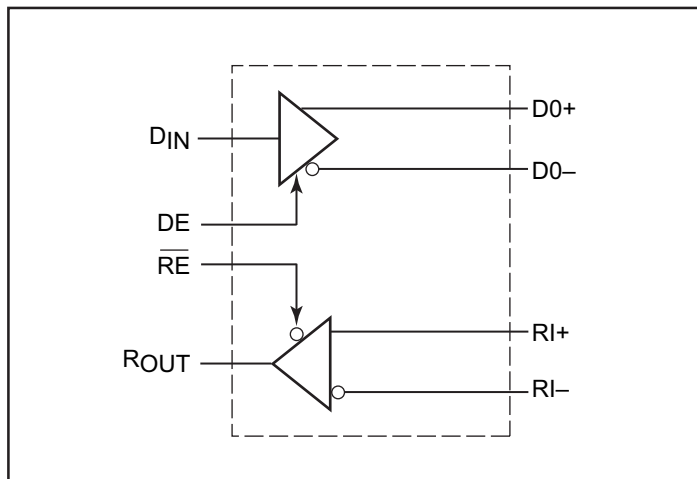
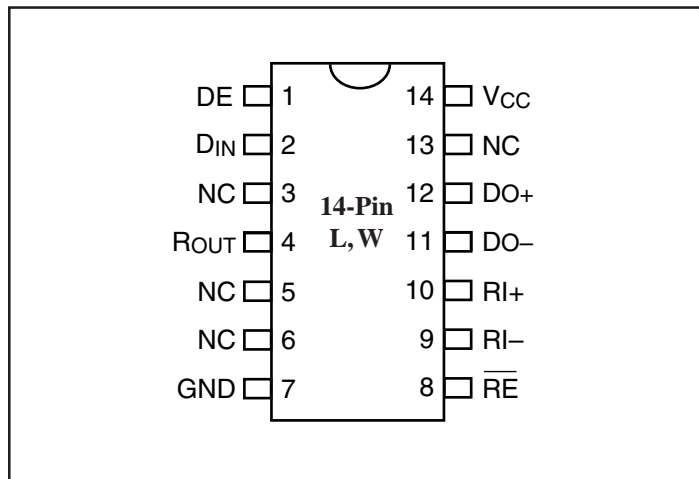
Single Bus LVDS Transceiver
Features

- Balanced Output Impedance
- Light Bus Loading: 5pF typical
- Glitch-free power up/down (Driver Disabled)
- High Signaling Rate Capability: >500 Mbps
- Driver:
 - $\pm 350\text{mV}$ Differential Swing into:
 - 100-ohm load (PI90LV019)
- Receiver:
 - Accepts $\pm 50\text{mV}$ (min.) Differential Swing with up to 2.0V ground potential difference
 - Propagation Delay of 3.3ns typ.
 - Low Voltage TTL (LVTTTL) Outputs
 - Open, Short, and Terminated Fail Safe
- Bus terminal ESD exceeds 9kV
- Industrial Temperature Operation (-40°C to $+85^{\circ}\text{C}$)
- Packaging: (Pb-free & Green available)
14-lead SOIC (W) and 14-lead TSSOP (L)

Description

The PI90LV019, differential line driver and receiver (transceiver), is compliant to IEEE1596.3 SCI and ANSI/TIA/EIA-644LVDS standards. The logic interface provides maximum flexibility resulting from four separate lines that are provided: D_{IN} , DE , RE , and R_{OUT} . These devices also feature flow through which allows easy PCB routing for short stubs between the bus pins and the connector.

The driver translates between TTL levels (single-ended) to Low Voltage Differential Signaling levels. This allows for high-speed operation, while consuming minimal power with reduced EMI. In addition the differential signaling provides common mode noise rejection of $\pm 1\text{V}$.

Block Diagram

Pin Configuration


Absolute Maximum Ratings^(1,2)

Supply Voltage (V _{CC})	3.6V
Enable Input Voltage (DE, \overline{RE})	-0.3V to (V _{CC} +0.3V)
Driver Input Voltage (DIN)	-0.3V to (V _{CC} +0.3V)
Receiver Output Voltage (R _{OUT})	-0.3V to (V _{CC} +0.3V)
Bus Pin Voltage (DO/RI±)	-0.3V to +3.9V
Driver Short Circuit	Continuous
ESD (HBM 1.5kohms, 100pF)	>9kV
Maximum Package Power Dissipation at 20°C	
SOIC	1025mW
Derate SOIC Package	8.2mW/°C

Storage Temperature Range	-65°C to +150°C
Lead Temperature Range (Soldering, 4s)	+260°C

Recommended Operating Conditions

	Min.	Max.	Units
Supply Voltage (V _{CC})	3.0	3.6	V
Receiver Input Voltage	0.0	2.9	V
Operating Free-Air Temperature	-40	+85	°C

Note:

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Table 1. Functional Mode

Mode Selected	DE	\overline{RE}
Driver Mode	H	H
Receiver Mode	L	L
3-State Mode	L	H
Full Duplex Mode	H	L

Table 2. Transmitter Mode

Inputs		Outputs	
DE	DI	DO+	DO-
H	L	L	H
H	H	H	L
H	2 > & > 0.8	X	X
L	X	Z	Z

Table 3. Receiver Mode

Inputs		Outputs
\overline{RE}	(RI+) - (RI-)	
L	L (< -100mV)	L
L	H (> +100mV)	H
L	100mV > & > -100mV	X
H	X	Z

Table 4. Device Pin Description

Pin Name	Pin #	Inputs/Outputs	Description
DIN	2	I	TTL Driver Input
DO±RI±	6,7	I/O	LVDS Driver Outputs/ LVDS Receiver Inputs
R _{OUT}	3	O	TTL Receiver Output
\overline{RE}	5	I	Receiver Enable TTL Input (Active Low)
DE	1	I	Driver Enable TTL Input (Active High)
GND	4	NA	Ground
V _{CC}	8	NA	Power Supply

DC Electrical Characteristics^(2,3)
 $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$, unless otherwise noted. $V_{CC} = 3.3\text{V} \pm 0.3\text{V}^{(2,3)}$

Symbol	Parameter	Conditions	Pin	Min.	Typ.	Max.	Units	
Differential Driver Characteristics								
V_{OD}	Output Differential Voltage	$R_L = 100\text{-ohms, (LV)}$ Figure 1	DO+ DO-	250	350	450	mV	
ΔV_{OD}	V_{OD} Magnitude Change				6	60		
V_{OS}	Offset Voltage			1	1.25	1.7	V	
ΔV_{OS}	Offset Magnitude Change				5	60	mV	
I_{OZD}	High Impedance Leakage	$V_{OUT} = V_{CC}$ or GND, $DE = 0\text{V}$		-10	± 1	+10	μA	
I_{OXD}	Power-Off Leakage	$V_{OUT} = 3.6\text{V}$ or GND, $V_{CC} = 0\text{V}$		-10	± 1	+10		
I_{OSD}	Output Short Circuit Current	$V_{OUT} = 0\text{V}$, $DE = V_{CC}$	LV	-10	-6	-4	mA	
Differential Receiver Characteristics								
V_{OH}	Voltage Output High	$V_{ID} = +100\text{mV}$	R_{OUT}	2.9	3.3		V	
		Inputs Open			2.9	3.3		
V_{OL}	Voltage Output Low	$I_{OL} = 2.0\text{mA}$, $V_{ID} = -100\text{mV}$				0.1		0.4
I_{OS}	Output Short Circuit Current	$V_{OUT} = 0\text{V}$		-75	-34	-20	mA	
V_{TH}	Input Threshold High		RI+ RI-			+100	mV	
V_{TL}	Input Threshold Low				-100			
I_{IN}	Input Current	$V_{IN} = +2.4\text{V}$, or 0V $V_{CC} = 3.6\text{V}$ or 0V			-10	± 1		± 10
Device Characteristics								
V_{IH}	Minimum Input High Voltage		D_{IN} , DE, RE	2.0		V_{CC}	V	
V_{IL}	Minimum Input Low Voltage				GND	0.8		
I_{IH}	Input High Current	$V_{IN} = V_{CC}$ or 2.4V				± 1		+10
I_{IL}	Input Low Current	$V_{IN} = \text{GND}$ or 0.4V			± 1	+10	μA	
V_{CL}	Input Diode Clamp Voltage	$I_{CLAMP} = -18\text{mA}$		-1.5	-0.7		V	
I_{CC}	No Load Driver Enabled	$D_{IN} = V_{CC}$ or GND $DE = V_{CC} = \text{RE}$	LV		4.0	8.0	mA	
I_{CCL}	Loaded driver enabled	$R_L = 100\text{ ohms}$ (all channels) $D_{IN} = V_{CC}$ or GND (all inputs) $DE = V_{CC}$, $RE = \text{GND}$	LV		20	30		
I_{CCZ}	No Load driver disabled	$D_{IN} = V_{CC}$ or GND, $DE = \text{GND}$, $RE = V_{CC}$	LV		2.2	8.0		
$C_{Doutput}$	Capacitance	—	DO+, DO-		5		pF	
C_{Rinput}	Capacitance		RI+, RI-		5			

Notes:

- “Absolute Maximum Ratings” are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of “Electrical Characteristics” specifies conditions of device operation.
- All currents into device pins are positive, all currents out of device pins are negative. All voltages are referenced to ground except: V_{OD} , V_{ID} , V_{TH} , and V_{TL} , unless otherwise specified.
- All typicals are given for $V_{CC} = +3.3\text{V}$ and $T_A = +25^\circ\text{C}$ unless otherwise stated.

Notes continued on next page...

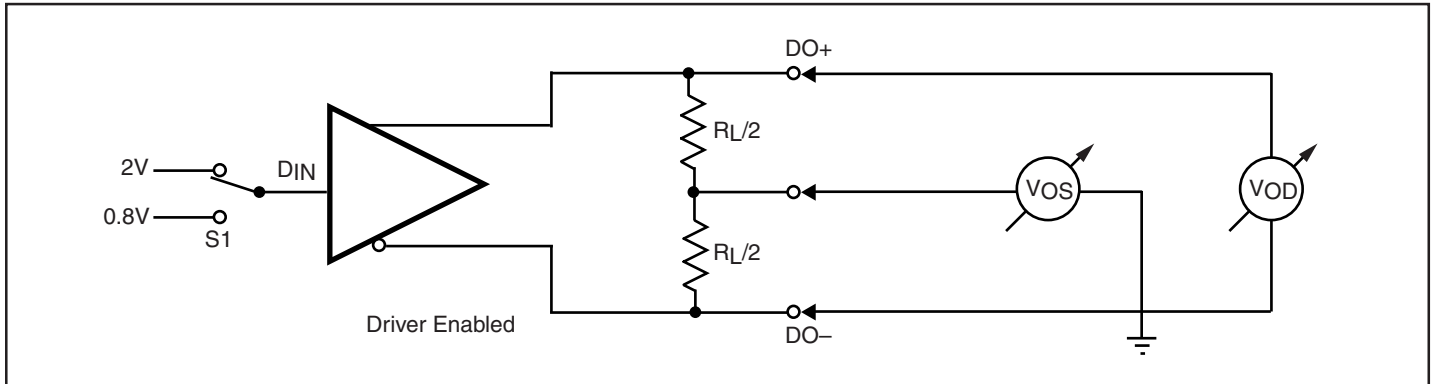
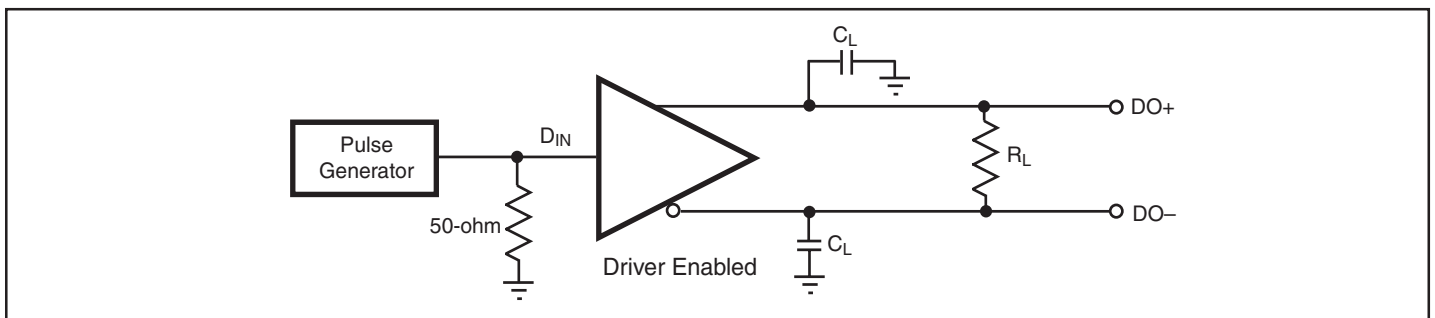
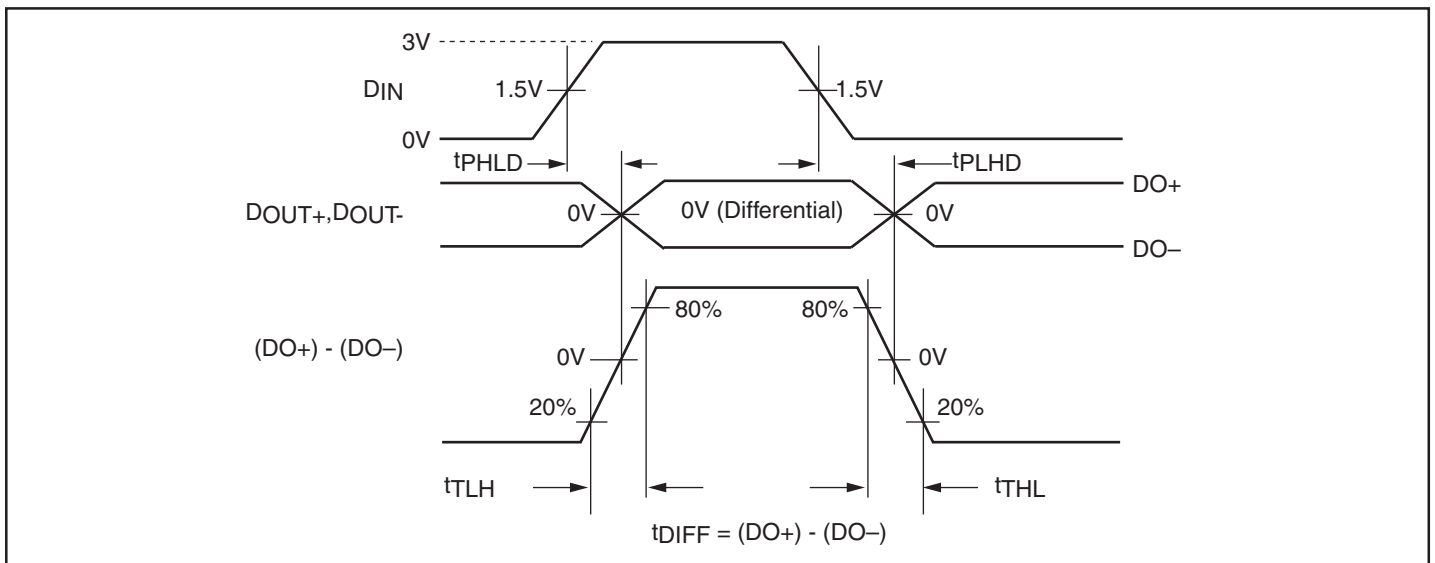
Notes (continued):

4. ESD Rating: HBM (15k-ohms, 100pF) > 2.0kV EAT (0-ohm, 200pF) > 300V.
5. C_L includes probe and fixture capacitance.
6. Generator waveforms for all tests unless otherwise specified: $f = 1\text{MHz}$, $Z_0 = 50\text{-ohms}$, $t_r, t_f \leq 6.0\text{ns}$ (0% - 100%) on control pins and $\leq 1.0\text{ns}$ for RI inputs.
7. For receiver disable delays, the switch is set to V_{CC} for t_{pZL} , and t_{PLZ} and to GND for t_{pZH} and t_{PHZ} .

AC Electrical Characteristics

$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$, $V_{CC} = 3.3\text{V} \pm 0.3\text{V}^{(6)}$

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
Driver Timing Requirements						
t_{PHLD}	Differential Propagation Delay High to Low	$R_L = 100\text{-ohms (LV)}$ $C_L = 10\text{pF}$ (Figures 2 & 3)	2.0	4.0	6.5	ns
t_{PLHD}	Differential Propagation Delay Low to High		1.0	5.6	7.0	
t_{SKD}	Differential Skew $ t_{PHLD} - t_{PLHD} $			0.4	1.0	
t_{TLH}	Transition Time Low to High		0.2	0.7	3.0	
t_{THL}	Transition Time High to Low		0.2	0.8	3.0	
t_{PHZ}	Disable Time High to Z	$R_L = 100\text{-ohms (LV)}$ $C_L = 10\text{pF}$ (Figures 2 & 3)	1.5	4.0	8.0	ns
t_{PLZ}	Disable Time Low to Z		2.5	5.3	9.0	
t_{pZH}	Enable Time Z to High		4.0	6.0	8.0	
t_{pZL}	Enable Time Z to Low		3.5	6.0	8.0	
Receiver Timing Requirements						
t_{PHLD}	Differential Propagation Delay High to Low	$C_L = 10\text{pF}$ $V_{ID} = 200\text{mV}$ Figures 6 & 7	1.3	2.1	3.0	ns
t_{PLHD}	Differential Propagation Delay Low to High		1.3	2.1	3.0	
t_{SKD}	Differential Skew $ t_{PHLD} - t_{PLHD} $			0.5	2.0	
t_r	Rise Time			0.8	1.4	
t_f	Fall Time			0.8	1.4	
t_{PHZ}	Disable Time High to Z	$R_L = 500\text{-ohms}$ $C_L = 10\text{pF}$ Figures 8 & 9	3.0	4.0	6.0	ns
t_{PLZ}	Disable Time Low to Z		3.0	4.5	6.0	
t_{pZH}	Enable Time Z to High		3.0	6.0	8.0	
t_{pZL}	Enable Time Z to Low		3.0	6.0	8.0	

Test Circuits and Timing Waveforms

Figure 1. Differential Driver DC Test Circuit

Figure 2. Differential Driver Propagation Delay and Transition Time Test Circuit

Figure 3. Driver Propagation Delay and Transition Time Waveforms

Test Circuits and Timing Waveforms (continued)

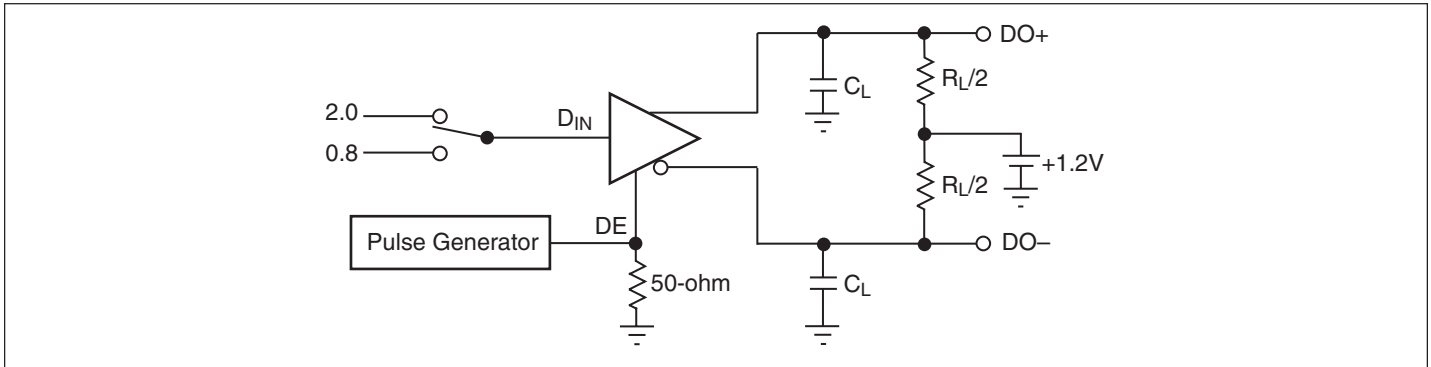


Figure 4. Driver Three-State Delay Test Circuit

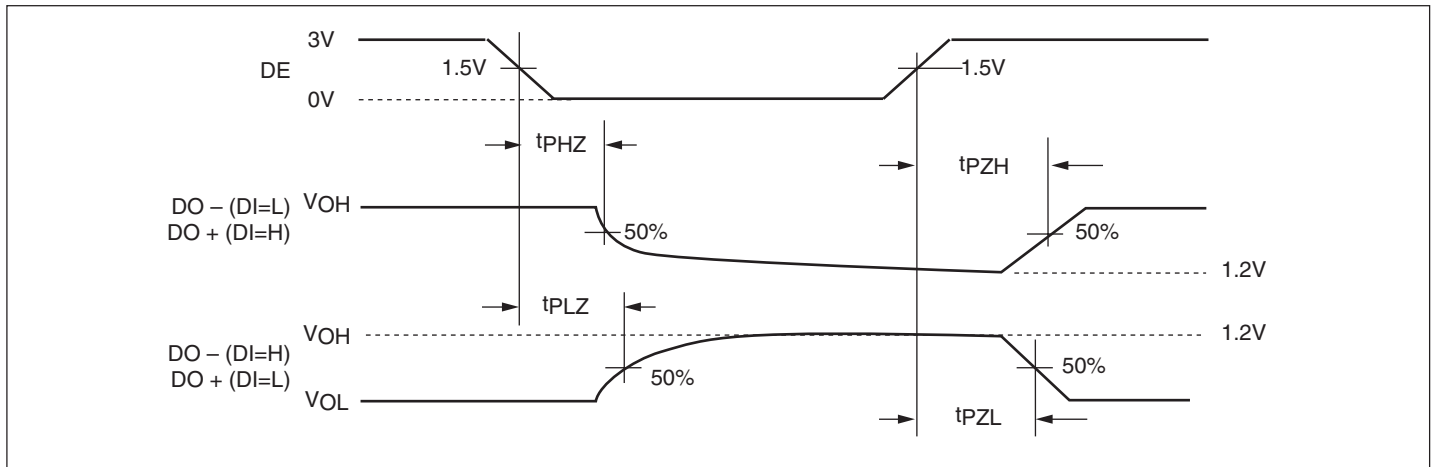


Figure 5. Driver Three-State Delay Waveforms

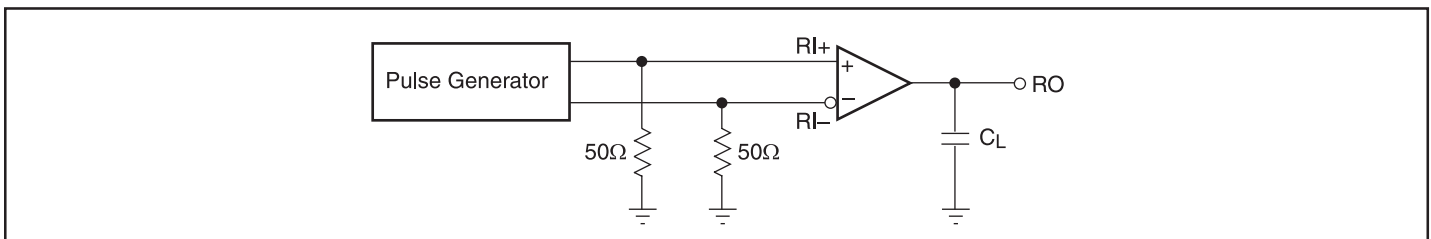


Figure 6. Receiver Propagation Delay and Transition Time Test Circuit

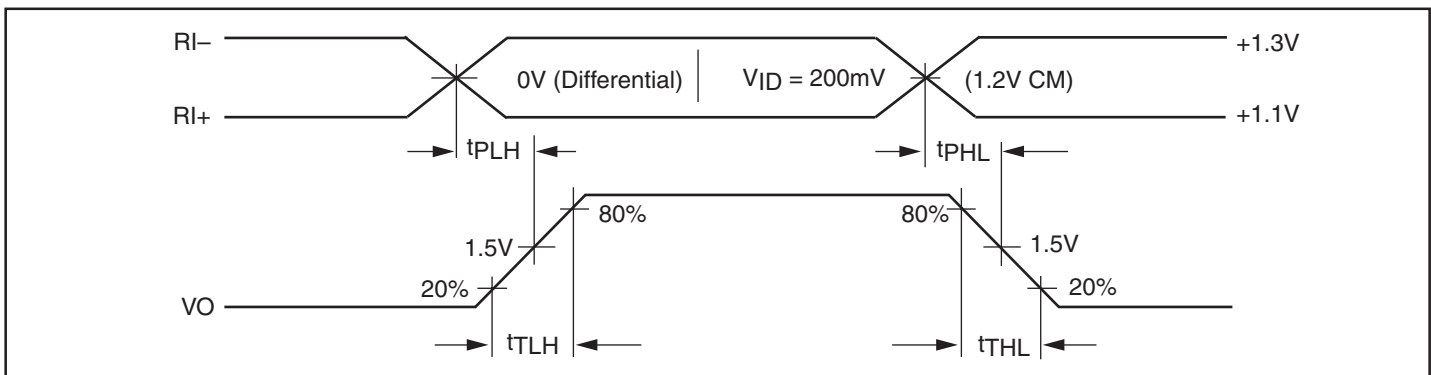


Figure 7. Receiver Propagation Delay and Transition Time Waveforms

Test Circuits and Timing Waveforms (continued)

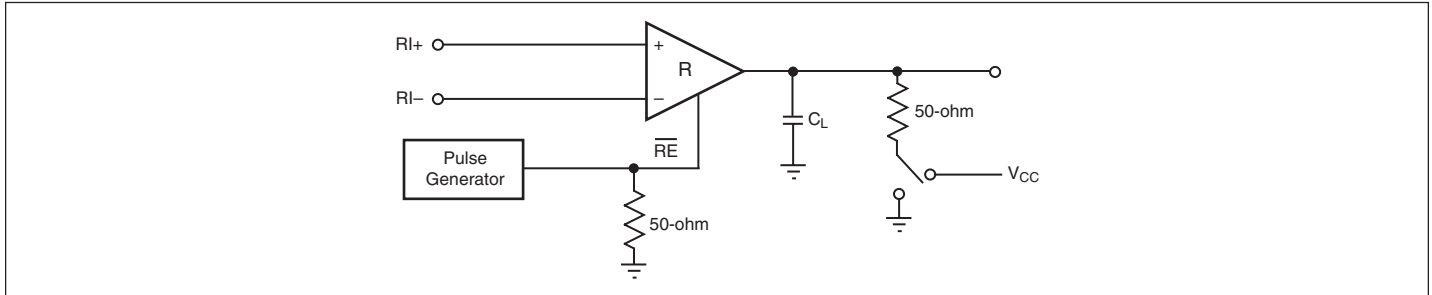


Figure 8. Receiver 3-State Delay Test Circuit

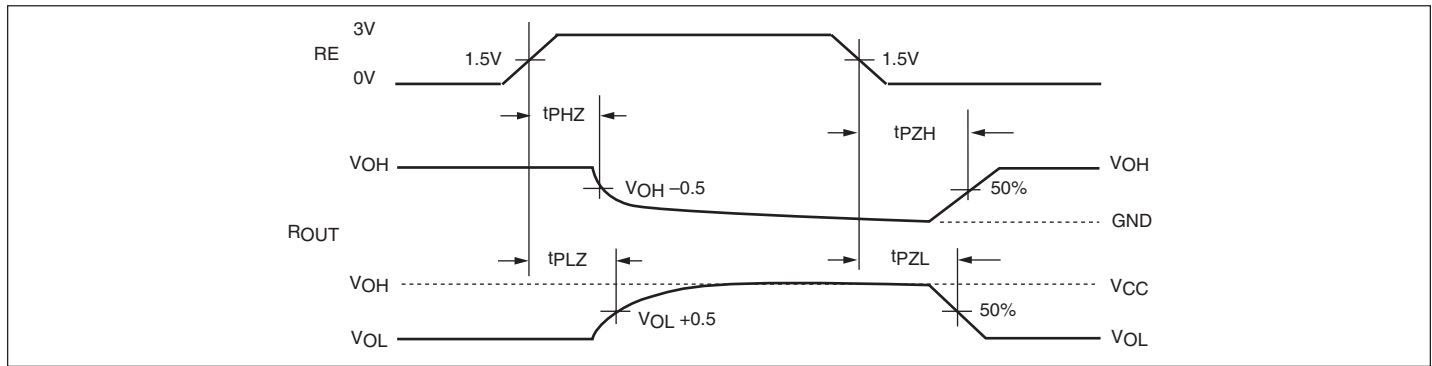


Figure 9. Receiver 3-State Delay Waveforms

Typical Bus Application Configurations

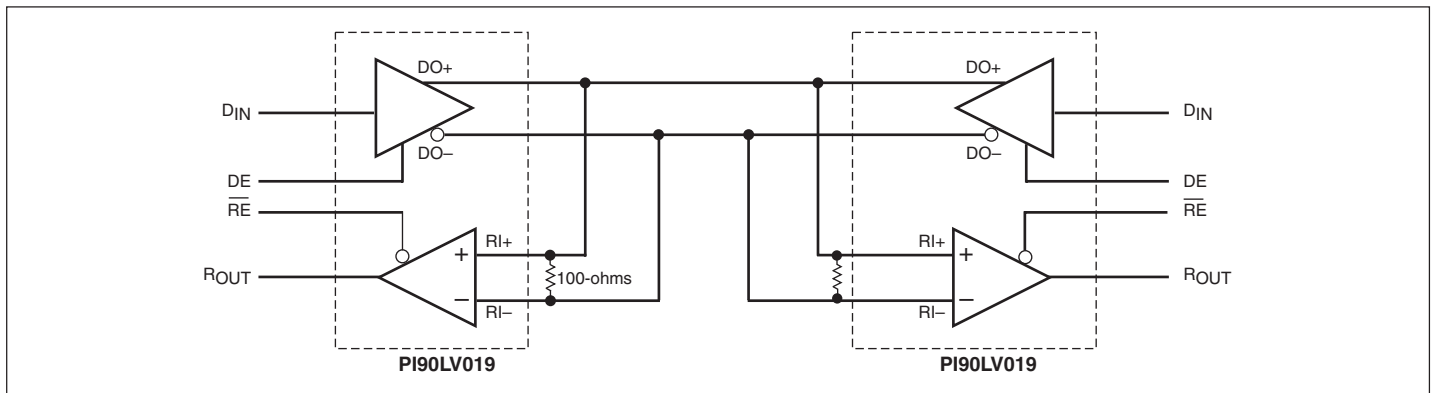


Figure 10. Bidirectional Half-Duplex Point-to-Point Applications

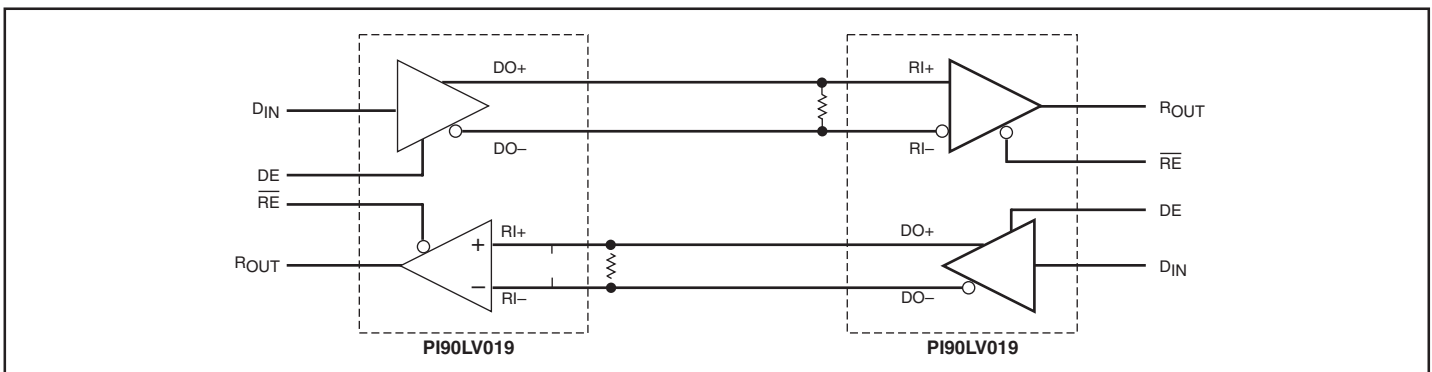
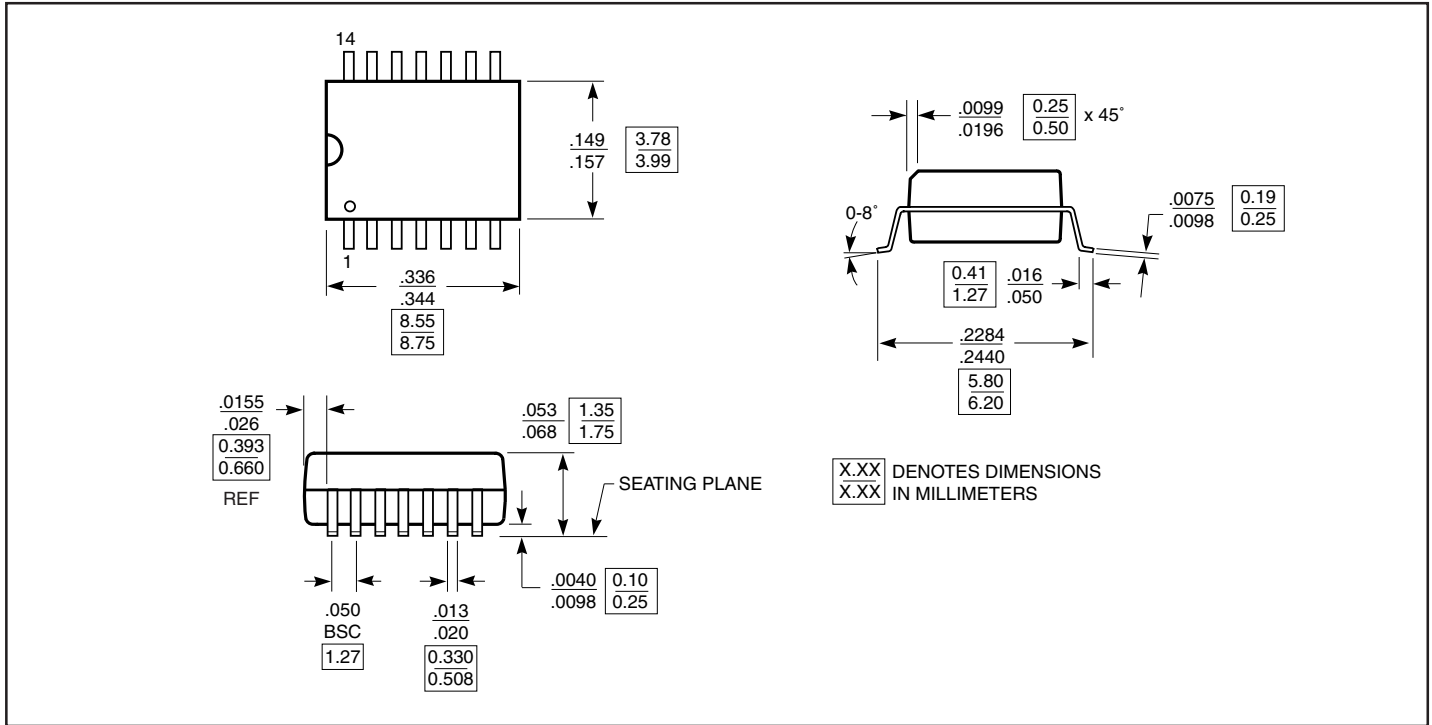
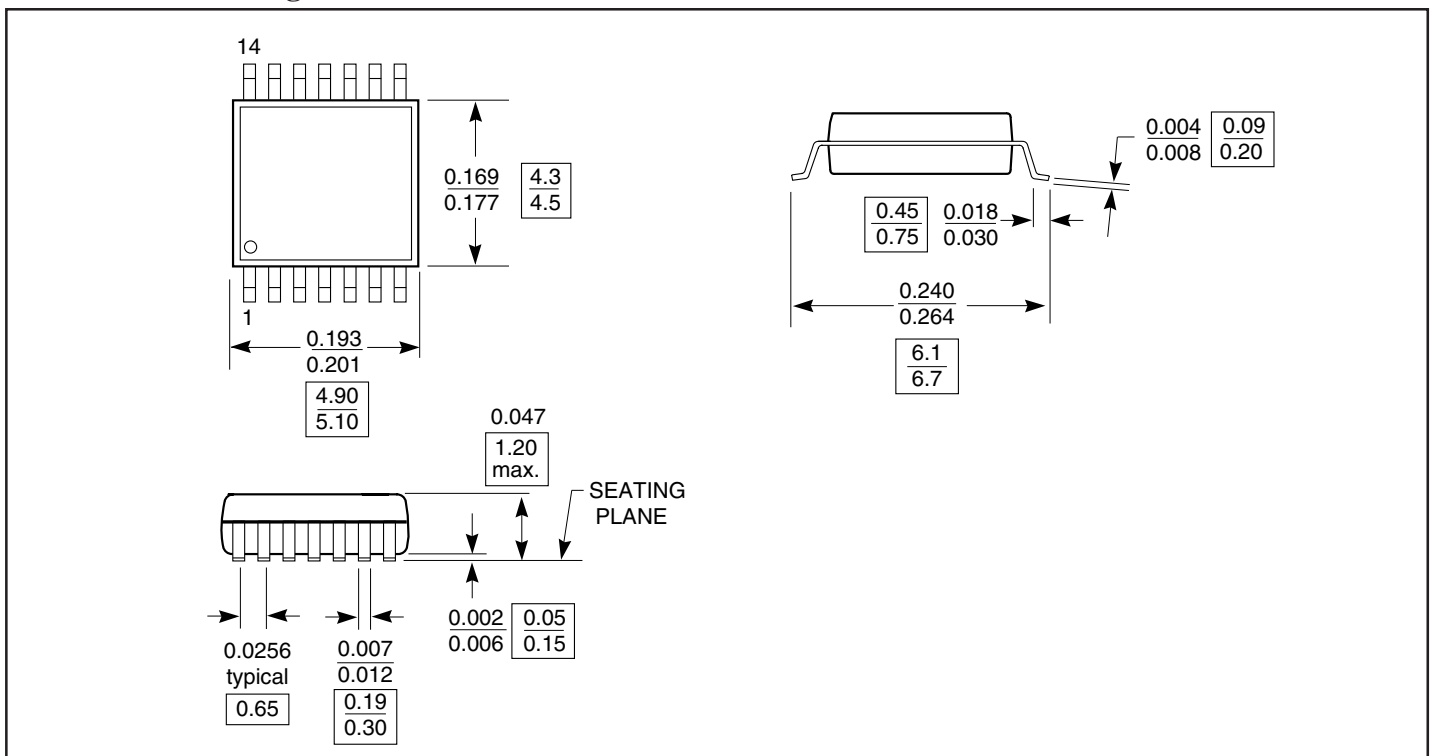


Figure 11. Full-Duplex Point-to-Point Application

14-Pin SOIC Package



14-Pin TSSOP Package



Ordering Information

Order Number	Pins - Package	Temperature
PI90LV019W	14 - SOIC	-40°C to 85°C
PI90LV019WE	14 - SOIC, Pb-free & Green	-40°C to 85°C
PI90LV019L	14 - TSSOP	-40°C to 85°C
PI90LV019LE	14 - TSSOP, Pb-free & Green	-40°C to 85°C