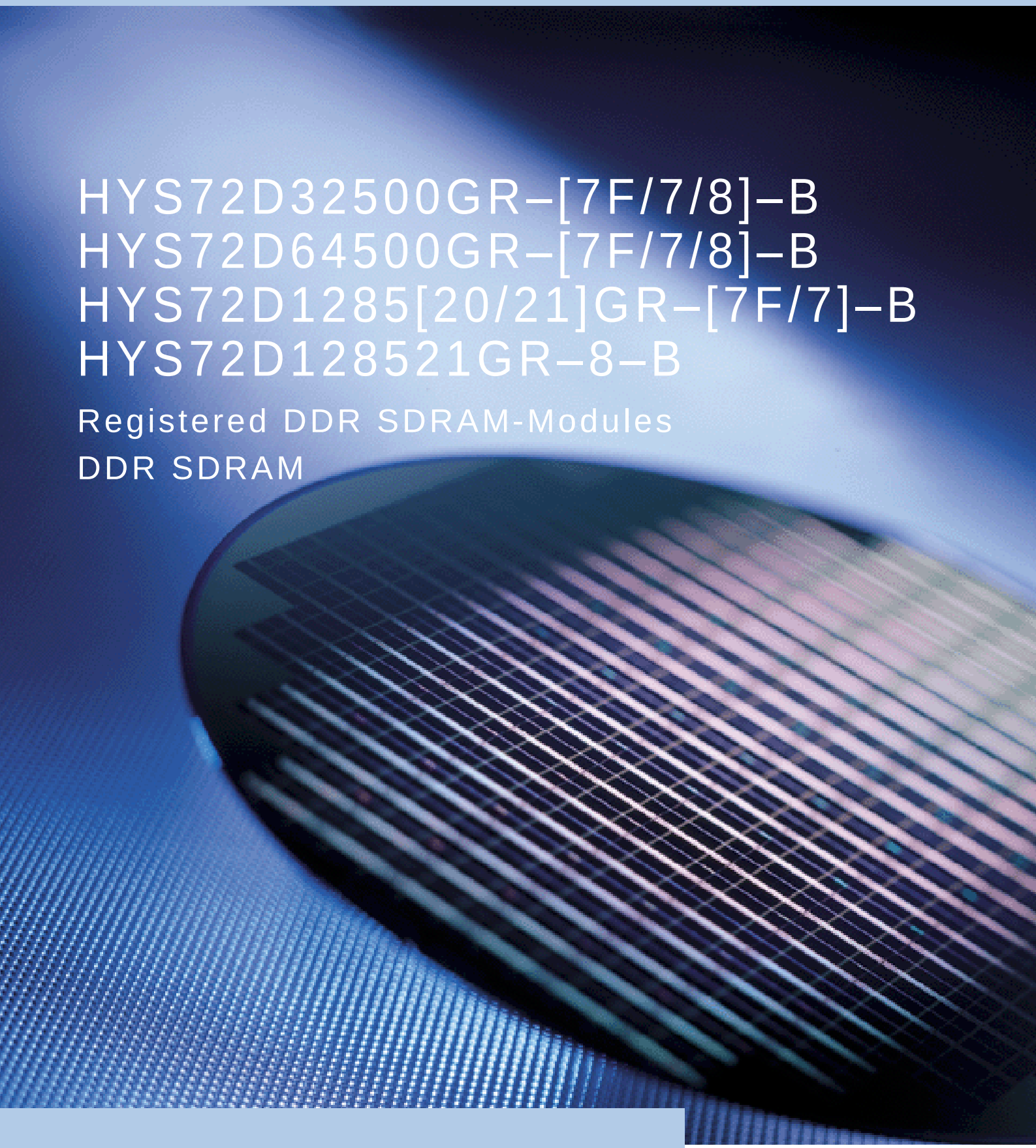
HYS72D32500GR–[7F/7/8]–B
HYS72D64500GR–[7F/7/8]–B
HYS72D1285[20/21]GR–[7F/7]–B
HYS72D128521GR–8–B

Registered DDR SDRAM-Modules
DDR SDRAM



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Edition 2004-01

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Data Sheet, Rev. 1.03, Jan. 2004

HYS72D32500GR–[7F/7/8]–B
HYS72D64500GR–[7F/7/8]–B
HYS72D1285[20/21]GR–[7F/7]–B
HYS72D128521GR–8–B

Registered DDR SDRAM-Modules
DDR SDRAM

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HYS72D32500GR–[7F/7/8]–B, HYS72D64500GR–[7F/7/8]–B, HYS72D1285[20/21]GR–[7F/7]–B

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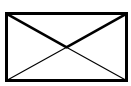


Table of Contents

1 Overview

1.1 Features

- 184-Pin Registered 8-Byte Dual-In-Line
  DDR SDRAM Module for “1U” PC, Workstation and Server main memory applications
- One rank 32M × 72, 64M × 72 and two ranks 128M × 72 organization
- JEDEC standard Double Data Rate Synchronous DRAMs (DDR SDRAM) with a single + 2.5 V (± 0.2 V) power supply
- Built with DDR SDRAMs in 66-Lead TSOPII package
- Programmable $\overline{\text{CAS}}$ Latency, Burst Length, and Wrap Sequence (Sequential & Interleave)
- Auto Refresh (CBR) and Self Refresh
- All inputs and outputs SSTL_2 compatible
- Re-drive for all input signals using register and PLL devices.
- Serial Presence Detect with E^2PROM
- Low Profile Modules form factor:
  133.35 mm × 30,48 mm (1.2”) × 4.00 mm
  (6,80 mm with stacked components)
- Based on JEDEC standard reference card layouts Raw Card L,M,N
- Gold plated contacts

Table 1 Performance

Part Number Speed Code			**–7F**	**–7**	**–8**	**Unit**
Module Speed Grade			DDR266F	DDR266A	DDR200A	–
Component Module			PC2100	PC2100	PC1600	–
max. Clock Frequency	@ CL = 2.5	fCK	143	143	125	MHz
	@ CL = 2	fCK	133	133	100	MHz

1.2 Description

The HYS72D[128/64/32]5[00/20/21]GR–[7F/7/8]-B are low profile versions of the standard Registered DIMM modules with 1.2” inch (30,48 mm) height for 1U Server Applications. The Low Profile DIMM versions are available as 32M × 72 (256MB), 64M × 72 (512MB) and 128M × 72 (1 GB).

The memory array is designed with Double Data Rate Synchronous DRAMs for ECC applications. All control and address signals are re-driven on the DIMM using register devices and a PLL for the clock distribution. This reduces capacitive loading to the system bus, but adds one cycle to the SDRAM timing. A variety of decoupling capacitors are mounted on the PC board. The DIMMs feature serial presence detect based on a serial E^2PROM device using the 2-pin I^2C protocol. The first 128 bytes are programmed with configuration data and the second 128 bytes are available to the customer.

Table 2 Ordering Information

Product Type	Compliance Code	Description	SDRAM Technology
PC2100 (CL = 2):			
HYS72D32500GR-7F-B	PC2100R-20220-L	one rank 256 MB Registered DIMM	256 Mbit (x8)
HYS72D32500GR-7-B	PC2100R-20330-L	one rank 256 MB Registered DIMM	256 Mbit (x8)
HYS72D64500GR-7F-B	PC2100R-20220-M	one rank 512 MB Registered DIMM	256 Mbit (x4)
HYS72D64500GR-7-B	PC2100R-20330-M	one rank 512 MB Registered DIMM	256 Mbit (x4)
HYS72D128520GR-7F-B	PC2100R-20220-N	two ranks 1 GByte Registered DIMM	256 MBit (x4) (stacked with soldering process)
HYS72D128520GR-7-B	PC2100R-20330-N	two ranks 1 GByte Registered DIMM	256 MBit (x4) (stacked with soldering process)
HYS72D128521GR-7F-B	PC2100R-20220-N	two ranks 1 GByte Registered DIMM	256 MBit (x4) (stacked with laser welding process)
HYS72D128521GR-7-B	PC2100R-20330-N	two ranks 1 GByte Registered DIMM	256 MBit (x4) (stacked with laser welding process)
PC1600 (CL = 2):			
HYS72D32500GR-8-B	PC1600R-20220-L	one rank 256 MB Registered DIMM	256 Mbit (x8)
HYS72D64500GR-8-B	PC1600R-20220-M	one rank 512 MB Registered DIMM	256 Mbit (x4)
HYS72D128521GR-8-B	PC1600R-20220-M	two ranks 1GByte Registered DIMM	256Mbit (x4) (stacked with laser welding process)

Note: All "product type" end with a place code designating the silicon-die revision. Reference information available on request. Example: HYS72D32500GR-7-B, indicating rev. C dies are used for SDRAM components. The "compliance code" is printed on the module labels describing the speed sort (for example "PC2100"), the latencies and SPD code definition (for example "20330" means CAS latency of 2.0 clocks, RCD[1)] latency of 3 clocks, Row Precharge latency of 3 clocks, and JEDEC SPD code definiton version 0), and the Raw Card used for this module.

1) RCD: Row-Column-Delay

2 Pin Configuration

Table 3 Pin Definitions and Functions

Symbol	Type	Function
A0 – A11, A12	Input	Address Inputs (A12 for 256 MB & 512 MB based modules)
BA0, BA1	Input	Bank Selects
DQ0 – DQ63	Input/Output	Data Input/Output
CB0 – CB7	Input/Output	Check Bits (×72 organization only)
$\overline{RAS}$	Input	Row Address Strobe
$\overline{CAS}$	Input	Column Address Strobe
$\overline{WE}$	Input	Read/Write Input
CKE0, CKE1	Input	Clock Enable
DQS0 – DQS8	Input/Output	SDRAM low data strobes
CK0, $\overline{CK0}$	Input	Differential Clock Input
DM0 – DM8	Input	SDRAM low data mask
DQS9 – DQS17	Input/Output	high data strobes
$\overline{CS0}$, $\overline{CS1}$	Input	Chip Selects
V_{DD}	Supply	Power (+2.5 V)
V_{SS}	Supply	Ground
V_{DDQ}	Supply	I/O Driver power supply
V_{DDID}	Output	V_{DD} Indentification flag
V_{DDSPD}	Supply	EEPROM power supply
V_{REF}	Supply	I/O reference supply
SCL	Input	Serial bus clock
SDA	Output	Serial bus data line
SA0 – SA2	Input	slave address select
NC	Input	no connect
DU	Input	don’t use
$\overline{RESET}$	Input	Reset pin (forces register inputs low) *)

*) for detailed description of the Power Up and Power Management on DDR Registered DIMMs see the Application Note at the end of this datasheet

Table 4 Address Format

Density	Organization	Memory Ranks	SDRAMs	# of SDRAMs	# of row/rank/ columns bits	Refresh	Period	Interval
256 MB	32M x 72	1	256Mbit 32M × 8	9	13 / 2 / 10	8K	64 ms	7.8 µs
512 MB	64M × 72	1	256Mbit 64M × 4	18	13 / 2 / 11	8K	64 ms	7.8 µs
1 GB	128M × 72	2	256Mbit 64M × 4	36 (stacked)	13 / 2 / 11	8K	64 ms	7.8 µs

Table 5 Pin Configuration

PIN#	Symbol	PIN#	Symbol	PIN#	Symbol	PIN#	Symbol
1	V_{REF}	48	A0	94	DQ4	141	A10
2	DQ0	49	CB2	95	DQ5	142	CB6
3	V_{SS}	50	V_{SS}	96	V_{DDQ}	143	V_{DDQ}
4	DQ1	51	CB3	97	DM0/DQS9	144	CB7
5	DQ0	52	BA1	98	DQ6	**KEY**	
6	DQ2	**KEY**		99	DQ7	145	V_{SS}
7	V_{DD}	53	DQ32	100	V_{SS}	146	DQ36
8	DQ3	54	V_{DDQ}	101	NC	147	DQ37
9	NC	55	DQ33	102	NC	148	V_{DD}
10	$\overline{\text{RESET}}$	56	DQS4	103	NC	149	DM4/DQS13
11	V_{SS}	57	DQ34	104	V_{DDQ}	150	DQ38
12	DQ8	58	VSS	105	DQ12	151	DQ39
13	DQ9	59	BA0	106	DQ13	152	V_{SS}
14	DQS1	60	DQ35	107	DM1/DQS10	153	DQ44
15	V_{DDQ}	61	DQ40	108	V_{DD}	154	$\overline{\text{RAS}}$
16	DU	62	V_{DDQ}	109	DQ14	155	DQ45
17	DU	63	$\overline{\text{WE}}$	110	DQ15	156	V_{DDQ}
18	V_{SS}	64	DQ41	111	CKE1	157	$\overline{\text{CS0}}$
19	DQ10	65	$\overline{\text{CAS}}$	112	V_{DDQ}	158	$\overline{\text{CS1}}$
20	DQ11	66	V_{SS}	113	NC	159	DM5/DQS14
21	CKE0	67	DQS5	114	DQ20	160	V_{SS}
22	V_{DDQ}	68	DQ42	115	NC / A12	161	DQ46
23	DQ16	69	DQ43	116	V_{SS}	162	DQ47
24	DQ17	70	VDD	117	DQ21	163	NC
25	DQS2	71	NC	118	A11	164	V_{DDQ}
26	V_{SS}	72	DQ48	119	DM2/DQS11	165	DQ52
27	A9	73	DQ49	120	V_{DD}	166	DQ53
28	DQ18	74	VSS	121	DQ22	167	NC
29	A7	75	DU	122	A8	168	V_{DD}
30	V_{DDQ}	76	DU	123	DQ23	169	DM6/DQS15

Table 5 Pin Configuration (cont'd)

PIN#	Symbol	PIN#	Symbol	PIN#	Symbol	PIN#	Symbol
31	DQ19	77	V_{DDQ}	124	V_{SS}	170	DQ54
32	A5	78	DQS6	125	A6	171	DQ55
33	DQ24	79	DQ50	126	DQ28	172	V_{DDQ}
34	V_{SS}	80	DQ51	127	DQ29	173	NC
35	DQ25	81	V_{SS}	128	V_{DDQ}	174	DQ60
36	DQS3	82	V_{DDID}	129	DM3/DQS12	175	DQ61
37	A4	83	DQ56	130	A3	176	V_{SS}
38	V_{DD}	84	DQ57	131	DQ30	177	DM7/DQS16
39	DQ26	85	V_{DD}	132	V_{SS}	178	DQ62
40	DQ27	86	DQS7	133	DQ31	179	DQ63
41	A2	87	DQ58	134	CB4	180	V_{DDQ}
42	V_{SS}	88	DQ59	135	CB5	181	SA0
43	A1	89	V_{SS}	136	V_{DDQ}	182	SA1
44	CB0	90	NC	137	CK0	183	SA2
45	CB1	91	SDA	138	$\overline{CK0}$	184	V_{DDSPD}
46	V_{DD}	92	SCL	139	V_{SS}	–	–
47	DQS8	93	V_{SS}	140	DM8/DQS17	–	–

Note: A12 is used for 256Mbit and 512Mbit based modules only

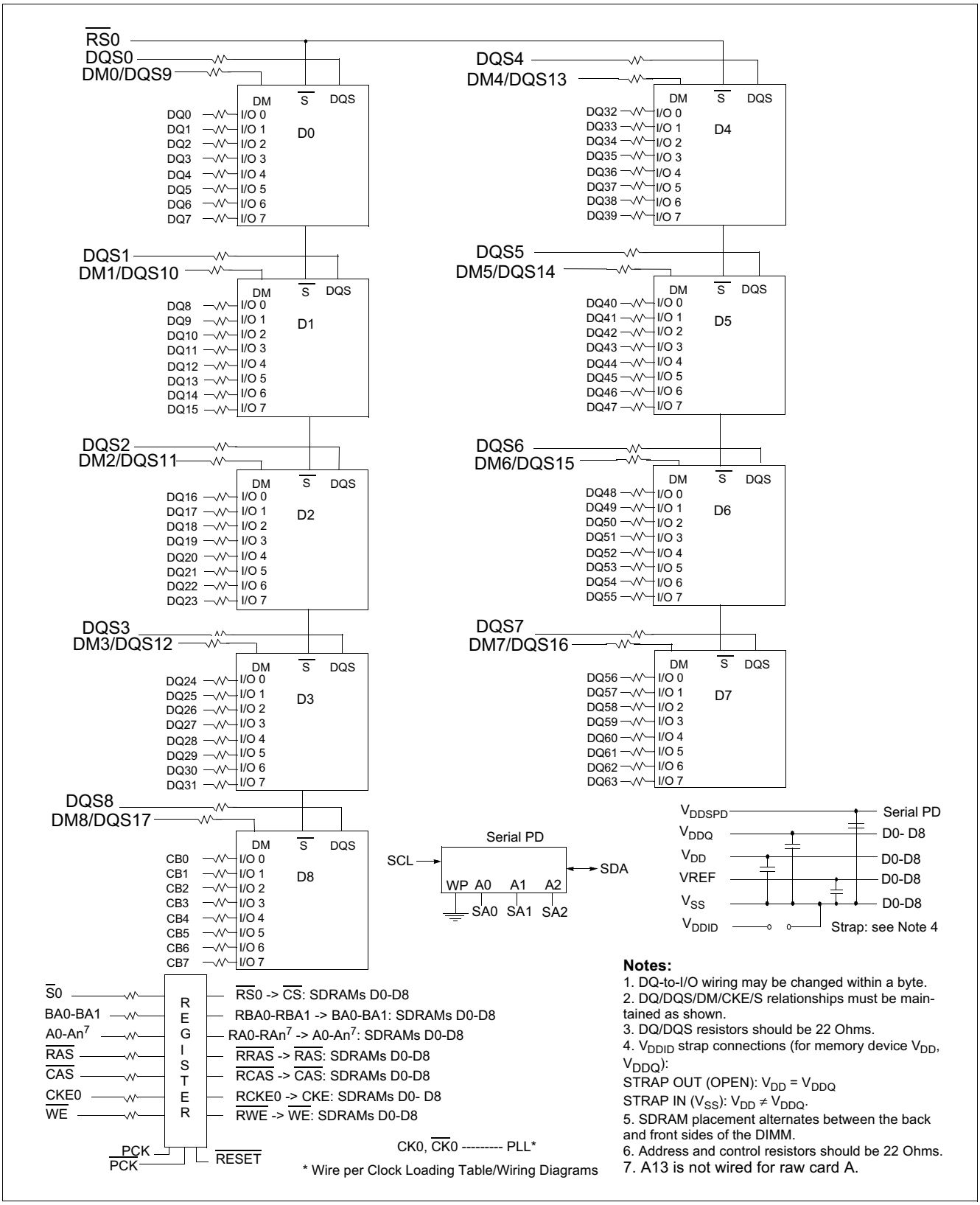


Figure 1 Block Diagram: One Rank 32M × 72 DDR SDRAM DIMM Module (×8 components) HYS72D32500GR on Raw Card L

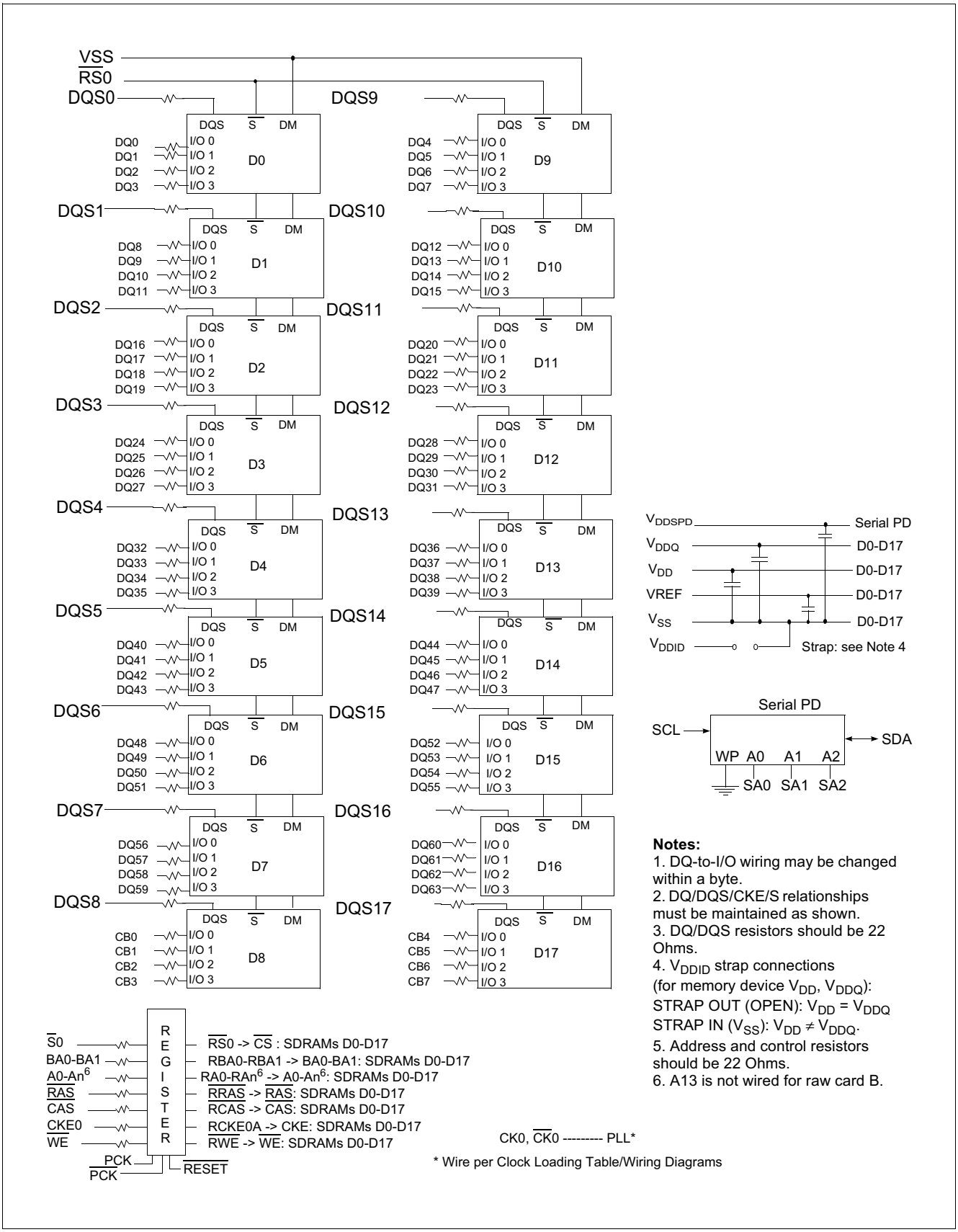


Figure 2 Block Diagram: One Rank 64M × 72 DDR SDRAM DIMM Module (×4 components) HYS72D64500GR on Raw Card M

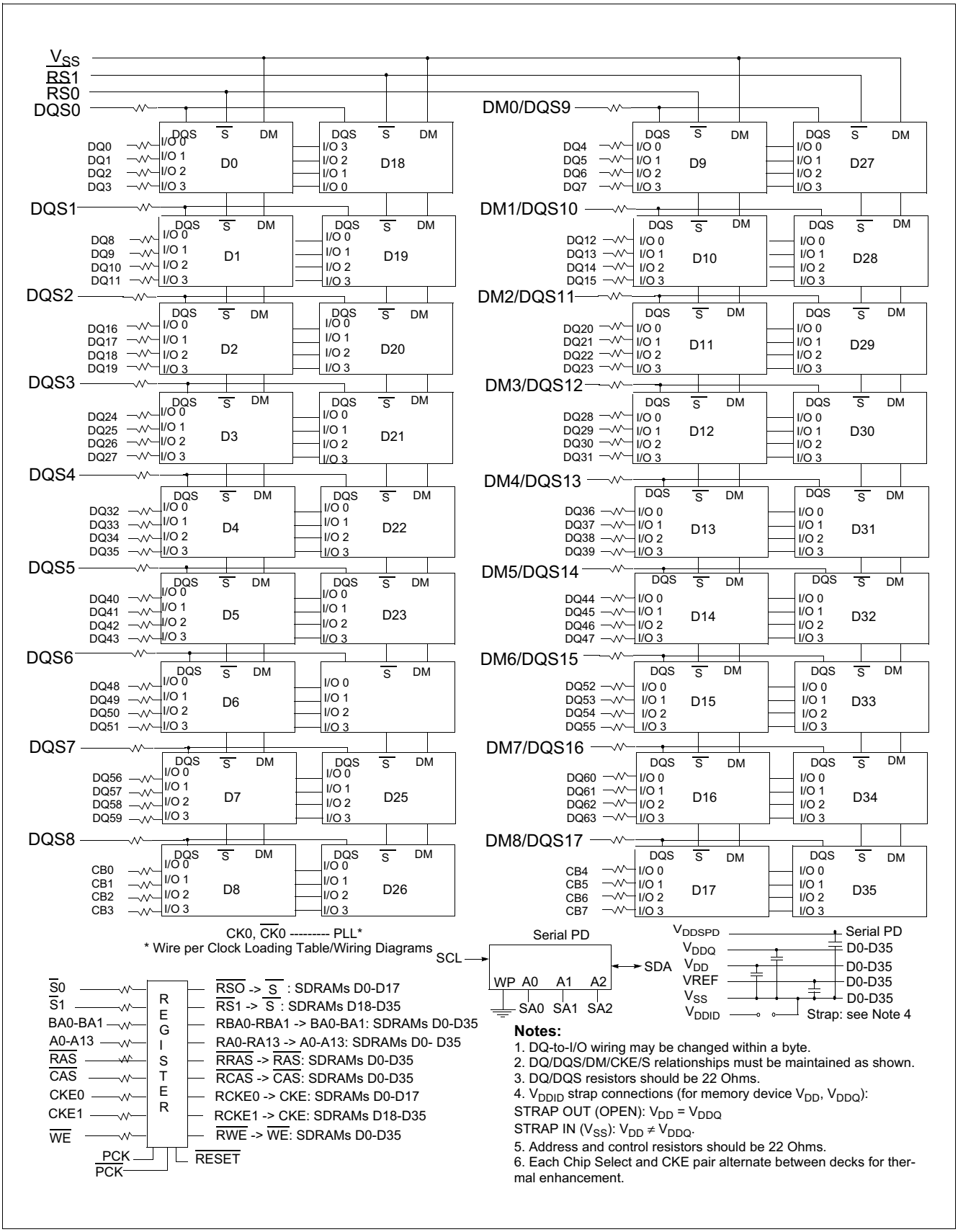


Figure 3 Block Diagram: Two Ranks 128M × 72 DDR SDRAM DIMM Modules (×4 components) HYS72D128520GR on Raw Card N

3 Electrical Characteristics

3.1 Operating Conditions

Table 6 Absolute Maximum Ratings

Parameter	Symbol	Values		Unit
		min.	max.	
Input/Output voltage relative to V_{SS}	V_{IN}, V_{OUT}	–0.5	3.6	V
Power supply voltage on V_{DD}/V_{DDQ} to V_{SS}	V_{DD}, V_{DDQ}	–0.5	3.6	V
Storage temperature range	T_{STG}	–55	+150	°C
Power dissipation (per SDRAM component)	P_D	–	1	W
Data out current (short circuit)	I_{OS}	–	50	mA

Attention: Permanent device damage may occur if "Absolute Maximum Ratings" are exceeded. Functional operation should be restricted to recommended operation conditions. Exposure to higher than recommended voltage for extended periods of time affect device reliability

Table 7 Supply Voltage Levels

Parameter	Symbol	Values			Unit/ Notes
		min.	nom.	max.	
Device Supply Voltage	V_{DD}	2.3	2.5	2.7	V
Output Supply Voltage	V_{DDQ}	2.3	2.5	2.7	V 1)
Input Reference Voltage	V_{REF}	0.49 × V_{DDQ}	0.5 × V_{DDQ}	0.51 × V_{DDQ}	V 2)
Termination Voltage	V_{TT}	V_{REF} – 0.04	V_{REF}	V_{REF} + 0.04	V 3)
EEPROM supply voltage	V_{DDSPD}	2.3	2.5	3.6	V

Note:

1. *Under all conditions, V_{DDQ} must be less than or equal to V_{DD}*
2. *Peak to peak AC noise on V_{REF} may not exceed ± 2% $V_{REF\ (DC)}$. V_{REF} is also expected to track noise variations in V_{DDQ}.*
3. *V_{TT} of the transmitting device must track V_{REF} of the receiving device*

.

Table 8 DC Operating Conditions (SSTL_2 Inputs)
(V_{DDQ} = 2.5 V, T_A = 70 °C, Voltage Referenced to V_{SS})

Parameter	Symbol	Values		Unit/ Notes
		min.	max.	
DC Input Logic High	$V_{IH,\ (DC)}$	V_{REF} +0.15	V_{DDQ} +0.3	V 1)
DC Input Logic Low	$V_{IL,\ (DC)}$	–0.30	V_{REF} –0.15	V
Input Leakage Current	I_{IL}	–5	5	µA 1)
Output Leakage Current	I_{OL}	–5	5	µA 2)

Note:

1. *The relationship between the V_{DDQ} of the driving device and the V_{REF} of the receiving device is what determines noise margins. However, in the case of $V_{IH\ (max.)}$ (input overdrive), it is the V_{DDQ} of the receiving device that is referenced. In the case where a device is implemented such that it supports SSTL_2 inputs but has no SSTL_2 outputs (such as a translator), and therefore no V_{DDQ} supply voltage connection, inputs must tolerate input overdrive to 3.0 V (High corner V_{DDQ} + 300 mV).*
2. *For any pin under test input of 0 V ≤ V_{IN} ≤ V_{DDQ} + 0.3 V. Values are shown per DDR-SDRAM component*

3.2 Current Specification and Conditions

Table 9 I_{DD} Conditions

Parameter	Symbol
Operating Current 0 one bank; active/ precharge; DQ, DM, and DQS inputs changing once per clock cycle; address and control inputs changing once every two clock cycles.	I_{DD0}
Operating Current 1 one bank; active/read/precharge; Burst Length = 4; see component data sheet.	I_{DD1}
Precharge Power-Down Standby Current all banks idle; power-down mode; CKE ≤ $V_{IL,MAX}$	I_{DD2P}
Precharge Floating Standby Current $\overline{CS}$ ≥ $V_{IH,,MIN}$, all banks idle; CKE ≥ $V_{IH,MIN}$; address and other control inputs changing once per clock cycle; V_{IN} = V_{REF} for DQ, DQS and DM.	I_{DD2F}
Precharge Quiet Standby Current $\overline{CS}$ ≥ V_{IHMIN}, all banks idle; CKE ≥ $V_{IH,MIN}$; V_{IN} = V_{REF} for DQ, DQS and DM; address and other control inputs stable at ≥ $V_{IH,MIN}$ or ≤ $V_{IL,MAX}$.	I_{DD2Q}
Active Power-Down Standby Current one bank active; power-down mode; CKE ≤ V_{ILMAX}; V_{IN} = V_{REF} for DQ, DQS and DM.	I_{DD3P}
Active Standby Current one bank active; $\overline{CS}$ ≥ $V_{IH,MIN}$; CKE ≥ $V_{IH,MIN}$; t_{RC} = $t_{RAS,MAX}$; DQ, DM and DQS inputs changing twice per clock cycle; address and control inputs changing once per clock cycle.	I_{DD3N}
Operating Current Read one bank active; Burst Length = 2; reads; continuous burst; address and control inputs changing once per clock cycle; 50% of data outputs changing on every clock edge; CL = 2 for DDR266(A), CL = 3 for DDR333 and DDR400B; I_{OUT} = 0 mA	I_{DD4R}
Operating Current Write one bank active; Burst Length = 2; writes; continuous burst; address and control inputs changing once per clock cycle; 50% of data outputs changing on every clock edge; CL = 2 for DDR266(A), CL = 3 for DDR333 and DDR400B	I_{DD4W}
Auto-Refresh Current t_{RC} = t_{RFCMIN}, burst refresh	I_{DD5}
Self-Refresh Current CKE ≤ 0.2 V; external clock on	I_{DD6}
Operating Current 7 four bank interleaving with Burst Length = 4; see component data sheet.	I_{DD7}

Table 10 I_{DD} Specifications –7F/–7

Product Type & Organisation	HYS72D32500GR–7F–B	HYS72D64500GR–7F–B	HYS72D128521GR–7F–B	HYS72D128520GR–7F–B	HYS72D32500GR–7–B	HYS72D64500GR–7–B	HYS72D128520GR–7–B	HYS72D128521GR–7–B	Unit	Note/ Test Conditions[5]
	256 MB	512 MB	1 GByte	1 GByte	256 MB	512 MB	1 GByte	1 GByte		
	×72	×72	×72	×72	×72	×72	×72	×72		
	1 Rank	1 Rank	2 Ranks	2 Ranks	1 Rank	1 Rank	2 Ranks	2 Ranks		
	–7F	–7F	–7F	–7F	–7	–7	–7	–7		
	max.	max.	max.	max.	max.	max.	max.	max.		
I_{DD0}	990	1980	2970	2970	900	1800	2790	2790	mA	1)4)
I_{DD1}	1080	2160	3150	3150	990	1980	2970	2970	mA	1)3)4)
I_{DD2P}	72	144	288	288	72	144	288	288	mA	2)4)
I_{DD2F}	360	720	1440	1440	360	720	1440	1440	mA	2)4)
I_{DD2Q}	225	450	900	900	225	450	900	900	mA	2)4)
I_{DD3P}	162	324	648	648	162	324	648	648	mA	2)4)
I_{DD3N}	495	990	1980	1980	495	990	1980	1980	mA	2)4)
I_{DD4R}	1035	2070	3060	3060	1035	2070	3060	3060	mA	1)3)4)
I_{DD4W}	1125	2250	3240	3240	1125	2250	3240	3240	mA	1)4)
I_{DD5}	1620	3240	4230	4230	1620	3240	4230	4230	mA	1)4)
I_{DD6}	23	45	90	90	23	45	90	90	mA	2)4)
I_{DD7}	2025	4050	5040	5040	2025	4050	5040	5040	mA	1)3)4)

1) The module I_{DD} values are calculated from the component I_{DD} datasheet values are:
$n * I_{DD}$×[component] for single bank modules (n: number of components per module bank)
$n * I_{DD}$×[component] + $n * I_{DD3N}$[component] for two bank modules (n: number of components per module bank)

2) The module I_{DD} values are calculated from the component I_{DD} datasheet values are:
$n * I_{DD}$×[component] for single bank modules (n: number of components per module bank)
$2 * n * I_{DD}$×[component] for single two bank modules (n: number of components per module bank)

3) DQ I/O (I_{DDQ}) currents are not included into calculations: module I_{DD} values will be measured differently depending on load conditions

4) DRAM component currents only: module I_{DD} will be measured differently depending upon register and PLL operation currents

5) Test condition for maximum values: V_{DD} = 2.7 V, T_A = 10 °C

Table 11 I_{DD} Specifications –8

Product Type & Organisation	HYS72D32500GR–8–B	HYS72D64500GR–8–B	HYS72D128521GR–8–B	Unit	Note/ Test Conditions[5]
	256 MB	512 MB	1 GByte		
	×72	×72	×72		
	1 Rank	1 Rank	2 Ranks		
	–8	–8	–8		
	max.	max.	max.		
I_{DD0}	810	1620	2430	mA	1)4)
I_{DD1}	900	1800	2610	mA	1)3)4)
I_{DD2P}	63	126	252	mA	2)4)
I_{DD2F}	315	630	1260	mA	2)4)
I_{DD2Q}	198	396	792	mA	2)4)
I_{DD3P}	144	288	576	mA	2)4)
I_{DD3N}	405	810	1620	mA	2)4)
I_{DD4R}	855	1710	2520	mA	1)3)4)
I_{DD4W}	945	1890	2700	mA	1)4)
I_{DD5}	1530	3060	3870	mA	1)4)
I_{DD6}	22,5	45	90	mA	2)4)
I_{DD7}	1890	3780	4590	mA	1)3)4)

1) The module I_{DD} values are calculated from the component I_{DD} datasheet values are:
$n * I_{DD}$×[component] for single bank modules (n: number of components per module bank)
$n * I_{DD}$×[component] + $n * I_{DD3N}$[component] for two bank modules (n: number of components per module bank)

2) The module I_{DD} values are calculated from the component I_{DD} datasheet values are:
$n * I_{DD}$×[component] for single bank modules (n: number of components per module bank)
$2 * n * I_{DD}$×[component] for single two bank modules (n: number of components per module bank)

3) DQ I/O (I_{DDQ}) currents are not included into calculations: module I_{DD} values will be measured differently depending on load conditions

4) DRAM component currents only: module I_{DD} will be measured differently depending upon register and PLL operation currents

5) Test condition for maximum values: V_{DD} = 2.7 V, T_A = 10 °C

3.3 AC Characteristics

Table 12 AC Timing - Absolute Specifications –8/–7/-7F

Parameter	Symbol	–8		–7		–7F		Unit	Note/ Test Condition [1]
		DDR200		DDR266A		DDR266F			
		Min.	Max.	Min.	Max.	Min.	Max.		
DQ output access time from CK/$\overline{CK}$	t_{AC}	–0.8	+0.8	–0.75	+0.75	–0.75	+0.75	ns	2)3)4)5)
DQS output access time from CK/$\overline{CK}$	t_{DQSCK}	–0.8	+0.8	–0.75	+0.75	–0.75	+0.75	ns	2)3)4)5)
CK high-level width	t_{CH}	0.45	0.55	0.45	0.55	0.45	0.55	t_{CK}	2)3)4)5)
CK low-level width	t_{CL}	0.45	0.55	0.45	0.55	0.45	0.55	t_{CK}	2)3)4)5)
Clock Half Period	t_{HP}	min. (t_{CL}, t_{CH})		min. (t_{CL}, t_{CH})		min. (t_{CL}, t_{CH})		ns	2)3)4)5)
Clock cycle time	$t_{CK2.5}$	8	12	7	12	7	12	ns	CL = 2.5 2)3)4)5)
	t_{CK2}	10	12	7.5	12	7.5	12	ns	CL = 2.0 2)3)4)5)
DQ and DM input hold time	t_{DH}	0.6	—	0.5	—	0.5	—	ns	2)3)4)5)
DQ and DM input setup time	t_{DS}	0.6	—	0.5	—	0.5	—	ns	2)3)4)5)
Control and Addr. input pulse width (each input)	t_{IPW}	2.5	—	2.2	—	2.2	—	ns	2)3)4)5)6)
DQ and DM input pulse width (each input)	t_{DIPW}	2.0	—	1.75	—	1.75	—	ns	2)3)4)5)6)
Data-out high-impedance time from CK/$\overline{CK}$	t_{HZ}	–0.8	+0.8	–0.75	+0.75	–0.75	+0.75	ns	2)3)4)5)7)
Data-out low-impedance time from CK/$\overline{CK}$	t_{LZ}	–0.8	+0.8	–0.75	+0.75	–0.75	+0.75	ns	2)3)4)5)7)
Write command to 1st DQS latching transition	t_{DQSS}	0.75	1.25	0.75	1.25	0.75	1.25	t_{CK}	2)3)4)5)
DQS-DQ skew (DQS and associated DQ signals)	t_{DQSQ}	—	+0.6	—	+0.5	—	+0.5	ns	2)3)4)5)
								ns	
Data hold skew factor	t_{QHS}	—	1.0	—	0.75	—	0.75	ns	2)3)4)5)
								ns	
DQ/DQS output hold time	t_{QH}	t_{HP} – t_{QHS}	—	t_{HP} – t_{QHS}	—	t_{HP} – t_{QHS}	—	ns	2)3)4)5)
DQS input low (high) pulse width (write cycle)	$t_{DQSL,H}$	0.35	—	0.35	—	0.35	—	t_{CK}	2)3)4)5)
DQS falling edge to CK setup time (write cycle)	t_{DSS}	0.2	—	0.2	—	0.2	—	t_{CK}	2)3)4)5)
DQS falling edge hold time from CK (write cycle)	t_{DSH}	0.2	—	0.2	—	0.2	—	t_{CK}	2)3)4)5)
Mode register set command cycle time	t_{MRD}	2	—	2	—	2	—	t_{CK}	2)3)4)5)
Write preamble setup time	t_{WPRES}	0	—	0	—	0	—	ns	2)3)4)5)8)
Write postamble	t_{WPST}	0.40	0.60	0.40	0.60	0.40	0.60	t_{CK}	2)3)4)5)9)
Write preamble	t_{WPRE}	0.25	—	0.25	—	0.25	—	t_{CK}	2)3)4)5)

Table 12 AC Timing - Absolute Specifications –8/–7/-7F

Parameter	Symbol	–8		–7		–7F		Unit	Note/ Test Condition [1]
		DDR200		DDR266A		DDR266F			
		Min.	Max.	Min.	Max.	Min.	Max.		
Address and control input setup time	t_{IS}	1.1	—	0.9	—	0.9	—	ns	fast slew rate 3)4)5)6)10)
		1.1	—	1.0	—	1.0	—	ns	slow slew rate 3)4)5)6)10)
Address and control input hold time	t_{IH}	1.1	—	0.9	—	0.9	—	ns	fast slew rate 3)4)5)6)10)
		1.1	—	1.0	—	1.0	—	ns	slow slew rate 3)4)5)6)10)
Read preamble	t_{RPRE}	0.9	1.1	0.9	1.1	0.9	1.1	t_{CK}	CL > 1.5 2)3)4)5)
Read preamble setup time	t_{RPRES}	1.5	—	NA		NA	—	t_{CK}	2)3)4)5)11)
Read postamble	t_{RPST}	0.40	0.60	0.40	0.60	0.40	0.60	ns	2)3)4)5)
Active to Precharge command	t_{RAS}	50	120E+3	45	120E+3	45	120E+3	t_{CK}	2)3)4)5)
Active to Active/Auto-refresh command period	t_{RC}	70	—	65	—	65	—	ns	2)3)4)5)
Auto-refresh to Active/Auto-refresh command period	t_{RFC}	80	—	75	—	75	—	ns	2)3)4)5)
Active to Read or Write delay	t_{RCD}	20	—	20	—	20	—	ns	2)3)4)5)
Precharge command period	t_{RP}	20	—	20	—	20	—	ns	2)3)4)5)
Active to Autoprecharge delay	t_{RAP}	20	—	20	—	20	—	ns	2)3)4)5)
Active bank A to Active bank B command	t_{RRD}	15	—	15	—	15	—	ns	2)3)4)5)
Write recovery time	t_{WR}	15	—	15	—	15	—	ns	2)3)4)5)
Auto precharge write recovery + precharge time	t_{DAL}	$(t_{wr}/t_{CK}) + (t_{rp}/t_{CK})$						t_{CK}	2)3)4)5)12)
Internal write to read command delay	t_{WTR}	1	—	1	—	1	—	t_{CK}	CL > 1.5 2)3)4)5)
Exit self-refresh to non-read command	t_{XSNR}	80	—	75	—	75	—	*ns*	2)3)4)5)
Exit self-refresh to read command	t_{XSRD}	200	—	200	—	200	—	t_{CK}	2)3)4)5)
Average Periodic Refresh Interval	t_{REFI}	—	7.8	—	7.8	—	7.8	µs	2)3)4)5)13)

1) 0 °C ≤ T_A ≤ 70 °C; V_{DDQ} = 2.5 V ± 0.2 V, V_{DD} = +2.5 V ± 0.2 V

2) Input slew rate ≥ 1 V/ns for DDR266a, DDR266F and = 1 V/ns for DDR200

3) The CK/$\overline{CK}$ input reference level (for timing reference to CK/$\overline{CK}$) is the point at which CK and $\overline{CK}$ cross: the input reference level for signals other than CK/$\overline{CK}$, is V_{REF}. CK/$\overline{CK}$ slew rate are ≥ 1.0 V/ns.

4) Inputs are not recognized as valid until V_{REF} stabilizes.

5) The Output timing reference level, as measured at the timing reference point indicated in AC Characteristics (note 3) is V_{TT}.

6) These parameters guarantee device timing, but they are not necessarily tested on each device.

7) t_{HZ} and t_{LZ} transitions occur in the same access time windows as valid data transitions. These parameters are not referred to a specific voltage level, but specify when the device is no longer driving (HZ), or begins driving (LZ).

8) The specific requirement is that DQS be valid (HIGH, LOW, or some point on a valid transition) on or before this CK edge. A valid transition is defined as monotonic and meeting the input slew rate specifications of the device. When no writes were previously in progress on the bus, DQS will be transitioning from Hi-Z to logic LOW. If a previous write was in progress, DQS could be HIGH, LOW, or transitioning from HIGH to LOW at this time, depending on t_{DQSS}.

9) The maximum limit for this parameter is not a device limit. The device operates with a greater value for this parameter, but system performance (bus turnaround) degrades accordingly.

10) Fast slew rate ≥ 1.0 V/ns , slow slew rate ≥ 0.5 V/ns and < 1 V/ns for command/address and CK & $\overline{CK}$ slew rate > 1.0 V/ns, measured between $V_{OH(ac)}$ and $V_{OL(ac)}$.

11) t_{RPRES} is defined for CL = 1.5 operation only

12) For each of the terms, if not already an integer, round to the next highest integer. t_{CK} is equal to the actual system clock cycle time.

13) A maximum of eight Autorefresh commands can be posted to any given DDR SDRAM device.

4 SPD Contents

Table 13 SPD Codes for HYS72D32500GR–[7F/7/8]-B

	Product Type & Organization	HYS72D32500GR–8–B	HYS72D32500GR–7–B	HYS72D32500GR–7F–B
		×72	×72	×72
		1 rank	1 rank	1 rank
		reg	reg	reg
	Label Code	PC1600R – 20220	PC2100R – 20330	PC2100R – 20220
	Jedec SPD Revision	Rev. 0.0	Rev. 0.0	Rev. 0.0
Byte#	Description	HEX	HEX	HEX
0	Programmed SPD Bytes in E2PROM	80	80	80
1	Total number of Bytes in E2PROM	08	08	08
2	Memory Type (DDR = 07h)	07	07	07
3	Number of Row Addresses	0D	0D	0D
4	Number of Column Addresses	0A	0A	0A
5	Number of DIMM Ranks	01	01	01
6	Data Width (LSB)	48	48	48
7	Data Width (MSB)	00	00	00
8	Interface Voltage Levels	04	04	04
9	tCK @ CLmax (Byte 18) [ns]	80	70	70
10	tAC SDRAM @ CLmax (Byte 18) [ns]	80	75	75
11	Error Correction Support	02	02	02
12	Refresh Rate	82	82	82
13	Primary SDRAM Width	08	08	08
14	Error Checking SDRAM Width	08	08	08
15	tCCD [cycles]	01	01	01
16	Burst Length Supported	0E	0E	0E
17	Number of Banks on SDRAM Device	04	04	04
18	CAS Latency	0C	0C	0C
19	CS Latency	01	01	01
20	Write Latency	02	02	02
21	DIMM Attributes	26	26	26
22	Component Attributes	C0	C0	C0
23	tCK @ CLmax -0.5 (Byte 18) [ns]	A0	75	75
24	tAC SDRAM @ CLmax -0.5 [ns]	80	75	75
25	tCK @ CLmax -1 (Byte 18) [ns]	00	00	00

Table 13 SPD Codes for HYS72D32500GR–[7F/7/8]-B

	Product Type & Organization	HYS72D32500GR–8–B	HYS72D32500GR–7–B	HYS72D32500GR–7F–B
		×72	×72	×72
		1 rank	1 rank	1 rank
		reg	reg	reg
	Label Code	PC1600R – 20220	PC2100R – 20330	PC2100R – 20220
	Jedec SPD Revision	Rev. 0.0	Rev. 0.0	Rev. 0.0
Byte#	Description	HEX	HEX	HEX
26	tAC SDRAM @ CLmax -1 [ns]	00	00	00
27	tRPmin [ns]	50	50	3C
28	tRRDmin [ns]	3C	3C	3C
29	tRCDmin [ns]	50	50	3C
30	tRASmin [ns]	32	2D	2D
31	Module Density per Rank	40	40	40
32	tAS, tCS [ns]	B0	90	90
33	tAH, TCH [ns]	B0	90	90
34	tDS [ns]	60	50	50
35	tDH [ns]	60	50	50
36-40	not used	00	00	00
41	tRCmin [ns]	46	41	3C
42	tRFCmin [ns]	50	4B	4B
43	tCKmax [ns]	30	30	30
44	tDQSQmax [ns]	3C	32	32
45	tQHSmax [ns]	A0	75	75
46	not used	00	00	00
47	DIMM PCB Height	00	00	00
48-61	not used	00	00	00
62	SPD Revision	00	00	00
63	Checksum of Byte 0-62	BF	CA	9D
64	JEDEC ID Code of Infineon (1)	C1	C1	C1
65	JEDEC ID Code of Infineon (2)	49	49	49
66	JEDEC ID Code of Infineon (3)	4E	4E	4E
67	JEDEC ID Code of Infineon (4)	46	46	46
68	JEDEC ID Code of Infineon (5)	49	49	49
69	JEDEC ID Code of Infineon (6)	4E	4E	4E

Table 13 SPD Codes for HYS72D32500GR–[7F/7/8]-B

	Product Type & Organization	HYS72D32500GR–8–B	HYS72D32500GR–7–B	HYS72D32500GR–7F–B
		×72	×72	×72
		1 rank	1 rank	1 rank
		reg	reg	reg
	Label Code	PC1600R – 20220	PC2100R – 20330	PC2100R – 20220
	Jedec SPD Revision	Rev. 0.0	Rev. 0.0	Rev. 0.0
Byte#	Description	HEX	HEX	HEX
70	JEDEC ID Code of Infineon (7)	45	45	45
71	JEDEC ID Code of Infineon (8)	4F	4F	4F
72	Module Manufacturer Location	xx	xx	xx
73	Part Number, Char 1	37	37	37
74	Part Number, Char 2	32	32	32
75	Part Number, Char 3	44	44	44
76	Part Number, Char 4	33	33	33
77	Part Number, Char 5	32	32	32
78	Part Number, Char 6	35	35	35
79	Part Number, Char 7	30	30	30
80	Part Number, Char 8	30	30	30
81	Part Number, Char 9	47	47	47
82	Part Number, Char 10	52	52	52
83	Part Number, Char 11	38	37	37
84	Part Number, Char 12	42	42	46
85	Part Number, Char 13	20	20	42
86	Part Number, Char 14	20	20	20
87	Part Number, Char 15	20	20	20
88	Part Number, Char 16	20	20	20
89	Part Number, Char 17	20	20	20
90	Part Number, Char 18	20	20	20
91	Module Revision Code	xx	xx	xx
92	Test Program Revision Code	xx	xx	xx
93	Module Manufacturing Date Year	xx	xx	xx
94	Module Manufacturing Date Week	xx	xx	xx
95	Module Serial Number (1)	xx	xx	xx
96	Module Serial Number (2)	xx	xx	xx

Table 13 SPD Codes for HYS72D32500GR–[7F/7/8]-B

	Product Type & Organization	HYS72D32500GR–8–B	HYS72D32500GR–7–B	HYS72D32500GR–7F–B
		×72	×72	×72
		1 rank	1 rank	1 rank
		reg	reg	reg
	Label Code	PC1600R – 20220	PC2100R – 20330	PC2100R – 20220
	Jedec SPD Revision	Rev. 0.0	Rev. 0.0	Rev. 0.0
Byte#	Description	HEX	HEX	HEX
97	Module Serial Number (3)	xx	xx	xx
98	Module Serial Number (4)	xx	xx	xx
99-127	not used	00	00	00

Table 14 SPD Codes for HYS72D64500GR–[7F/7/8]–B

	Product Type & Organization	HYS72D64500GR–7F–B	HYS72D64500GR–7–B	HYS72D64500GR–8–B
		×72	×72	×72
		1 rank	1 rank	1 rank
		reg	reg	reg
	Label Code	PC2100R – 20220	PC2100R – 20330	PC1600R – 20220
	Jedec SPD Revision	Rev. 0.0	Rev. 0.0	Rev. 0.0
Byte#	Description	HEX	HEX	HEX
0	Programmed SPD Bytes in E2PROM	80	80	80
1	Total number of Bytes in E2PROM	08	08	08
2	Memory Type (DDR = 07h)	07	07	07
3	Number of Row Addresses	0D	0D	0D
4	Number of Column Addresses	0B	0B	0B
5	Number of DIMM Ranks	01	01	01

Table 14 SPD Codes for HYS72D64500GR–[7F/7/8]–B

	Product Type & Organization	HYS72D64500GR–7F–B	HYS72D64500GR–7–B	HYS72D64500GR–8–B
		×72	×72	×72
		1 rank	1 rank	1 rank
		reg	reg	reg
	Label Code	PC2100R – 20220	PC2100R – 20330	PC1600R – 20220
	Jedec SPD Revision	Rev. 0.0	Rev. 0.0	Rev. 0.0
Byte#	Description	HEX	HEX	HEX
6	Data Width (LSB)	48	48	48
7	Data Width (MSB)	00	00	00
8	Interface Voltage Levels	04	04	04
9	tCK @ CLmax (Byte 18) [ns]	70	70	80
10	tAC SDRAM @ CLmax (Byte 18) [ns]	75	75	80
11	Error Correction Support	02	02	02
12	Refresh Rate	82	82	82
13	Primary SDRAM Width	04	04	04
14	Error Checking SDRAM Width	04	04	04
15	tCCD [cycles]	01	01	01
16	Burst Length Supported	0E	0E	0E
17	Number of Banks on SDRAM Device	04	04	04
18	CAS Latency	0C	0C	0C
19	CS Latency	01	01	01
20	Write Latency	02	02	02
21	DIMM Attributes	26	26	26
22	Component Attributes	C0	C0	C0
23	tCK @ CLmax -0.5 (Byte 18) [ns]	75	75	A0
24	tAC SDRAM @ CLmax -0.5 [ns]	75	75	80
25	tCK @ CLmax -1 (Byte 18) [ns]	00	00	00
26	tAC SDRAM @ CLmax -1 [ns]	00	00	00
27	tRPmin [ns]	3C	50	50
28	tRRDmin [ns]	3C	3C	3C
29	tRCDmin [ns]	3C	50	50
30	tRASmin [ns]	2D	2D	32
31	Module Density per Rank	80	80	80
32	tAS, tCS [ns]	90	90	B0

Table 14 SPD Codes for HYS72D64500GR–[7F/7/8]–B

	Product Type & Organization	HYS72D64500GR–7F–B	HYS72D64500GR–7–B	HYS72D64500GR–8–B
		×72	×72	×72
		1 rank	1 rank	1 rank
		reg	reg	reg
	Label Code	PC2100R – 20220	PC2100R – 20330	PC1600R – 20220
	Jedec SPD Revision	Rev. 0.0	Rev. 0.0	Rev. 0.0
Byte#	Description	HEX	HEX	HEX
33	tAH, TCH [ns]	90	90	B0
34	tDS [ns]	50	50	60
35	tDH [ns]	50	50	60
36-40	not used	00	00	00
41	tRCmin [ns]	3C	41	46
42	tRFCmin [ns]	4B	4B	50
43	tCKmax [ns]	30	30	30
44	tDQSQmax [ns]	32	32	3C
45	tQHSmax [ns]	75	75	A0
46	not used	00	00	00
47	DIMM PCB Height	00	00	00
48-61	not used	00	00	00
62	SPD Revision	00	00	00
63	Checksum of Byte 0-62	D6	03	F8
64	JEDEC ID Code of Infineon (1)	C1	C1	C1
65	JEDEC ID Code of Infineon (2)	49	49	49
66	JEDEC ID Code of Infineon (3)	4E	4E	4E
67	JEDEC ID Code of Infineon (4)	46	46	46
68	JEDEC ID Code of Infineon (5)	49	49	49
69	JEDEC ID Code of Infineon (6)	4E	4E	4E
70	JEDEC ID Code of Infineon (7)	45	45	45
71	JEDEC ID Code of Infineon (8)	4F	4F	4F
72	Module Manufacturer Location	xx	xx	xx
73	Part Number, Char 1	37	37	37
74	Part Number, Char 2	32	32	32
75	Part Number, Char 3	44	44	44
76	Part Number, Char 4	36	36	36

Table 14 SPD Codes for HYS72D64500GR–[7F/7/8]–B

	Product Type & Organization	HYS72D64500GR–7F–B	HYS72D64500GR–7–B	HYS72D64500GR–8–B
		×72	×72	×72
		1 rank	1 rank	1 rank
		reg	reg	reg
	Label Code	PC2100R – 20220	PC2100R – 20330	PC1600R – 20220
	Jedec SPD Revision	Rev. 0.0	Rev. 0.0	Rev. 0.0
Byte#	Description	HEX	HEX	HEX
77	Part Number, Char 5	34	34	34
78	Part Number, Char 6	35	35	35
79	Part Number, Char 7	30	30	30
80	Part Number, Char 8	30	30	30
81	Part Number, Char 9	47	47	47
82	Part Number, Char 10	52	52	52
83	Part Number, Char 11	37	37	38
84	Part Number, Char 12	46	42	42
85	Part Number, Char 13	42	20	20
86	Part Number, Char 14	20	20	20
87	Part Number, Char 15	20	20	20
88	Part Number, Char 16	20	20	20
89	Part Number, Char 17	20	20	20
90	Part Number, Char 18	20	20	20
91	Module Revision Code	xx	xx	xx
92	Test Program Revision Code	xx	xx	xx
93	Module Manufacturing Date Year	xx	xx	xx
94	Module Manufacturing Date Week	xx	xx	xx
95	Module Serial Number (1)	xx	xx	xx
96	Module Serial Number (2)	xx	xx	xx
97	Module Serial Number (3)	xx	xx	xx
98	Module Serial Number (4)	xx	xx	xx
99-127	not used	00	00	00

Table 15 SPD Codes for HYS72D1285[20/21]GR[–7F/7]–B, HYS72D128521GR–8

	Part Number & Organization	HYS72D128520GR–7–B	HYS72D128520GR–7F–B	HYS72D128521GR–8–B	HYS72D128521GR–7–B	HYS72D128521GR–7F–B
		×72	×72	×72	×72	×72
		2 Ranks	2 Ranks	2 Ranks	2 Ranks	2 Ranks
		reg	reg	reg	reg	reg
	Label Code	PC2100R-20330-N	PC2100R-20220-N	PC1600R-20220-N	PC2100R-20330-N	PC2100R-20220-N
	Jedec SPD Revision					
Byte#	**Description**	**HEX**	**HEX**	**HEX**	**HEX**	**HEX**
0	Programmed SPD Bytes in E2PROM	80	80	80	80	80
1	Total number of Bytes in E2PROM	08	08	08	08	08
2	Memory Type (DDR = 07h)	07	07	07	07	07
3	Number of Row Addresses	0D	0D	0D	0D	0D
4	Number of Column Addresses	0B	0B	0B	0B	0B
5	Number of DIMM Ranks	02	02	02	02	02
6	Data Width (LSB)	48	48	48	48	48
7	Data Width (MSB)	00	00	00	00	00
8	Interface Voltage Levels	04	04	04	04	04
9	tCK @ CLmax (Byte 18) [ns]	70	70	80	70	70
10	tAC SDRAM @ CLmax (Byte 18) [ns]	75	75	80	75	75
11	Error Correction Support	02	02	02	02	02
12	Refresh Rate	82	82	82	82	82
13	Primary SDRAM Width	04	04	04	04	04
14	Error Checking SDRAM Width	04	04	04	04	04
15	tCCD [cycles]	01	01	01	01	01
16	Burst Length Supported	0E	0E	0E	0E	0E
17	Number of Banks on SDRAM Device	04	04	04	04	04
18	CAS Latency	0C	0C	0C	0C	0C
19	CS Latency	01	01	01	01	01
20	Write Latency	02	02	02	02	02
21	DIMM Attributes	26	26	26	26	26
22	Component Attributes	C0	C0	C0	C0	C0
23	tCK @ CLmax -0.5 (Byte 18) [ns]	75	75	A0	75	75
24	tAC SDRAM @ CLmax -0.5 [ns]	75	75	80	75	75
25	tCK @ CLmax -1 (Byte 18) [ns]	00	00	00	00	00
26	tAC SDRAM @ CLmax -1 [ns]	00	00	00	00	00

Table 15 SPD Codes for HYS72D1285[20/21]GR[–7F/7]–B, HYS72D128521GR–8

	Part Number & Organization	HYS72D128520GR–7–B	HYS72D128520GR–7F–B	HYS72D128521GR–8–B	HYS72D128521GR–7–B	HYS72D128521GR–7F–B
		×72	×72	×72	×72	×72
		2 Ranks	2 Ranks	2 Ranks	2 Ranks	2 Ranks
		reg	reg	reg	reg	reg
	Label Code	PC2100R-20330-N	PC2100R-20220-N	PC1600R-20220-N	PC2100R-20330-N	PC2100R-20220-N
	Jedec SPD Revision					
Byte#	Description	HEX	HEX	HEX	HEX	HEX
27	tRPmin [ns]	50	3C	50	50	3C
28	tRRDmin [ns]	3C	3C	3C	3C	3C
29	tRCDmin [ns]	50	3C	50	50	3C
30	tRASmin [ns]	2D	2D	32	2D	2D
31	Module Density per Rank	80	80	80	80	80
32	tAS, tCS [ns]	90	90	B0	90	90
33	tAH, TCH [ns]	90	90	B0	90	90
34	tDS [ns]	50	50	60	50	50
35	tDH [ns]	50	50	60	50	50
36	not used	00	00	00	00	00
37	not used	00	00	00	00	00
38	not used	00	00	00	00	00
39	not used	00	00	00	00	00
40	not used	00	00	00	00	00
41	tRCmin [ns]	41	3C	46	41	3C
42	tRFCmin [ns]	4B	4B	50	4B	4B
43	tCKmax [ns]	30	30	30	30	30
44	tDQSQmax [ns]	32	32	3C	32	32
45	tQHSmax [ns]	75	75	A0	75	75
46	not used	00	00	00	00	00
47	DIMM PCB Height	00	00	00	00	00
48-61	not used	00	00	00	00	00
62	SPD Revision	00	00	00	00	00
63	Checksum of Byte 0-62	04	D7	F9	04	D7
64	JEDEC ID Code of Infineon (1)	C1	C1	C1	C1	C1
65	JEDEC ID Code of Infineon (2)	49	49	49	49	49
66	JEDEC ID Code of Infineon (3)	4E	4E	4E	4E	4E

Table 15 SPD Codes for HYS72D1285[20/21]GR[–7F/7]–B, HYS72D128521GR–8

	Part Number & Organization	HYS72D128520GR–7–B	HYS72D128520GR–7F–B	HYS72D128521GR–8–B	HYS72D128521GR–7–B	HYS72D128521GR–7F–B
		×72	×72	×72	×72	×72
		2 Ranks	2 Ranks	2 Ranks	2 Ranks	2 Ranks
		reg	reg	reg	reg	reg
	Label Code	PC2100R-20330-N	PC2100R-20220-N	PC1600R-20220-N	PC2100R-20330-N	PC2100R-20220-N
	Jedec SPD Revision					
Byte#	**Description**	**HEX**	**HEX**	**HEX**	**HEX**	**HEX**
67	JEDEC ID Code of Infineon (4)	46	46	46	46	46
68	JEDEC ID Code of Infineon (5)	49	49	49	49	49
69	JEDEC ID Code of Infineon (6)	4E	4E	4E	4E	4E
70	JEDEC ID Code of Infineon (7)	45	45	45	45	45
71	JEDEC ID Code of Infineon (8)	4F	4F	4F	4F	4F
72	Module Manufacturer Location	xx	xx	xx	xx	xx
73	Part Number, Char 1	37	37	37	37	37
74	Part Number, Char 2	32	32	32	32	32
75	Part Number, Char 3	44	44	44	44	44
76	Part Number, Char 4	31	31	31	31	31
77	Part Number, Char 5	32	32	32	32	32
78	Part Number, Char 6	38	38	38	38	38
79	Part Number, Char 7	35	35	35	35	35
80	Part Number, Char 8	32	32	32	32	32
81	Part Number, Char 9	30	31	31	31	31
82	Part Number, Char 10	47	47	47	47	47
83	Part Number, Char 11	52	52	52	52	52
84	Part Number, Char 12	37	37	38	37	37
85	Part Number, Char 13	42	46	42	42	46
86	Part Number, Char 14	20	42	20	20	42
87	Part Number, Char 15	20	20	20	20	20
88	Part Number, Char 16	20	20	20	20	20
89	Part Number, Char 17	20	20	20	20	20
90	Part Number, Char 18	20	20	20	20	20
91	Module Revision Code	xx	xx	xx	xx	xx
92	Test Program Revision Code	xx	xx	xx	xx	xx
93	Module Manufacturing Date Year	xx	xx	xx	xx	xx

Table 15 SPD Codes for HYS72D1285[20/21]GR[–7F/7]–B, HYS72D128521GR–8

	Part Number & Organization	HYS72D128520GR–7–B	HYS72D128520GR–7F–B	HYS72D128521GR–8–B	HYS72D128521GR–7–B	HYS72D128521GR–7F–B
		×72	×72	×72	×72	×72
		2 Ranks	2 Ranks	2 Ranks	2 Ranks	2 Ranks
		reg	reg	reg	reg	reg
	Label Code	PC2100R-20330-N	PC2100R-20220-N	PC1600R-20220-N	PC2100R-20330-N	PC2100R-20220-N
	Jedec SPD Revision					
Byte#	**Description**	**HEX**	**HEX**	**HEX**	**HEX**	**HEX**
94	Module Manufacturing Date Week	xx	xx	xx	xx	xx
95	Module Serial Number (1)	xx	xx	xx	xx	xx
96	Module Serial Number (2)	xx	xx	xx	xx	xx
97	Module Serial Number (3)	xx	xx	xx	xx	xx
98	Module Serial Number (4)	xx	xx	xx	xx	xx
99-127	not used	00	00	00	00	00

5 Package Outlines

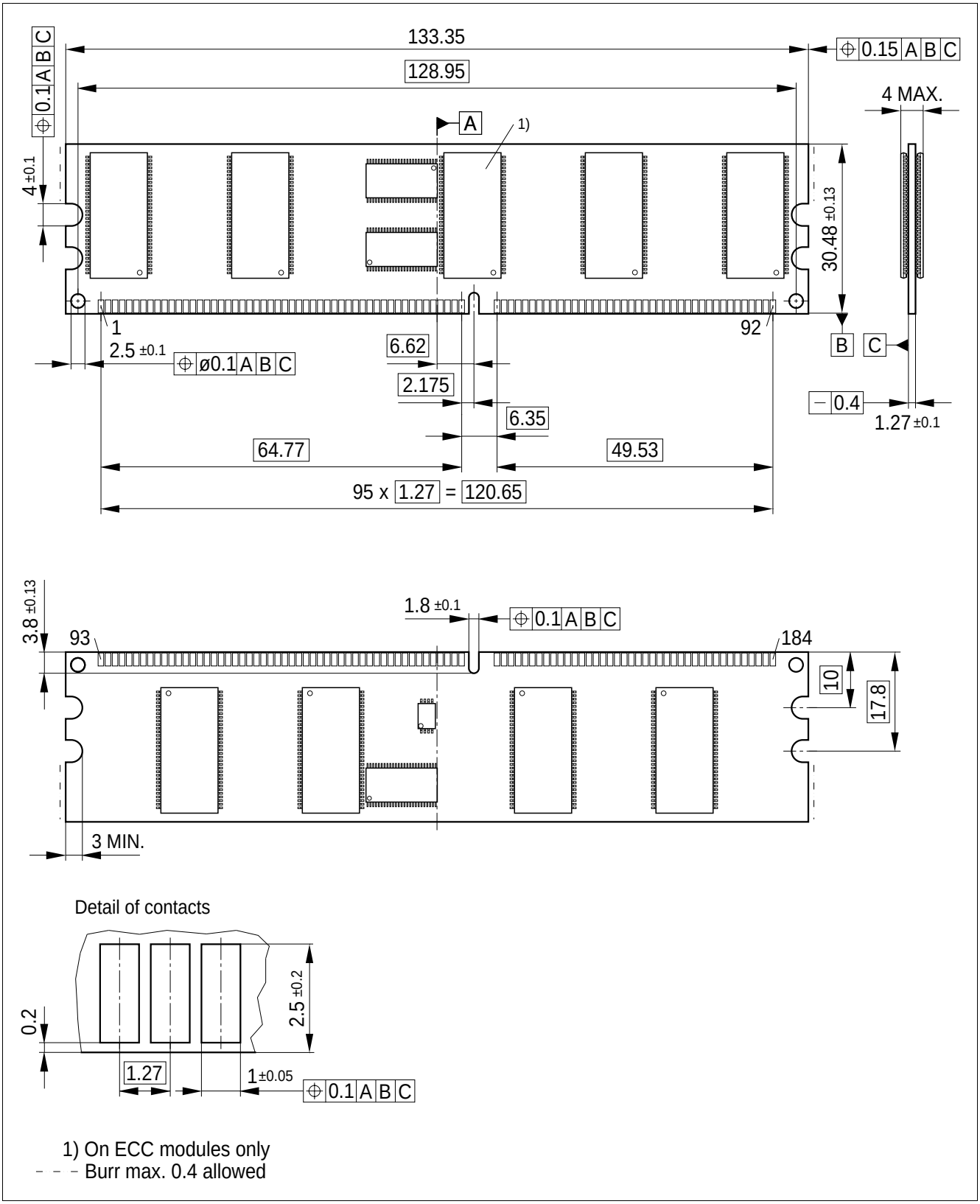
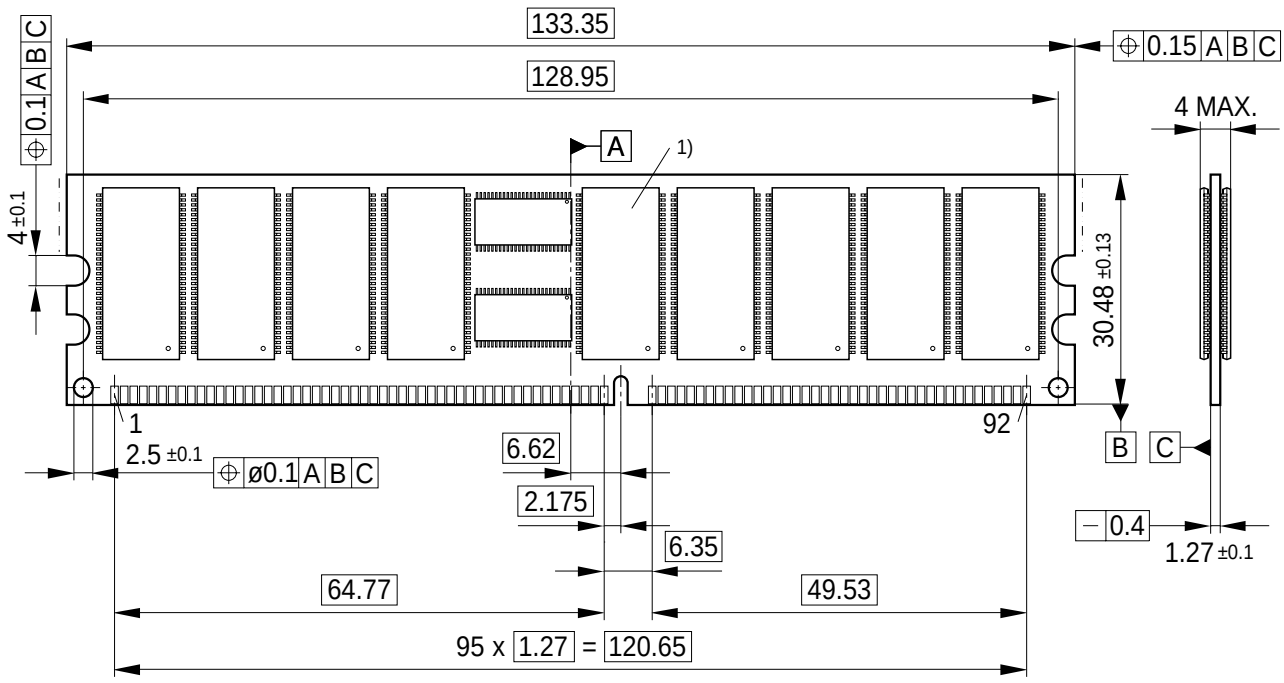
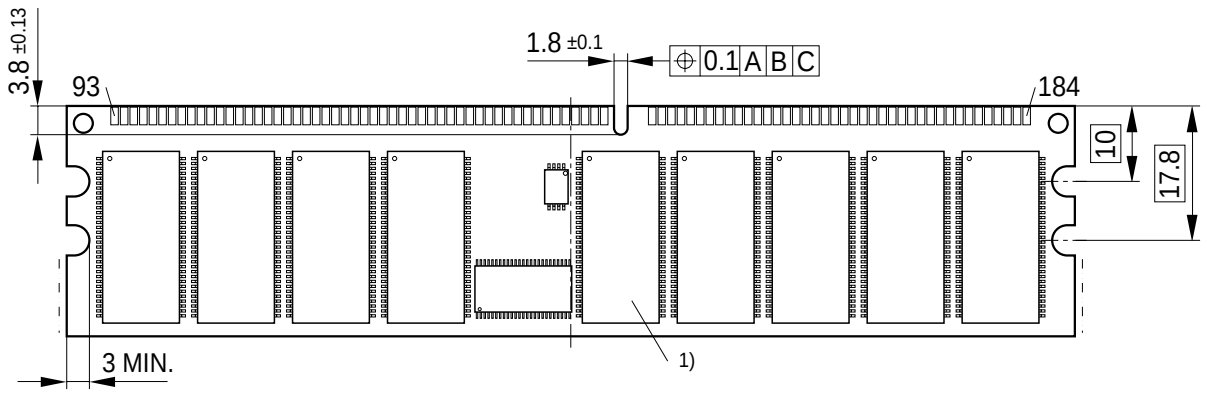
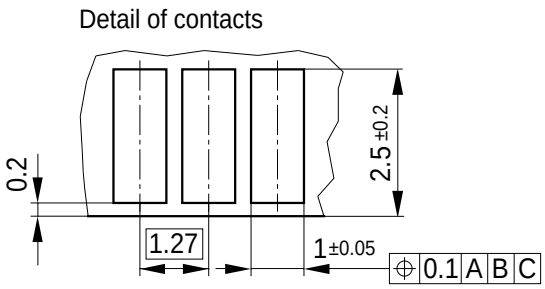


Figure 4 Package Outlines Raw Card L (L-DIM-184-13)







1) On ECC modules only
– – – Burr max. 0.4 allowed

Figure 5 Package Outlines Raw Card M (L-DIM-184-12)

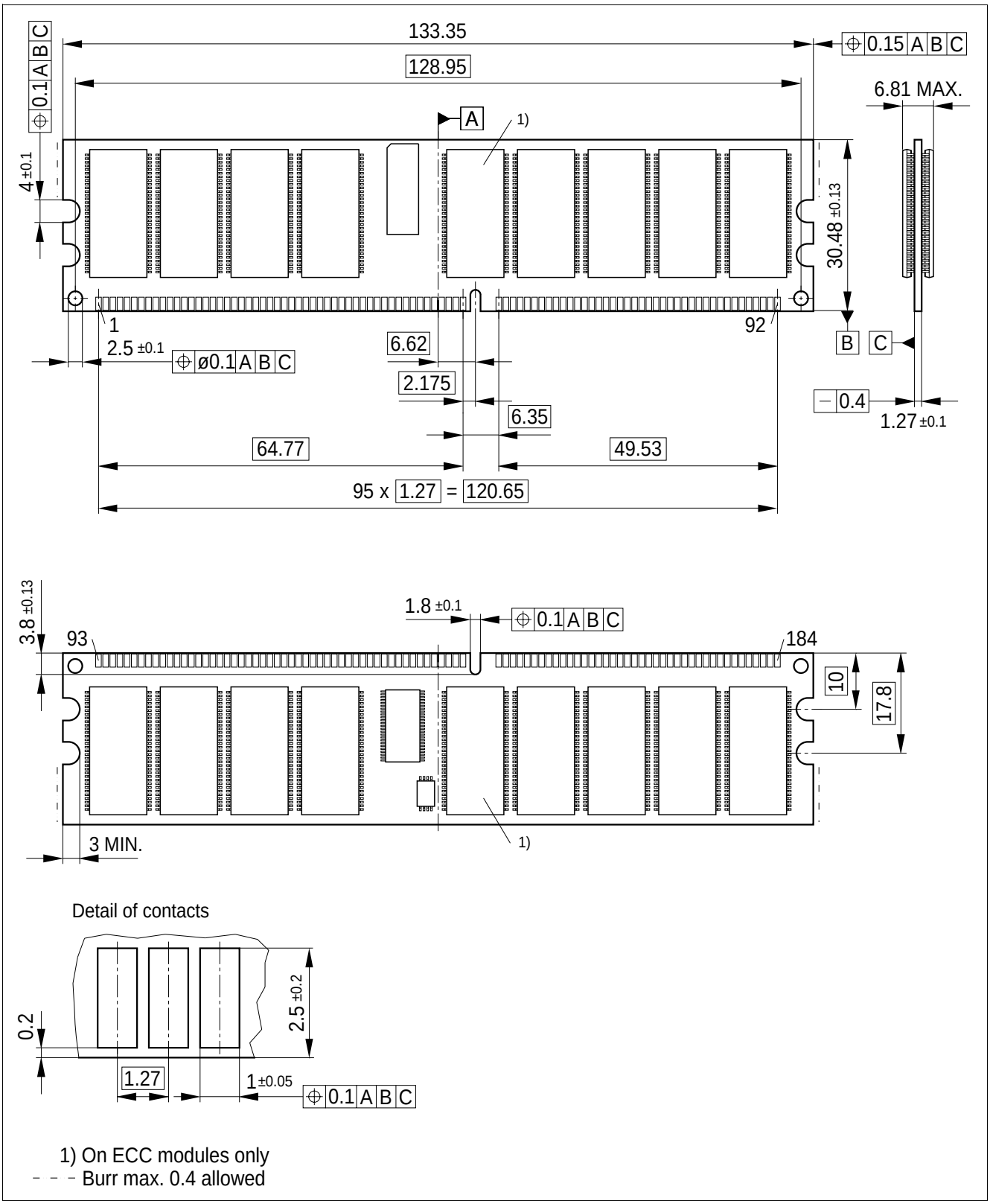


Figure 6 Package Outlines Raw Card N (L-DIM-184-14)

6 Application Note

Power Up and Power Management on DDR Registered DIMMs (according to JEDEC ballot JC-42.5 Item 1173)

184-pin Double Data Rate (DDR) Registered DIMMs include two new features to facilitate controlled power-up and to minimize power consumption during low power mode. One feature is externally controlled via a system-generated RESET signal; the second is based on module detection of the input clocks. These enhancements permit the modules to power up with SDRAM outputs in a High-Z state (eliminating risk of high current dissipations and/or dotted I/Os), and result in the powering-down of module support devices (registers and Phase-Locked Loop) when the memory is in Self-Refresh mode.

The new RESET pin controls power dissipation on the module's registers and ensures that CKE and other SDRAM inputs are maintained at a valid 'low' level during power-up and self refresh. When RESET is at a low level, all the register outputs are forced to a low level, and all differential register input receivers are powered down, resulting in very low register power consumption. The $\overline{\text{RESET}}$ pin, located on DIMM tab #10, is driven from the system as an asynchronous signal according to the attached details. Using this function also permits the system and DIMM clocks to be stopped during memory Self Refresh operation, while ensuring that the SDRAMs stay in Self Refresh mode.

Table 16 $\overline{\text{RESET}}$ Truth Table

Register Inputs				Register Outputs
$\overline{\text{RESET}}$	CK	$\overline{\text{CK}}$	Data in (D)	Data out (Q)
H	Rising	Falling	H	H
H	Rising	Falling	L	L
H	L or H	L or H	X	Qo
H	High Z	High Z	X	Illegal input conditions
L	X or Hi-Z	X or Hi-Z	X or Hi-Z	L
X: Don't care, Hi-Z: High Impedance, Qo: Data latched at the previous of CK rising and $\overline{\text{CK}}$ falling				

As described in the table above, a low on the $\overline{\text{RESET}}$ input ensures that the Clock Enable (CKE) signal(s) are maintained low at the SDRAM pins (CKE being one of the 'Q' signals at the register output). Holding CKE low maintains a high impedance state on the SDRAM DQ, DQS and DM outputs — where they will remain until activated by a valid 'read' cycle. CKE low also maintains SDRAMs in Self Refresh mode when applicable.

The DDR PLL devices automatically detect clock activity above 20MHz. When an input clock frequency of 20MHz or greater is detected, the PLL begins operation and initiates clock frequency lock (the minimum operating frequency at which all specifications will be met is 95MHz). If the clock input frequency drops below 20MHz (actual detect frequency will vary by vendor), the PLL VCO (Voltage Controlled Oscillator) is stopped, outputs are made High-Z, and the differential inputs are powered down — resulting in a total PLL current consumption of less than 1mA. Use of this low power PLL function makes the use of the PLL $\overline{\text{RESET}}$ (or $\overline{\text{G}}$ pin) unnecessary, and it is tied inactive on the DIMM.

This application note describes the required and optional system sequences associated with the DDR Registered DIMM '$\overline{\text{RESET}}$' function. It is important to note that all references to CKE refer to both CKE0 and CKE1 for a 2-bank DIMM. Because $\overline{\text{RESET}}$ applies to all DIMM register devices, it is therefore not possible to uniquely control CKE to one physical DIMM bank through the use of the $\overline{\text{RESET}}$ pin.

Power-Up Sequence with $\overline{\text{RESET}}$ — Required

1. The system sets $\overline{\text{RESET}}$ at a valid low level.
   This is the preferred default state during power-up. This input condition forces all register outputs to a low state independent of the condition on the register inputs (data and clock), ensuring that CKE is at a stable low-level at the DDR SDRAMs.
2. The power supplies should be initialized according to the JEDEC-approved initialization sequence for DDR SDRAMs.
3. Stabilization of Clocks to the SDRAM
   The system must drive clocks to the application frequency (PLL operation is not assured until the input clock reaches 20 MHz). Stability of clocks at the SDRAMs will be affected by all applicable system clock devices, and time must be allotted to permit all clock devices to settle. Once a stable clock is received at the DIMM PLL, the required PLL stabilization time (assuming power to the DIMM is stable) is 100 microseconds. When a stable clock is present at the SDRAM input (driven from the PLL), the DDR SDRAM requires 200 µsec prior to SDRAM operation.
4. The system applies valid logic levels to the data inputs of the register (address and controls at the DIMM connector).
   CKE must be maintained low and all other inputs should be driven to a known state. In general these commands can be determined by the system designer. One option is to apply an SDRAM ‘NOP’ command (with CKE low), as this is the first command defined by the JEDEC initialization sequence (ideally this would be a ‘NOP Deselect’ command). A second option is to apply low levels on all of the register inputs to be consistent with the state of the register outputs.
5. The system switches $\overline{\text{RESET}}$ to a logic ‘high’ level.
   The SDRAM is now functional and prepared to receive commands. Since the $\overline{\text{RESET}}$ signal is asynchronous, setting the $\overline{\text{RESET}}$ timing in relation to a specific clock edge is not required (during this period, register inputs must remain stable).
6. The system must maintain stable register inputs until normal register operation is attained.
   The registers have an activation time that allows their clock receivers, data input receivers, and output drivers sufficient time to be turned on and become stable. During this time the system must maintain the valid logic levels described in step 5. It is also a functional requirement that the registers maintain a low state at the CKE outputs to guarantee that the DDR SDRAMs continue to receive a low level on CKE. Register activation time (t (ACT)), from asynchronous switching of $\overline{\text{RESET}}$ from low to high until the registers are stable and ready to accept an input signal, is specified in the register and DIMM do-umentation.
7. The system can begin the JEDEC-defined DDR SDRAM power-up sequence (according to the JEDEC-pproved initialization sequence).

Self Refresh Entry ($\overline{\text{RESET}}$ low, clocks powered off) — Optional

Self Refresh can be used to retain data in DDR SDRAM DIMMs even if the rest of the system is powered down and the clocks are off. This mode allows the DDR SDRAMs on the DIMM to retain data without external clocking. Self Refresh mode is an ideal time to utilize the $\overline{\text{RESET}}$ pin, as this can reduce register power consumption ($\overline{\text{RESET}}$ low deactivates register CK and CK, data input receivers, and data output drivers).

1. 1. The system applies Self Refresh entry command.
   (CKE→Low, $\overline{\text{CS}}$→Low, $\overline{\text{RAS}}$ → Low, $\overline{\text{CAS}}$→ Low, $\overline{\text{WE}}$→ High)

Note: Note: The commands reach the DDR SDRAM one clock later due to the additional register pipelining on a Registered DIMM. After this command is issued to the SDRAM, all of the address and control and clock input conditions to the SDRAM are Don’t Cares— with the exception of CKE.

2. The system sets $\overline{\text{RESET}}$ at a valid low level.
   This input condition forces all register outputs to a low state, independent of the condition on the registerm inputs (data and clock), and ensures that CKE, and all other control and address signals, are a stable low-level at the DDR SDRAMs. Since the $\overline{\text{RESET}}$ signal is asynchronous, setting the $\overline{\text{RESET}}$ timing in relation to a specific clock edge is not required.
3. The system turns off clock inputs to the DIMM. (Optional)
   a. In order to reduce DIMM PLL current, the clock inputs to the DIMM are turned off, resulting in High-Z clock

inputs to both the SDRAMs and the registers. This must be done after the RESET deactivate time of the register (t (INACT). The deactivate time defines the time in which the clocks and the control and address signals must maintain valid levels after RESET low has been applied and is specified in the register and DIMM documentation.
b.The system may release DIMM address and control inputs to High-Z.
This can be done after the RESET deactivate time of the register. The deactivate time defines the time in which the clocks and the control and the address signals must maintain valid levels after RESET low has been applied. It is highly recommended that CKE continue to remain low during this operation.

4. The DIMM is in lowest power Self Refresh mode.

Self Refresh Exit (RESET low, clocks powered off) — Optional

1. Stabilization of Clocks to the SDRAM.
   The system must drive clocks to the application frequency (PLL operation is not assured until the input clock reaches ~20MHz). Stability of clocks at the SDRAMs will be affected by all applicable system clock devices, and time must be allotted to permit all clock devices to settle. Once a stable clock is received at the DIMM PLL, the required PLL stabilization time (assuming power to the DIMM is stable) is 100 microseconds.
2. The system applies valid logic levels to the data inputs of the register (address and controls at the DIMM connector).
   CKE must be maintained low and all other inputs should be driven to a known state. In general these commands can be determined by the system designer. One option is to apply an SDRAM ‘NOP’ command (with CKE low), as this is the first command defined by the JEDEC Self Refresh Exit sequence (ideally this would be a ‘NOP Deselect’ command). A second option is to apply low levels on all of the register inputs, to be consistent with the state of the register outputs.
3. The system switches RESET to a logic ‘high’ level.
   The SDRAM is now functional and prepared to receive commands. Since the RESET signal is asynchronous, RESET timing relationship to a specific clock edge is not required (during this period, register inputs must remain stable).
4. The system must maintain stable register inputs until normal register operation is attained.
   The registers have an activation time that allows the clock receivers, input receivers, and output drivers sufficient time to be turned on and become stable. During this time the system must maintain the valid logic levels described in Step 2. It is also a functional requirement that the registers maintain a low state at the CKE outputs to guarantee that the DDR SDRAMs continue to receive a low level on CKE. Register activation time (t (ACT)), from asynchronous switching of RESET from low to high until the registers are stable and ready to accept an input signal, is specified in the register and DIMM do-umentation.
5. System can begin the JEDEC-defined DDR SDRAM Self Refresh Exit Procedure.

Self Refresh Entry (RESET low, clocks running) — Optional

Although keeping the clocks running increases power consumption from the on-DIMM PLL during self refresh, this is an alternate operating mode for these DIMMs.

1. 1. System enters Self Refresh entry command.
   (CKE→ Low, CS→ Low, RAS→ Low, CAS→ Low, WE→ High)

Note: Note: The commands reach the DDR SDRAM one clock later due to the additional register pipelining on a Registered DIMM. After this command is issued to the SDRAM, all of the address and control and clock input conditions to the SDRAM are Don’t Cares — with the exception of CKE.

2. The system sets RESET at a valid low level.
   This input condition forces all register outputs to a low state, independent of the condition on the data and clock register inputs, and ensures that CKE is a stable low-level at the DDR SDRAMs.
3. The system may release DIMM address and control inputs to High-Z.
   This can be done after the RESET deactivate time of the register (t (INACT)). The deactivate time describes the time in which the clocks and the control and the address signals must maintain valid levels after RESET low has been applied. It is highly recommended that CKE continue to remain low during the operation.
4. The DIMM is in a low power, Self Refresh mode.

Self Refresh Exit ($\overline{\text{RESET}}$ low, clocks running) — Optional

1. The system applies valid logic levels to the data inputs of the register (address and controls at the DIMM connector). CKE must be maintained low and all other inputs should be driven to a known state. In general these commands can be determined by the system designer. One option is to apply an SDRAM ‘NOP’ command (with CKE low), as this is the first command defined by the Self Refresh Exit sequence (ideally this would be a ‘NOP Deselect’ command). A second option is to apply low levels on all of the register inputs to be consistent with the state of the register outputs.
2. The system switches $\overline{\text{RESET}}$ to a logic 'high' level.
   The SDRAM is now functional and prepared to receive commands. Since the $\overline{\text{RESET}}$ signal is asynchronous, it does not need to be tied to a particular clock edge (during this period, register inputs must continue to remain stable).
3. The system must maintain stable register inputs until normal register operation is attained.
   The registers have an activation time that allows the clock receivers, input receivers, and output drivers sufficient time to be turned on and become stable. During this time the system must maintain the valid logic levels described in Step 1. It is also a functional requirement that the registers maintain a low state at the CKE outputs in order to guarantee that the DDR SDRAMs continue to receive a low level on CKE. This activation time, from asynchronous switching of $\overline{\text{RESET}}$ from low to high, until the registers are stable and ready to accept an input signal, is t (ACT) as specified in the register and DIMM documentation.
4. The system can begin JEDEC defined DDR SDRAM Self Refresh Exit Procedure.

Self Refresh Entry/Exit ($\overline{\text{RESET}}$ high, clocks running) — Optional

As this sequence does not involve the use of the $\overline{\text{RESET}}$ function, the JEDEC standard SDRAM specification explains in detail the method for entering and exiting Self Refresh for this case.

Self Refresh Entry ($\overline{\text{RESET}}$ high, clocks powered off) — Not Permissible

In order to maintain a valid low level on the register output, it is required that either the clocks be running and the system drive a low level on CKE, or the clocks are powered off and $\overline{\text{RESET}}$ is asserted low according to the sequence defined in this application note. In the case where $\overline{\text{RESET}}$ remains high and the clocks are powered off, the PLL drives a High-Z clock input into the register clock input. Without the low level on $\overline{\text{RESET}}$ an unknown DIMM state will result.

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