

NTMFS4120N

Power MOSFET

30 V, 31 A, Single N-Channel,
SO-8 Flat Lead

Features

- Low $R_{DS(on)}$
- Optimized Gate Charge
- Low Inductance SO-8 Package
- These are Pb-Free Devices

Applications

- Notebooks, Graphics Cards
- DC-DC Converters
- Synchronous Rectification

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Value	Unit			
Drain-to-Source Voltage	V_{DSS}	30	V			
Gate-to-Source Voltage	V_{GS}	± 20	V			
Continuous Drain Current (Note 1)	Steady State	$T_A = 25^\circ\text{C}$	I_D	18	A	
		$T_A = 85^\circ\text{C}$				13
		$t \leq 10 \text{ s}$				$T_A = 25^\circ\text{C}$
Power Dissipation (Note 1)	Steady State	$T_A = 25^\circ\text{C}$	P_D	2.2	W	
				$t \leq 10 \text{ s}$		6.9
Continuous Drain Current (Note 2)	Steady State	$T_A = 25^\circ\text{C}$	I_D	11	A	
		$T_A = 85^\circ\text{C}$		8.0		
		$T_A = 25^\circ\text{C}$		P_D		0.9
Power Dissipation (Note 2)						
Pulsed Drain Current	$t_p = 10 \mu\text{s}$	I_{DM}	94	A		
Operating Junction and Storage Temperature	T_J, T_{stg}	-55 to 150	$^\circ\text{C}$			
Source Current (Body Diode)	I_S	7.0	A			
Single Pulse Drain-to-Source Avalanche Energy ($V_{DD} = 30 \text{ V}$, $V_{GS} = 10 \text{ V}$, $I_{PK} = 30 \text{ A}$, $L = 1 \text{ mH}$, $R_G = 25 \Omega$)	E_{AS}	450	mJ			
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)	T_L	260	$^\circ\text{C}$			

THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Junction-to-Case - Steady State	$R_{\theta JC}$	1.7	$^\circ\text{C/W}$
Junction-to-Ambient - Steady State (Note 1)	$R_{\theta JA}$	55.8	
Junction-to-Ambient - $t \leq 10 \text{ s}$ (Note 1)	$R_{\theta JA}$	18	
Junction-to-Ambient - Steady State (Note 2)	$R_{\theta JA}$	139.1	

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

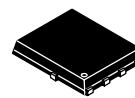
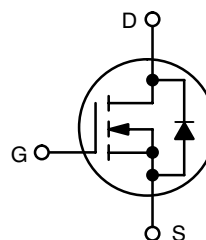
1. Surface mounted on FR4 board using 1 in sq pad size (Cu area = 1.127 in sq [1 oz] including traces).
2. Surface mounted on FR4 board using the minimum recommended pad size (Cu area = 1.0 in sq).



ON Semiconductor®

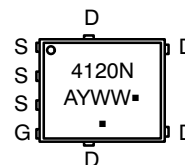
<http://onsemi.com>

$V_{(BR)DSS}$	$R_{DS(on)}$ Typ	I_D Max (Note 1)
30 V	3.5 m Ω @ 10 V	31 A
	4.2 m Ω @ 4.5 V	



SO-8 FLAT LEAD
CASE 488AA
STYLE 1

MARKING DIAGRAM



4120N = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb-Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

Device	Package	Shipping†
NTMFS4120NT1G	SO-8 FL (Pb-Free)	1500 Tape & Reel
NTMFS4120NT3G	SO-8 FL (Pb-Free)	5000 Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

NTMFS4120N

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	30			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$			21		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	$V_{GS} = 0\text{ V}, V_{DS} = 24\text{ V}$	$T_J = 25^\circ\text{C}$		1.0	μA
			$T_J = 125^\circ\text{C}$		10	
Gate-to-Source Leakage Current	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = 20\text{ V}$			100	nA

ON CHARACTERISTICS (Note 3)

Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = 250\ \mu\text{A}$	1.0		2.5	V
Negative Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$			7.4		mV/°C
Drain-to-Source On Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 26\text{ A}$		3.5	4.5	m Ω
		$V_{GS} = 4.5\text{ V}, I_D = 24\text{ A}$		4.2	5.5	
Forward Transconductance	g_{FS}	$V_{DS} = 15\text{ V}, I_D = 26\text{ A}$		35		S

CHARGES, CAPACITANCES AND GATE RESISTANCE

Input Capacitance	C_{ISS}	$V_{GS} = 0\text{ V}, f = 1.0\text{ MHz}, V_{DS} = 24\text{ V}$		3600		pF
Output Capacitance	C_{OSS}			640		
Reverse Transfer Capacitance	C_{RSS}			380		
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 4.5\text{ V}, V_{DS} = 15\text{ V}, I_D = 24\text{ A}$		33	50	nC
Threshold Gate Charge	$Q_{G(TH)}$			4.4		
Gate-to-Source Charge	Q_{GS}			13		
Gate-to-Drain Charge	Q_{GD}			14		
Gate Resistance	R_G			1.0		

SWITCHING CHARACTERISTICS (Note 4)

Turn-On Delay Time	$t_{d(ON)}$	$V_{GS} = 4.5\text{ V}, V_{DS} = 15\text{ V}, I_D = 1.0\text{ A}, R_G = 3.0\ \Omega$		24		ns
Rise Time	t_r			32		
Turn-Off Delay Time	$t_{d(OFF)}$			27		
Fall Time	t_f			31		

DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	V_{SD}	$V_{GS} = 0\text{ V}, I_S = 6.0\text{ A}$	$T_J = 25^\circ\text{C}$		0.74	1.0	V
			$T_J = 125^\circ\text{C}$		0.6		
Reverse Recovery Time	t_{RR}	$V_{GS} = 0\text{ V}, dI_S/dt = 100\text{ A}/\mu\text{s}, I_S = 6.0\text{ A}$		36		ns	
Charge Time	t_a			18			
Discharge Time	t_b			18			
Reverse Recovery Charge	Q_{RR}			34			nC

3. Pulse Test: Pulse Width $\leq 300\ \mu\text{s}$, Duty Cycle $\leq 2\%$.

4. Switching characteristics are independent of operating junction temperatures.

TYPICAL PERFORMANCE CURVES

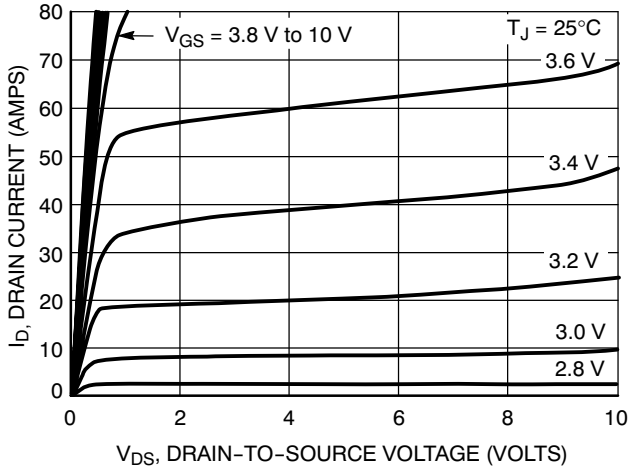


Figure 1. On-Region Characteristics

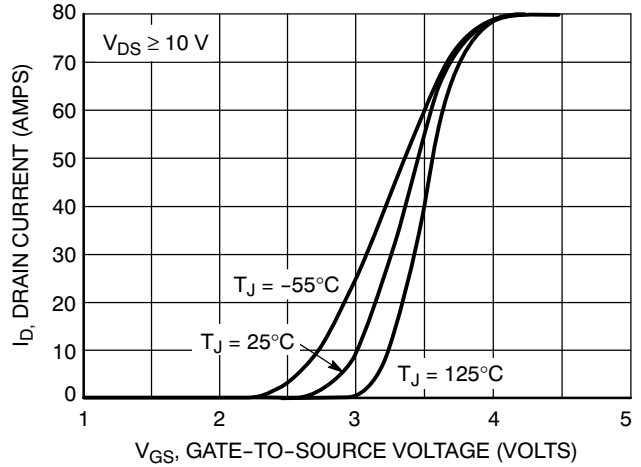


Figure 2. Transfer Characteristics

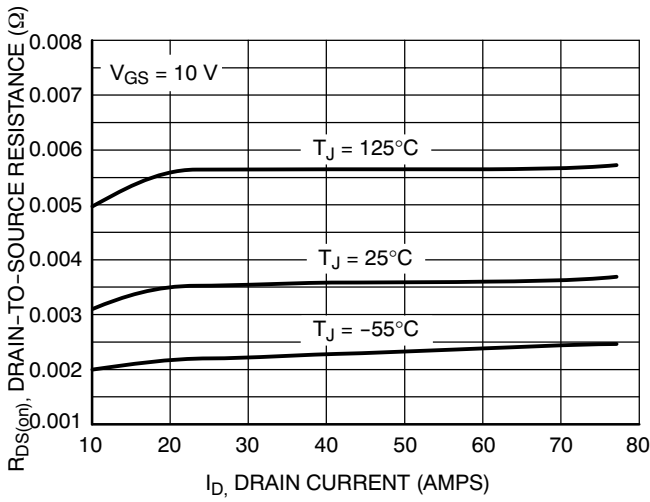


Figure 3. On-Resistance vs. Drain Current and Temperature

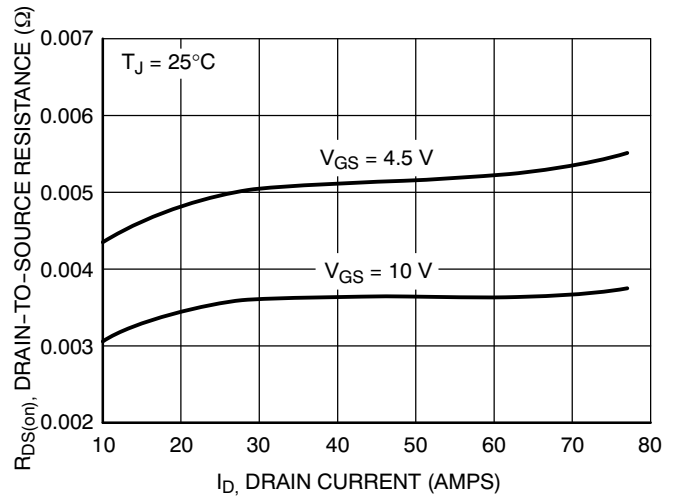


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

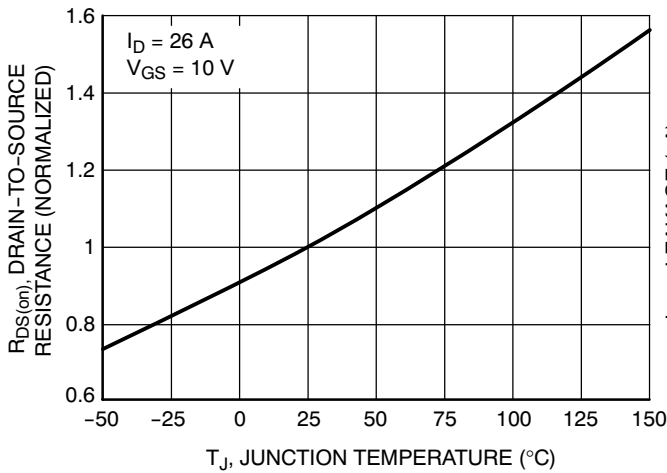


Figure 5. On-Resistance Variation with Temperature

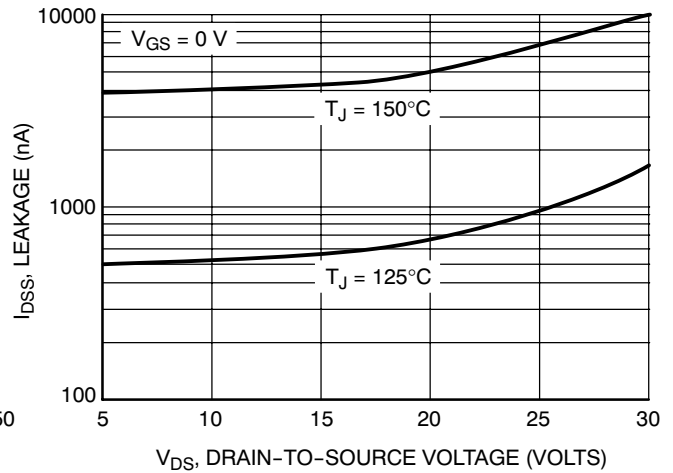


Figure 6. Drain-to-Source Leakage Current vs. Voltage

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TYPICAL PERFORMANCE CURVES

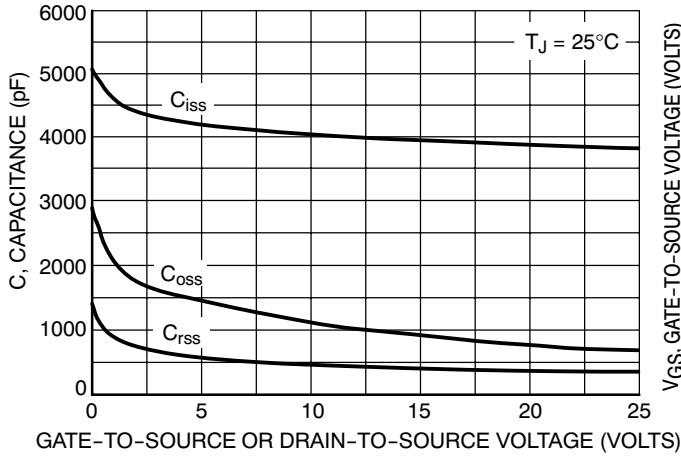


Figure 7. Capacitance Variation

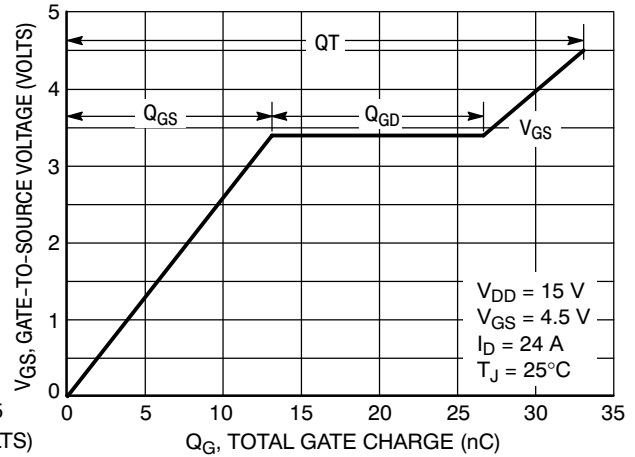


Figure 8. Gate-To-Source and Drain-To-Source Voltage vs. Total Charge

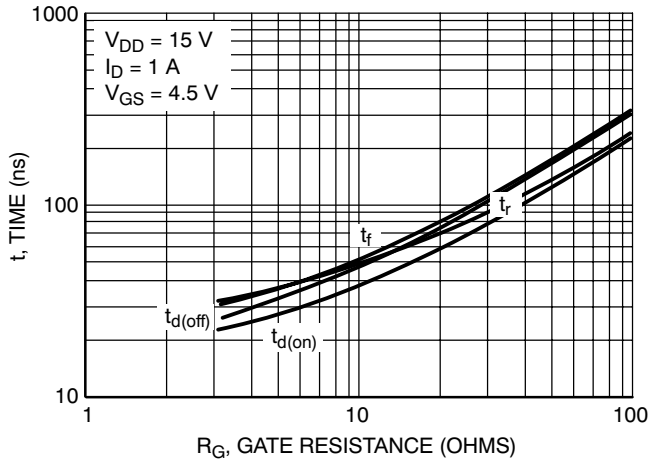


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

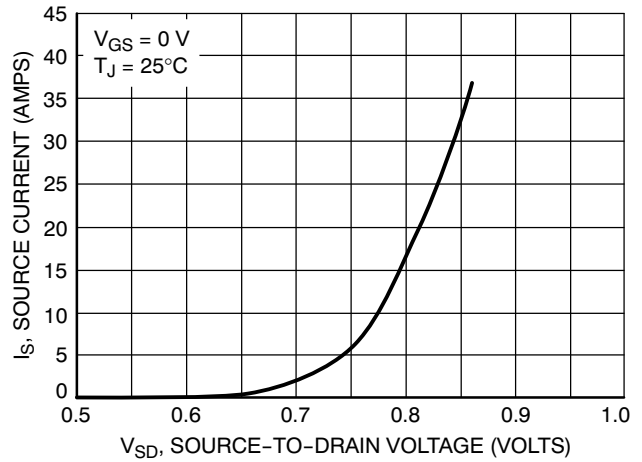


Figure 10. Diode Forward Voltage vs. Current

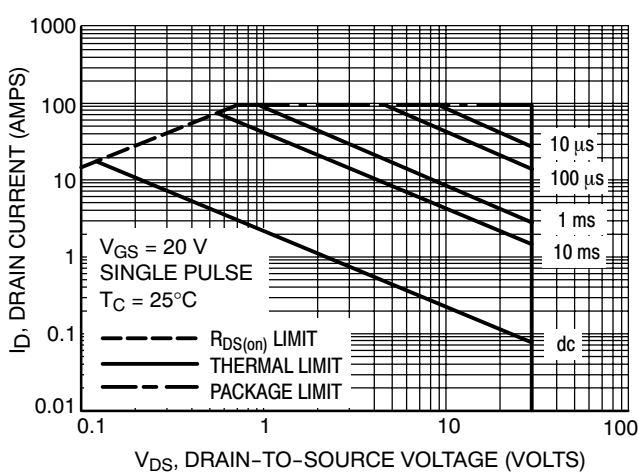


Figure 11. Maximum Rated Forward Biased Safe Operating Area

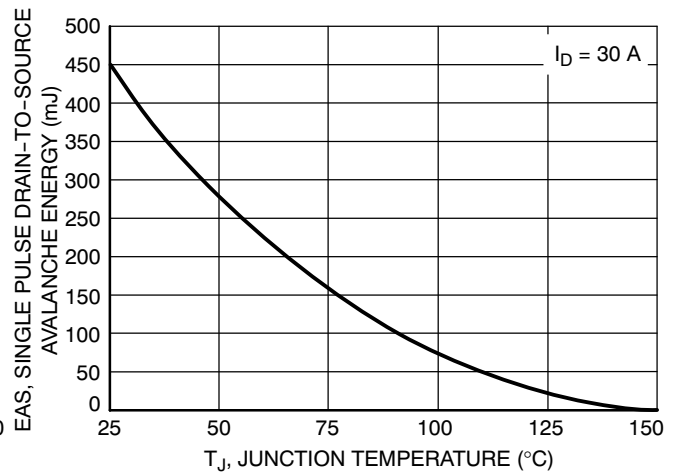


Figure 12. Maximum Avalanche Energy vs Starting Junction Temperature

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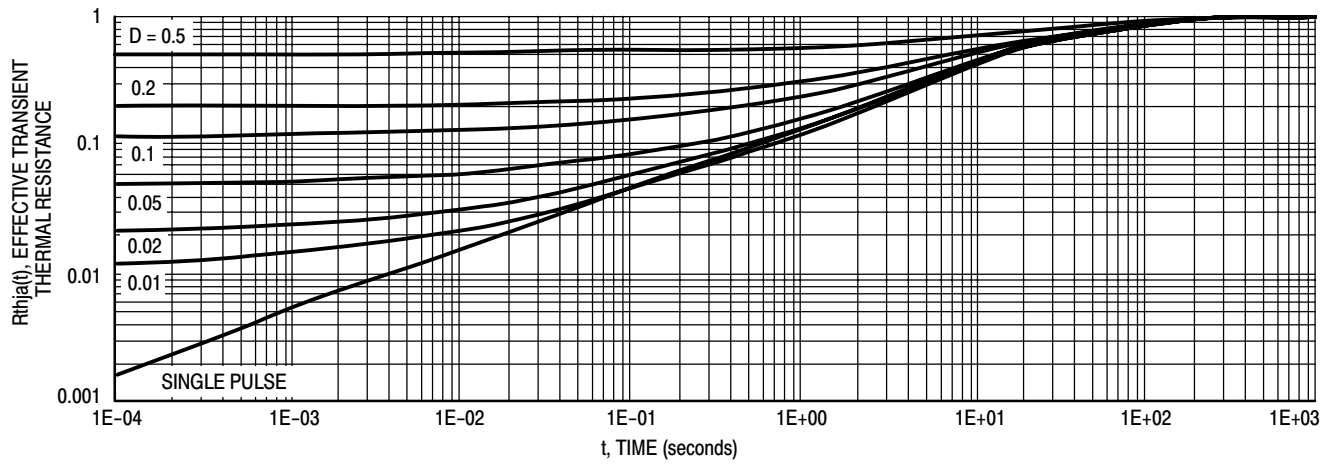
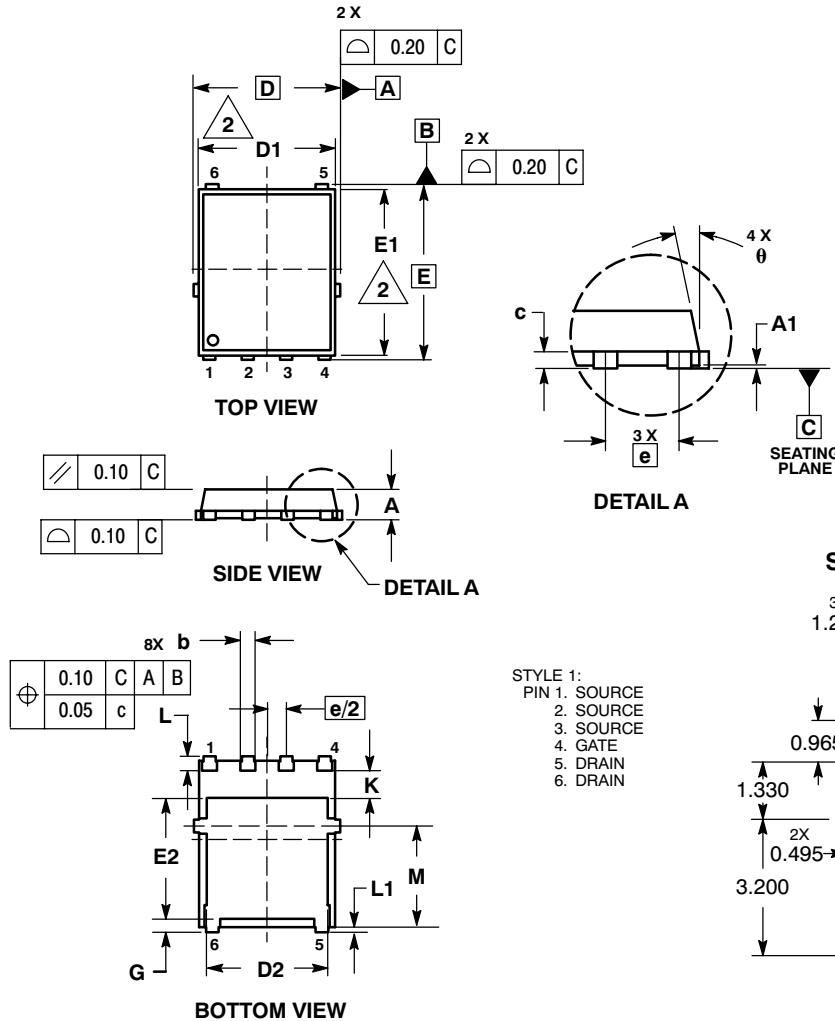


Figure 13. Thermal Response

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PACKAGE DIMENSIONS

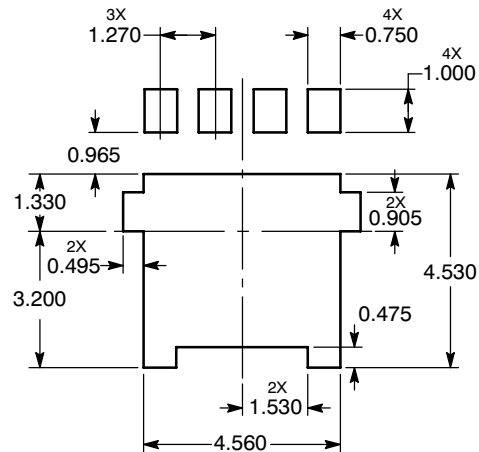
DFN6 5x6, 1.27P (SO8 FL)
CASE 488AA-01
ISSUE C



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
 2. CONTROLLING DIMENSION: MILLIMETER.
 3. DIMENSION D1 AND E1 DO NOT INCLUDE MOLD FLASH PROTRUSIONS OR GATE BURRS.

DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.90	1.00	1.10
A1	0.00	---	0.05
b	0.33	0.41	0.51
c	0.23	0.28	0.33
D	5.15 BSC		
D1	4.50	4.90	5.10
D2	3.50	---	4.22
E	6.15 BSC		
E1	5.50	5.80	6.10
E2	3.45	---	4.30
e	1.27 BSC		
G	0.51	0.61	0.71
K	0.51	---	---
L	0.51	0.61	0.71
L1	0.05	0.17	0.20
M	3.00	3.40	3.80
theta	0°	---	12°

SOLDERING FOOTPRINT*



- STYLE 1:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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