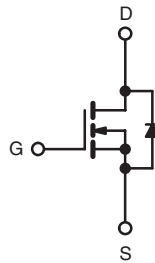
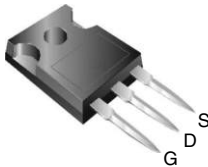


## Power MOSFET

PRODUCT SUMMARY	
$V_{DS}$ (V)	500
$R_{DS(on)}$ ( $\Omega$ )	$V_{GS} = 10\text{ V}$ 0.135
$Q_g$ (Max.) (nC)	190
$Q_{gs}$ (nC)	59
$Q_{gd}$ (nC)	84
Configuration	Single

TO-247



N-Channel MOSFET

### FEATURES

- Low Gate Charge  $Q_g$  Results in Simple Drive Requirement
- Improved Gate, Avalanche and Dynamic  $dV/dt$  Ruggedness
- Fully Characterized Capacitance and Avalanche Voltage and Current
- Low  $R_{DS(on)}$
- Lead (Pb)-free Available



RoHS\*  
COMPLIANT

### APPLICATIONS

- Switch Mode Power Supply (SMPS)
- Uninterruptible Power Supply
- High Speed Power Switching
- Hard Switching and High Frequency Circuits

ORDERING INFORMATION	
Package	TO-247
Lead (Pb)-free	IRFP32N50KPbF SiHFP32N50K-E3
SnPb	IRFP32N50K SiHFP32N50K


ABSOLUTE MAXIMUM RATINGS $T_C = 25\text{ }^\circ\text{C}$ , unless otherwise noted				
PARAMETER		SYMBOL	LIMIT	UNIT
Drain-Source Voltage		$V_{DS}$	500	V
Gate-Source Voltage		$V_{GS}$	$\pm 30$	
Continuous Drain Current	$V_{GS}$ at 10 V	$I_D$	$T_C = 25\text{ }^\circ\text{C}$	A
			$T_C = 100\text{ }^\circ\text{C}$	
Pulsed Drain Current <sup>a</sup>		$I_{DM}$	130	
Linear Derating Factor			3.7	$W/^\circ\text{C}$
Single Pulse Avalanche Energy <sup>b</sup>		$E_{AS}$	450	mJ
Repetitive Avalanche Current <sup>a</sup>		$I_{AR}$	32	A
Repetitive Avalanche Energy <sup>a</sup>		$E_{AR}$	46	mJ
Maximum Power Dissipation	$T_C = 25\text{ }^\circ\text{C}$	$P_D$	460	W
Peak Diode Recovery $dV/dt^c$		$dV/dt$	13	V/ns
Operating Junction and Storage Temperature Range		$T_J, T_{stg}$	- 55 to + 150	$^\circ\text{C}$
Soldering Recommendations (Peak Temperature)	for 10 s		300 <sup>d</sup>	
Mounting Torque	6-32 or M3 screw		10	lbf · in
			1.1	N · m

#### Notes

- Repetitive rating; pulse width limited by maximum junction temperature.
- Starting  $T_J = 25\text{ }^\circ\text{C}$ ,  $L = 0.87\text{ mH}$ ,  $R_G = 25\text{ }^\circ\Omega$ ,  $I_{AS} = 32\text{ A}$ .
- $I_{SD} \leq 32\text{ A}$ ,  $dI/dt \leq 197\text{ A}/\mu\text{s}$ ,  $V_{DD} \leq V_{DS}$ ,  $T_J \leq 150\text{ }^\circ\text{C}$ .
- 1.6 mm from case.

\* Pb containing terminations are not RoHS compliant, exemptions may apply from case.

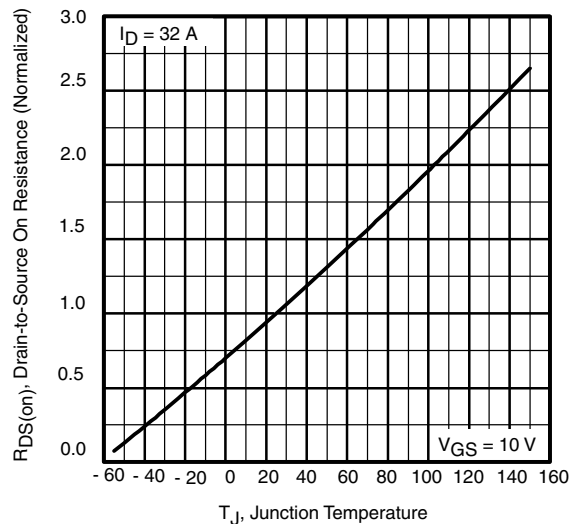
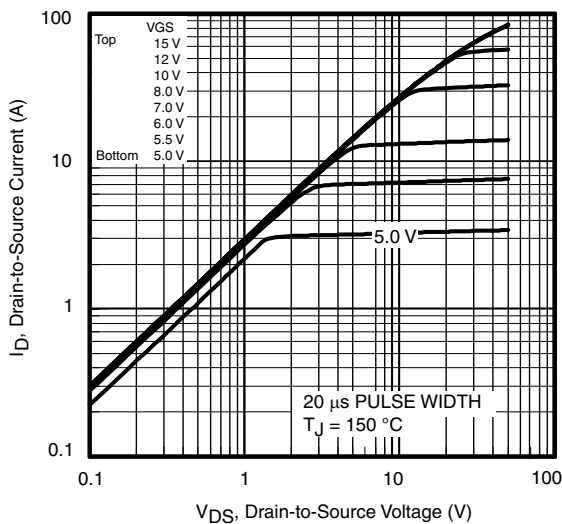
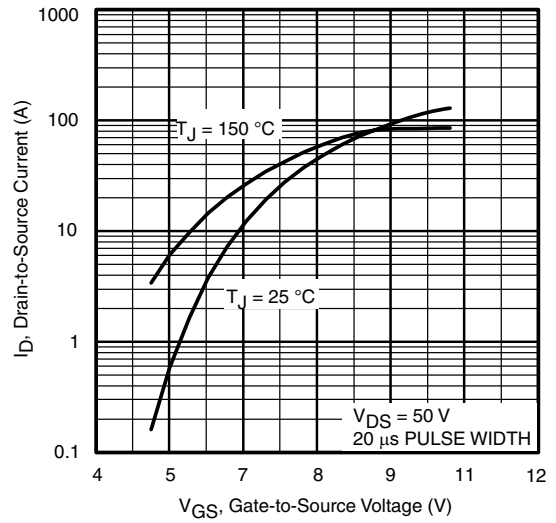
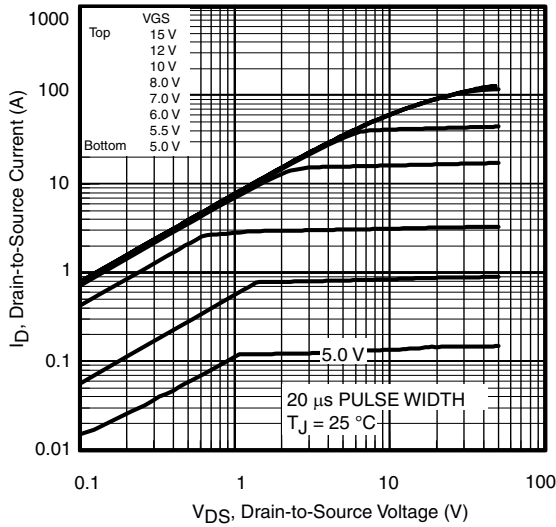
THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	$R_{thJA}$	-	40	°C/W
Case-to-Sink, Flat, Greased Surface	$R_{thCS}$	0.24	-	
Maximum Junction-to-Case (Drain)	$R_{thJC}$	-	0.26	

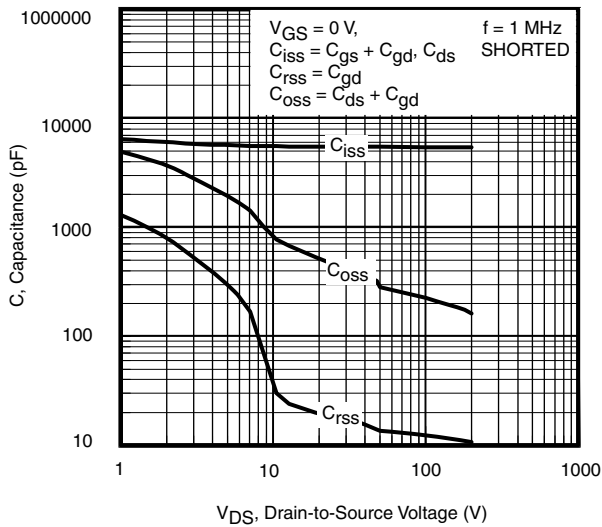
SPECIFICATIONS $T_J = 25\text{ }^\circ\text{C}$ , unless otherwise noted						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>Static</b>						
Drain-Source Breakdown Voltage	$V_{DS}$	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	500	-	-	V
$V_{DS}$ Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to $25\text{ }^\circ\text{C}$ , $I_D = 1\text{ mA}$	-	0.54	-	V/°C
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	3.0	-	5.0	V
Gate-Source Leakage	$I_{GSS}$	$V_{GS} = \pm 30\text{ V}$	-	-	$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 500\text{ V}, V_{GS} = 0\text{ V}$	-	-	50	$\mu\text{A}$
		$V_{DS} = 400\text{ V}, V_{GS} = 0\text{ V}, T_J = 150\text{ }^\circ\text{C}$	-	-	250	
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 32\text{ A}^b$	-	0.135	0.16	$\Omega$
Forward Transconductance	$g_{fs}$	$V_{DS} = 50\text{ V}, I_D = 32\text{ A}$	14	-	-	S
<b>Dynamic</b>						
Input Capacitance	$C_{iss}$	$V_{GS} = 0\text{ V}, V_{DS} = 25\text{ V}, f = 1.0\text{ MHz}$ , see fig. 5	-	5280	-	pF
Output Capacitance	$C_{oss}$		-	550	-	
Reverse Transfer Capacitance	$C_{rss}$		-	45	-	
Output Capacitance	$C_{oss}$	$V_{GS} = 0\text{ V}$	$V_{DS} = 1.0\text{ V}, f = 1.0\text{ MHz}$	-	5630	-
Effective Output Capacitance	$C_{oss\text{ eff.}}$		$V_{DS} = 400\text{ V}, f = 1.0\text{ MHz}$	-	155	-
Total Gate Charge	$Q_g$	$V_{GS} = 10\text{ V}, I_D = 32\text{ A}, V_{DS} = 400\text{ V}^b$	$V_{DS} = 0\text{ V to } 400\text{ V}^c$	-	265	-
Gate-Source Charge	$Q_{gs}$		-	-	190	nC
Gate-Drain Charge	$Q_{gd}$		-	-	59	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 250\text{ V}, I_D = 32\text{ A}, R_G = 4.3\text{ }\Omega, V_{GS} = 10\text{ V}^b$	-	28	-	ns
Rise Time	$t_r$		-	120	-	
Turn-Off Delay Time	$t_{d(off)}$		-	48	-	
Fall Time	$t_f$		-	54	-	
<b>Drain-Source Body Diode Characteristics</b>						
Continuous Source-Drain Diode Current	$I_S$	MOSFET symbol showing the integral reverse p - n junction diode 	-	-	32	A
Pulsed Diode Forward Current <sup>a</sup>	$I_{SM}$		-	-	130	
Body Diode Voltage	$V_{SD}$	$T_J = 25\text{ }^\circ\text{C}, I_S = 32\text{ A}, V_{GS} = 0\text{ V}^b$	-	-	1.5	V
Body Diode Reverse Recovery Time	$t_{rr}$	$T_J = 25\text{ }^\circ\text{C}, I_F = 32\text{ A}, dI/dt = 100\text{ A}/\mu\text{s}^b$	-	530	800	ns
Body Diode Reverse Recovery Charge	$Q_{rr}$		-	9.0	13.5	$\mu\text{C}$
Body Diode Reverse Recovery Current	$I_{RRM}$		-	30	-	A
Forward Turn-On Time	$t_{on}$	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S$ and $L_D$ )				

### Notes

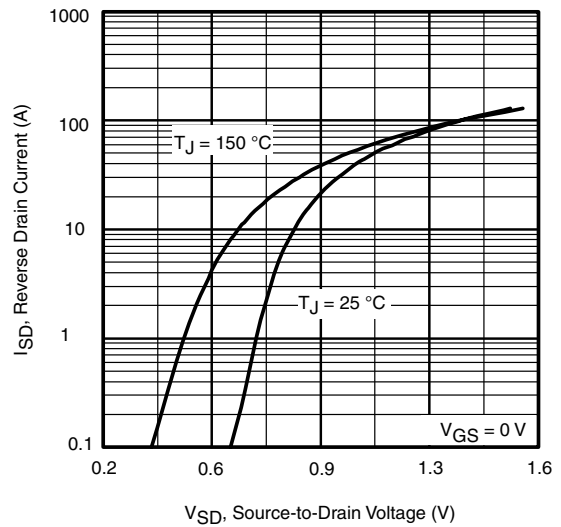
- Repetitive rating; pulse width limited by maximum junction temperature.
- Pulse width  $\leq 400\text{ }\mu\text{s}$ ; duty cycle  $\leq 2\%$ .
- $C_{oss\text{ eff.}}$  is a fixed capacitance that gives the same charging time as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 80%  $V_{DS}$ .

**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted

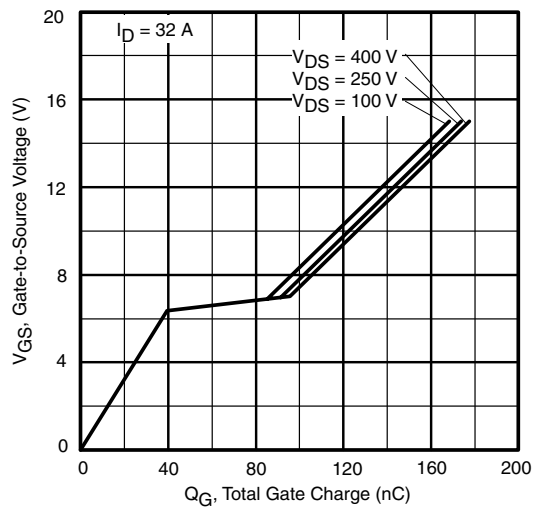




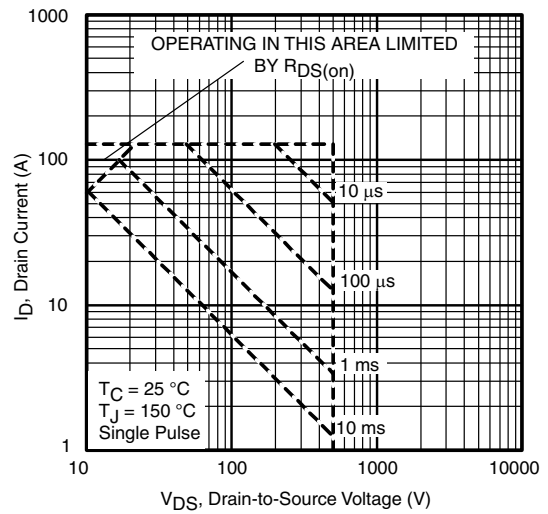
**Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage**



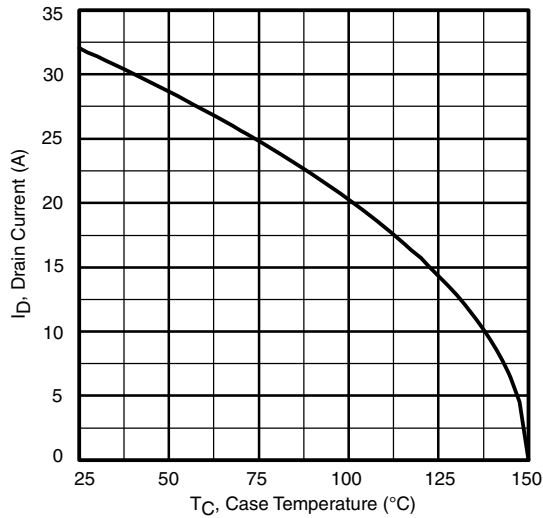
**Fig. 7 - Typical Source-Drain Diode Forward Voltage**



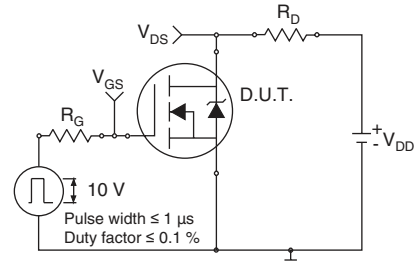
**Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage**



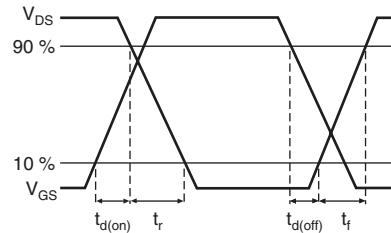
**Fig. 8 - Maximum Safe Operating Area**



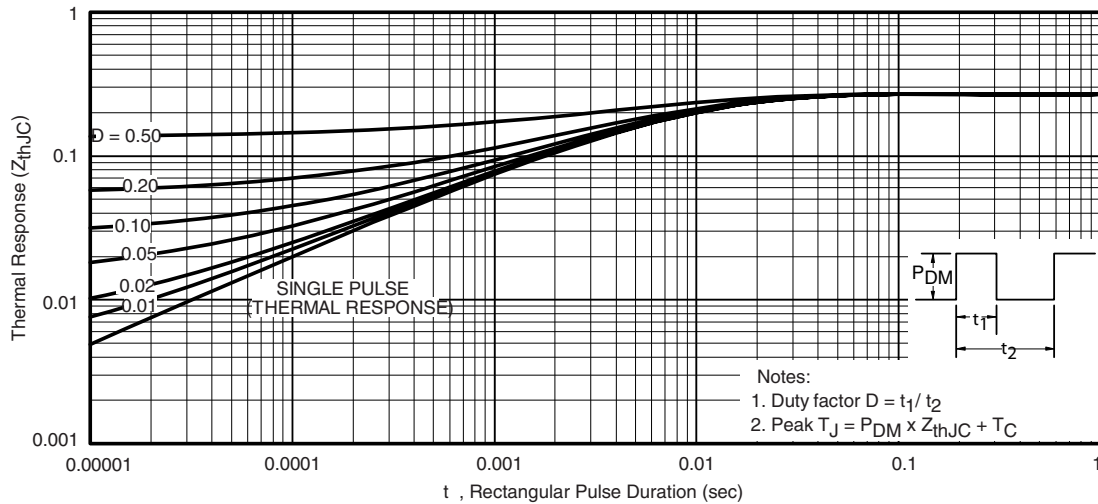
**Fig. 9 - Maximum Drain Current vs. Case Temperature**



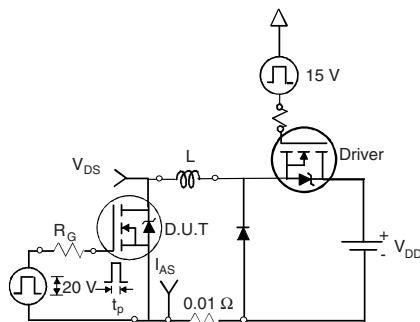
**Fig. 10a - Switching Time Test Circuit**



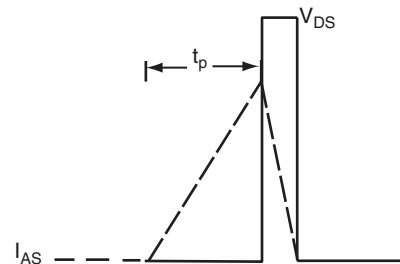
**Fig. 10b - Switching Time Waveforms**



**Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case**



**Fig. 12a - Unclamped Inductive Test Circuit**



**Fig. 12b - Unclamped Inductive Waveforms**

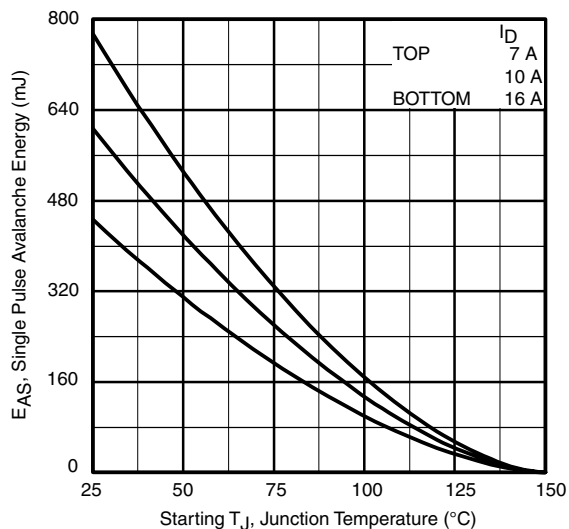


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

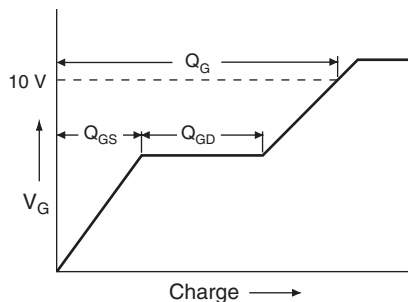


Fig. 13a - Basic Gate Charge Waveform

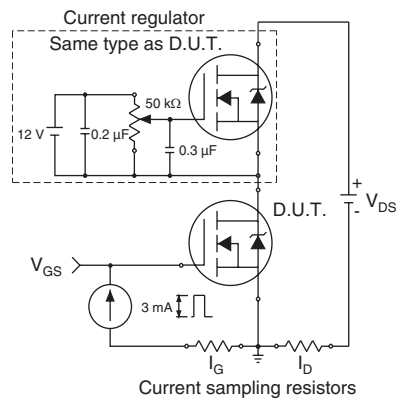


Fig. 13b - Gate Charge Test Circuit

## Peak Diode Recovery $dV/dt$ Test Circuit

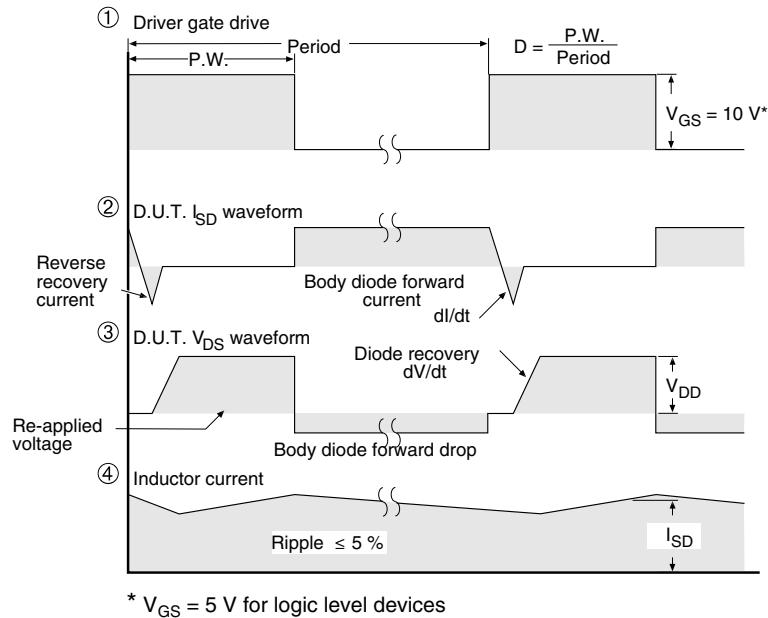
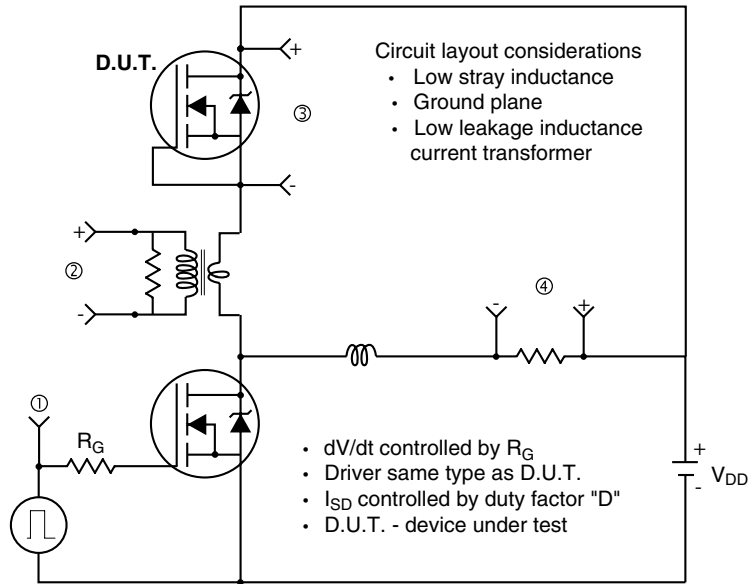


Fig. 14 - For N-Channel

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