Mobile DDR SDRAM

2M x 16 Bit x 4 Banks
Mobile DDR SDRAM

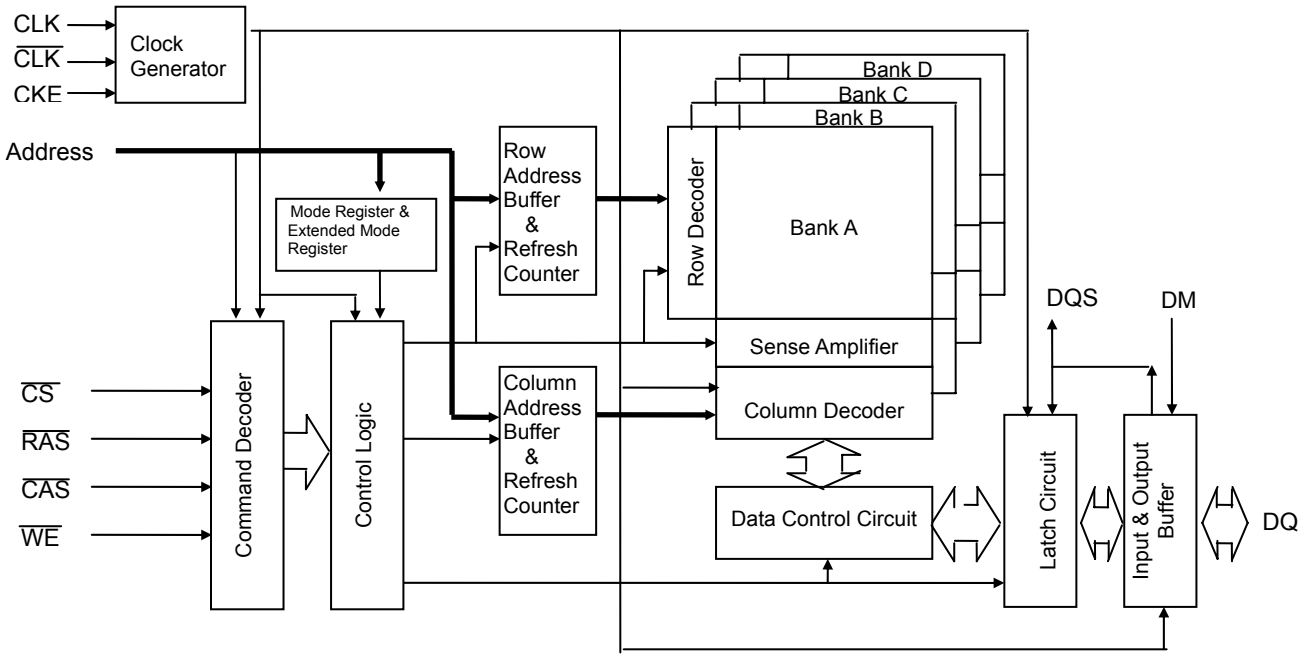
Features

- JEDEC Standard
- Internal pipelined double-data-rate architecture, two data access per clock cycle
- Bi-directional data strobe (DQS)
- No DLL; CLK to DQS is not synchronized.
- Differential clock inputs (CLK and $\overline{CLK}$)
- Quad bank operation
- CAS Latency : 2, 3
- Burst Type : Sequential and Interleave
- Burst Length : 2, 4, 8
- Special function support
  - PASR (Partial Array Self Refresh)
  - Internal TCSR (Temperature Compensated Self Refresh)
  - DS (Driver Strength)
- All inputs except data & DM are sampled at the rising edge of the system clock(CLK)
- Data I/O transitions on both edges of data strobe (DQS)
- DQS is edge-aligned with data for READ; center-aligned with data for WRITE
- Data mask (DM) for write masking only
- V_{DD}/V_{DDQ} = 1.7V ~ 1.9V
- Auto & Self refresh
- 15.6us refresh interval (64ms refresh period, 4K cycle)
- 1.8V LVCMOS-compatible inputs
- 60 ball BGA package

Ordering information :

Part NO.	MAX FREQ	VDD	PACKAGE	COMMENTS
M53D128168A -7.5BG	133MHz	1.8V	8x10 mm BGA	Pb-free
M53D128168A -10BG	100MHz			Pb-free
M53D128168A -7.5BAG	133MHz		8x13 mm BGA	Pb-free
M53D128168A -10BAG	100MHz			Pb-free

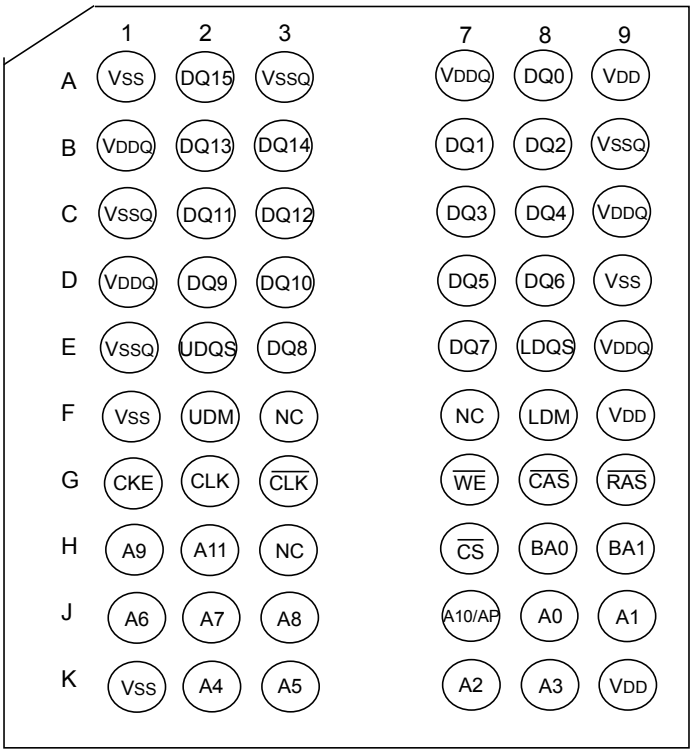
Functional Block Diagram



Pin Arrangement

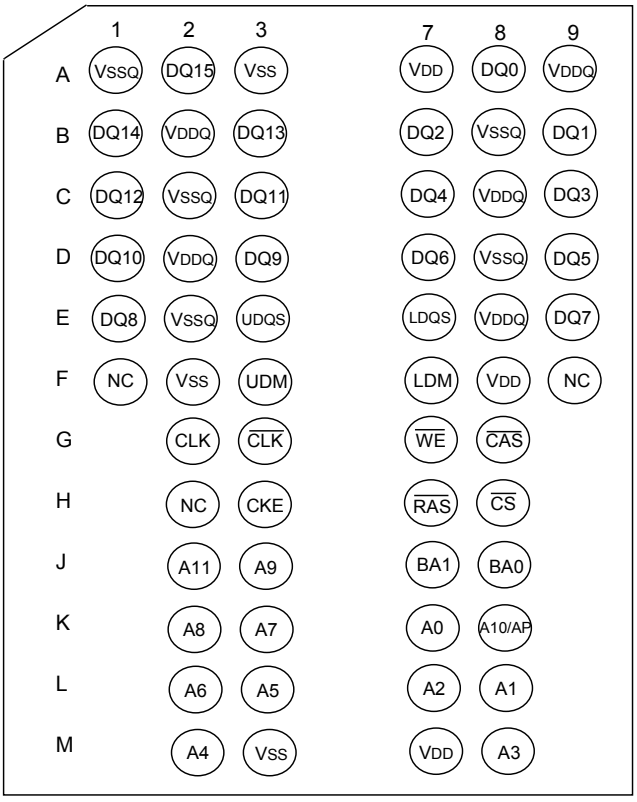
60 Ball BGA (8x10mm)

TOP View



60 Ball BGA (8x13mm)

TOP View



Pin Description

Pin Name	Function	Pin Name	Function
A0~A11, BA0,BA1	Address inputs - Row address A0~A11 - Column address A0~A8 A10/AP : AUTO Precharge BA0, BA1 : Bank selects (4 Banks)	LDM, UDM	DM is an input mask signal for write data. LDM corresponds to the data on DQ0~DQ7; UDM correspond to the data on DQ8~DQ15.
DQ0~DQ15	Data-in/Data-out	CLK, $\overline{CLK}$	Clock input
$\overline{RAS}$	Row address strobe	CKE	Clock enable
$\overline{CAS}$	Column address strobe	$\overline{CS}$	Chip select
$\overline{WE}$	Write enable	V_{DDQ}	Supply Voltage for DQ
V_{SS}	Ground	V_{SSQ}	Ground for DQ
V_{DD}	Power	NC	No connection
LDQS, UDQS	Bi-directional Data Strobe. LDQS corresponds to the data on DQ0~DQ7; UDQS correspond to the data on DQ8~DQ15.		

Absolute Maximum Rating

Parameter	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	-0.5 ~ 2.7	V
Voltage on V_{DD} supply relative to V_{SS}	V_{DD}	-0.5 ~ 2.7	V
Voltage on V_{DDQ} supply relative to V_{SS}	V_{DDQ}	-0.5 ~ 2.7	V
Storage temperature	T_{STG}	-55 ~ +150	°C
Power dissipation	P_D	1.0	W
Short circuit current	I_{OS}	50	mA

Note : Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.
Functional operation should be restricted to recommend operation condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC Operation Condition & Specifications

DC Operation Condition

Recommended operating conditions (Voltage reference to V_{SS} = 0V, T_A = 0 to 70 °C)

Parameter	Symbol	Min	Max	Unit	Note
Supply voltage	V_{DD}	1.7	1.9	V	
I/O Supply voltage	V_{DDQ}	1.7	1.9	V	
Input logic high voltage	V_{IH} (DC)	0.7 x V_{DDQ}	V_{DDQ} + 0.3	V	
Input logic low voltage	V_{IL} (DC)	-0.3	0.3 x V_{DDQ}	V	
Output logic high voltage	V_{OH} (DC)	0.9 x V_{DDQ}	-	V	I_{OH} = -0.1mA
Output logic low voltage	V_{OL} (DC)	-	0.1 x V_{DDQ}	V	I_{OL} = 0.1mA
Input Voltage Level, CLK and $\overline{CLK}$ inputs	V_{IN} (DC)	-0.3	V_{DDQ} + 0.3	V	
Input Differential Voltage, CLK and $\overline{CLK}$ inputs	V_{ID} (DC)	0.4 x V_{DDQ}	V_{DDQ} + 0.3	V	1
Input leakage current	I_I	-2	2	μA	
Output leakage current	I_{OZ}	-5	5	μA	

Notes:

1. V_{ID} is the magnitude of the difference between the input level on CLK and the input level on $\overline{CLK}$.

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DC CHARACTERISTICS

Recommended operating condition unless otherwise noted，TA = 0 to 70 °C

Parameter	Symbol	Test Condition	Version		Unit
			-7.5	-10	
Operating Current (One Bank Active)	I_{CC0}	t_{RC}= t_{RC} (min), t_{CK} = t_{CK} (min), CKE = High, /CS = High between valid commands, address inputs are switching, data input signals are stable	60	50	mA
Precharge Standby Current in power-down mode	I_{CC2P}	All banks idle, CKE = Low, /CS = High, t_{CK} = t_{CK} (min), address & control inputs are switching, data input signals are stable	0.5		mA
	I_{CC2PS}	All banks idle, CKE = Low, /CS = High, t_{CK} = Low, /t_{CK} (min) =High, address & control inputs are switching, data input signals are stable	0.5		mA
Precharge Standby Current in non power-down mode	I_{CC2N}	All banks idle, CKE = Low, /CS = High, t_{CK} = t_{CK} (min), address & control inputs are switching, data input signals are stable	28	22	mA
	I_{CC2NS}	All banks idle, CKE = Low, CS = High, t_{CK} = Low, /t_{CK} (min) =High, address & control inputs are switching, data input signals are stable	28	22	mA
Active Standby Current in power-down mode	I_{CC3P}	One bank active, CKE = Low, CS = High, t_{CK} = t_{CK} (min), address & control inputs are switching, data input signals are stable	5		mA
	I_{CC3PS}	One bank active, CKE = Low, CS = High, t_{CK} = Low, /t_{CK} (min) =High, address & control inputs are switching, data input signals are stable	2		
Active Standby Current in non power-down mode (One Bank Active)	I_{CC3N}	One bank active, CKE = Low, CS = High, t_{CK} = t_{CK} (min), address & control inputs are switching, data input signals are stable	45	35	mA
	I_{CC3NS}	One bank active, CKE = Low, CS = High, t_{CK} = Low, /t_{CK} (min) =High, address & control inputs are switching, data input signals are stable	25	20	mA
Operating Current (Burst Mode)	I_{CC4R}	One bank active, BL=4, t_{CK} = t_{CK} (min), continuous read bursts, I_{OUT} = 0 mA, address inputs are switching, 50% data changing each burst	90	75	mA
	I_{CC4W}	One bank active, BL=4, t_{CK} = t_{CK} (min), continuous write bursts, I_{OUT} = 0 mA, address inputs are switching, 50% data changing each burst	90	75	mA
Refresh Current	I_{CC5}	Burst refresh, t_{RC}= t_{RC} (min), t_{CK} = t_{CK} (min), CKE = High, address inputs are switching, data input signals are stable	75	60	mA

Self Refresh Current	I_{CC6}	CKE = Low, CS = High, t_{ck} = t_{ck} (min), address & control & data inputs are stable	TCSR range	15	45	70	85	°C
			4 Banks	340	360	380	400	uA
			2 Bank	290	310	320	350	
			1 Bank	240	260	280	300	
Deep Power Down Current	I_{CC7}	address & control & data inputs are stable		10				uA

Note: 1. It has +/- 5 ° **C** tolerance.

2. I_{CC} specifications are tested after the device is properly intialized.

3. Definitions for I_{CC}: LOW is defined as $V_{IN} \leq 0.1 * V_{DDQ}$;

HIGH is defined as $V_{IN} \geq 0.9 * V_{DDQ}$;

STABLE is defined as inputs stable at a HIGH or LOW level ;

SWITCHING is defined as: - address and command: inputs changing between HIGH and LOW once per two clock cycles ;

- data bus inputs: DQ changing between HIGH and LOW once per clock cycle; DM and DQS are STABLE.

AC Operation Conditions & Timing Specification

AC Operation Conditions

Parameter	Symbol	Min	Max	Unit	Note
Input High (Logic 1) Voltage, DQ, DQS and DM signals	V_{IH}(AC)	0.8 x V_{DDQ}	V_{DDQ}+0.3	V	
Input Low (Logic 0) Voltage, DQ, DQS and DM signals	V_{IL}(AC)	-0.3	0.2 x V_{DDQ}	V	
Input Different Voltage, CLK and $\overline{CLK}$ inputs	V_{ID}(AC)	0.6 x V_{DDQ}	V_{DDQ}+0.3	V	1
Input Crossing Point Voltage, CLK and $\overline{CLK}$ inputs	V_{IX}(AC)	0.4 x V_{DDQ}	0.6 x V_{DDQ}	V	2

Note1. V_{ID} is the magnitude of the difference between the input level on CLK and the input on $\overline{CLK}$.

2. The value of V_{IX} is expected to equal 0.5*V_{DDQ} of the transmitting device and must track variations in the DC level of the same.

Input / Output Capacitance

(V_{DD} = 1.8V, V_{DDQ} =1.8V, T_A = 25 °C , f = 1MHz)

Parameter	Symbol	Min	Max	Unit
Input capacitance (A0~A11, BA0~BA1, CKE, $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)	C_{IN1}	1.5	3.0	pF
Input capacitance (CLK, $\overline{CLK}$)	C_{IN2}	1.5	3.5	pF
Data & DQS input/output capacitance	C_{OUT}	2.0	4.5	pF
Input capacitance (DM)	C_{IN3}	2.0	4.5	pF

AC Operating Test Conditions (V_{DD} = 1.7V~ 1.9V, T_A = 0℃ to 70℃)

(V_{DD} = 1.8V, V_{DDQ} =1.8V, T_A = 25℃, f = 1MHz)

Parameter	Value	Unit
Input signal minimum slew rate	1.0	V/ns
Input levels (V_{IH}/V_{IL})	0.8 x V_{DDQ} / 0.2 x V_{DDQ}	V
Input timing measurement reference level	0.5 x V_{DDQ}	V
Output timing measurement reference level	0.5 x V_{DDQ}	V

AC Timing Parameter & Specifications

(V_{DD} = 1.7V~1.9V, V_{DDQ}=1.7V~1.9V, T_A =0℃ to 70℃)

Parameter		Symbol	-7.5		-10		
			min	max	min	max	
Clock Period	CL3	t_{CK}	7.5	-	10	-	ns
	CL2		12	-	15	-	
Access time from CLK/ $\overline{CLK}$		t_{AC}	2	7	2	9	ns
CLK high-level width		t_{CH}	0.45	0.55	0.45	0.55	t_{CK}
CLK low-level width		t_{CL}	0.45	0.55	0.45	0.55	t_{CK}
Data strobe edge to clock edge		t_{DQSCK}	2	7	2	9	ns
Clock to first rising edge of DQS delay		t_{DQSS}	0.75	1.25	0.75	1.25	t_{CK}
Data-in and DM setup time (to DQS)		t_{DS}	0.75	-	1.1	-	ns
Data-in and DM hold time (to DQS)		t_{DH}	0.75	-	1.1	-	ns
DQ and DM input pulse width (for each input)		t_{DIPW}	t_{DS} + t_{DH}		t_{DS} + t_{DH}		ns
Input setup time (fast slew rate)		t_{IS}	2.0	-	2.0	-	ns
Input hold time (fast slew rate)		t_{IH}	1.3	-	1.5	-	ns
Input setup time (slow slew rate)		t_{IS}	2.0	-	2.0	-	ns
Input hold time (slow slew rate)		t_{IH}	1.5	-	1.7	-	ns
Control and Address input pulse width		t_{IPW}	3.0	-	3.4	-	ns
DQS input high pulse width		t_{DQSH}	0.4	0.6	0.4	0.6	t_{CK}
DQS input low pulse width		t_{DQSL}	0.4	0.6	0.4	0.6	t_{CK}
DQS falling edge to CLK rising-setup time		t_{DSS}	0.2	-	0.2	-	t_{CK}
DQS falling edge from CLK rising-hold time		t_{DSH}	0.2	-	0.2	-	t_{CK}
Data strobe edge to output data edge		t_{DQSQ}	-	0.6	-	0.7	ns
Data-out high-impedance window from CLK/ $\overline{CLK}$		t_{HZ}	-	6.0	-	7.0	ns
Data-out low-impedance window from CLK/ $\overline{CLK}$		t_{LZ}	1.0	-	1.0	-	ns

AC Timing Parameter & Specifications-continued

Parameter	Symbol	-7.5		-10		
		min	max	min	max	
Half Clock Period	t_{HP}	t_{CL}min or t_{CH}min	-	t_{CL}min or t_{CH}min	-	ns
DQ-DQS output hold time	t_{QH}	t_{HP}min-t_{QHS}	-	t_{HP}min-t_{QHS}	-	ns
Data hold skew factor	t_{QHS}	-	0.75	-	1.0	ns
ACTIVE to PRECHARGE command	t_{RAS}	45	70K	50	70K	ns
Row Cycle Time	t_{RC}	67.5	-	80	-	ns
AUTO REFRESH Row Cycle Time	t_{RFC}	80	-	90	-	ns
ACTIVE to READ,WRITE delay	t_{RCD}	22.5	-	30	-	ns
PRECHARGE command period	t_{RP}	22.5	-	30	-	ns
Minimum t_{CKE} High/Low time	t_{CKE}	2		2		t_{CK}
ACTIVE bank A to ACTIVE bank B command	t_{RRD}	15	-	15	-	ns
Write recovery time	t_{WR}	15	-	15	-	t_{CK}
Write data in to READ command delay	t_{WTR}	1	-	1	-	t_{CK}
Col. Address to Col. Address delay	t_{CCD}	1	-	1	-	t_{CK}
Average periodic refresh interval	t_{REFI}	-	15.6	-	15.6	us
Write preamble	t_{WPRE}	0.25	-	0.25	-	t_{CK}
Write postamble	t_{WPST}	0.4	0.6	0.4	0.6	t_{CK}
DQS read preamble	t_{RPRE}	0.9	1.1	0.9	1.1	t_{CK}
DQS read postamble	t_{RPST}	0.4	0.6	0.4	0.6	t_{CK}
Clock to DQS write preamble setup time	t_{WPRES}	0	-	0	-	ns
Load Mode Register / Extended Mode register cycle time	t_{MRD}	2	-	2	-	t_{CK}
Exit self refresh to first valid command	t_{XSR}	120	-	120	-	ns
Exit power-down mode to first valid command	t_{XP}	25	-	25	-	ns
Autoprecharge write recovery+Precharge time	t_{DAL}	(t_{WR}/t_{CK}) + (t_{RP}/t_{CK})	-	(t_{WR}/t_{CK}) + (t_{RP}/t_{CK})	-	ns

Command Truth Table

COMMAND			CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DM	BA0,1	A10/AP	A11, A9~A0	Note
Register	Extended MRS		H	X	L	L	L	L	X	OP CODE			1,2
Register	Mode Register Set		H	X	L	L	L	L	X	OP CODE			1,2
Refresh	Auto Refresh		H	H	L	L	L	H	X	X			3
	Self Refresh	Entry		L									3
		Exit	L	H	L	H	H	H	X	X			3
					H	X	X	X					3
Bank Active & Row Addr.			H	X	L	L	H	H	X	V	Row Address		
Read & Column Address	Auto Precharge Disable		H	X	L	H	L	H	X	V	L	Column Address	4
	Auto Precharge Enable										H		4
Write & Column Address	Auto Precharge Disable		H	X	L	H	L	L	X	V	L	Column Address	4
	Auto Precharge Enable										H		4,6
Deep Power Down	Entry		H	L	L	H	H	L	X	X			
	Exit		L	H	H	X	X	X	X				
Burst Stop			H	X	L	H	H	L	X	X			7
Precharge	Bank Selection		H	X	L	L	H	L	X	V	L	X	
	All Banks									X	H		5
Active Power Down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
		Exit	L	H	X	X	X	X	X				
Precharge Power Down Mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DM			H	X					V	X			8
No Operation Command			H	X	H	X	X	X	X	X			
					L	H	H	H					

(V = Valid, X = Don't Care, H = Logic High, L = Logic Low)

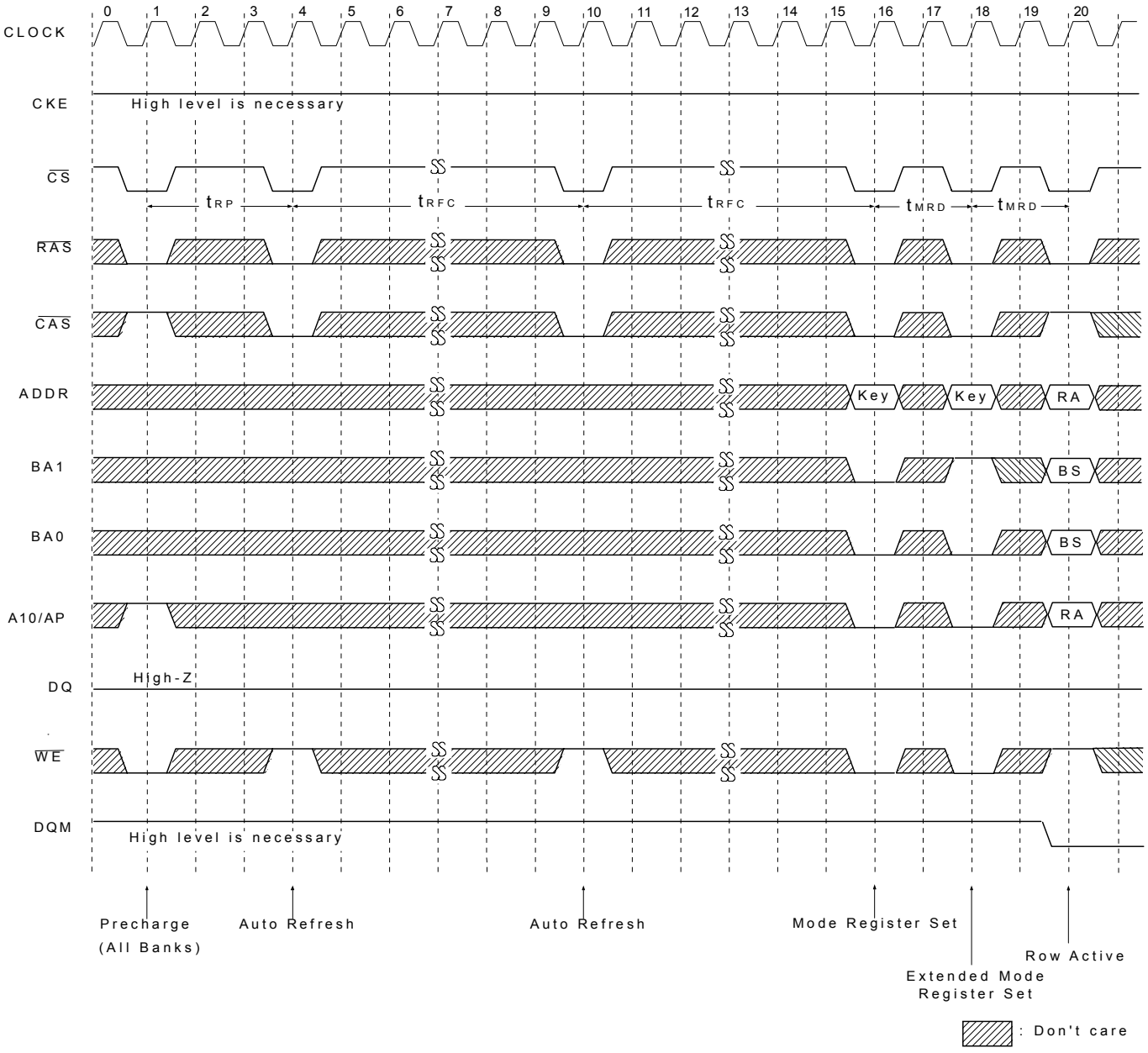
1. OP Code: Operand Code. A0~A11 & BA0~BA1 : Program keys. (@EMRS/MRS)
2. EMRS/MRS can be issued only at all banks precharge state.
   A new command can be issued 2 clock cycles after EMRS or MRS.
3. Auto refresh functions are same as the CBR refresh of DRAM.
   The automatical precharge without row precharge command is meant by "Auto"..
   Auto/self refresh can be issued only at all banks precharge state.
4. BA0~BA1 : Bank select addresses.
   If both BA0 and BA1 are "Low" at read, write, row active and precharge, bank A is selected.
   If BA0 is "High" and BA1 is "Low" at read, write, row active and precharge, bank B is selected.
   If BA0 is "Low" and BA1 is "High" at read, write, row active and precharge, bank C is selected.
   If both BA0 and BA1 are "High" at read, write, row active and precharge, bank D is selected.
5. If A10/AP is "High" at row precharge, BA0 and BA1 are ignored and all banks are selected.
6. During burst write with auto precharge, new read/write command can not be issued.
   Another bank read/write command can be issued after the end of burst.
   New row active of the associated bank can be issued at t_{RP} after end of burst.
7. Burst stop command is valid at every burst length.
8. DM sampling at the rising and falling edges of the DQS and Data-in are masked at the both edges (Write DM latency is 0).

Basic Functionality

Power-Up and Initialization Sequence

The following sequence is required for POWER UP and Initialization.

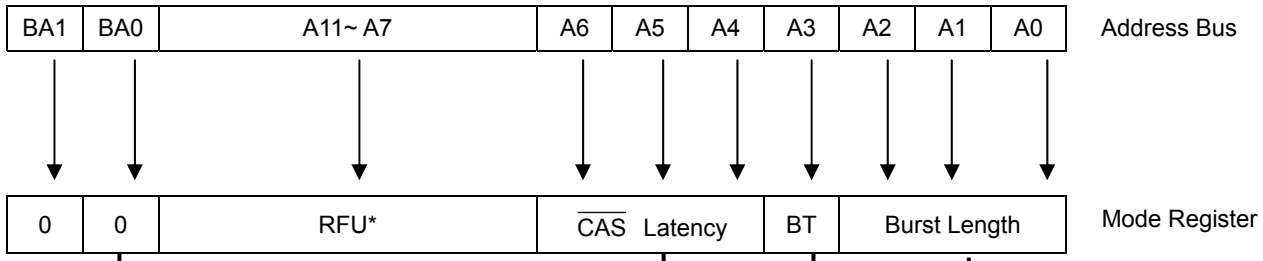
1. Apply power and attempt to maintain CKE at a low state (all other inputs may be undefined.)
   - Apply V_{DD} before or at the same time as V_{DDQ}.
2. Start clock and maintain stable condition for a minimum.
3. The minimum of 200us after stable power and clock (CLK, $\overline{CLK}$),apply NOP & take CKE high.
4. Issue precharge commands for all banks of the device.
5. Issue 2 or more auto-refresh commands.
6. Issue mode register set command to initialize the mode register.
7. Issue extended mode register set command to set PASR and DS.



Mode Register Definition

Mode Register Set (MRS)

The mode register stores the data for controlling the various operating modes of Mobile DDR SDRAM. It programs $\overline{CAS}$ latency, addressing mode, burst length and various vendor specific options to make Mobile DDR SDRAM useful for variety of different applications. The default value of the register is not defined, therefore the mode register must be written in the power up sequence of Mobile DDR SDRAM. The mode register is written by asserting low on $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ and BA0 (The Mobile DDR SDRAM should be in all bank precharge with CKE already high prior to writing into the mode register). The state of address pins A0~A11 in the same cycle as $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ and BA0 going low is written in the mode register. Two clock cycles are requested to complete the write operation in the mode register. The mode register contents can be changed using the same command and clock cycle requirements during operation as long as all banks are in the idle state. The mode register is divided into various fields depending on functionality. The burst length uses A0~A2, addressing mode uses A3, $\overline{CAS}$ latency (read latency from column address) uses A4~A6. A7~A11 is used for test mode. A7~A11 must be set to low for normal MRS operation. Refer to the table for specific codes for various burst length, addressing modes and $\overline{CAS}$ latencies.



A3	Burst Type
0	Sequential
1	Interleave

BA1	BA0	Operating Mode
0	0	MRS Cycle
1	0	EMRS Cycle

CAS Latency			
A6	A5	A4	Latency
0	0	0	Reserve
0	0	1	Reserve
0	1	0	2
0	1	1	3
1	0	0	Reserve
1	0	1	Reserve
1	1	0	Reserve
1	1	1	Reserve

Burst Length

A2	A1	A0	Latency	
			Sequential	Interleave
0	0	0	Reserve	Reserve
0	0	1	2	2
0	1	0	4	4
0	1	1	8	8
1	0	0	Reserve	Reserve
1	0	1	Reserve	Reserve
1	1	0	Reserve	Reserve
1	1	1	Reserve	Reserve

* RFU should stay “0” during MRS cycle

Burst Address Ordering for Burst Length

Burst Length	Starting Address (A2, A1,A0)	Sequential Mode	Interleave Mode
2	xx0	0, 1	0, 1
	xx1	1, 0	1, 0
4	x00	0, 1, 2, 3	0, 1, 2, 3
	x01	1, 2, 3, 0	1, 0, 3, 2
	x10	2, 3, 0, 1	2, 3, 0, 1
	x11	3, 0, 1, 2	3, 2, 1, 0
8	000	0, 1, 2, 3, 4, 5, 6, 7	0, 1, 2, 3, 4, 5, 6, 7
	001	1, 2, 3, 4, 5, 6, 7, 0	1, 0, 3, 2, 5, 4, 7, 6
	010	2, 3, 4, 5, 6, 7, 0, 1	2, 3, 0, 1, 6, 7, 4, 5
	011	3, 4, 5, 6, 7, 0, 1, 2	3, 2, 1, 0, 7, 6, 5, 4
	100	4, 5, 6, 7, 0, 1, 2, 3	4, 5, 6, 7, 0, 1, 2, 3
	101	5, 6, 7, 0, 1, 2, 3, 4	5, 4, 7, 6, 1, 0, 3, 2
	110	6, 7, 0, 1, 2, 3, 4, 5	6, 7, 4, 5, 2, 3, 0, 1
	111	7, 0, 1, 2, 3, 4, 5, 6	7, 6, 5, 4, 3, 2, 1, 0

Extended Mode Register Set (EMRS)

The extended mode register stores for selecting PASR and DS. The extended mode register set must be done before any active command after the power up sequence. The extended mode register is written by asserting low on $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ and high on BA1,low on BA0(The Mobile DDR SDRAM should be in all bank precharge with CKE already high prior to writing into the extended more register). The state of address pins A0~An in the same cycle as $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ going low is written in the extended mode register. Refer to the table for specific codes.

The extended mode register can be changed by using the same command and clock cycle requirements during operations as long as all banks are in the idle state. The default value extended mode register is defined as half driving strength and all banks refreshed.

Internal Temperature Compensated Self Refresh (TCSR)

1. In order to save power consumption, Mobile DDR SDRAM includes the internal temperature sensor and control units to control the self refresh cycle automatically according to the three temperature range : 15°C, 45°C, 70°C and 85°C.
2. If the EMRS for external TCSR is issued by the controller, this EMRS code for TCSR is ignored.
3. It has +/-5°C tolerance

BA1	BA0	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	Address bus
1	0	0	0	0	0	0	DS		RFU*		PASR			Extended Mode Register Set

	A2-A0	Self Refresh Coverage
PASR	000	4Bank
	001	2 Bank (BankA& BankB) or (BA1=0)
	010	1 Bank (BankA) or (BA0=BA1=0)
	011	R
	100	R
	101	R
	111	R

Internal TCSR

	A6-A5	Driver Strength
DS	00	Full Strength
	01	1/2 Strength
	10	1/4 Strength
	11	R

Remark R : Reserved

* RFU should stay “0” during EMRS cycle

Precharge

The precharge command is used to precharge or close a bank that has activated. The precharge command is issued when $\overline{CS}$, $\overline{RAS}$ and $\overline{WE}$ are low and $\overline{CAS}$ is high at the rising edge of the clock. The precharge command can be used to precharge each bank respectively or all banks simultaneously. The bank select addresses (BA0, BA1) are used to define which bank is precharged when the command is initiated. For write cycle, t_{WR}(min.) must be satisfied until the precharge command can be issued. After t_{RP} from the precharge, an active command to the same bank can be initiated.

Burst Selection for Precharge by Bank address bits

A10/AP	BA1	BA0	Precharge
0	0	0	Bank A Only
0	0	1	Bank B Only
0	1	0	Bank C Only
0	1	1	Bank D Only
1	X	X	All Banks

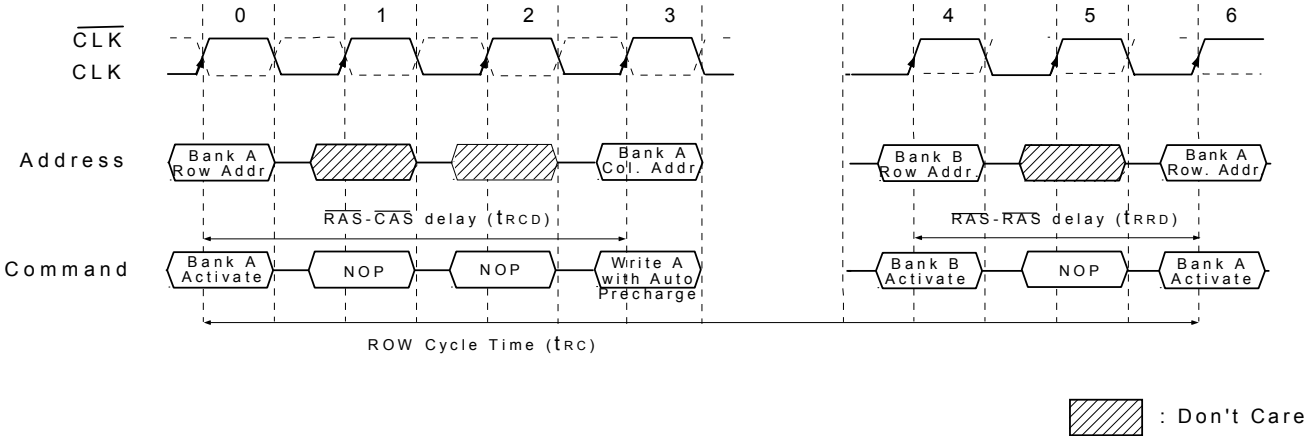
NOP & Device Deselect

The device should be deselected by deactivating the $\overline{CS}$ signal. In this mode, Mobile DDR SDRAM should ignore all the control inputs. The Mobile DDR SDRAM is put in NOP mode when $\overline{CS}$ is actived and by deactivating $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$. For both Deselect and NOP, the device should finish the current operation when this command is issued.

Row Active

The Bank Activation command is issued by holding $\overline{CAS}$ and $\overline{WE}$ high with $\overline{CS}$ and $\overline{RAS}$ low at the rising edge of the clock (CLK). The Mobile DDR SDRAM has four independent banks, so two Bank Select addresses (BA0, BA1) are required. The Bank Activation command to the first read or write command must meet or exceed the minimum of $\overline{RAS}$ to $\overline{CAS}$ delay time (t_{RCD} min). Once a bank has been activated, it must be precharged before another Bank Activation command can be applied to the same bank. The minimum time interval between interleaved Bank Activation command (Bank A to Bank B and vice versa) is the Bank to Bank delay time (t_{RRD} min).

Bank Activation Command Cycle ($\overline{CAS}$ Latency = 3)



Read Bank

This command is used after the row activate command to initiate the burst read of data. The read command is initiated by activating $\overline{CS}$, $\overline{CAS}$, and deasserting $\overline{WE}$ at the same clock sampling (rising) edge as described in the command truth table. The length of the burst and the CAS latency time will be determined by the values programmed during the MRS command.

Write Bank

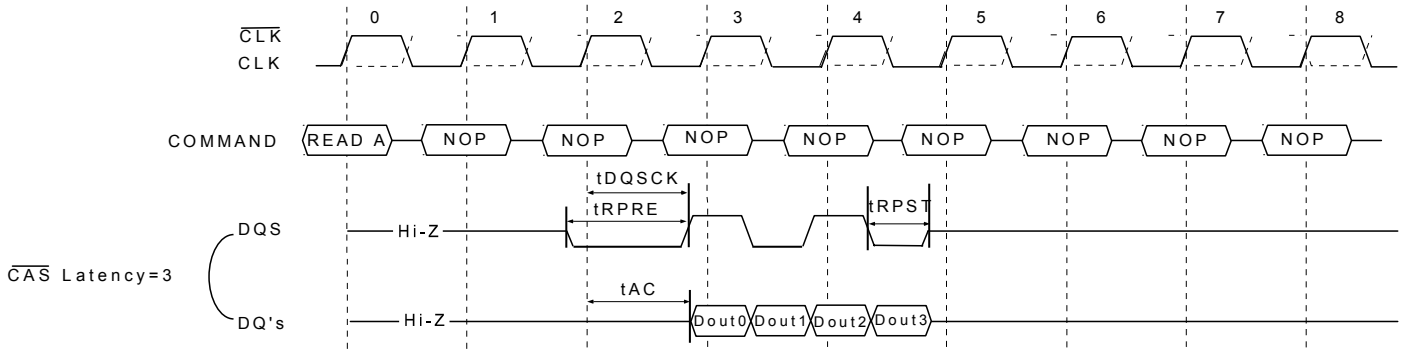
This command is used after the row activate command to initiate the burst write of data. The write command is initiated by activating $\overline{CS}$, $\overline{CAS}$, and $\overline{WE}$ at the same clock sampling (rising) edge as describe in the command truth table. The length of the burst will be determined by the values programmed during the MRS command.

Essential Functionality for Mobile DDR SDRAM

Burst Read Operation

Burst Read operation in Mobile DDR SDRAM is in the same manner as the current Mobile DDR SDRAM such that the Burst read command is issued by asserting $\overline{CS}$ and $\overline{CAS}$ low while holding $\overline{RAS}$ and $\overline{WE}$ high at the rising edge of the clock (CLK) after t_{RCD} from the bank activation. The address inputs determine the starting address for the Burst, The Mode Register sets type of burst (Sequential or interleave) and burst length (2, 4, 8). The first output data is available after the $\overline{CAS}$ Latency from the READ command, and the consecutive data are presented on the falling and rising edge of Data Strobe (DQS) adopted by Mobile DDR SDRAM until the burst length is completed.

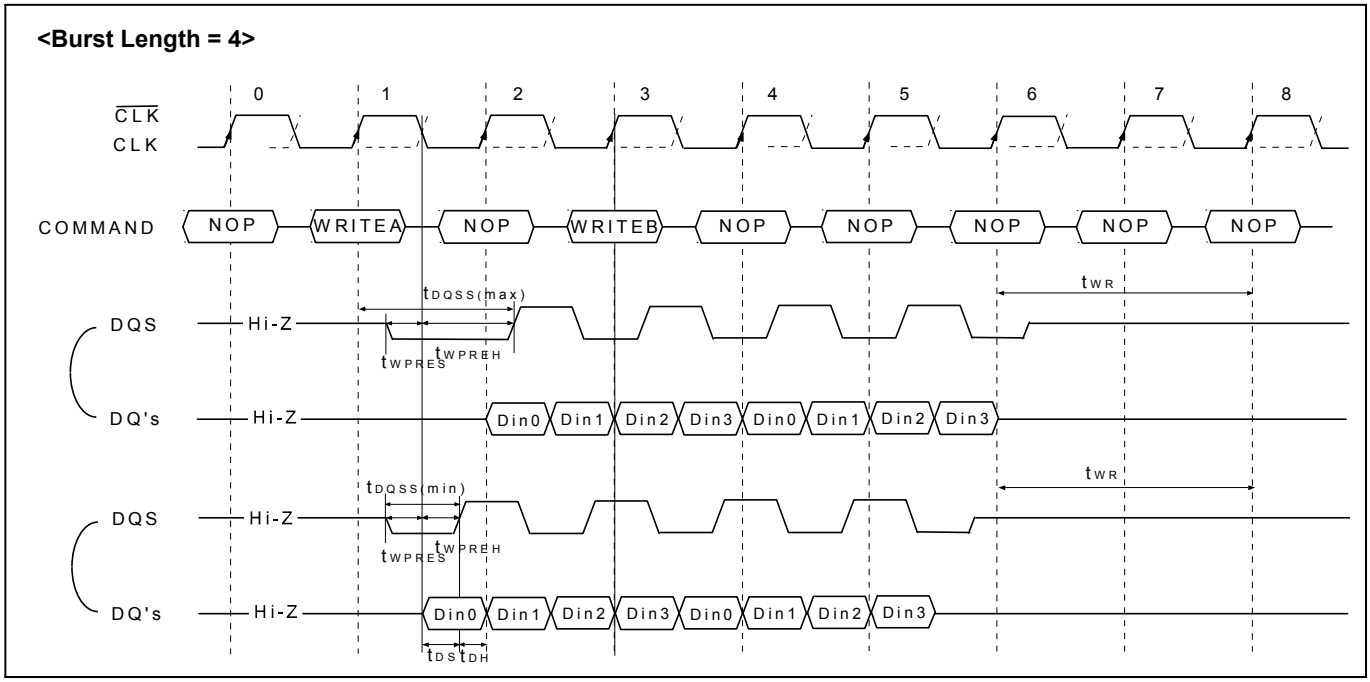
<Burst Length = 4, $\overline{CAS}$ Latency = 3>



Burst Write Operation

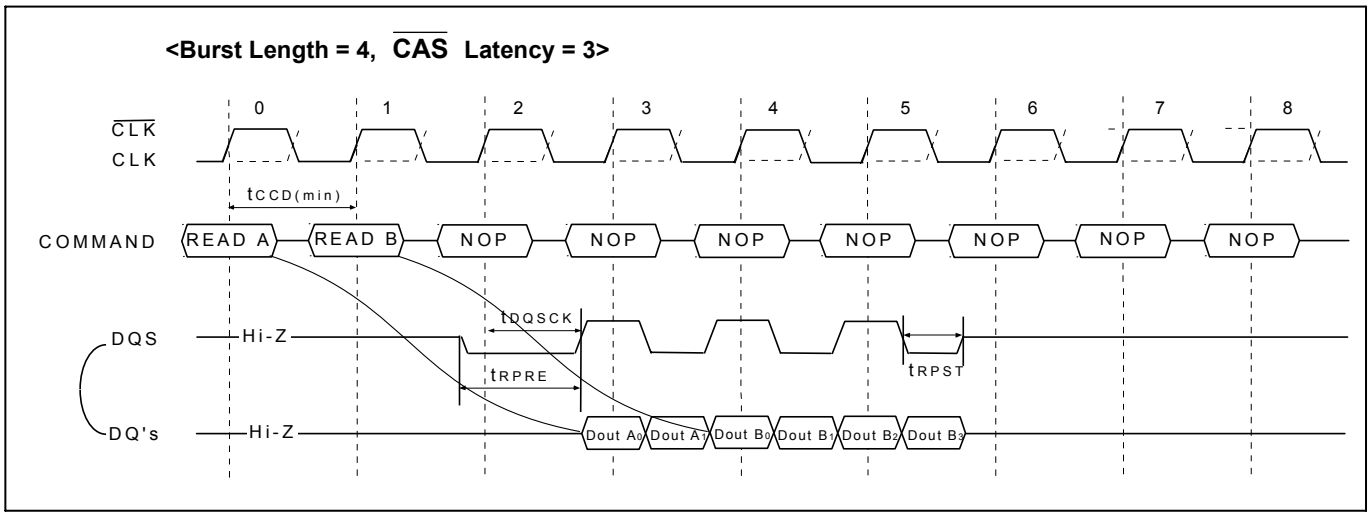
The Burst Write command is issued by having $\overline{CS}$, $\overline{CAS}$ and $\overline{WE}$ low while holding $\overline{RAS}$ high at the rising edge of the clock (CLK). The address inputs determine the starting column address. There is no write latency relative to DQS required for burst write cycle. The first data of a burst write cycle must be applied on the DQ pins t_{DS} (Data-in setup time) prior to data strobe edge enabled after t_{DQSS} from the rising edge of the clock (CLK) that the write command is issued. The remaining data inputs must be supplied on each subsequent falling and rising edge of Data Strobe until the burst length is completed. When the burst has been finished, any additional data supplied to the DQ pins will be ignored.

<Burst Length = 4>



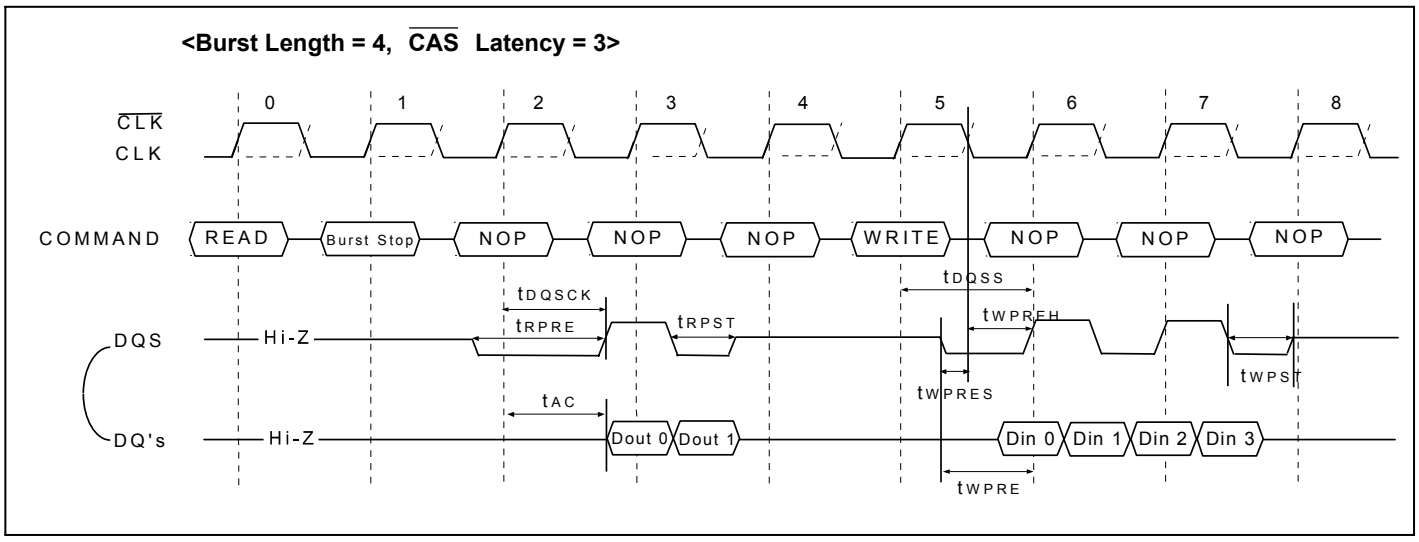
Read Interrupted by a Read

A Burst Read can be interrupted before completion of the burst by new Read command of any bank. When the previous burst is interrupted, the remaining addresses are overridden by the new address with the full burst length. The data from the first Read command continues to appear on the outputs until the $\overline{CAS}$ latency from the interrupting Read command is satisfied. At this point the data from the interrupting Read command appears. Read to Read interval is minimum 1 Clock.



Read Interrupted by a Write & Burst Stop

To interrupt a burst read with a write command, Burst Stop command must be asserted to avoid data contention on the I/O bus by placing the DQ's(Output drivers) in a high impedance state. To insure the DQ's are tri-stated one cycle before the beginning the write operation, Burt stop command must be applied at least RU(CL) clocks 〔RU means round up to the nearest integer〕 before the Write command.

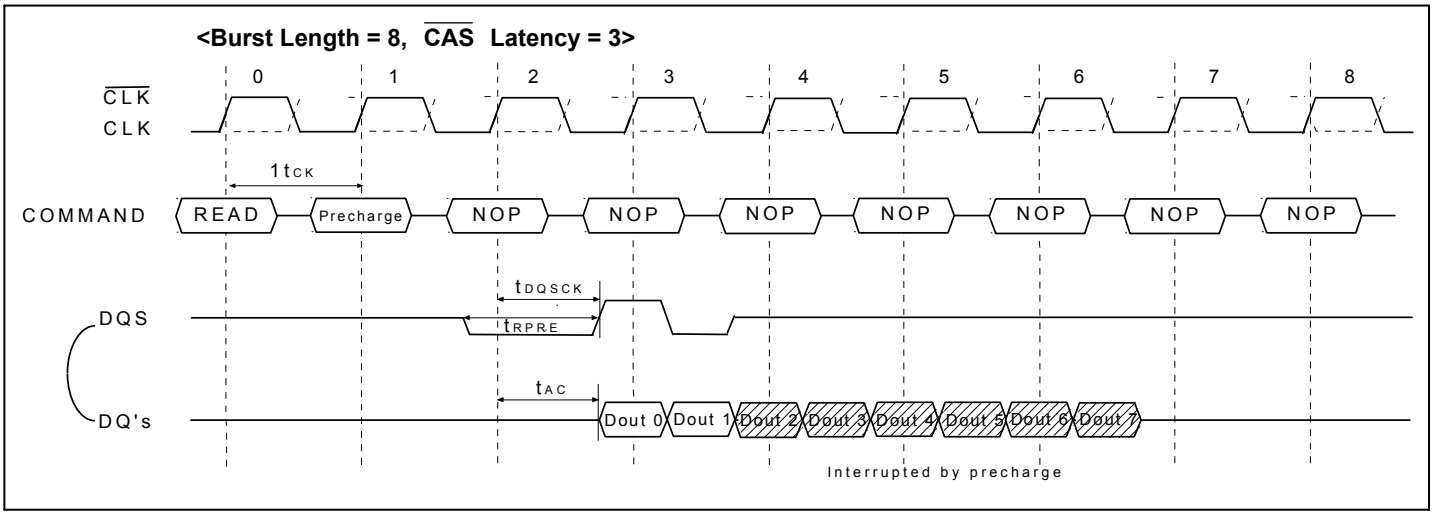


The following functionality establishes how a Write command may interrupt a Read burst.

1. For Write commands interrupting a Read burst, a Burst Terminate command is required to stop the read burst and tristate the DQ bus prior to valid input write data. Once the Burst Terminate command has been issued, the minimum delay to a Write command = RU(CL) [CL is the $\overline{CAS}$ Latency and RU means round up to the nearest integer].
2. It is illegal for a Write command to interrupt a Read with autoprecharge command.

Read Interrupted by a Precharge

A Burst Read operation can be interrupted by precharge of the same bank. The minimum 1 clock is required for the read to precharge intervals. A precharge command to output disable latency is equivalent to the $\overline{CAS}$ latency.



When a burst Read command is issued to a Mobile DDR SDRAM, a Precharge command may be issued to the same bank before the Read burst is complete. The following functionality determines when a Precharge command may be given during a Read burst and when a new Bank Activate command may be issued to the same bank.

1. For the earliest possible Precharge command without interrupting a Read burst, the Precharge command may be given on the rising clock edge which is CL clock cycles before the end of the Read burst where CL is the $\overline{CAS}$ Latency. A new Bank Activate command may be issued to the same bank after t_{RP} (RAS precharge time).

2. When a Precharge command interrupts a Read burst operation, the Precharge command may be given on the rising clock edge which is CL clock cycles before the last data from the interrupted Read burst where CL is the $\overline{CAS}$ Latency. Once the last data word has been output, the output buffers are tristated. A new Bank Activate command may be issued to the same bank after t_{RP}.

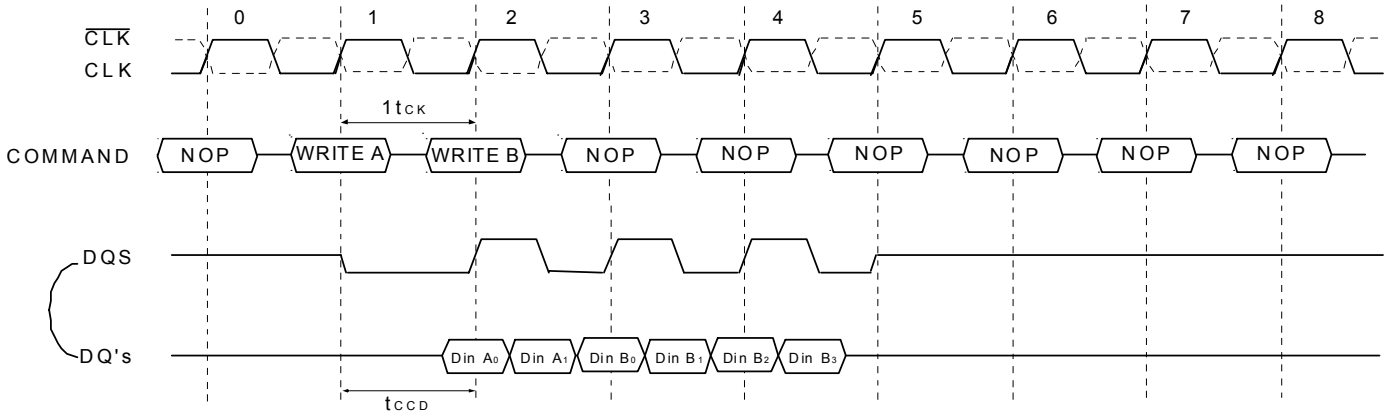
3. For a Read with autoprecharge command, a new Bank Activate command may be issued to the same bank after t_{RP} where t_{RP} begins on the rising clock edge which is CL clock cycles before the end of the Read burst where CL is the $\overline{CAS}$ Latency. During Read with autoprecharge, the initiation of the internal precharge occurs at the same time as the earliest possible external Precharge command would initiate a precharge operation without interrupting the Read burst as described in 1 above.

4. For all cases above, t_{RP} is an analog delay that needs to be converted into clock cycles. The number of clock cycles between a Precharge command and a new Bank Activate command to the same bank equals t_{RP} / t_{CK} (where t_{CK} is the clock cycle time) with the result rounded up to the nearest integer number of clock cycles.
   In all cases, a Precharge operation cannot be initiated unless t_{RAS}(min) [minimum Bank Activate to Precharge time] has been satisfied. This includes Read with autoprecharge commands where t_{RAS}(min) must still be satisfied such that a Read with autoprecharge command has the same timing as a Read command followed by the earliest possible Precharge command which does not interrupt the burst.

Write Interrupted by a Write

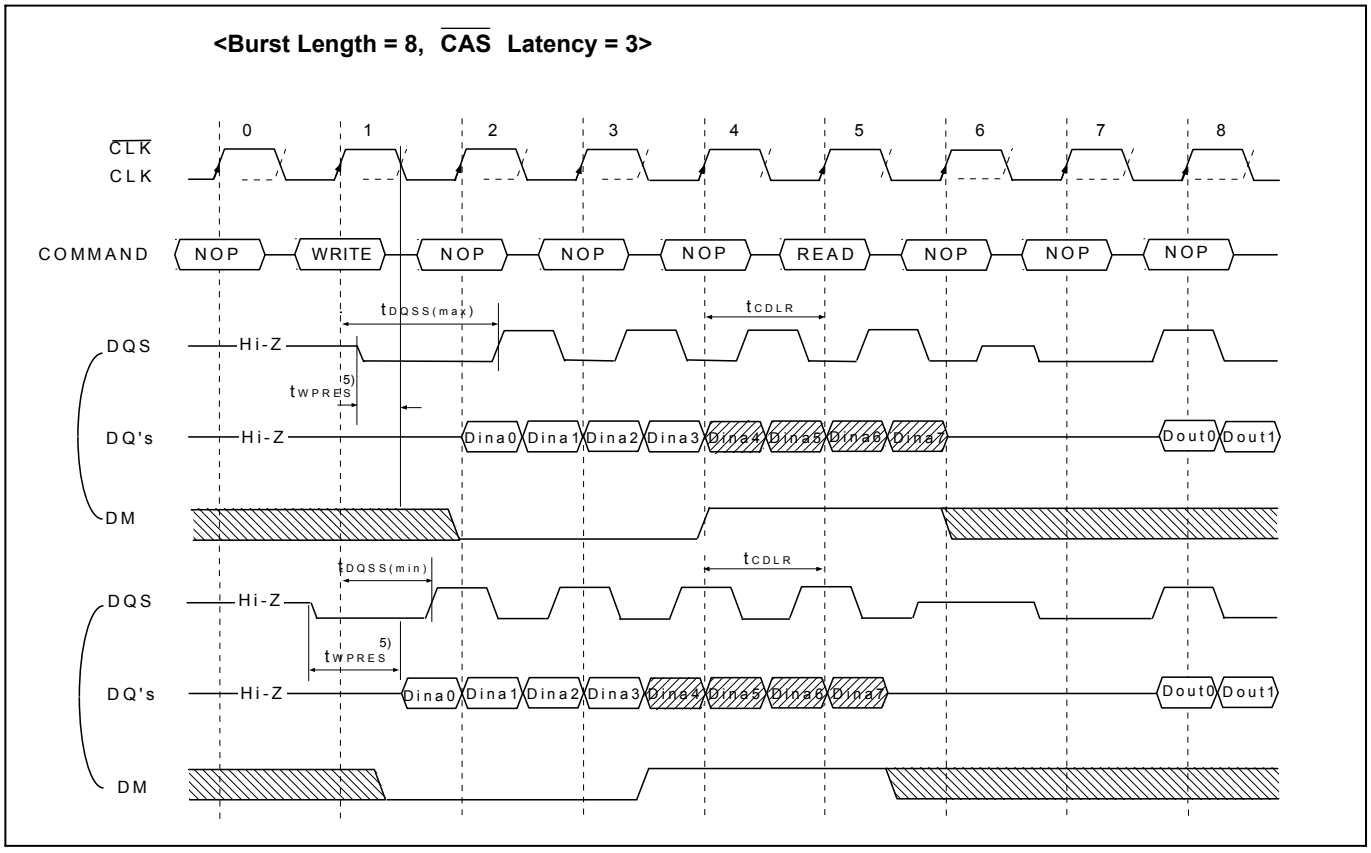
A Burst Write can be interrupted before completion of the burst by a new Write command, with the only restriction that the interval that separates the commands must be at least one clock cycle. When the previous burst is interrupted, the remaining addresses are overridden by the new address and data will be written into the device until the programmed burst length is satisfied.

<Burst Length = 4>



Write Interrupted by a Read & DM

A burst write can be interrupted by a read command of any bank. The DQ's must be in the high impedance state at least one clock cycle before the interrupting read data appear on the outputs to avoid data contention. When the read command is registered, any residual data from the burst write cycle must be masked by DM. The delay from the last data to read command (t_{WTR}) is required to avoid the data contention Mobile DDR SDRAM inside. Data that are presented on the DQ pins before the read command is initiated will actually be written to the memory. Read command interrupting write can not be issued at the next clock edge of that of write command.

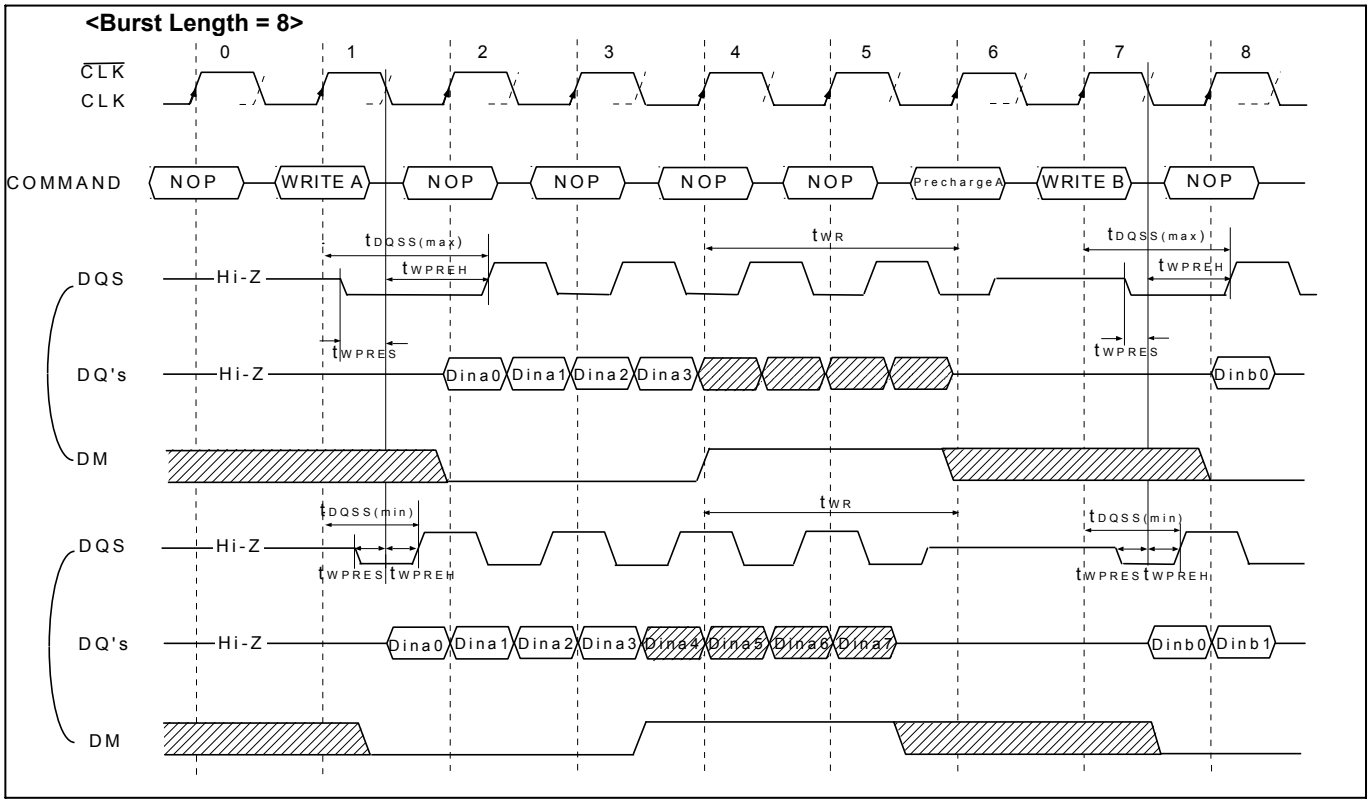


The following functionality established how a Read command may interrupt a Write burst and which input data is not written into the memory.

1. For Read commands interrupting a Write burst, the minimum Write to Read command delay is 2 clock cycles. The case where the Write to Read delay is 1 clock cycle is disallowed.
2. For read commands interrupting a Write burst, the DM pin must be used to mask the input data words which immediately precede the interrupting Read operation and the input data word which immediately follows the interrupting Read operation.
3. For all cases of a Read interrupting a Write, the DQ and DQS buses must be released by the driving chip (i.e., the memory controller) in time to allow the buses to turn around before the Mobile DDR SDRAM drives them during a read operation.
4. If input Write data is masked by the Read command, the DQS inputs are ignored by the Mobile DDR SDRAM.
5. It is illegal for a Read command interrupt a Write with autoprecharge command.

Write Interrupted by a Precharge & DM

A burst write operation can be interrupted before completion of the burst by a precharge of the same bank. Random column access is allowed. A write recovery time (t_{WR}) is required from the last data to precharge command. When precharge command is asserted, any residual data from the burst write cycle must be masked by DM.



Precharge timing for Write operations in Mobile DDR SDRAM requires enough time to allow “Write recovery” which is the time required by a Mobile DDR SDRAM core to properly store a full “0” or “1” level before a Precharge operation. For Mobile DDR SDRAM, a timing parameter, t_{WR}, is used to indicate the required of time between the last valid write operation and a Precharge command to the same bank.

The precharge timing for writes is a complex definition since the write data is sampled by the data strobe and the address is sampled by the input clock. Inside the Mobile DDR SDRAM, the data path is eventually synchronizes with the address path by switching clock domains from the data strobe clock domain to the input clock domain.

This makes the definition of when a precharge operation can be initiated after a write very complex since the write recovery parameter must reference only the clock domain that is used to time the internal write operation i.e., the input clock domain.

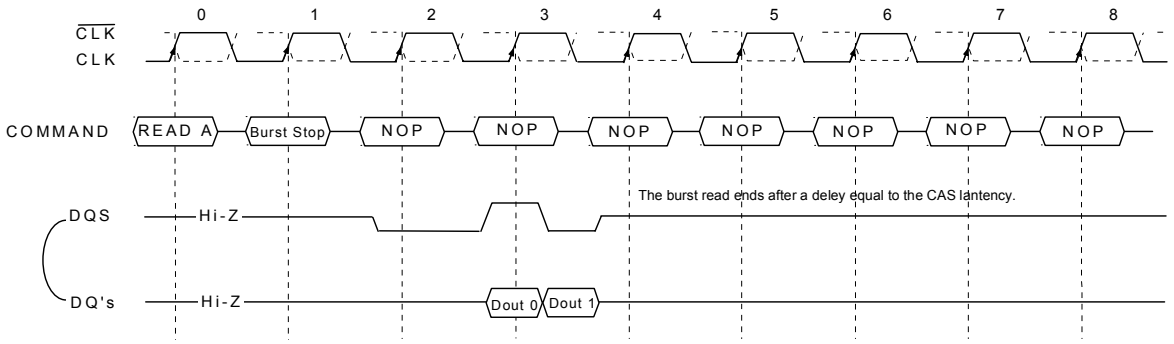
t_{WR} starts on the rising clock edge after the last possible DQS edge that strobed in the last valid and ends on the rising clock edge that strobes in the precharge command.

1. For the earliest possible Precharge command following a Write burst without interrupting the burst, the minimum time for write recovery is defined by t_{WR}.
2. When a precharge command interrupts a Write burst operation, the data mask pin, DM, is used to mask input data during the time between the last valid write data and the rising clock edge in which the Precharge command is given. During this time, the DQS input is still required to strobe in the state of DM. The minimum time for write recovery is defined by t_{WR}.
3. For a Write with autoprecharge command, a new Bank Activate command may be issued to the same bank after $t_{WR} + t_{RP}$ where $t_{WR} + t_{RP}$ starts on the falling DQS edge that strobed in the last valid data and ends on the rising clock edge that strobes in the Bank Activate commands. During write with autoprecharge, the initiation of the internal precharge occurs at the same time as the earliest possible external Precharge command without interrupting the Write burst as described in 1 above.
4. In all cases, a Precharge operation cannot be initiated unless t_{RAS}(min) [minimum Bank Activate to Precharge time] has been satisfied. This includes Write with autoprecharge commands where t_{RAS}(min) must still be satisfied such that a Write with autoprecharge command has the same timing as a Write command followed by the earliest possible Precharge command which does not interrupt the burst.

Burst Stop

The burst stop command is initiated by having $\overline{RAS}$ and $\overline{CAS}$ high with $\overline{CS}$ and $\overline{WE}$ low at the rising edge of the clock (CLK). The burst stop command has the fewest restriction making it the easiest method to use when terminating a burst read operation before it has been completed. When the burst stop command is issued during a burst read cycle, the pair of data and DQS (Data Strobe) go to a high impedance state after a delay which is equal to the CAS latency set in the mode register. The burst stop command, however, is not supported during a write burst operation.

<Burst Length = 4, $\overline{CAS}$ Latency = 3 >



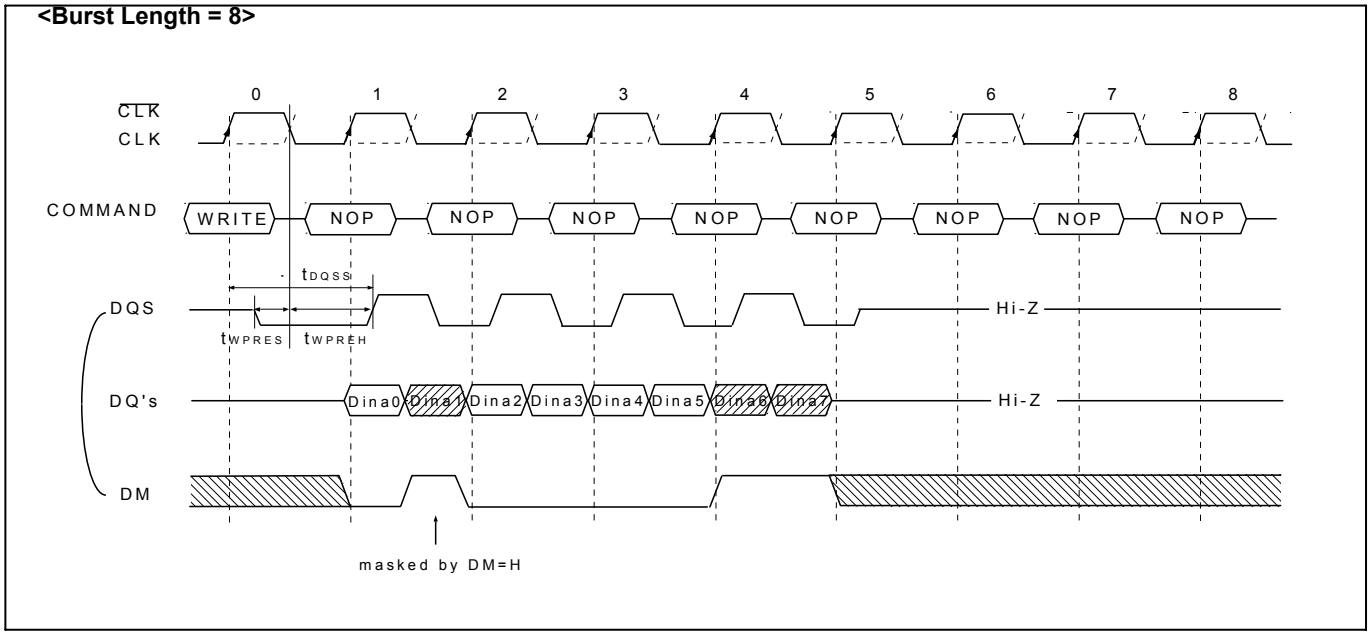
The Burst Stop command is a mandatory feature for Mobile DDR SDRAM. The following functionality is required.

1. The BST command may only be issued on the rising edge of the input clock, CLK.
2. BST is only a valid command during Read burst.
3. BST during a Write burst is undefined and shall not be used.
4. BST applies to all burst lengths.
5. BST is an undefined command during Read with autoprecharge and shall not be used.
6. When terminating a burst Read command, the BST command must be issued L_{BST} ("BST Latency") clock cycles before the clock edge at which the output buffers are tristated, where L_{BST} equals the $\overline{CAS}$ latency for read operations.
7. When the burst terminates, the DQ and DQS pins are tristated.

The BST command is not byte controllable and applies to all bits in the DQ data word and the (all) DQS pin(s).

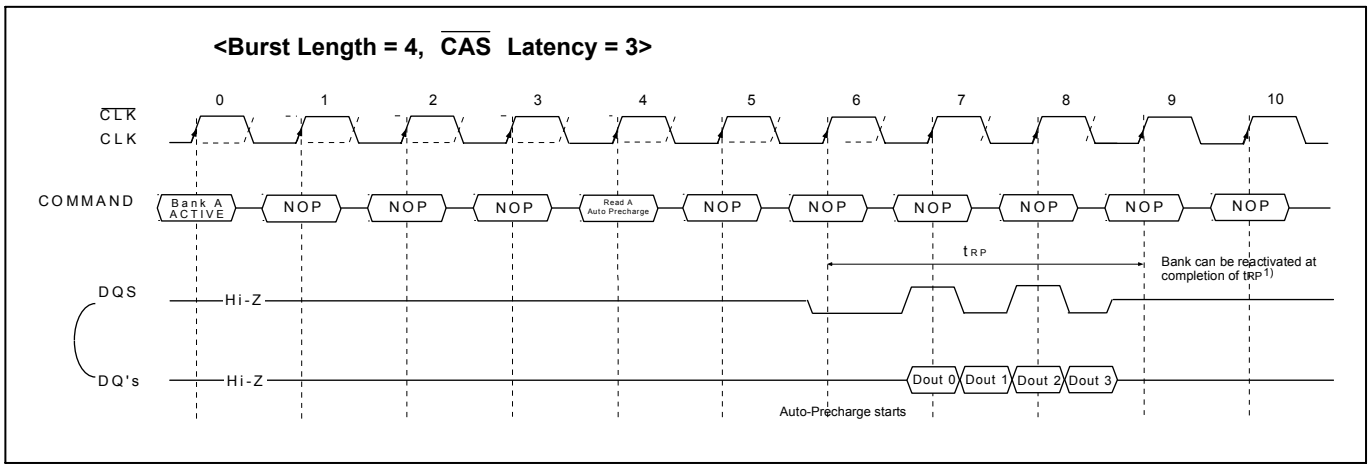
DM masking

The Mobile DDR SDRAM has a data mask function that can be used in conjunction with data write cycle. Not read cycle. When the data mask is activated (DM high) during write operation, Mobile DDR SDRAM does not accept the corresponding data. (DM to data-mask latency is zero) DM must be issued at the rising or falling edge of data strobe.



Read With Auto Precharge

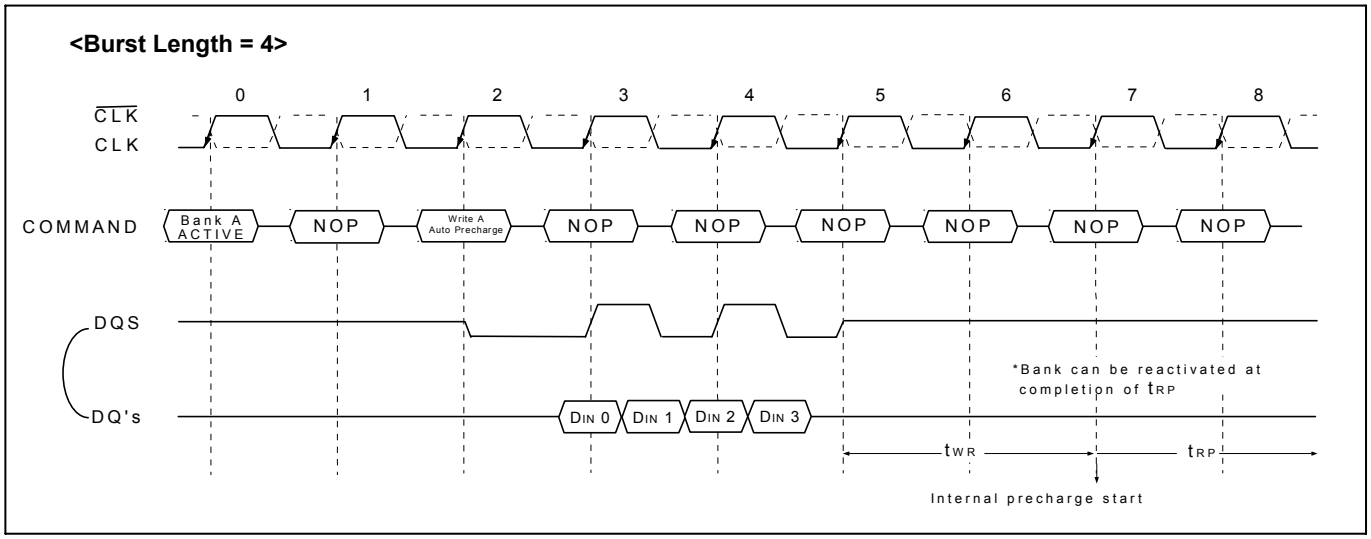
If a read with auto-precharge command is initiated, the Mobile DDR SDRAM automatically enters the precharge operation BL/2 clock later from a read with auto-precharge command when t_{RAS}(min) is satisfied. If not, the start point of precharge operation will be delayed until t_{RAS}(min) is satisfied. Once the precharge operation has started the bank cannot be reactivated and the new command can not be asserted until the precharge time (t_{RP}) has been satisfied



Note : At burst read / write with auto precharge, $\overline{CAS}$ interrupt of the same bank is illegal.

Write with Auto Precharge

If A10 is high when write command is issued, the write with auto-precharge function is performed. Any new command to the same bank should not be issued until the internal precharge is completed. The internal precharge begins after keeping t_{WR}(min).

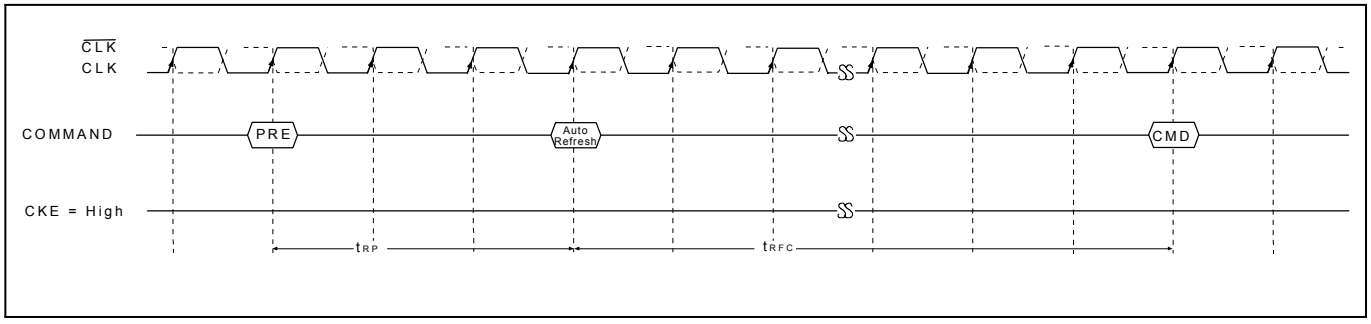


Auto Refresh & Self Refresh

Auto Refresh

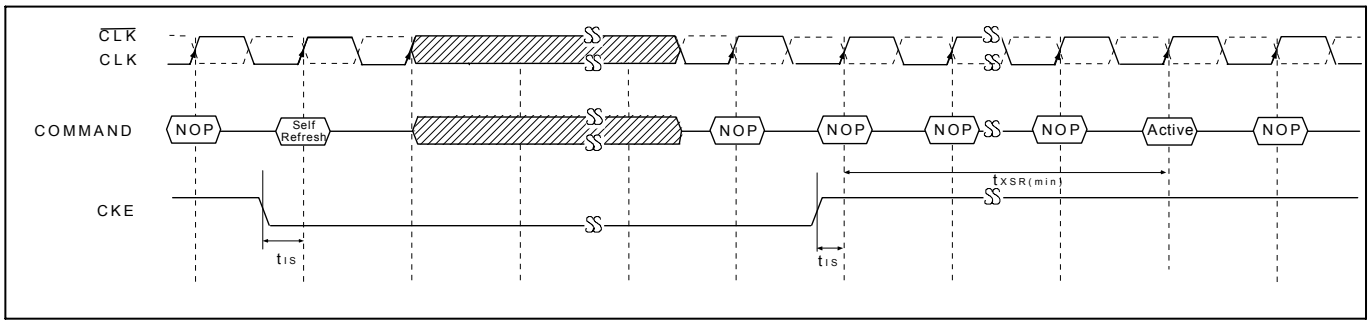
An auto refresh command is issued by having $\overline{CS}$, $\overline{RAS}$ and $\overline{CAS}$ held low with CKE and $\overline{WE}$ high at the rising edge of the clock(CLK). All banks must be precharged and idle for t_{RP}(min) before the auto refresh command is applied. No control of the external address pins is requires once this cycle has started because of the internal address counter. When the refresh cycle has completed, all banks will be in the idle state. A delay between the auto refresh command and the next activate command or subsequent auto refresh command must be greater than or equal to the t_{RFC}(min).

A maximum of eight consecutive AUTO REFRSH commands (with tRFCmin) can be posted to any given Mobile DDR SDRAM, and the maximum absolute interval between any AUTO REFRESH command and the next AUTO REFRESH command is 8x15.6 μm.



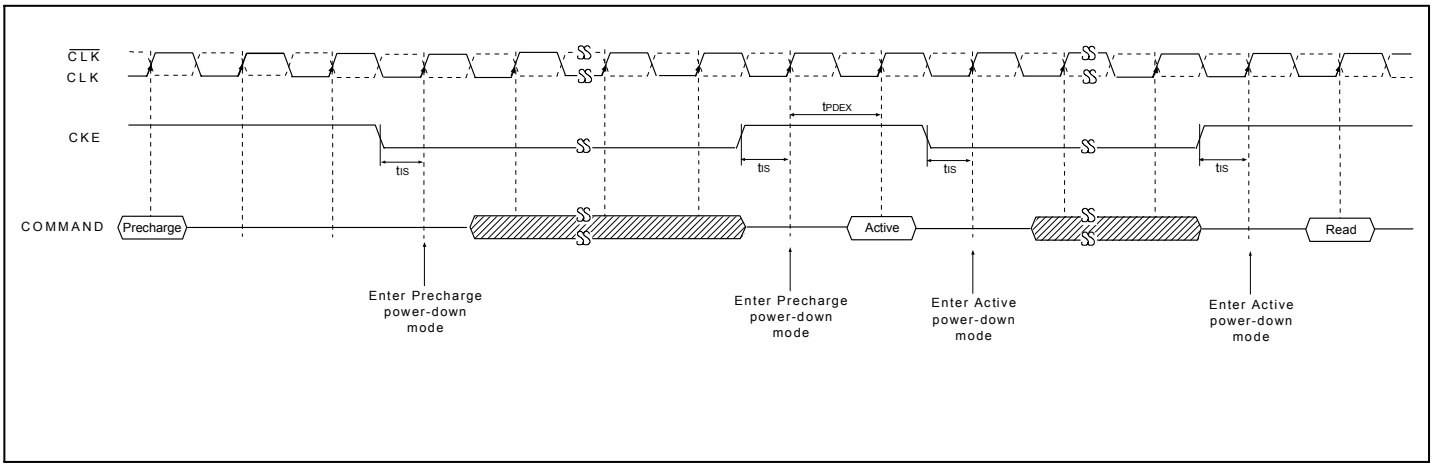
Self Refresh

A self refresh command is defines by having $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$ and CKE held low with $\overline{WE}$ high at the rising edge of the clock (CLK). Once the self refresh command is initiated, CKE must be held low to keep the device in self refresh mode. During the self refresh operation, all inputs except CKE are ignored. The clock is internally disabled during self refresh operation to reduce power consumption. The self refresh is exited by supplying stable clock input before returning CKE high, asserting deselect or NOP command and then asserting CKE high for longer than t_{XSRD} for locking of DLL.



Power Down

The device enters power down mode when CKE Low, and it exits when CKE High. Once the power down mode is initiated, all of the receiver circuits except CLK and CKE are gated off to reduce power consumption. All banks should be in idle state prior to entering the precharge power down mode and CKE should be set in high for at least t_{PDEX} prior to Row active command. Refresh operations cannot be performed during power down mode, therefore the device cannot remain in power down mode longer than the refresh period(t_{REF}) of the device.



Functional Truth Table.

Current	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address	Command	Action
IDLE	H	X	X	X	X	DESEL	NOP
	L	H	H	H	X	NOP	NOP
	L	H	H	L	BA	Burst Stop	ILLEGAL*2
	L	H	L	X	BA, CA, A10	READ / WRITE	ILLEGAL*2
	L	L	H	H	BA, RA	Active	Bank Active, Latch RA
	L	L	H	L	BA, A10	PRE / PREA	NOP*4
	L	L	L	H	X	Refresh	AUTO-Refresh*5
	L	L	L	L	Op-Code Mode-Add	MRS	Mode Register Set*5
ROW ACTIVE	H	X	X	X	X	DESEL	NOP
	L	H	H	H	X	NOP	NOP
	L	H	H	L	BA	Burst Stop	NOP
	L	H	L	H	BA, CA, A10	READ / READA	Begin Read, Latch CA, Determine Auto -precharge
	L	H	L	L	BA, CA, A10	WRITE / WRITEA	Begin Write, Latch CA, Determine Auto -precharge
	L	L	H	H	BA, RA	Active	Bank Active/ILLEGAL*2
	L	L	H	L	BA, A10	PRE / PREA	Precharge/Precharge All
	L	L	L	H	X	Refresh	ILLEGAL
	L	L	L	L	Op-Code Mode-Add	MRS	ILLEGAL
READ	H	X	X	X	X	DESEL	NOP (Continue Burst to END)
	L	H	H	H	X	NOP	NOP (Continue Burst to END)
	L	H	H	L	BA	Burst Stop	Terminate Burst
	L	H	L	H	BA, CA, A10	READ / READA	Terminate Burst, Latch CA, Begin New Read, Determine Auto-Precharge*3
	L	H	L	L	BA, CA, A10	WRITE / WRITEA	ILLEGAL
	L	L	H	H	BA, RA	Active	Bank Active/ILLEGAL*2
	L	L	H	L	BA, A10	PRE / PREA	Terminate Burst, Precharge
	L	L	L	H	X	Refresh	ILLEGAL
	L	L	L	L	Op-Code Mode-Add	MRS	ILLEGAL

Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address	Command	Action
WRITE	H	X	X	X	X	DESEL	NOP (Continue Burst to end)
	L	H	H	H	X	NOP	NOP (Continue Burst to end)
	L	H	H	L	BA	Burst Stop	ILLEGAL
	L	H	L	H	BA, CA, A10	READ/READA	Terminate Burst With DM=High, Latch CA, Begin Read, Determine Auto-Precharge*3
	L	H	L	L	BA, CA, A10	WRITE/WRITEA	Terminate Burst, Latch CA, Begin new Write, Determine Auto-Precharge*3
	L	L	H	H	BA, RA	Active	Bank Active/ILLEGAL*2
	L	L	H	L	BA, A10	PRE / PREA	Terminal Burst With DM=High, Precharge
	L	L	L	H	X	Refresh	ILLEGAL
	L	L	L	L	Op-Code Mode-Add	MRS	ILLEGAL
READ with AUTO PRECHARGE	H	X	X	X	X	DESEL	NOP (Continue Burst to end)
	L	H	H	H	X	NOP	NOP (Continue Burst to end)
	L	H	H	L	BA	Burst Stop	ILLEGAL
	L	H	L	H	BA, CA, A10	READ	READ*7
	L	H	L	L	BA, CA, A10	WRITE	ILLEGAL
	L	L	H	H	BA, RA	Active	Bank Active/ILLEGAL*2
	L	L	H	L	BA, A10	PRE / PREA	ILLEGAL*2
	L	L	L	H	X	Refresh	ILLEGAL
	L	L	L	L	Op-Code Mode-Add	MRS	ILLEGAL
WRITE with AUTO PRECHARGE	H	X	X	X	X	DESEL	NOP (Continue Burst to END)
	L	H	H	H	X	NOP	NOP (Continue Burst to END)
	L	H	H	L	BA	Burst Stop	ILLEGAL
	L	H	L	H	BA, CA, A10	READ	ILLEGAL
	L	H	L	L	BA, CA, A10	WRITE	Write
	L	L	H	H	BA, RA	Active	Bank Active/ILLEGAL*2
	L	L	H	L	BA, A10	PRE / PREA	ILLEGAL*2
	L	L	L	H	X	Refresh	ILLEGAL
	L	L	L	L	Op-Code Mode-Add	MRS	ILLEGAL

Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address	Command	Action
PRE-CHARGING	H	X	X	X	X	DESEL	NOP (Idle after t_{RP})
	L	H	H	H	X	NOP	NOP (Idle after t_{RP})
	L	H	H	L	BA	Burst Stop	ILLEGAL*2
	L	H	L	X	BA, CA, A10	READ/WRITE	ILLEGAL*2
	L	L	H	H	BA, RA	Active	ILLEGAL*2
	L	L	H	L	BA, A10	PRE / PREA	NOP*4 (Idle after t_{RP})
	L	L	L	H	X	Refresh	ILLEGAL
	L	L	L	L	Op-Code Mode-Add	MRS	ILLEGAL
ROW ACTIVATING	H	X	X	X	X	DESEL	NOP (ROW Active after t_{RCD})
	L	H	H	H	X	NOP	NOP (ROW Active after t_{RCD})
	L	H	H	L	BA	Burst Stop	ILLEGAL*2
	L	H	L	X	BA, CA, A10	READ / WRITE	ILLEGAL*2
	L	L	H	H	BA, RA	Active	ILLEGAL*2
	L	L	H	L	BA, A10	PRE / PREA	ILLEGAL*2
	L	L	L	H	X	Refresh	ILLEGAL
	L	L	L	L	Op-Code Mode-Add	MRS	ILLEGAL
WRITE RECOVERING	H	X	X	X	X	DESEL	NOP
	L	H	H	H	X	NOP	NOP
	L	H	H	L	BA	Burst Stop	ILLEGAL*2
	L	H	L	H	BA, CA, A10	READ	ILLEGAL*2
	L	H	L	L	BA, CA, A10	WRITE	WRITE
	L	L	H	H	BA, RA	Active	ILLEGAL*2
	L	L	H	L	BA, A10	PRE / PREA	ILLEGAL*2
	L	L	L	H	X	Refresh	ILLEGAL
	L	L	L	L	Op-Code Mode-Add	MRS	ILLEGAL

Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address	Command	Action
RE-FRESHING	H	X	X	X	X	DESEL	NOP (Idle after t_{RP})
	L	H	H	H	X	NOP	NOP (Idle after t_{RP})
	L	H	H	L	BA	Burst Stop	ILLEGAL
	L	H	L	X	BA, CA, A10	READ/WRITE	ILLEGAL
	L	L	H	H	BA, RA	Active	ILLEGAL
	L	L	H	L	BA, A10	PRE / PREA	ILLEGAL
	L	L	L	H	X	Refresh	ILLEGAL
	L	L	L	L	Op-Code Mode-Add	MRS	ILLEGAL
MODE REGISTER SETTING	H	X	X	X	X	DESEL	NOP (Idle after t_{RP})
	L	H	H	H	X	NOP	NOP (Idle after t_{RP})
	L	H	H	L	BA	Burst Stop	ILLEGAL
	L	H	L	X	BA, CA, A10	READ / WRITE	ILLEGAL
	L	L	H	H	BA, RA	Active	ILLEGAL
	L	L	H	L	BA, A10	PRE / PREA	ILLEGAL
	L	L	L	H	X	Refresh	ILLEGAL
	L	L	L	L	Op-Code Mode-Add	MRS	ILLEGAL

ABBREVIATIONS :

H = High Level, L = Low level, V = Valid, X = Don't Care

BA = Bank Address, RA =Row Address, CA = Column Address, NOP = No Operation

Note :

1. All entries assume that CKE was High during the preceding clock cycle and the current clock cycle.
2. ILLEGAL to bank in specified state; function may be legal in the bank indicated by BA, depending on the state of the bank.
3. Must satisfy bus contention, bus turn around and write recovery requirements.
4. NOP to bank precharging or in idle state. May precharge bank indicated by BA.
5. ILLEGAL of any bank is not idle.
6. Same bank's previous auto precharg will not be performed. But if the bank is different, previous auto precharge will be performed.
7. Refer to "Read with Auto Precharge: for more detailed information.
   ILLEGAL = Device operation and / or data integrity are not guaranteed.

Current State	CKE n-1	CKE n	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Add	Action
SELF-REFRESHING*1	H	X	X	X	X	X	X	INVALID
	L	H	H	X	X	X	X	Exit Self-Refresh
	L	H	L	H	H	H	X	Exit Self-Refresh
	L	H	L	H	H	L	X	ILLEGAL
	L	H	L	H	L	X	X	ILLEGAL
	L	H	L	L	X	X	X	ILLEGAL
	L	L	X	X	X	X	X	NOP (Maintain Self-Refresh)
POWER DOWN	H	X	X	X	X	X	X	INVALID
	L	H	X	X	X	X	X	Exit Power Down
	L	L	X	X	X	X	X	NOP (Maintain Power Down)
DEEP POWER DOWN	H	X	X	X	X	X	X	INVALID
	L	H	H	X	X	X	X	Exit Deep Power Down *3
	L	L	X	X	X	X	X	NOP (Maintain Deep Power Down)
ALL BANKS IDLE*2	H	H	X	X	X	X	X	Refer to Function True Table
	H	L	L	L	L	H	X	Enter Self-Refresh
	H	L	H	X	X	X	X	Exit Power Down
	H	L	L	H	H	H	X	Exit Power Down
	H	L	L	H	H	L	X	ILLEGAL
	H	L	L	H	L	X	X	ILLEGAL
	H	L	L	L	X	X	X	ILLEGAL
	L	L	L	X	X	X	X	Refer to Current State = Power Down
ANY STATE other than listed above	H	H	X	X	X	X	X	Refer to Function True Table

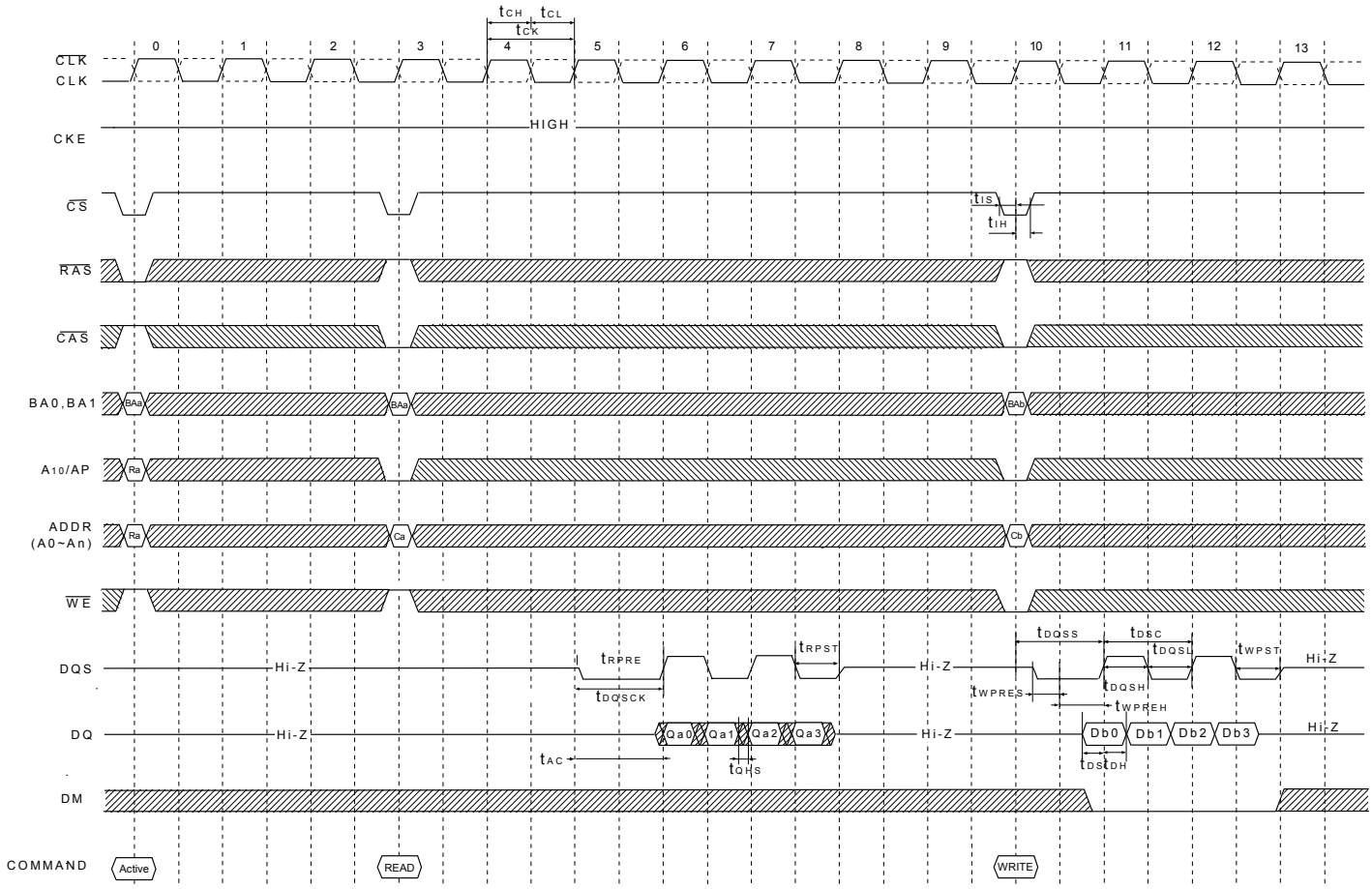
ABBREVIATIONS :

H = High Level, L = Low level, V = Valid, X = Don't Care

Note :

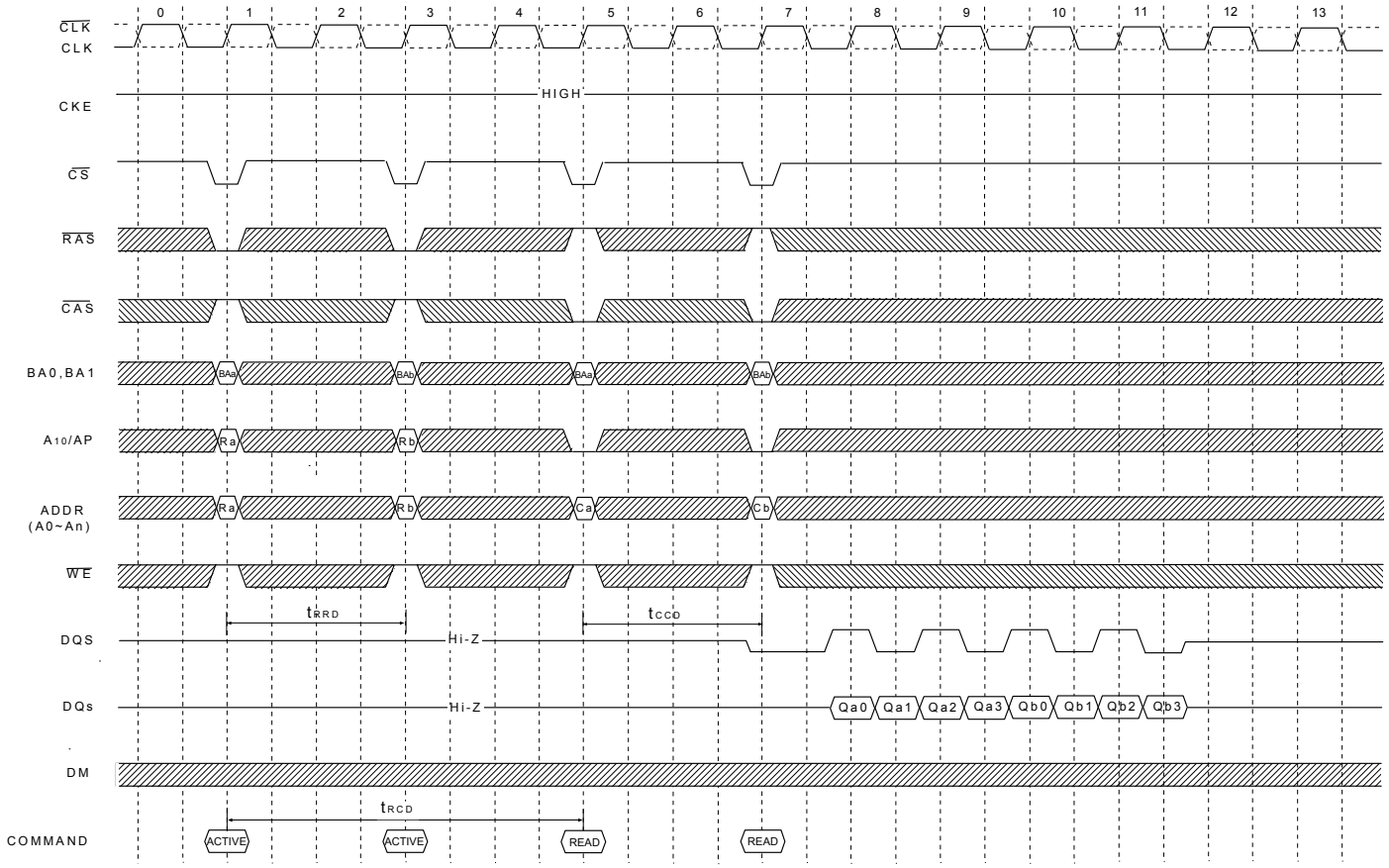
1. CKE Low to High transition will re-enable CLK, $\overline{CLK}$ and other inputs asynchronously. A minimum setup time must be satisfied before issuing any command other than EXIT.
2. Power-Down and Self-Refresh can be entered only from All Bank Idle state.
3. The Deep Power Down mode is exited by asserting CKE high and full initialization is required after exiting Deep Power Down mode.

Basic Timing (Setup, Hold and Access Time @ BL=4, CL=3)

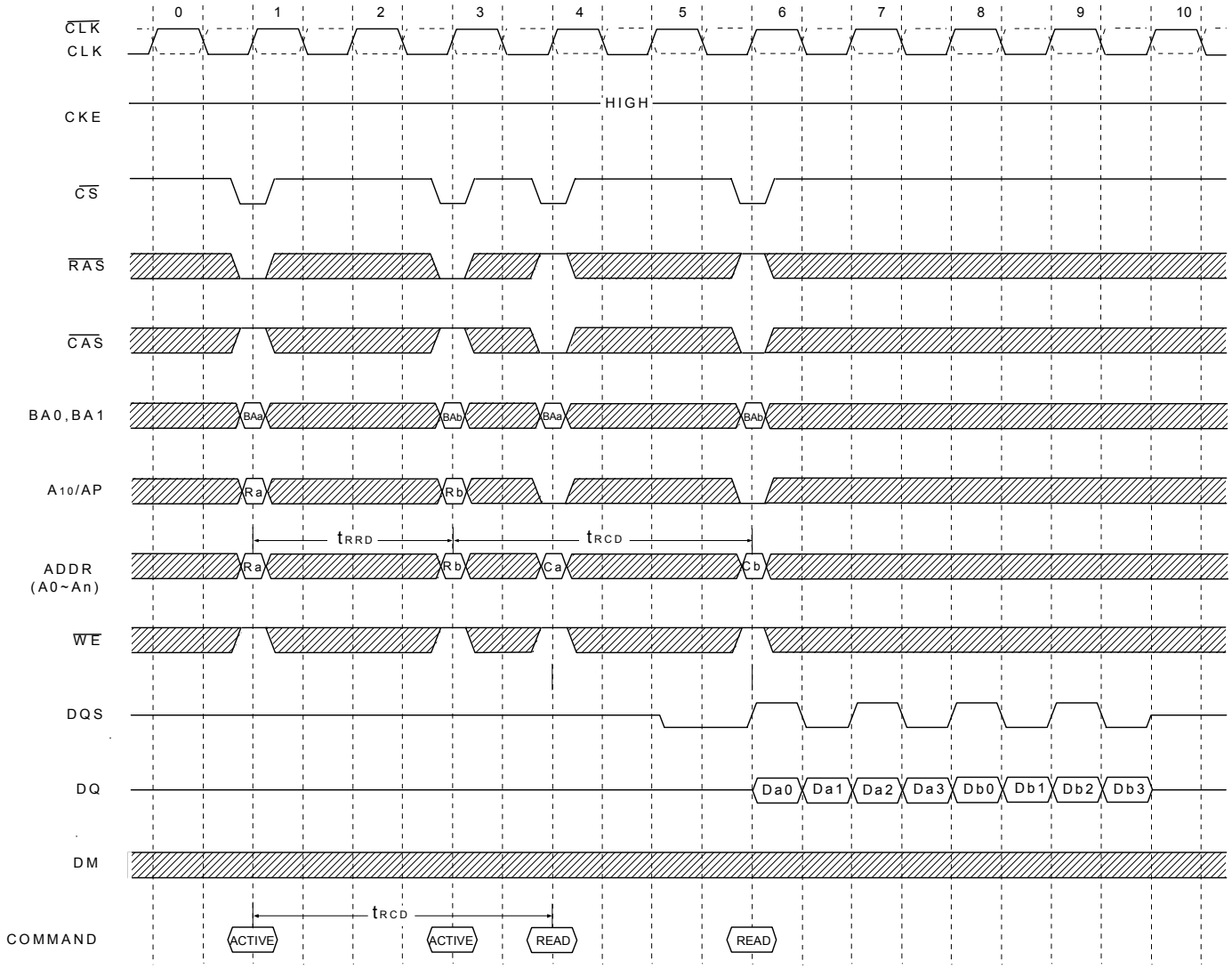


Note 1. t_{HP} is lesser of t_{CL} or t_{CH} clock transition collectively when a bank is active.

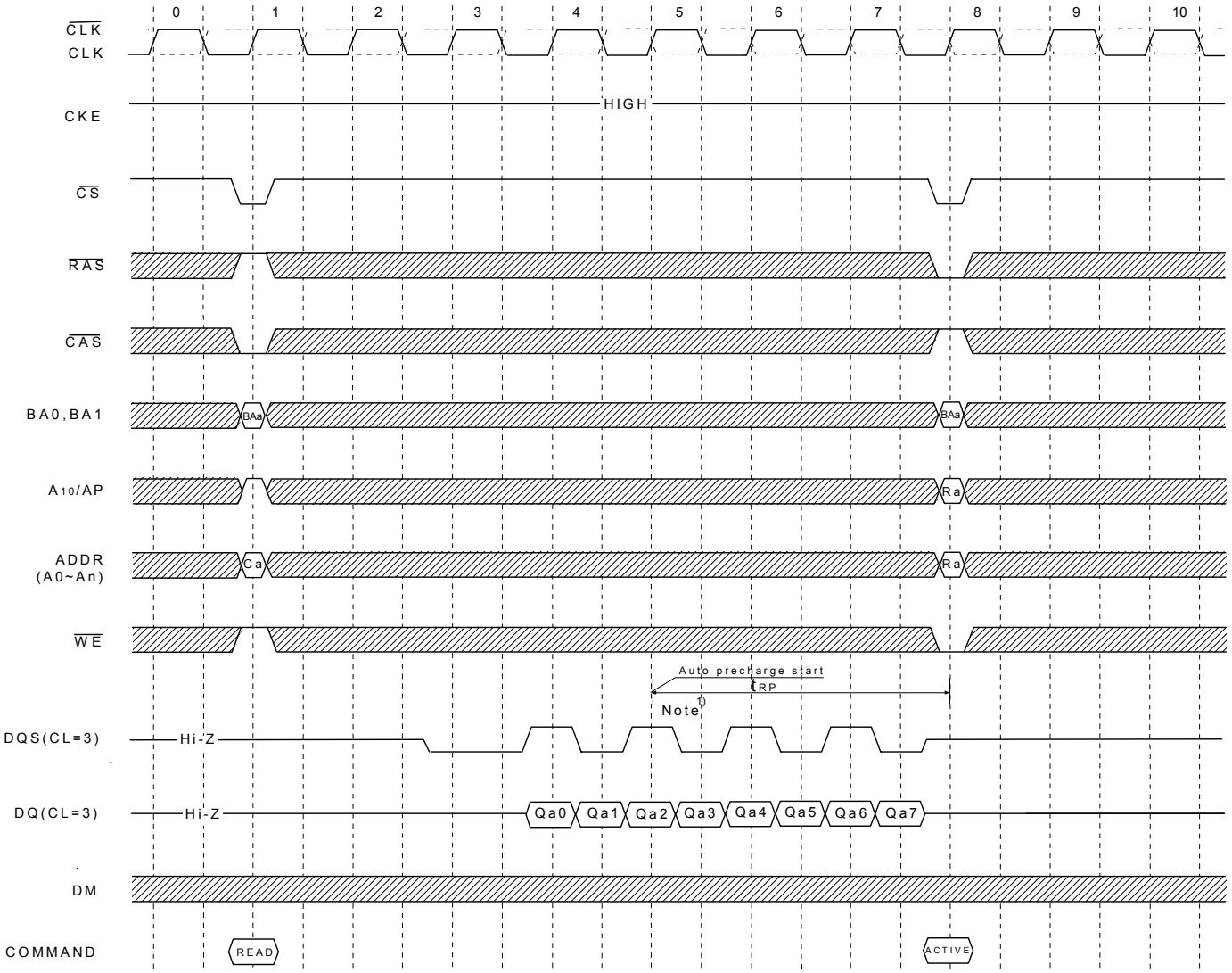
Multi Bank Interleaving READ (@BL=4, CL=3)



Multi Bank Interleaving WRITE (@BL=4)

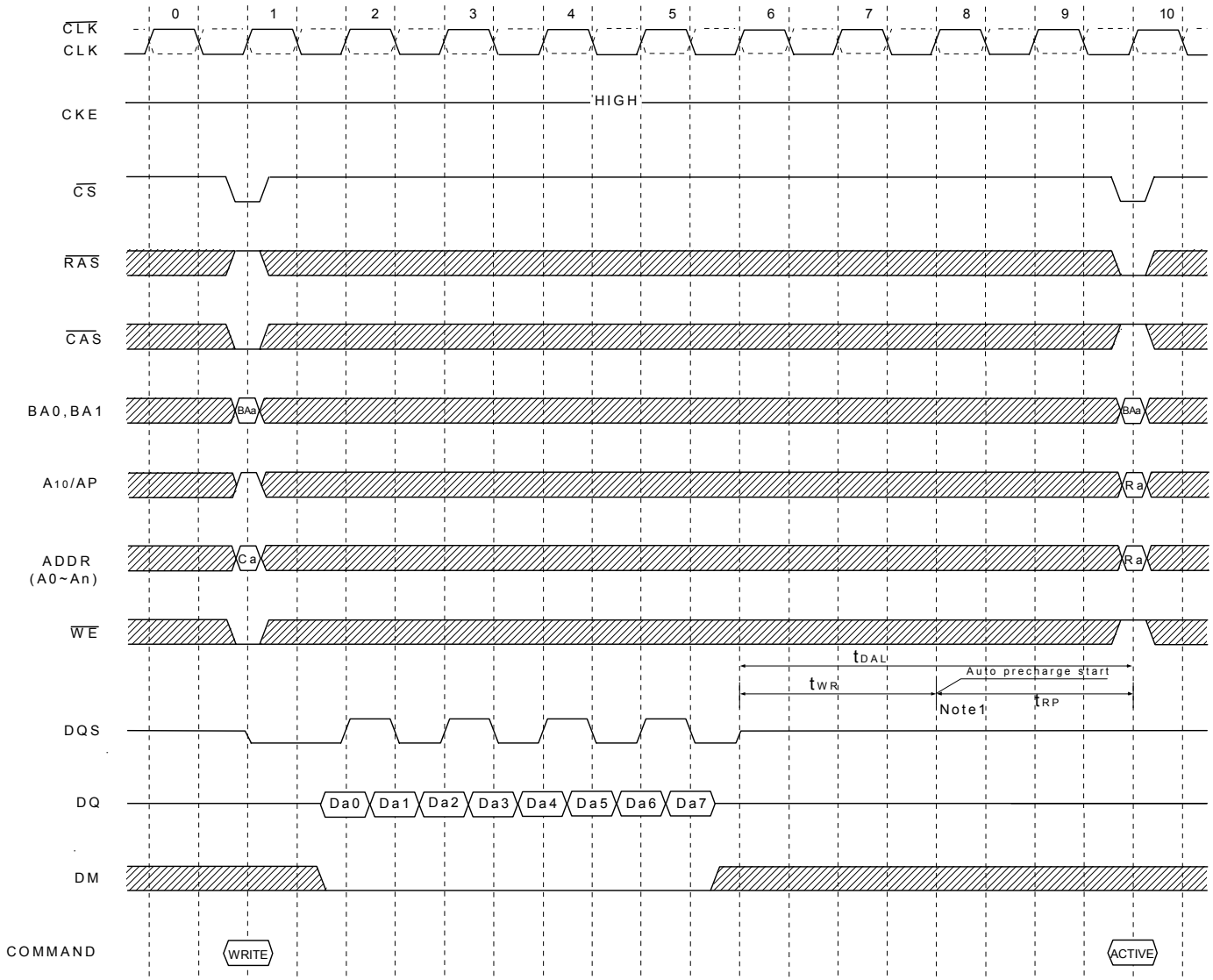


Read with Auto Precharge (@BL=8)



Note 1. The row active command of the precharge bank can be issued after t_{RP} from this point.
The new read/write command of another activated bank can be issued from this point.
At burst read/write with auto precharge, $\overline{CAS}$ interrupt of the same bank is illegal.

Write with Auto Precharge (@BL=8)



Note 1. The row active command of the precharge bank can be issued after t_{RP} from this point.
The new read/write command of another activated bank can be issued from this point.
At burst read/write with auto precharge, $\overline{CAS}$ interrupt of the same/another bank is illegal.

Read Interrupted by Precharge (@BL=8)

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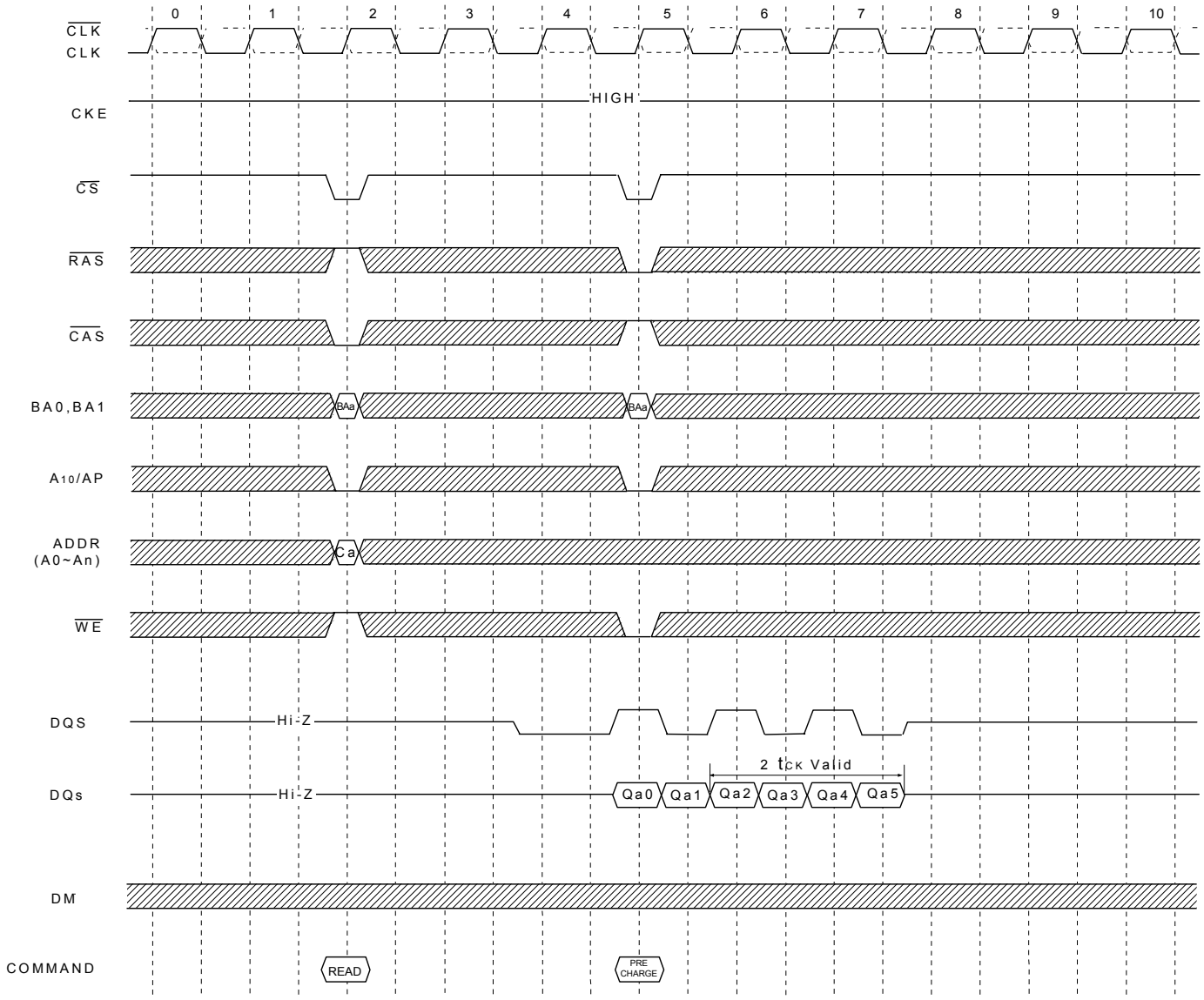
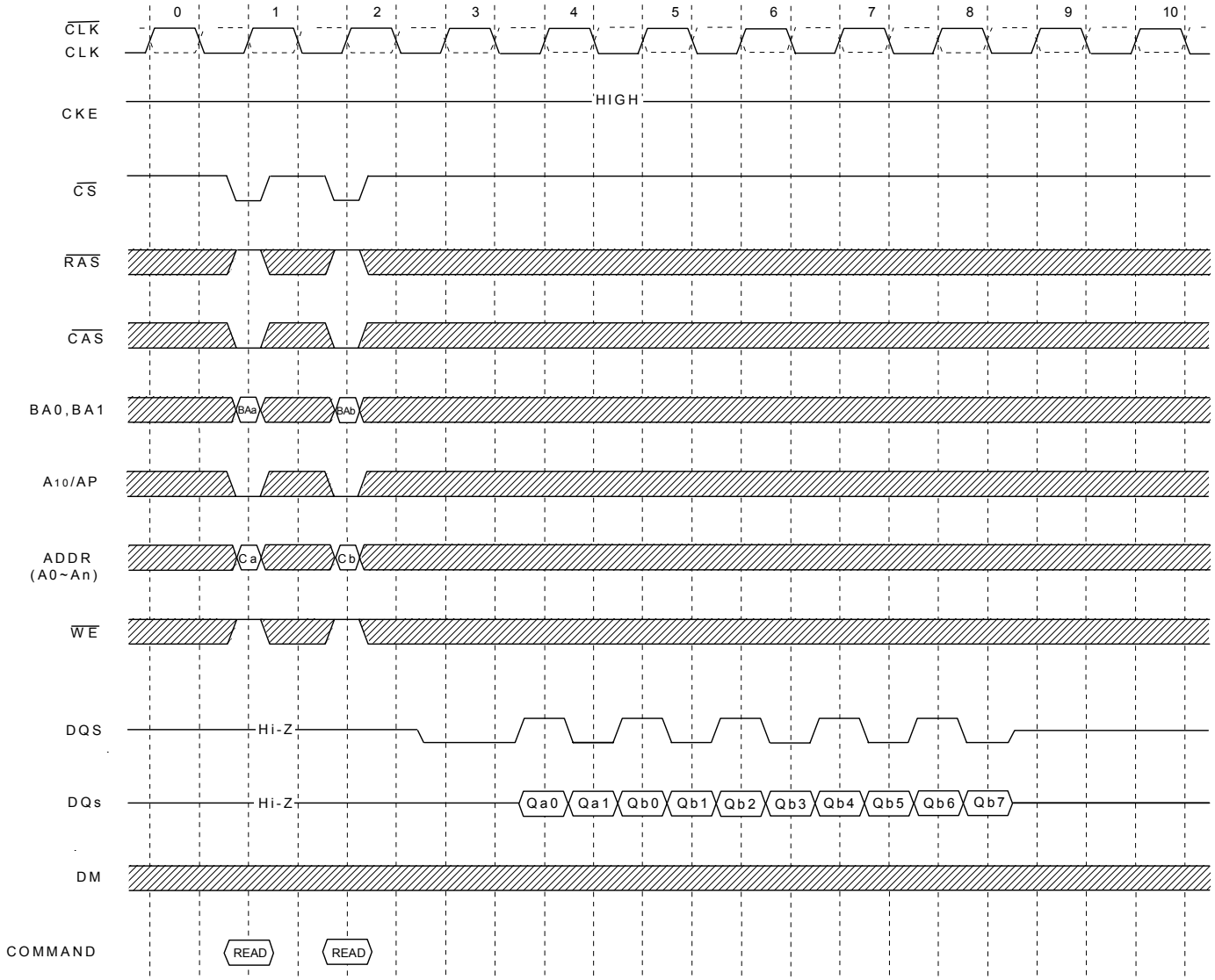
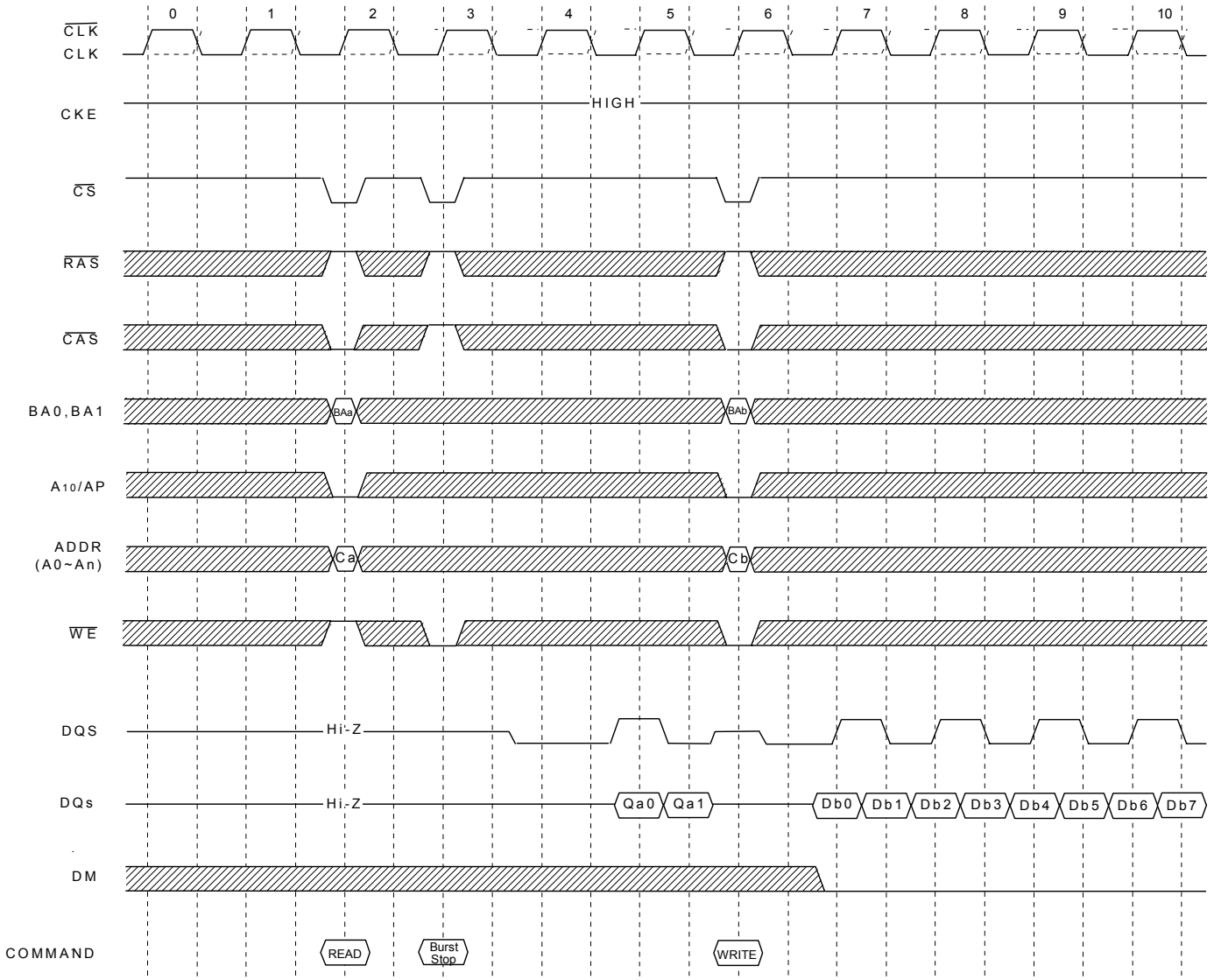


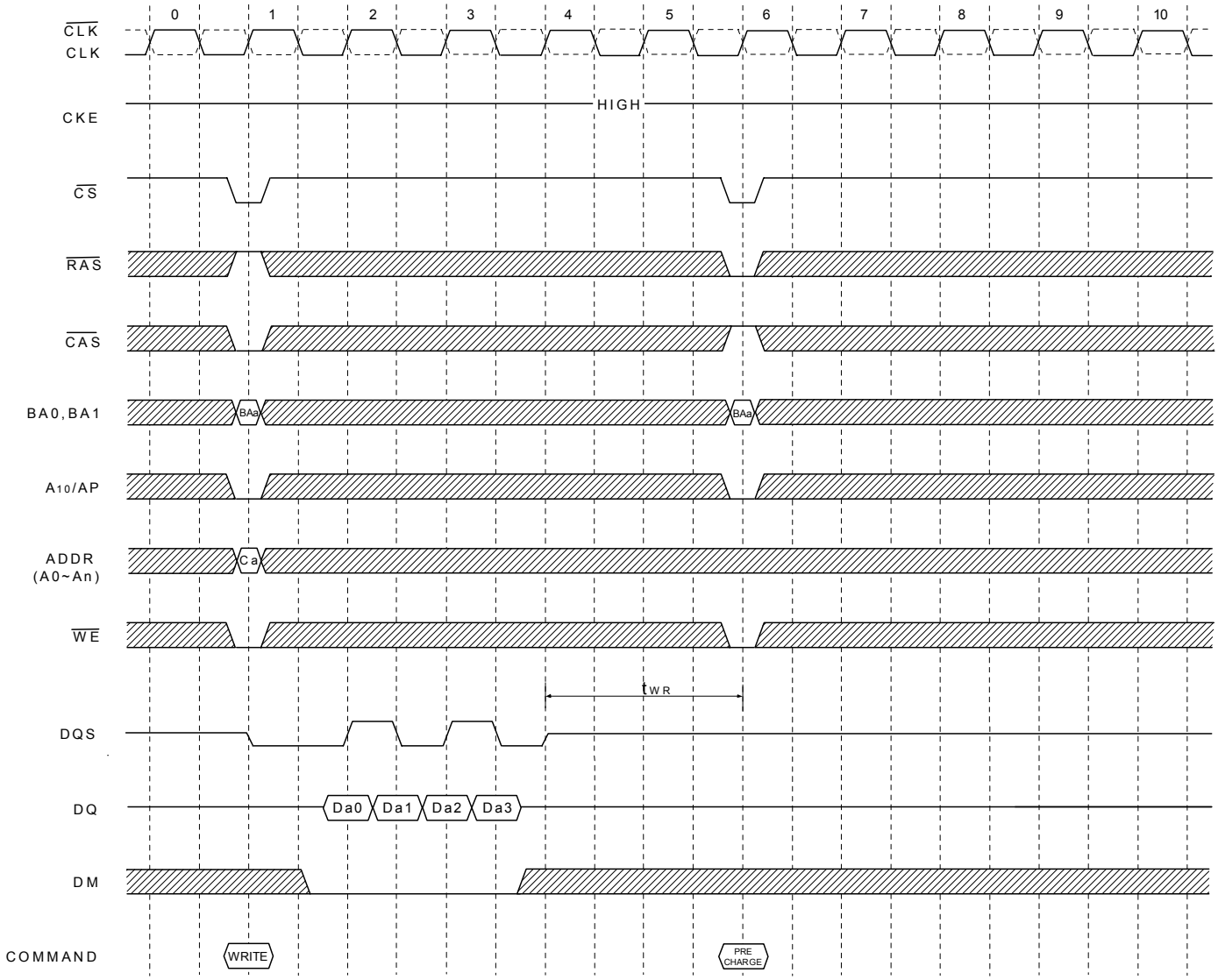
Read Interrupted by a Read (@BL=8, CL=3)



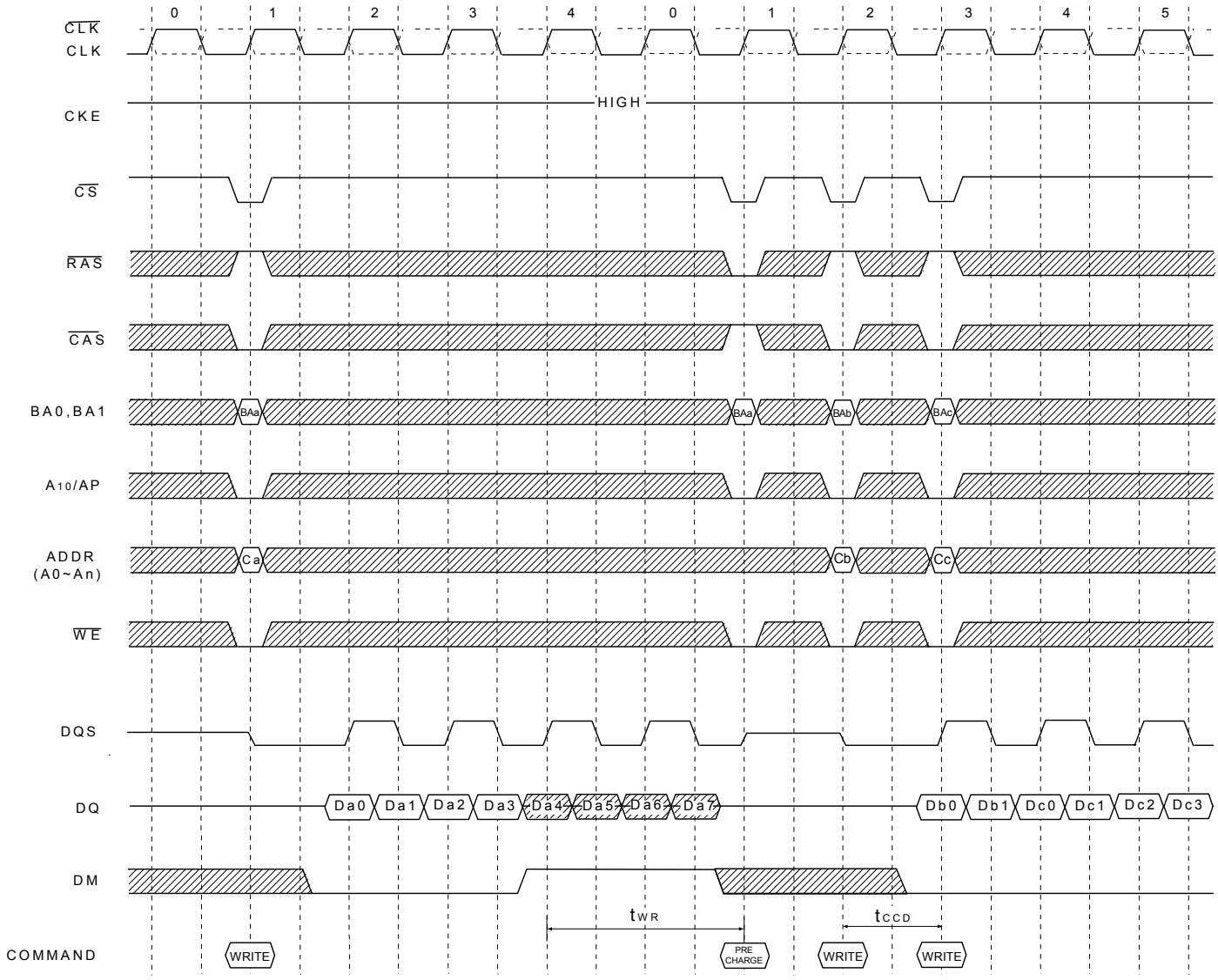
Read Interrupted by a Write & Burst stop (@BL=8, CL=3)



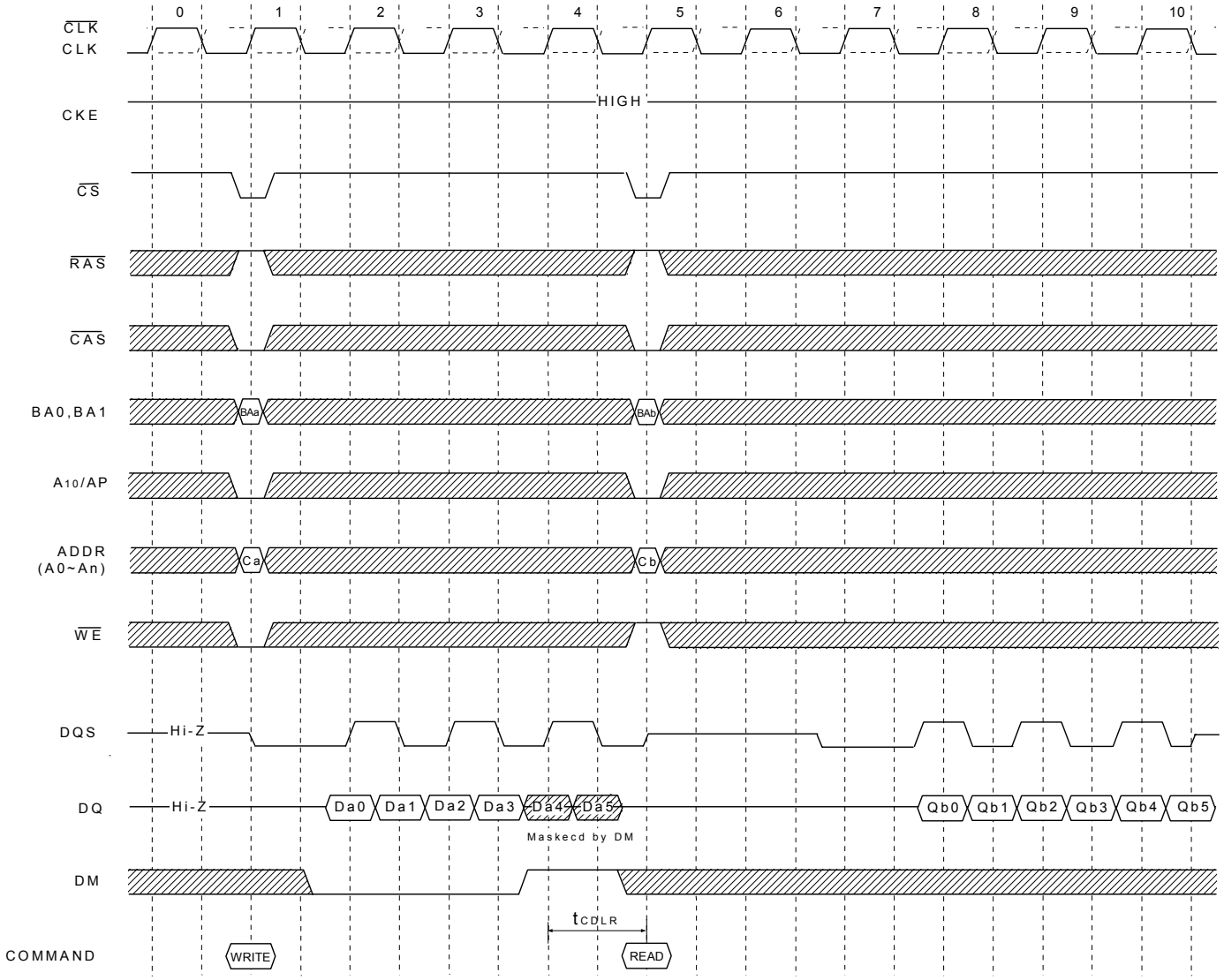
Write followed by Precharge (@BL=4)



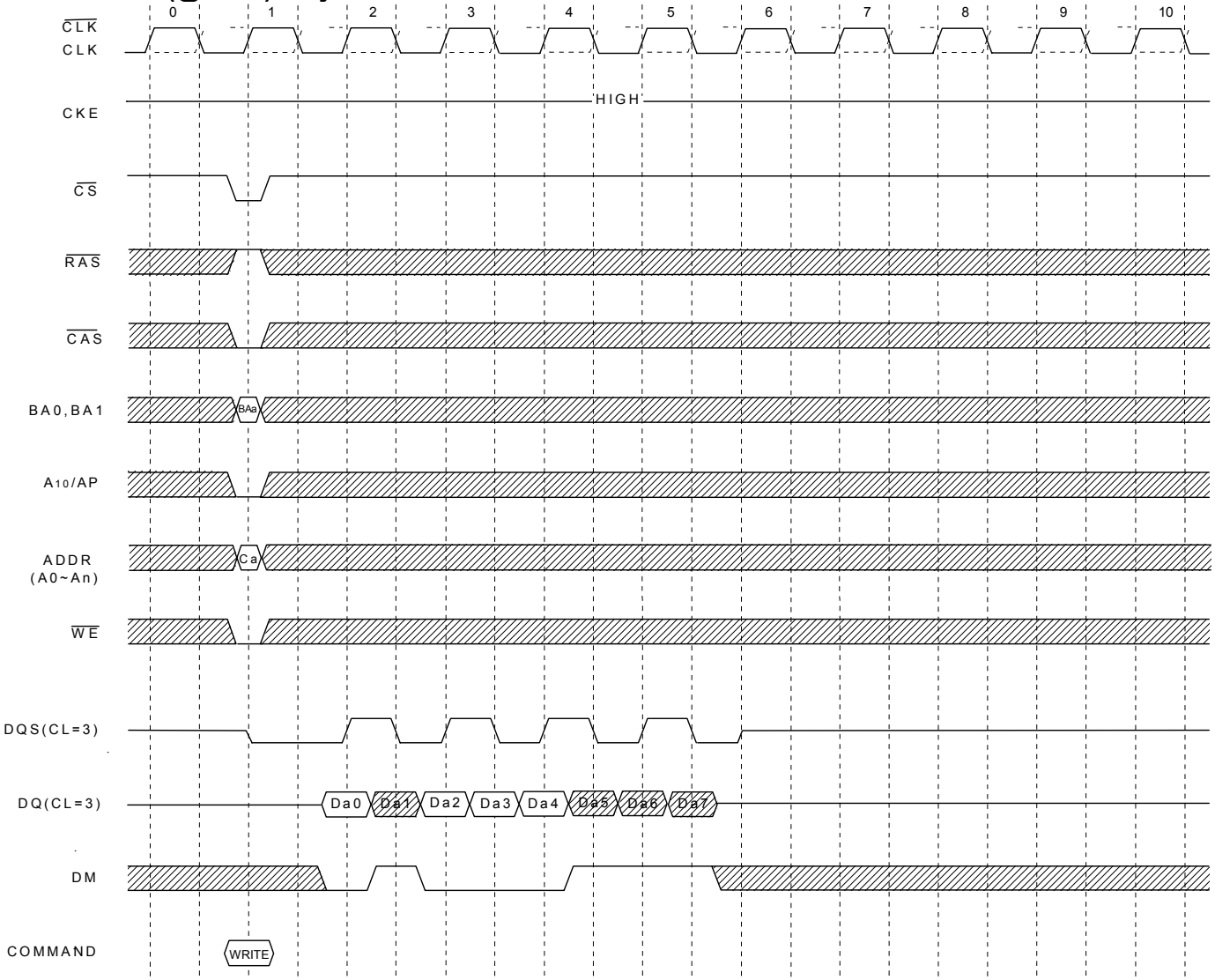
Write Interrupted by Precharge & DM (@BL=8)



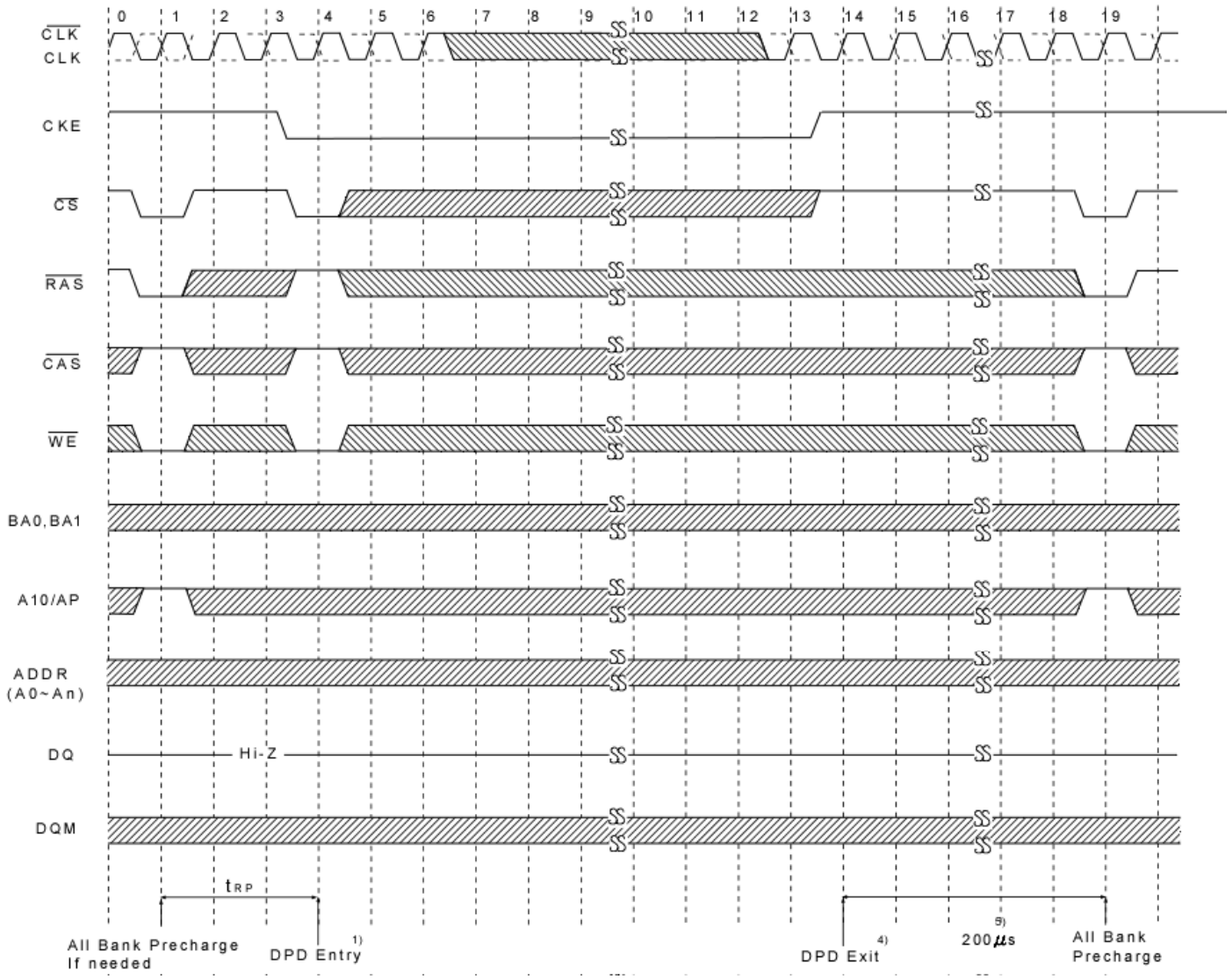
Write Interrupted by a Read (@BL=8, CL=3)



DM Function (@BL=8) only for write



Deep Power Down Mode Entry & Exit Cycle



Note :

DEFINITION OF DEEP POWER MODE FOR Mobile DDR SDRAM :
Deep Power Down Mode is an operating mode to achieve maximum power reduction by cutting the power of the whole memory of the device. Once the device enters in Deep Power Down Mode, data will not be retained. Full initialization is required when the device exits from Deep Power Down Mode.

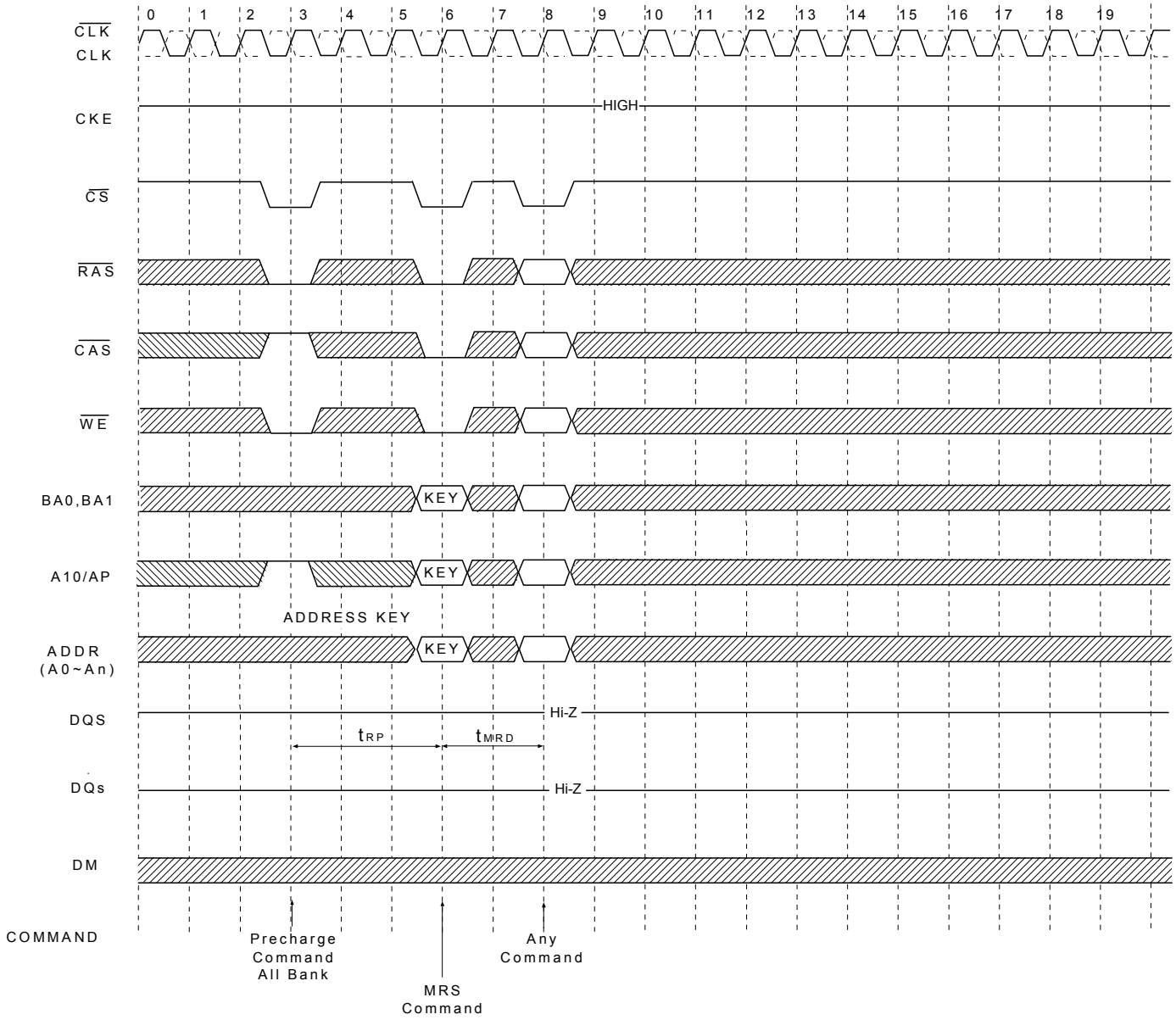
TO ENTER DEEP POWER DOWN MODE

1) The deep power down mode is entered by having $\overline{CS}$ and held low with $\overline{RAS}$ and $\overline{CAS}$ high at the rising edge of the clock. While CKE is low.
2) Clock must be stable before exited deep power down mode.
3) Device must be in the all banks idle state prior to entering Deep Power Down mode.

TO EXIT DEEP POWER DOWN MODE

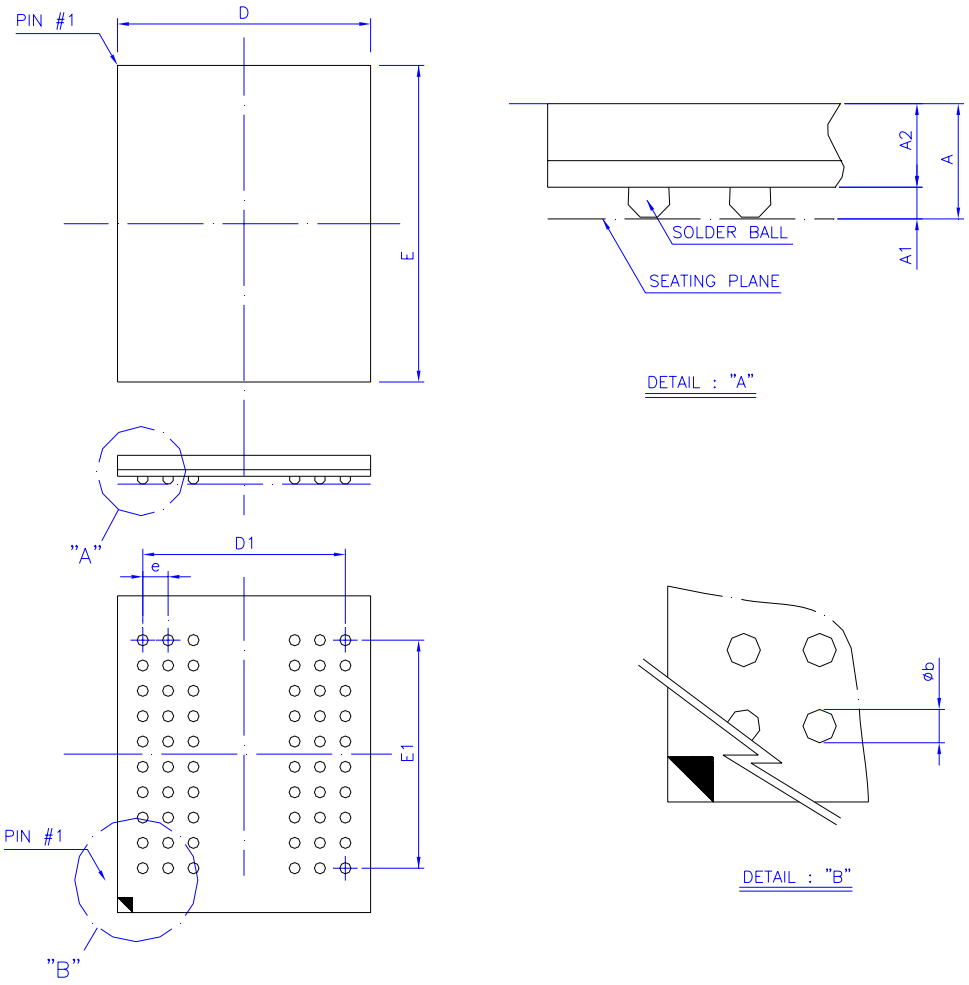
4) The deep power down mode is exited by asserting CKE high.
5) In case of 2/CS, 2CKE device with 2/CS & 2CKE, 200 μs wait tine is required even if only 1 device exits from Deep Power Down.
6) Upon exiting deep power down an all bank precharge command must be issued followed by two auto refresh commands and a load mode register sequence.

Mode Register Set



PACKING DIMENSIONS

60-BALL DDR SDRAM (8x10 mm)

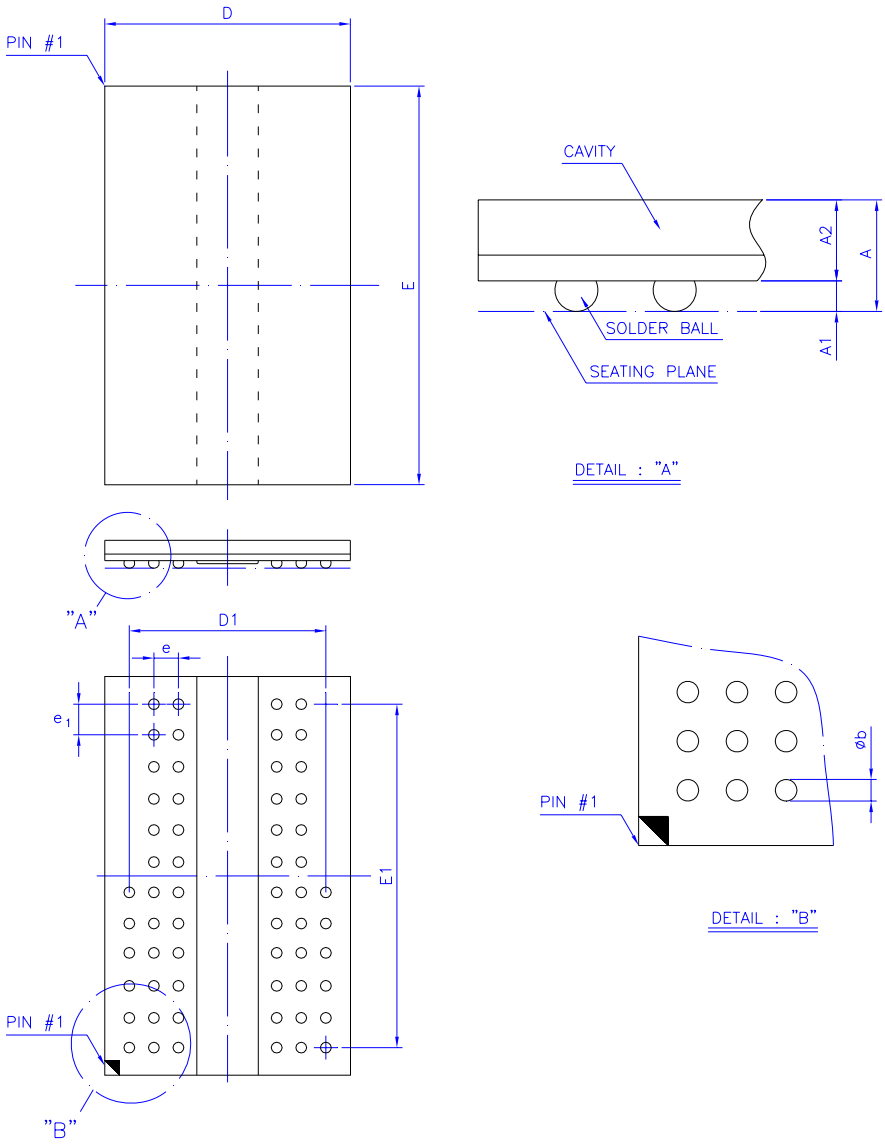


Symbol	Dimension in mm			Dimension in inch		
	Min	Norm	Max	Min	Norm	Max
A	——	——	1.00	——	——	0.039
A_1	0.25	0.30	0.35	0.010	0.012	0.014
A_2	——	0.66	——	——	0.026	——
Φ_b	0.35	0.40	0.45	0.014	0.016	0.018
D	7.95	8.00	8.05	0.313	0.315	0.317
E	9.95	10.00	10.05	0.392	0.394	0.396
D_1	6.40 BSC			0.252 BSC		
E_1	7.20 BSC			0.283 BSC		
e	0.80 BSC			0.031 BSC		

Controlling dimension : Millimeter.

PACKING DIMENSIONS

60-BALL DDR SDRAM (8x13 mm)



Symbol	Dimension in mm			Dimension in inch		
	Min	Norm	Max	Min	Norm	Max
A	——	——	1.20	——	——	0.047
A_1	0.30	0.35	0.40	0.012	0.014	0.016
A_2	——	——	0.80	——	——	0.031
Φ_b	0.40	0.45	0.50	0.016	0.018	0.020
D	7.90	8.00	8.10	0.311	0.315	0.319
E	12.90	13.00	13.10	0.508	0.512	0.516
D_1	——	6.40	——	——	0.252	——
E_1	——	11.0	——	——	0.433	——
e	——	0.80	——	——	0.031	——
e_1	——	1.00	——	——	0.039	——

Controlling dimension : Millimeter.

Revision History

Revision	Date	Description
1.0	2007.11.16	Original
1.1	2008.01.02	1. Change BGA package 2. Modify tIS
1.2	2008.01.16	Add 8x10mm BGA package
1.3	2008.06.13	1. Move Revision History to the last 2. Modify tIS
1.4	2008.09.01	Modify the arrangement of 60 Ball BGA (ball F1 : V_{REF} => NC)

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