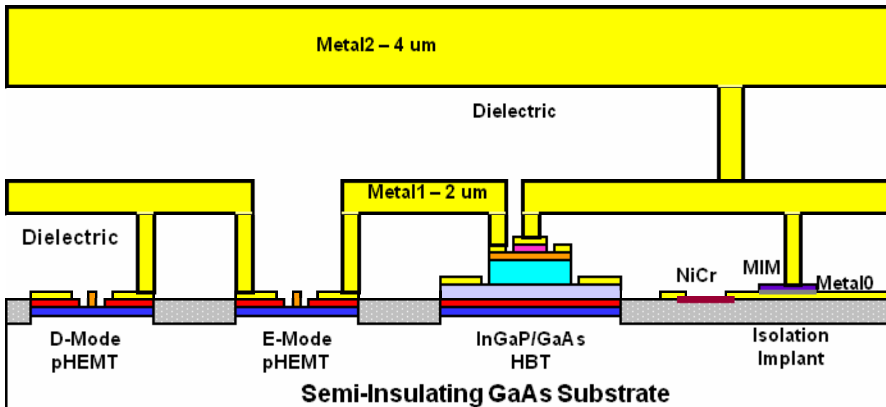
TriQuint SEMICONDUCTOR

TQBiHEMT

Combined 0.7µm E/D pHEMT & 2µm HBT Foundry Service



TQBiHEMT Process Cross-Section

General Description

TriQuint's TQBiHEMT process is based on our production-released 0.7 µm TQPED and TQHBT3.1 processes. TQPED includes E-Mode and D-Mode pHEMT transistors. TQHBT3.1 is a 2 µm emitter InGaP HBT process designed for high ruggedness, high power applications. TQBiHEMT combines both processes onto a single wafer, enabling designers to integrate highly efficient, high power InGaP HBT PAs onto a single die with switches, LNAs, mixers and other functions that exhibit higher performance with a pHEMT realization. This process is targeted for integration of power amplifiers with linear, low loss and high isolation RF switch applications, converters and integrated RF Front Ends. The three metal interconnecting layers are encapsulated in a high performance dielectric that allows wiring flexibility, optimized die size and plastic packaging simplicity. Precision NiCr resistors and high value MIM capacitors are included allowing higher levels of integration, while maintaining smaller, cost – effective die sizes.

Features

- E-Mode, 0.30 V, Vth
- D-Mode, -0.8 V Vp
- InGaAs Active Layer pHEMT Process + InGaP HBT
- 0.7 µm Optical Lithography- Gates
- 2 µm Optical Lithography- Emitters; Beta = 75
- High Density Interconnects:
  - 2 Global
  - 1 Local
- High-Q Passives
- Thin Film Resistors
- High Value Capacitors (1200 pF/µm^2)
- Backside Vias Optional
- Based on Production TQPED pHEMT and TQHBT3.1 HBT

Applications

- Integration of Highly Efficient and Linear Power Amplifiers
- Low Loss, High Isolation, Low-Harmonic Content Switches
- Integrated digital control logic for Switches and Transceivers
- Converters
- Integrated RF Front Ends– LNA, SW, PA
- Wireless Transceivers, Base stations, Direct Broadcast Satellite Radars, Digital Radios, RF / Mixed Signal ICs
- Power Detectors and Couplers

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TQBiHEMT Process Details

Transistor Details @ Vds = 3.0V			
Element	Parameter	Typical*	Units
D-Mode pHEMT	Vp (1uA/um)	-0.8	V
	Idss	160	mA/mm
	Imax	430	mA/mm
	Breakdown, Vdg	10 min, 18 typ	V
	Ft @ 50% Idss	21	GHz
	Fmax @ 50% Idss	38	GHz
	Gm (50% Idss)	225	mS/mm
	Ron	2.3	Ohms * mm
E-Mode pHEMT	Vth (1uA/um)	+0.30	V
	Idss (max)	0.01	uA/um
	Imax	175	mA/mm
	Breakdown, Vdg	10 min, 18 typ	V
	Ft @ 50% Idss	20	GHz
	Fmax @ 50% Idss	39	GHz
	Gm (50% Imax)	355	mS/mm
	Ron	3.0	Ohms * mm
HBT	Beta	75	
	BVcbo	24	v
	Ft	30	GHz
	Fmax	60	GHz
(For a 3x3x45µm unit cell:)	BVceo	14	V
	BVbeo	7	V
Common Process Element Details			
Gate Length		0.7	µm
Interconnect		3	Metal Layers
MIM Caps	Value	1200	pF/mm2
Resistors	NiCr	50	Ohms/sq
	Bulk	360	Ohms/sq

*Values for reference only: Actual specifications subject to change without notice prior to Production Release.

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Maximum Ratings

Parameter	Value	Unit
Storage Temperature Range	-65 to +150	Deg C
Operating Temperature Range	-55 to +150	Deg C
EFET/DFET Transistor (Vs open; Idg = 1uA/um)	10	V
HBT Junction Current Density	20	kA/cm^2
Capacitor	40	V

Prototyping and Development

- Prototype Development Quick Turn (PDQ):
  - Shared mask set
  - Bi-Monthly, starting in 3rd Quarter 2008
  - 5 to 6 week cycle time
- Prototype Wafer Option (PWO):
  - Customer-specific masks; Customer schedule
  - 2 wafers delivered
  - 8 week cycle time

Design Tool Status

- Preliminary Design Manual includes Device Library of circuit elements: FETs, diodes, thin film resistors, capacitors, inductors
- Preliminary Layout Library in GSD II format
- Cadence Development Kit with PCells and Layout Rule Sets for Design Rule Check in Cadence
- Preliminary Design Kit for Agilent's ADS design environment
- Preliminary Design Kit for AWR's Microwave Office design environment planned

Training

- GaAs Design Classes:
  - Half-Day Introduction; Upon request
  - Three-Day Technical Training, typically mid-year.

Process Qualification Status

- New Process based on mature TQPED and TQHBT3.1 150-mm processes
- Process in final stages of development
- Full 150mm wafer Process Qualification by June 2008
- For more information on Quality and Reliability, contact TriQuint or visit: www.triquint.com/company/quality

Applications Support Services

- Tiling of GDSII stream files including PCM
- Design Rule Check services
- Packaging Development Engineering
- Test Development Engineering:
  - On-wafer
  - Packaged parts
- Yield Enhancement Engineering
- Failure Analysis

Manufacturing Services

- Mask making
- Production 150-mm wafer fab
- Wafer Thinning
- Wafer Sawing
- Substrate Vias
- DC Diesort Testing
- Plastic Packaging
- RF Packaged Part Testing

Please contact your local TriQuint Semiconductor Representative/ Distributor or Foundry Services Division for Additional information:
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