

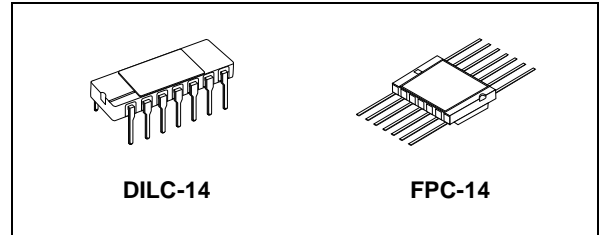
## RAD-HARD DUAL BINARY COUNTER

- HIGH SPEED:  
 $f_{MAX} = 79 \text{ MHz (TYP.) at } V_{CC} = 6V$
- LOW POWER DISSIPATION:  
 $I_{CC} = 4\mu\text{A (MAX.) at } T_A = 25^\circ\text{C}$
- HIGH NOISE IMMUNITY:  
 $V_{NIH} = V_{NIL} = 28\% V_{CC} \text{ (MIN.)}$
- SYMMETRICAL OUTPUT IMPEDANCE:  
 $|I_{OH}| = I_{OL} = 4\text{mA (MIN.)}$
- BALANCED PROPAGATION DELAYS:  
 $t_{PLH} \cong t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE:  
 $V_{CC} \text{ (OPR)} = 2V \text{ to } 6V$
- PIN AND FUNCTION COMPATIBLE WITH 54 SERIES 393
- SPACE GRADE-1: ESA SCC QUALIFIED
- 50 krad QUALIFIED, 100 krad AVAILABLE ON REQUEST
- NO SEL UNDER HIGH LET HEAVY IONS IRRADIATION
- DEVICE FULLY COMPLIANT WITH SCC-9204-074

### DESCRIPTION

The M54HC393 is an high speed CMOS DUAL BINARY COUNTER fabricated with silicon gate C<sup>2</sup>MOS technology.

This counter circuit contains independent ripple carry counters and two 4-bit ripple carry binary



### ORDER CODES

PACKAGE	FM	EM
DILC	M54HC14D	M54HC14D1
FPC	M54HC14K	M54HC14K1

counters, which can be cascaded to create a single divide by 256 counter.

Each 4-bit counter is increases during the high to low transition (negative edge) of the clock input, and each has an independent clear input. When CLEAR is set to low, all four bits of each counter are set to a low level. This enables count truncation and allows the implementation of divide by N counter configurations.

All inputs are equipped with protection circuits against static discharge and transient excess voltage.

### PIN CONNECTION

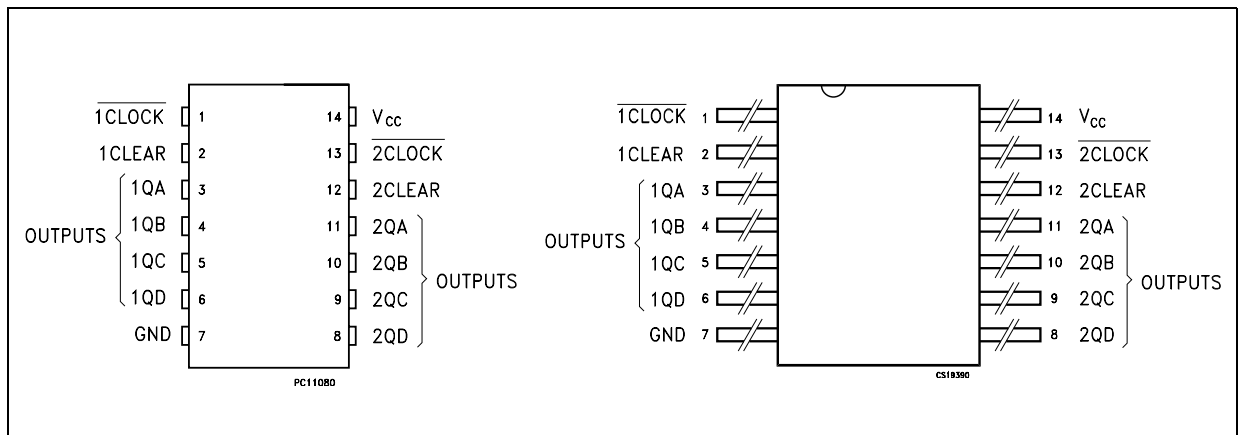


Figure 1: IEC Logic Symbols

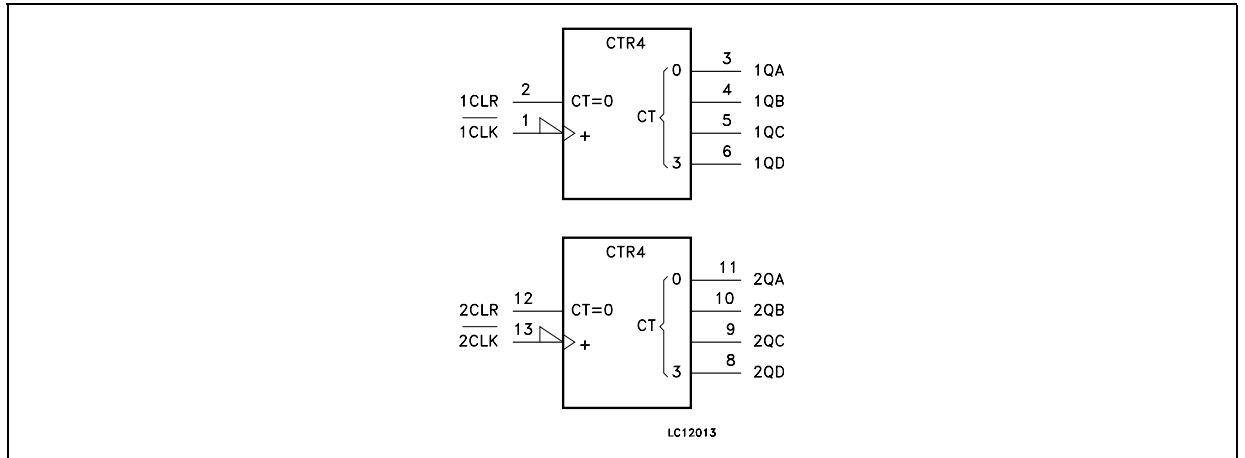


Figure 2: Input And Output Equivalent Circuit

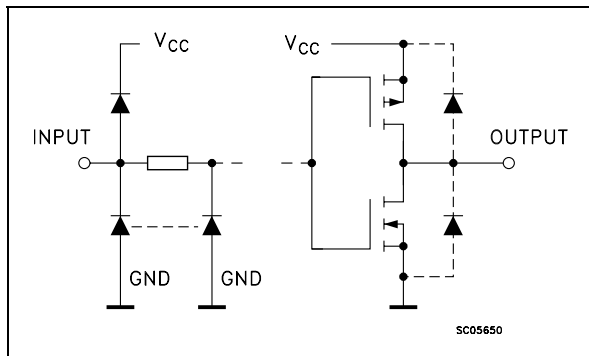




Table 1: Pin Description

PIN N°	SYMBOL	NAME AND FUNCTION
1, 13	$\overline{1 \text{ CLOCK}}$ 2 CLOCK	Clock Input Divide by 2 Section (HIGH to LOW Edge-Triggered)
2, 12	1 CLEAR 2 CLEAR	Asynchronous Master Reset Inputs
3, 4, 5, 6	1QA to 1QD	Flip Flop Outputs
11, 10, 9, 8	2QA to 2QD	Flip Flop Outputs
7	GND	Ground (0V)
14	V <sub>CC</sub>	Positive Supply Voltage

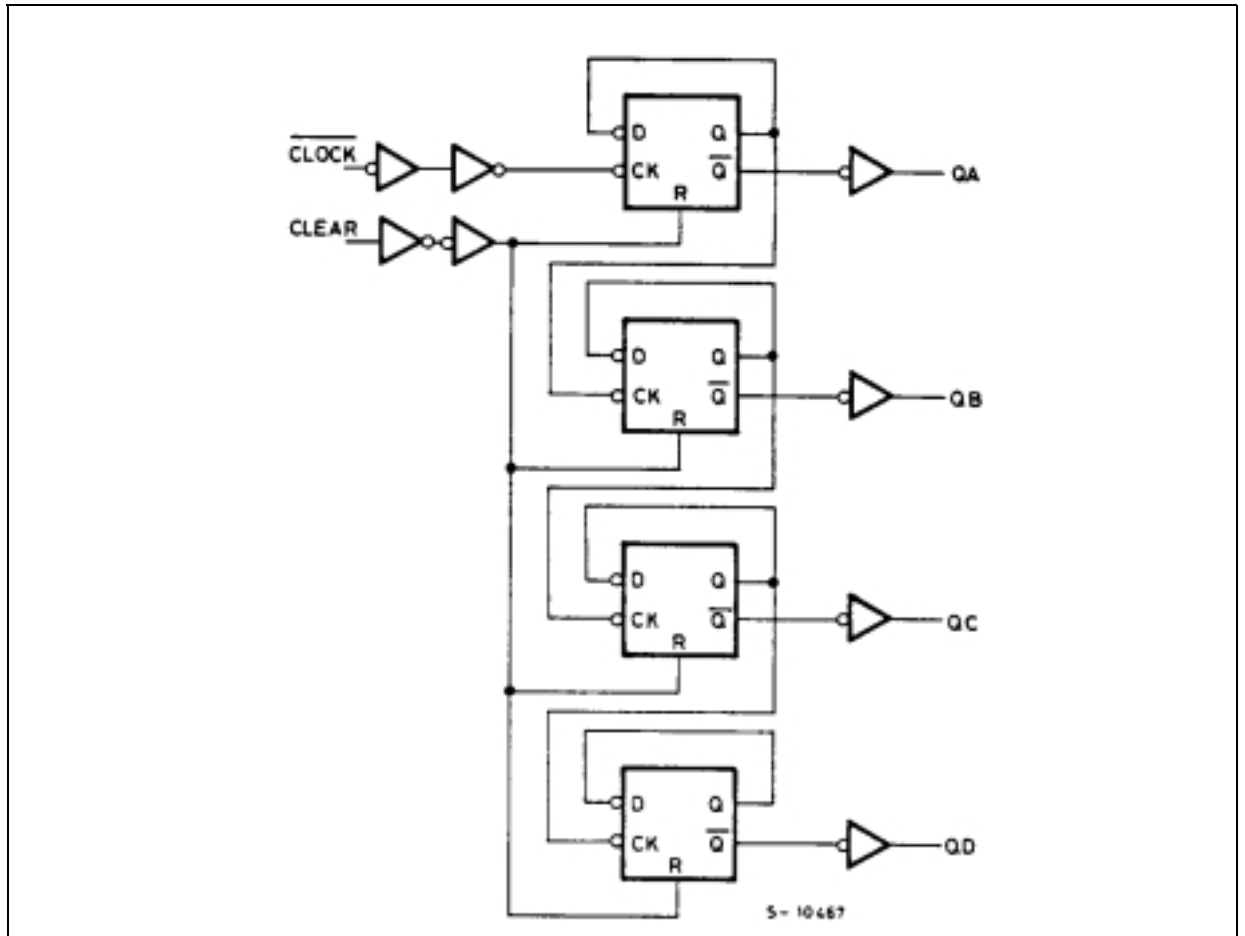
Table 2: Truth Table

INPUTS		OUTPUTS			
$\overline{\text{CLOCK}}$	CLEAR	QD	QC	QB	QA
X	H	L	L	L	L
	L	COUNT UP			
	L	NO CHANGE			

X : Don't Care

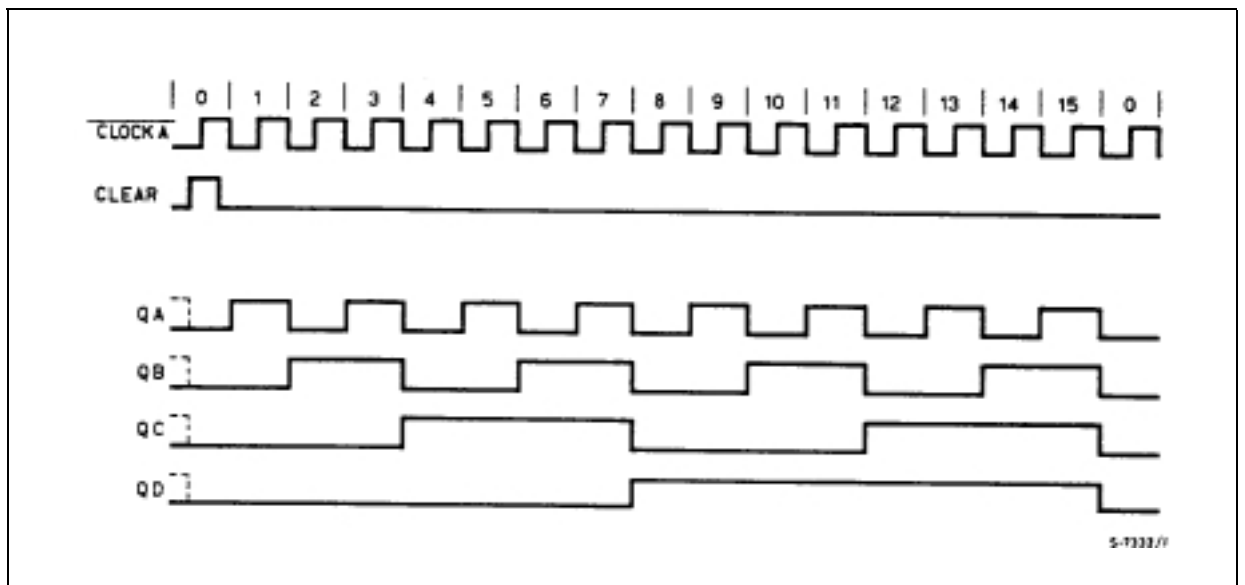
COUNT	OUTPUTS			
	QD	QC	QB	QA
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

Figure 3: Logic Diagram



This logic diagram has not be used to estimate propagation delays

Figure 4: Timing Chart



**Table 3: Absolute Maximum Ratings**

Symbol	Parameter	Value	Unit
$V_{CC}$	Supply Voltage	-0.5 to +7	V
$V_I$	DC Input Voltage	-0.5 to $V_{CC} + 0.5$	V
$V_O$	DC Output Voltage	-0.5 to $V_{CC} + 0.5$	V
$I_{IK}$	DC Input Diode Current	$\pm 20$	mA
$I_{OK}$	DC Output Diode Current	$\pm 20$	mA
$I_O$	DC Output Current	$\pm 25$	mA
$I_{CC}$ or $I_{GND}$	DC $V_{CC}$ or Ground Current	$\pm 50$	mA
$P_D$	Power Dissipation	300	mW
$T_{stg}$	Storage Temperature	-65 to +150	°C
$T_L$	Lead Temperature (10 sec)	265	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied

**Table 4: Recommended Operating Conditions**

Symbol	Parameter	Value	Unit	
$V_{CC}$	Supply Voltage	2 to 6	V	
$V_I$	Input Voltage	0 to $V_{CC}$	V	
$V_O$	Output Voltage	0 to $V_{CC}$	V	
$T_{op}$	Operating Temperature	-55 to 125	°C	
$t_r, t_f$	Input Rise and Fall Time	$V_{CC} = 2.0V$	0 to 1000	ns
		$V_{CC} = 4.5V$	0 to 500	ns
		$V_{CC} = 6.0V$	0 to 400	ns

Table 5: DC Specifications

Symbol	Parameter	Test Condition		Value						Unit	
		V <sub>CC</sub> (V)		T <sub>A</sub> = 25°C			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.		Max.
V <sub>IH</sub>	High Level Input Voltage	2.0		1.5			1.5		1.5		V
		4.5		3.15			3.15		3.15		
		6.0		4.2			4.2		4.2		
V <sub>IL</sub>	Low Level Input Voltage	2.0				0.5		0.5		0.5	V
		4.5				1.35		1.35		1.35	
		6.0				1.8		1.8		1.8	
V <sub>OH</sub>	High Level Output Voltage	2.0	I <sub>O</sub> =-20 μA	1.9	2.0		1.9		1.9		V
		4.5	I <sub>O</sub> =-20 μA	4.4	4.5		4.4		4.4		
		6.0	I <sub>O</sub> =-20 μA	5.9	6.0		5.9		5.9		
		4.5	I <sub>O</sub> =-4.0 mA	4.18	4.31		4.13		4.10		
		6.0	I <sub>O</sub> =-5.2 mA	5.68	5.8		5.63		5.60		
V <sub>OL</sub>	Low Level Output Voltage	2.0	I <sub>O</sub> =20 μA		0.0	0.1		0.1		0.1	V
		4.5	I <sub>O</sub> =20 μA		0.0	0.1		0.1		0.1	
		6.0	I <sub>O</sub> =20 μA		0.0	0.1		0.1		0.1	
		4.5	I <sub>O</sub> =4.0 mA		0.17	0.26		0.33		0.40	
		6.0	I <sub>O</sub> =5.2 mA		0.18	0.26		0.33		0.40	
I <sub>I</sub>	Input Leakage Current	6.0	V <sub>I</sub> = V <sub>CC</sub> or GND			± 0.1		± 1		± 1	μA
I <sub>CC</sub>	Quiescent Supply Current	6.0	V <sub>I</sub> = V <sub>CC</sub> or GND			4		40		80	μA

Table 6: AC Electrical Characteristics ( $C_L = 50$  pF, Input  $t_r = t_f = 6$  ns)

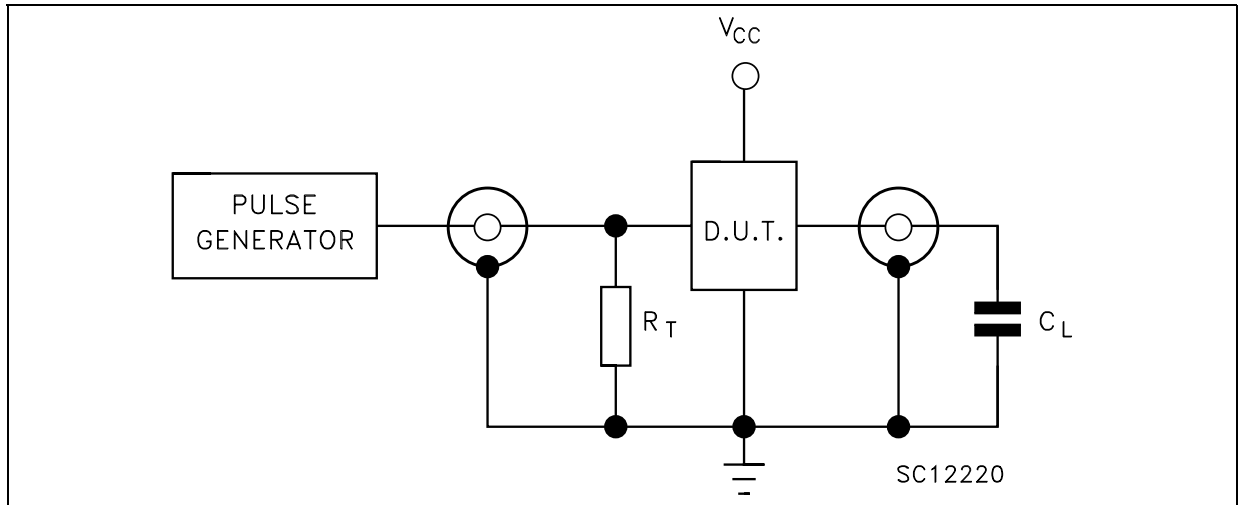
Symbol	Parameter	Test Condition		Value						Unit	
				$T_A = 25^\circ\text{C}$			$-40$ to $85^\circ\text{C}$		$-55$ to $125^\circ\text{C}$		
				Min.	Typ.	Max.	Min.	Max.	Min.		Max.
$t_{TLH}$ $t_{THL}$	Output Transition Time	$V_{CC}$ (V)			30	75		95		110	ns
					8	15		19		22	
					7	13		16		19	
$t_{PLH}$ $t_{PHL}$	Propagation Delay Time (CLOCK - QA)	$V_{CC}$ (V)			50	120		150		180	ns
					15	24		30		36	
					13	20		26		31	
$t_{PLH}$ $t_{PHL}$	Propagation Delay Time (CLOCK - QB)	$V_{CC}$ (V)			70	160		200		240	ns
					20	32		40		48	
					17	27		34		41	
$t_{PLH}$ $t_{PHL}$	Propagation Delay Time (CLOCK - QC)	$V_{CC}$ (V)			90	195		245		295	ns
					25	39		49		59	
					21	33		42		50	
$t_{PLH}$ $t_{PHL}$	Propagation Delay Time (CLOCK - QD)	$V_{CC}$ (V)			120	230		290		345	ns
					30	46		58		69	
					26	39		49		59	
$t_{PHL}$	Propagation Delay Time (CLEAR - Qn)	$V_{CC}$ (V)			55	150		190		225	ns
					18	30		38		45	
					15	26		32		38	
$f_{MAX}$	Maximum Clock Frequency	$V_{CC}$ (V)		8.4	17		6.8		5.6		MHz
				42	67		34		28		
				50	79		40		33		
$t_{W(H)}$ $t_{W(L)}$	Minimum Pulse Width (CLOCK)	$V_{CC}$ (V)			28	75		95		110	ns
					7	15		19		22	
					6	13		16		19	
$t_{W(H)}$	Minimum Pulse Width (CLEAR)	$V_{CC}$ (V)			28	75		95		110	ns
					7	15		19		22	
					6	13		16		19	
$t_{REM}$	Minimum Removal Time	$V_{CC}$ (V)				25		30		35	ns
						5		6		7	
						5		5		6	

Table 7: Capacitive Characteristics

Symbol	Parameter	Test Condition		Value						Unit	
				$T_A = 25^\circ\text{C}$			$-40$ to $85^\circ\text{C}$		$-55$ to $125^\circ\text{C}$		
				Min.	Typ.	Max.	Min.	Max.	Min.		Max.
$C_{IN}$	Input Capacitance				5	10		10		10	pF
$C_{PD}$	Power Dissipation Capacitance (note 1)				35						pF

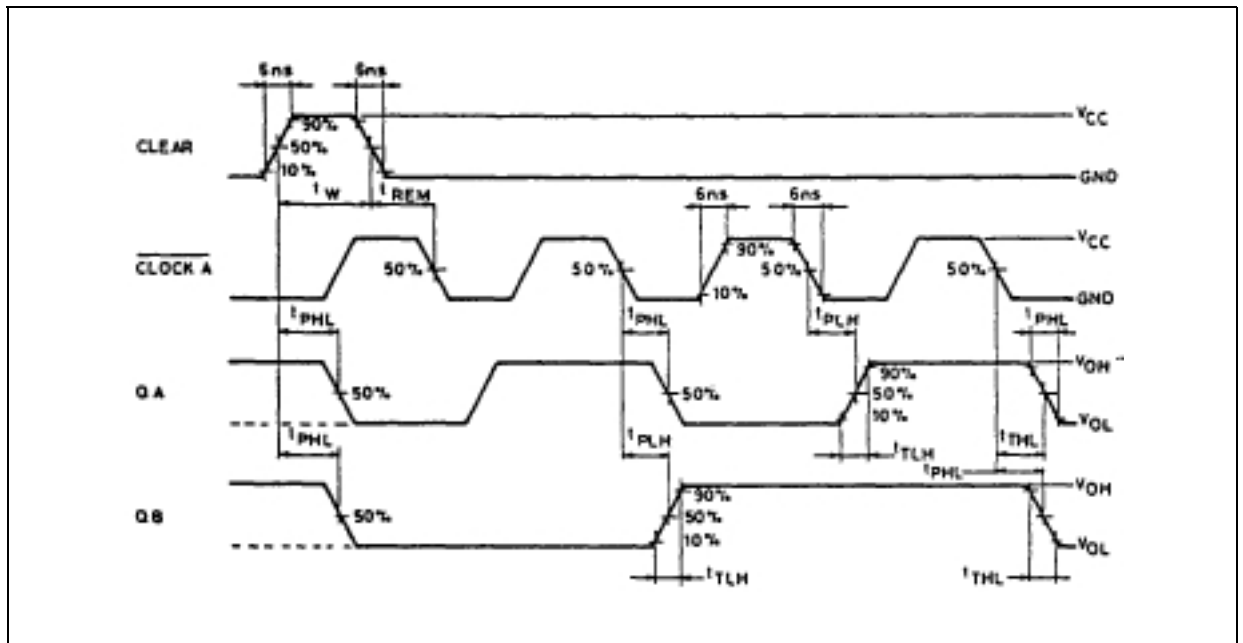
1)  $C_{PD}$  is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operating current can be obtained by the following equation.  $I_{CC(opr)} = C_{PD} \times V_{CC} \times f_{IN} + I_{CC}/4$  (per FLIP FLOP)

Figure 5: Test Circuit



$C_L$  = 50pF or equivalent (includes jig and probe capacitance)  
 $R_T$  =  $Z_{OUT}$  of pulse generator (typically 50 $\Omega$ )

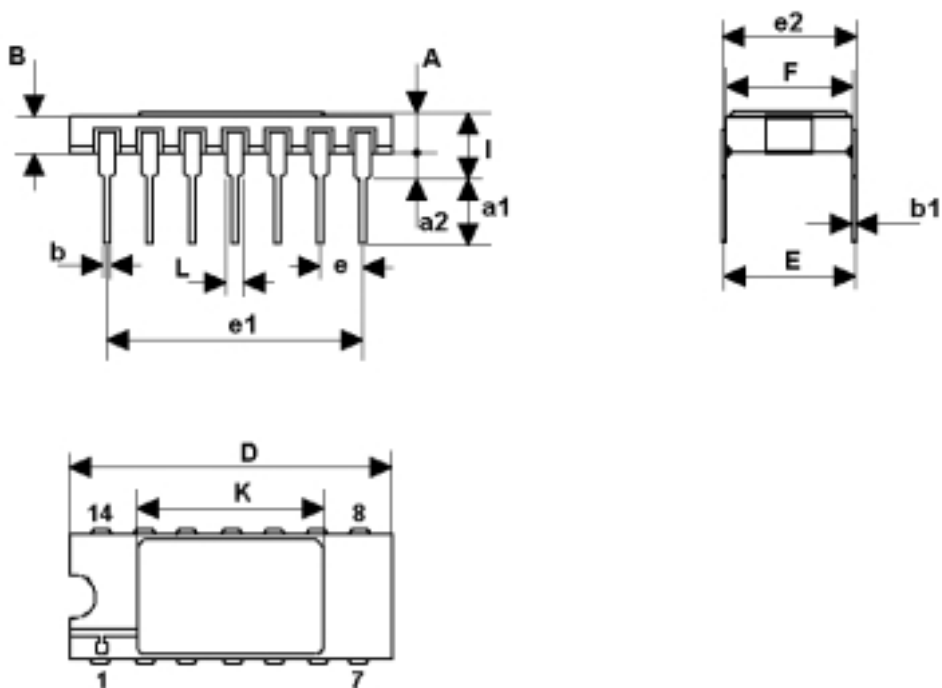
Figure 6: Waveform - Minimum Removal And Propagation Delay Times, Minimum Pulse Width (f=1MHz; 50% duty cycle)





## DILC-14 MECHANICAL DATA

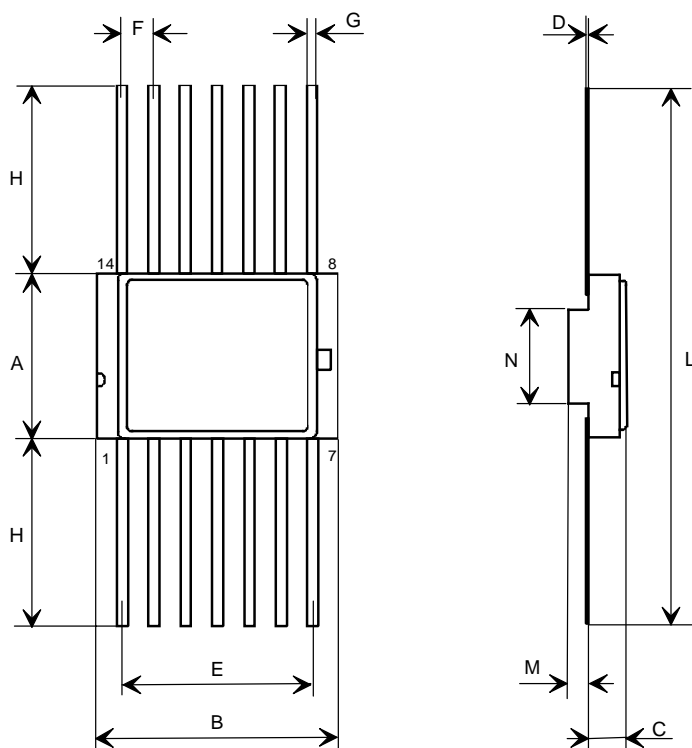
DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	2.1		22.54	0.083		0.100
a1	3.00		3.70	0.118		0.146
a2	0.63	0.88	1.14	0.025	0.035	0.045
B	1.82	2.03	2.39	0.072	0.080	0.094
b	0.40	0.45	0.50	0.016	0.018	0.020
b1	0.20	0.254	0.30	0.008	0.010	0.012
D	18.79	19.00	19.20	0.740	0.748	0.756
e	7.36	7.62	7.87	0.290	0.300	0.310
e1		2.54			0.100	
e2	15.11	15.24	15.37	0.595	0.600	0.605
e3	7.62	7.87	8.12	0.300	0.310	0.320
F	7.11		7.75	0.280		0.305
I			3.70			0.146
K	10.90		12.1	0.429		0.476
L	1.14	1.27	1.5	0.045	0.050	0.059



0016173H

## FPC-14 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	6.75	6.91	7.06	0.266	0.272	0.278
B	9.76	9.95	10.14	0.384	0.392	0.399
C	1.49		1.95	0.059		0.077
D	0.10	0.127	0.15	0.004	0.005	0.006
E	7.50	7.62	7.75	0.295	0.300	0.305
F		1.27			0.050	
G	0.38	0.43	0.48	0.015	0.017	0.019
H		6.0			0.236	
L	18.75		22.0	0.738		0.866
M		0.38			0.015	
N		4.31			0.170	



016029E

**Table 8: Revision History**

Date	Revision	Description of Changes
10-May-2004	1	First Release

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