Triple Half Bridges

TLE 6208-3 G

AEC Qualified RoHS

1 Overview

PG-DSO-14-35
Enhanced Power

1.1 Features

- Three Half-Bridges
- Optimized for DC motor management applications
- Delivers up to 0.6 A continuous, 1.2 A peak current
- $R_{DS\ ON}$; typ. 0.8 Ω, @ 25 °C per switch
- Output: short circuit protected and diagnosis
- Overtemperature-Protection with hysteresis and diagnosis
- Standard SPI-Interface/Daisy chain capable
- Very low current consumption in stand-by (Inhibit) mode (typ. 10 µA for power and 2 µA for logic supply, @ 25 °C)
- Over- and Undervoltage-Lockout
- CMOS/TTL compatible inputs with hysteresis
- No crossover current
- Internal clamp diodes
- Enhanced power P-DSO-Package
- Programming compatibility to the TLE 5208-6
- Green Product (RoHS compliant)
- AEC Qualified

Type	Package
TLE 6208-3 G	PG-DSO-14-35

Functional Description

The TLE 6208-3 G is a fully protected **Tri**ple-**H**alf-**B**ridge-**D**river designed specifically for automotive and industrial motion control applications. The part is based on the Siemens power technology SPT® which allows bipolar and CMOS control circuitry in accordance with DMOS power devices existing on the same monolithic circuitry.
In motion control up to 2 actuators (DC-Motors) can be connected to the 3 halfbridge-outputs (cascade configuration). Operation modes forward (cw), reverse (ccw), brake and high impedance are controlled from a standard SPI-Interface. The possibility to control the outputs via software from a central logic, allows limiting the power dissipation. So the standard P-DSO-14-package meets the application requirements and saves PCB-Board-space and cost. Furthermore the build-in features like Over- and Undervoltage-Lockout, Over-Temperature-Protection and the very low quiescent current in stand-by mode opens a wide range of automotive- and industrial-applications.

1.2 Pin Configuration (top view)

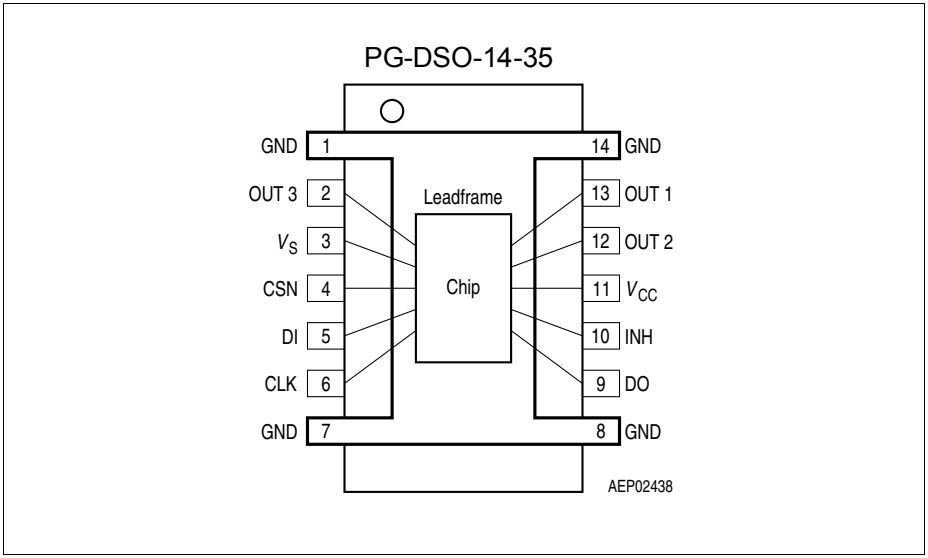

Figure 1

1.3 Pin Definitions and Functions

Pin No.	Symbol	Function
1	GND	**Ground;** Reference potential; internal connection to pin 7, 8 and 14; cooling tab; to reduce thermal resistance place cooling areas on PCB close to these pins.
2	OUT3	**Halfbridge-Output 3;** Internally contected to Highside-Switch 3 and Lowside-Switch 3. The HS-Switch is a Power-MOS open drain with internal reverse diode; The LS-Switch is a Power-MOS open source with internal reverse diode; no internal clamp diode or active zenering; short circuit protected and open load controlled.
3	V_S	**Power Supply;** needs a blocking capacitor as close as possible to GND Value: 22 µF electrolytic in parallel to 220 nF ceramic.
5	DI	**Serial Data Input;** receives serial data from the control device; serial data transmitted to DI is an 16bit control word with the Least Significant Bit (LSB) being transferred first: the input has an active pull down and requires CMOS logic level inputs; DI will accept data on the falling edge of CLK-signal; see **Table Input Data Protocol**.
4	CSN	**Chip-Select-Not Input;** CSN is an active low input; serial communication is enabled by pulling the CSN terminal low; CSN input should only be transitioned when CLK is low; CSN has an internal active pull up and requires CMOS logic level inputs.
6	CLK	**Serial Clock Input;** clocks the shiftregister; CLK has an internal active pull down and requires CMOS logic level inputs.
7, 8, 14	GND	**Ground;** see pin 1.
9	DO	**Serial-Data-Output;** this 3-state output transfers diagnosis data to the control device; the output will remain 3-stated unless the device is selected by a low on Chip-Select-Not (CSN); see **Table Diagnosis Data Protocol**.
10	INH	**Inhibit Input;** has an internal pull down; device is switched in standby condition by pulling the INH terminal low.
11	V_{CC}	**Logic Supply Voltage;** needs a blocking capacitor as close as possible to GND; Value: 10 µF electrolytic in parallel to 220 nF ceramic.
12	OUT2	**Halfbridge-Output 2;** see pin 2.
13	OUT1	**Halfbridge-Output 1;** see pin 2.

1.4 Functional Block Diagram

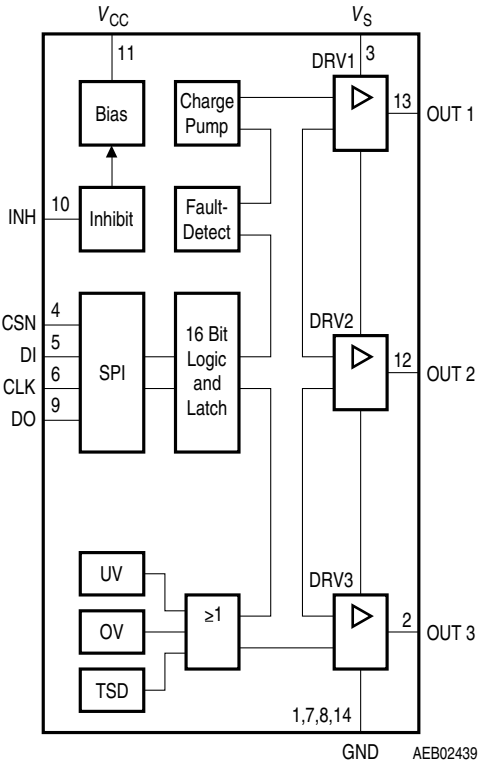

Figure 2 Block Diagram

1.5 Circuit Description

Figure 2 shows a block schematic diagram of the module. There are 3 halfbridge drivers on the right-hand side. An HS driver and an LS driver are combined to form a halfbridge driver in each case. The drivers communicate via the internal data bus with the logic and the other control and monitoring functions: undervoltage (UV), overvoltage (OV), overtemperature (TSD), charge pump and fault detect.

Two connection interfaces are provided for supply to the module: All power drivers are connected to the supply voltage V_S. These are monitored by overvoltage and undervoltage comparators with hysteresis, so that the correct function can be checked in the application at any time.

The logic is supplied by the V_{CC} voltage, typ. with 5 V. The V_{CC} voltage uses an internally generated Power-On Reset (POR) to initialize the module at power-on. The advantage of this system is that information stored in the logic remains intact in the event of short-term failures in the supply voltage V_S. The system can therefore continue to operate following V_S undervoltage, without having to be reprogrammed. The “undervoltage” information is stored, and can be read out via the interface. The same logically applies for overvoltage. “Interference spikes” on V_S are therefore effectively suppressed.

The situation is different in the case of undervoltage on the V_{CC} connection pin. If this occurs, then the internally stored data is deleted, and the output levels are switched to high-impedance status (tristate). The module is initialized by V_{CC} following restart (Power-On Reset = POR).

The 16-bit wide programming word or control word (see **Table Input Data Protocol**) is read in via the DI data input, and this is synchronized with the clock input CLK. The status word appears synchronously at the DO data output (see **Table Diagnosis Data Protocol**). It is also possible to connect two **TLE 6208-3 G** in a daisy chain configuration. The DO data output of one device is connected with the DI data input of the second device. In this configuration these two devices are controlled with a single CSN chip select and using a 32-bit wide control word.

The transmission cycle begins when the chip is selected with the CSN input (H to L). If the CSN input changes from L to H then the word which has been read in becomes the control word. The DO output switches to tristate status at this point, thereby releasing the DO bus circuit for other uses.

The INH inhibit input can be used to cut off the complete module. This reduces the current consumption to just a few µA, and results in the loss of any data stored. The output levels are switched to tristate status. The module is reinitialized with the internally generated POR (Power-On Reset) at restart.

This feature allows the use of this module in battery-operated applications (vehicle body control applications).

Every driver block from DRV 1 to 3 contains a low-side driver and a high-side driver. Both drivers are connected internally to form a half-bridge at the output. This reduction of output pins was necessary to meet the small P-DSO-14 package.

When commutating inductive loads, the dissipated power peak can be significantly reduced by activating the transistor located parallel to the internal freewheeling diode. A special, integrated “timer” for power ON/OFF times ensures that there is no crossover current.

Input Data Protocol

BIT	
15	OVLO on/off
14	not used
13	Overcurrent SD on/off
12	not used
11	not used
10	not used
9	not used
8	not used
7	not used
6	HS-Switch 3
5	LS-Switch 3
4	HS-Switch 2
3	LS-Switch 2
2	HS-Switch 1
1	LS-Switch 1
0	Status Register Reset

H = ON
L = OFF

Diagnosis Data Protocol

BIT	
15	Power supply fail
14	Underload
13	Overload
12	not used
11	not used
10	not used
9	not used
8	not used
7	not used
6	Status HS-Switch 3
5	Status LS-Switch 3
4	Status HS-Switch 2
3	Status LS-Switch 2
2	Status HS-Switch 1
1	Status LS-Switch 1
0	Temp. Prewarning

H = ON
L = OFF

Fault Result Table

Fault	Diag.-Bit	Result
Overcurrent (load)	13	Only the failed output is switched OFF. Function can be deactivated by bit No. 13.
Short circuit to GND (high-side-switch)	13	Only the failed output is switched OFF. Function can be deactivated by bit No. 13.

Fault Result Table

Fault	Diag.-Bit	Result
Short circuit to V_S (low-side-switch)	13	Only the failed output is switched OFF. Function can be deactivated by bit No. 13.
Temperature warning	0	Reaction of control device needed.
Temperature shut down (SD)	–	All outputs OFF. Temperature warning is set before.
Underload/Openload	14	Reaction of control device needed.
Undervoltage lockout (UVLO)	15	All outputs OFF.
Overvoltage lockout (OVLO)	15	All outputs OFF. Function can be deactivated by bit No. 15.

H = failure;
L = no failure.

2 Electrical Characteristics

2.1 Absolute Maximum Ratings

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
Supply voltage	V_S	– 0.3	40	V	–
Supply voltage	V_S	– 1	–	V	t < 0.5 s; I_S > – 2 A
Logic supply voltage	V_{CC}	– 0.3	5.5	V	0 V < V_S < 40 V
Logic input voltages (DI, CLK, CSN, INH)	V_I	– 0.3	5.5	V	0 V < V_S < 40 V 0 V < V_{CC} < 5.5 V
Logic output voltage (DO)	V_{DO}	– 0.3	5.5	V	0 V < V_S < 40 V 0 V < V_{CC} < 5.5 V
Output voltage (OUT 1-3)	V_{OUT}	– 0.3	40	V	0 V < V_S < 40 V
Output current (cont.)	I_{OUT1-3}	–	–	A	internal limited
Output current (peak)	I_{OUT1-3}	–	–	A	internal limited
Note: Current limits are mentioned in the overcurrent section of electrical charateristics					
Junction temperature	T_j	– 40	150	°C	–
Storage temperature	T_{stg}	– 50	150	°C	–

2 Electrical Characteristics

2.1 Absolute Maximum Ratings (cont'd)

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
ESD voltage, human body model, according to: • MIL STD 883D, • ANSI EOS\ESD S5.1 • JEDEC JESD22-A114	$V_{ESD\text{-}HBM}$	–	–	4kV	all pins
	$V_{ESD\text{-}HBM\text{-}OUT}$	–	–	8kV	only pins 2, 12 and 13 (outputs)
ESD voltage, mashine model, according to: • ANSI EOS\ESD S5.2 • JEDEC JESD22-A115	$V_{ESD\text{-}MM}$	–	–	300V	all pins

Note: Stresses above those listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2.2 Operating Range

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
Supply voltage	V_S	$V_{UV\ OFF}$	40	V	After V_S rising above $V_{UV\ ON}$
Supply voltage slew rate	dV_S/dt	–	10	V/µs	–
Logic supply voltage	V_{CC}	4.75	5.50	V	–
Supply voltage increasing	V_S	– 0.3	$V_{UV\ ON}$	V	Outputs in tristate
Supply voltage decreasing	V_S	– 0.3	$V_{UV\ OFF}$	V	Outputs in tristate
Logic input voltage (DI, CLK, CSN, INH)	V_I	– 0.3	V_{CC}	V	–
SPI clock frequency	f_{CLK}	–	1	MHz	–
Junction temperature	T_j	– 40	150	°C	–

Thermal Resistances

2.2 Operating Range (cont'd)

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
Junction pin	$R_{thj\text{-}pin}$	–	30	K/W	measured to pin 1, 7, 8, 14
Junction ambient	R_{thjA}	–	65	K/W	–

Note: In the operating range, the functions given in the circuit description are fulfilled.

2.3 Electrical Characteristics

8 V < V_S < 40 V; 4.75 V < V_{CC} < 5.25 V; INH = High; all outputs open; – 40 °C < T_j < 150 °C; unless otherwise specified

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Current Consumption						
Quiescent current	I_S	–	8	20	µA	INH = Low; V_S = 13.2 V T_j = 25 °C
Quiescent current	I_S	–	–	30	µA	INH = Low; V_S = 13.2 V;
Logic-Supply current	I_{CC}	–	2	10	µA	INH = Low
Logic-Supply current	I_{CC}	–	1	2	mA	SPI not active
Supply current	I_S	–	2	5	mA	–
Over- and Under-Voltage Lockout						
UV-Switch-ON voltage	$V_{UV\ ON}$	–	6.5	7	V	V_S increasing
UV-Switch-OFF voltage	$V_{UV\ OFF}$	5.6	6.1	6.6	V	V_S decreasing
UV-ON/OFF-Hysteresis	$V_{UV\ HY}$	–	0.4	–	V	$V_{UV\ ON} - V_{UV\ OFF}$
OV-Switch-OFF voltage	$V_{OV\ OFF}$	34	37	40	V	V_S increasing
OV-Switch-ON voltage	$V_{OV\ ON}$	30	33	36	V	V_S decreasing
OV-ON/OFF-Hysteresis	$V_{OV\ HY}$	–	4	–	V	$V_{OV\ OFF} - V_{OV\ ON}$

2.3 Electrical Characteristics (cont'd)

8 V < V_S < 40 V; 4.75 V < V_{CC} < 5.25 V; INH = High; all outputs open; – 40 °C < T_j < 150 °C; unless otherwise specified

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Outputs OUT1-3						
Static Drain-Source-On Resistance						
Source (High-Side) I_{OUT} = – 0.5 A	$R_{DS\ ON\ H}$	–	0.8	0.95	Ω	8 V < V_S < 40 V T_j = 25 °C
			–	1.6	Ω	8 V < V_S < 40 V
			1	–	Ω	$V_{S\ OFF}$ < V_S ≤ 8 V T_j = 25 °C
			–	2	Ω	$V_{S\ OFF}$ < V_S ≤ 8 V
Sink (Low-Side) I_{OUT} = 0.5 A	$R_{DS\ ON\ L}$	–	0.75	0.9	Ω	8 V < V_S < 40 V T_j = 25 °C
			–	1.5	Ω	8 V < V_S < 40 V
			1	–	Ω	$V_{S\ OFF}$ < V_S ≤ 8 V T_j = 25 °C
			–	2	Ω	$V_{S\ OFF}$ < V_S ≤ 8 V
Leakage Current						
Source-Output-Stage 1 to 3	I_{QLH}	– 5	– 1	–	µA	V_{OUT1-3} = 0 V
Sink-Output-Stage 1 to 3	I_{QLL}	–	150	300	µA	V_{OUT1-3} = V_S
Overcurrent						
Source shutdown threshold	I_{SDU}	– 2	– 1.3	– 1	A	–
Sink shutdown threshold	I_{SDL}	1	1.2	2	A	–
Current limit	I_{OCL}	–	2.4	4	A	sink and source
Shutdown delay time	t_{dSD}	10	28	40	µs	sink and source
Open Circuit/Underload Detection						
Detection current	I_{OCD}	15	30	45	mA	–

2.3 Electrical Characteristics (cont'd)

8 V < V_S < 40 V; 4.75 V < V_{CC} < 5.25 V; INH = High; all outputs open; – 40 °C < T_j < 150 °C; unless otherwise specified

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Delay time	t_{dOC}	200	370	600	µs	–
Output Delay Times; V_S = 13.2 V; R_{Load} = 25 Ω (device not in stand-by for t > 1 ms)						
Source ON	$t_{d\ ON\ H}$	–	8	20	µs	–
Source OFF	$t_{d\ OFF\ H}$	–	4	20	µs	–
Sink ON	$t_{d\ ON\ L}$	–	7	20	µs	–
Sink OFF	$t_{d\ OFF\ L}$	–	3	20	µs	–
Dead time	$t_{D\ HL}$	1	3	–	µs	$t_{d\ ON\ L} - t_{d\ OFF\ H}$
Dead time	$t_{D\ LH}$	1	5	–	µs	$t_{d\ ON\ H} - t_{d\ OFF\ L}$
Output Switching Times; V_S = 13.2 V; R_{Load} = 25 Ω (device not in stand-by for t > 1 ms)						
Source ON	$t_{ON\ H}$	–	5	20	µs	–
Source OFF	$t_{OFF\ H}$	–	2	5	µs	–
Sink ON	$t_{ON\ L}$	–	2.0	10	µs	–
Sink OFF	$t_{OFF\ L}$	–	1.5	5	µs	–
Clamp Diodes Forward Voltage						
Upper	V_{FU}	–	0.9	1.3	V	I_F = 0.5 A
Lower	V_{FL}	–	0.9	1.3	V	I_F = 0.5 A
Inhibit Input						
H-input voltage threshold	V_{IH}	–	0.52	0.7	V_{CC}	–
L-input voltage threshold	V_{IL}	0.2	0.48	–	V_{CC}	–
Hysteresis of input voltage	V_{IHY}	50	200	500	mV	–
Pull down current	I_I	5	25	100	µA	$V_I = 0.2 \times V_{CC}$
Input capacitance	C_I	–	10	15	pF	0 V < V_{CC} < 5.25 V

2.3 Electrical Characteristics (cont'd)

8 V < V_S < 40 V; 4.75 V < V_{CC} < 5.25 V; INH = High; all outputs open; – 40 °C < T_j < 150 °C; unless otherwise specified

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		

Note: Capacitances are guaranteed by design.

SPI-Interface

Delay Time from Stand-by to Data In/Power on Reset

Setup time	t_{set}	–	–	100	µs	–

Logic Inputs DI, CLK and CSN

H-input voltage threshold	V_{IH}	–	0.52	0.7	V_{CC}	–
L-input voltage threshold	V_{IL}	0.2	0.48	–	V_{CC}	–
Hysteresis of input voltage	V_{IHY}	50	200	500	mV	–
Pull up current at pin CSN	I_{ICSN}	– 50	– 25	– 10	µA	$V_{CSN} = 0.7 \times V_{CC}$
Pull down current at pin DI	I_{IDI}	10	25	50	µA	$V_{DI} = 0.2 \times V_{CC}$
Pull down current at pin CLK	I_{ICLK}	10	25	50	µA	$V_{CLK} = 0.2 \times V_{CC}$
Input capacitance at pin CSN, DI or CLK	C_I	–	10	15	pF	0 V < V_{CC} < 5.25 V

Note: Capacitances are guaranteed by design.

Logic Output DO

H-output voltage level	V_{DOH}	V_{CC} – 1.0	V_{CC} – 0.7	–	V	I_{DOH} = 1 mA
L-output voltage level	V_{DOL}	–	0.2	0.4	V	I_{DOL} = – 1.6 mA
Tri-state leakage current	I_{DOLK}	– 10	0	10	µA	$V_{CSN} = V_{CC}$ 0 V < V_{DO} < V_{CC}
Tri-state input capacitance	C_{DO}	–	10	15	pF	$V_{CSN} = V_{CC}$ 0 V < V_{CC} < 5.25 V

Note: Capacitances are guaranteed by design.

2.3 Electrical Characteristics (cont'd)

8 V < V_S < 40 V; 4.75 V < V_{CC} < 5.25 V; INH = High; all outputs open; – 40 °C < T_j < 150 °C; unless otherwise specified

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Data Input Timing						
Clock period	t_{pCLK}	1000	–	–	ns	–
Clock high time	t_{CLKH}	500	–	–	ns	–
Clock low time	t_{CLKL}	500	–	–	ns	–
Clock low before CSN low	t_{bef}	500	–	–	ns	–
CSN setup time	t_{lead}	500	–	–	ns	–
CLK setup time	t_{lag}	500	–	–	ns	–
Clock low after CSN high	t_{beh}	500	–	–	ns	–
DI setup time	t_{DISU}	250	–	–	ns	–
DI hold time	t_{DIHO}	250	–	–	ns	–
Input signal rise time at pin DI, CLK and CSN	t_{rIN}	–	–	200	ns	–
Input signal fall time at pin DI, CLK and CSN	t_{fIN}	–	–	200	ns	–
Data Output Timing						
DO rise time	t_{rDO}	–	50	100	ns	C_L = 100 pF
DO fall time	t_{fDO}	–	50	100	ns	C_L = 100 pF
DO enable time	t_{ENDO}	–	–	250	ns	low impedance
DO disable time	t_{DISDO}	–	–	250	ns	high impedance
DO valid time	t_{VADO}	–	100	250	ns	V_{DO} < 0.2 V_{CC}; V_{DO} > 0.7 V_{CC}; C_L = 100 pF
Thermal Prewarning and Shutdown						
Thermal prewarning junction temperature	T_{jPW}	120	145	170	°C	–

2.3 Electrical Characteristics (cont'd)

8 V < V_S < 40 V; 4.75 V < V_{CC} < 5.25 V; INH = High; all outputs open; – 40 °C < T_j < 150 °C; unless otherwise specified

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Temperature prewarning hysteresis	ΔT	–	30	–	K	–
Thermal shutdown junction temperature	T_{jSD}	150	175	200	°C	–
Thermal switch-on junction temperature	T_{jSO}	120	–	170	°C	–
Temperature shutdown hysteresis	ΔT	–	30	–	K	–
Ratio of SD to PW temperature	T_{jSD}/T_{jPW}	1.05	1.20	–	–	–

Note: Temperatures are guaranteed by design.
The listed characteristics are ensured over the operating range of the integrated circuit. Typical characteristics specify mean values expected over the production spread. If not otherwise specified, typical characteristics apply at T_A = 25 °C and the given supply voltage.

3 Timing Diagrams

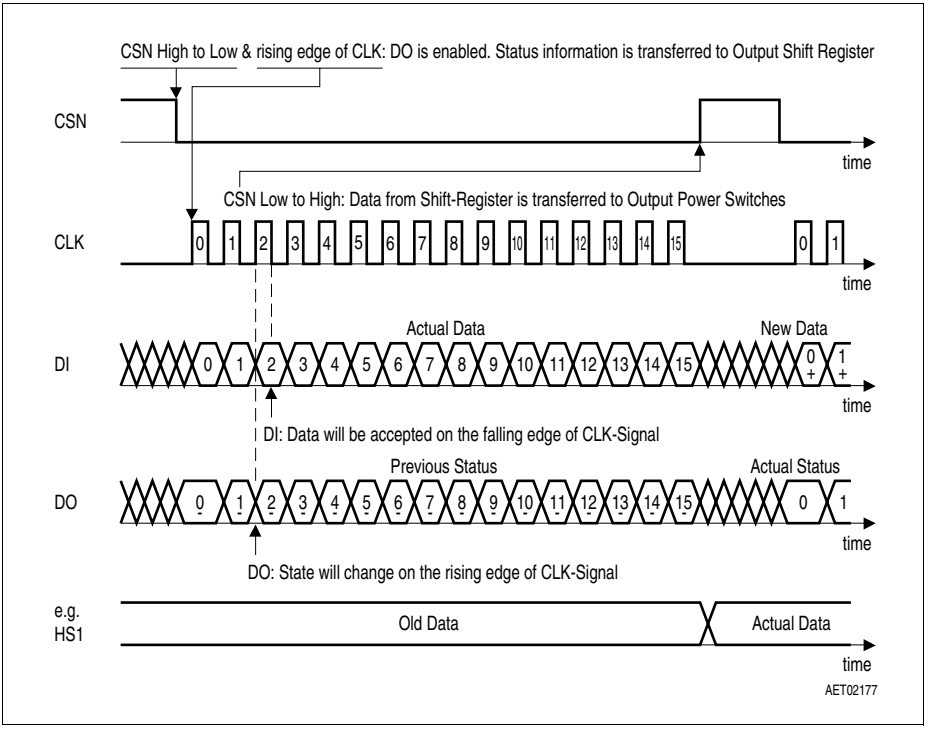

Figure 3 Data Transfer Timing

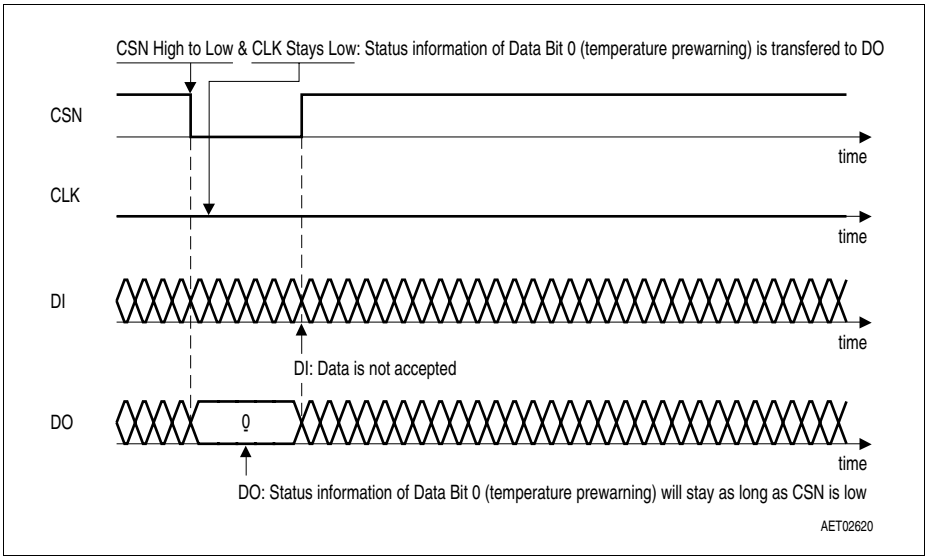

Figure 4 Timing for Temperature Prewarning only

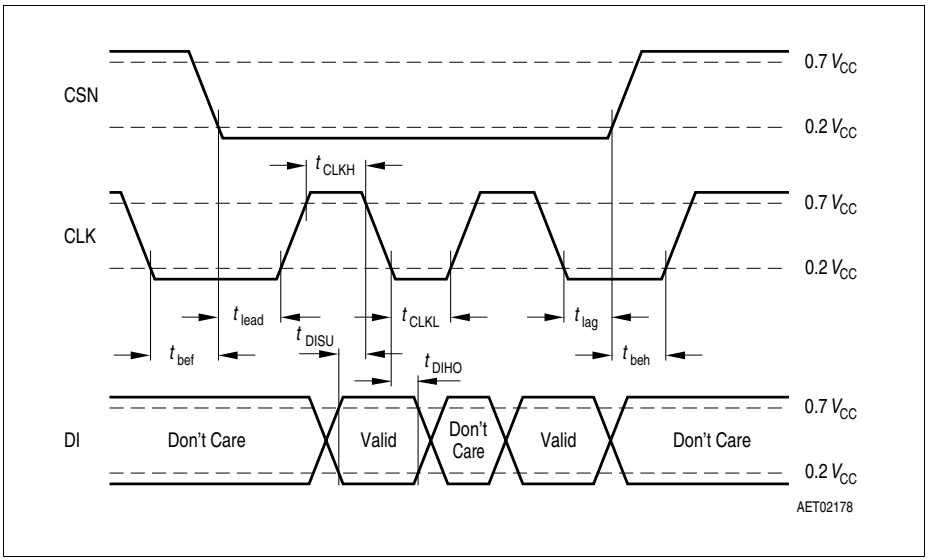

Figure 5 SPI-Input Timing

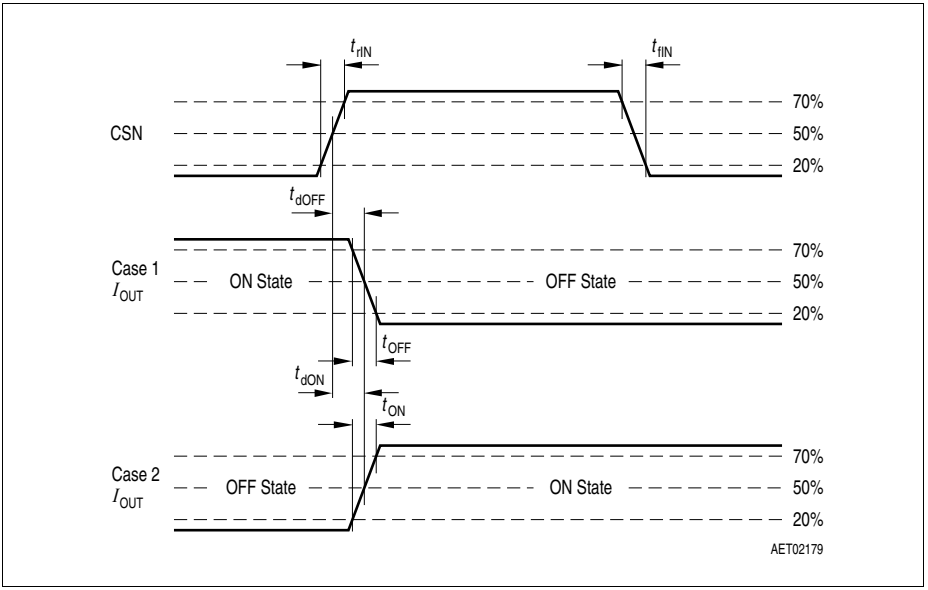

Figure 6 Turn OFF/ON Time

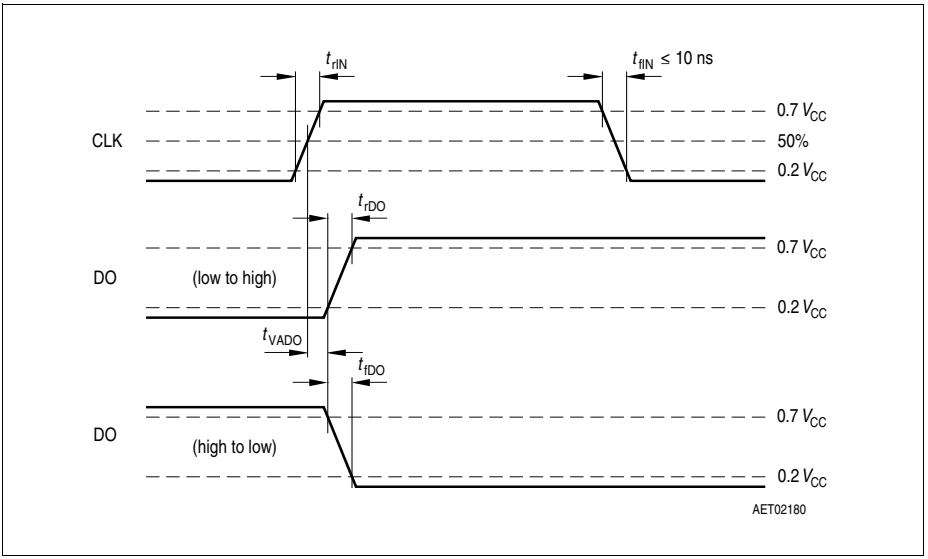

Figure 7 DO Valid Data Delay Time and Valid Time

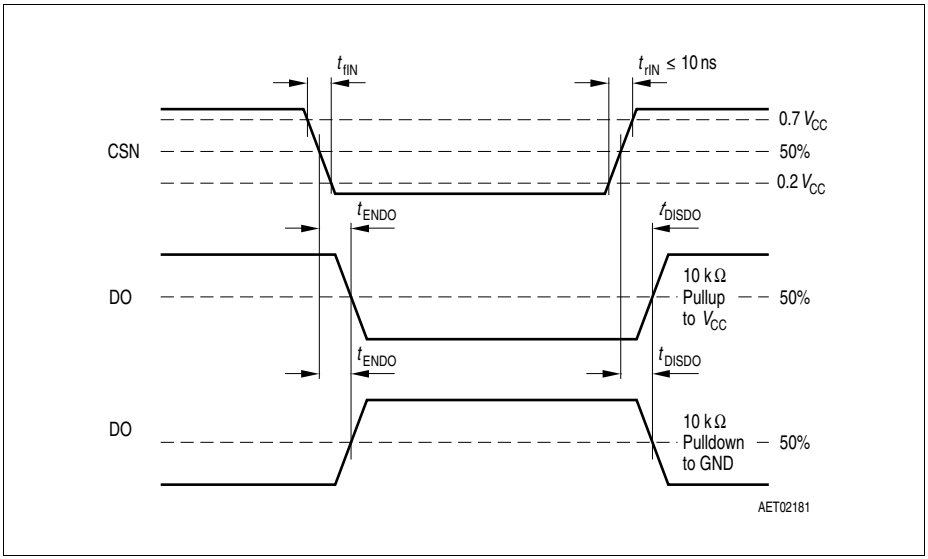

Figure 8 DO Enable and Disable Time

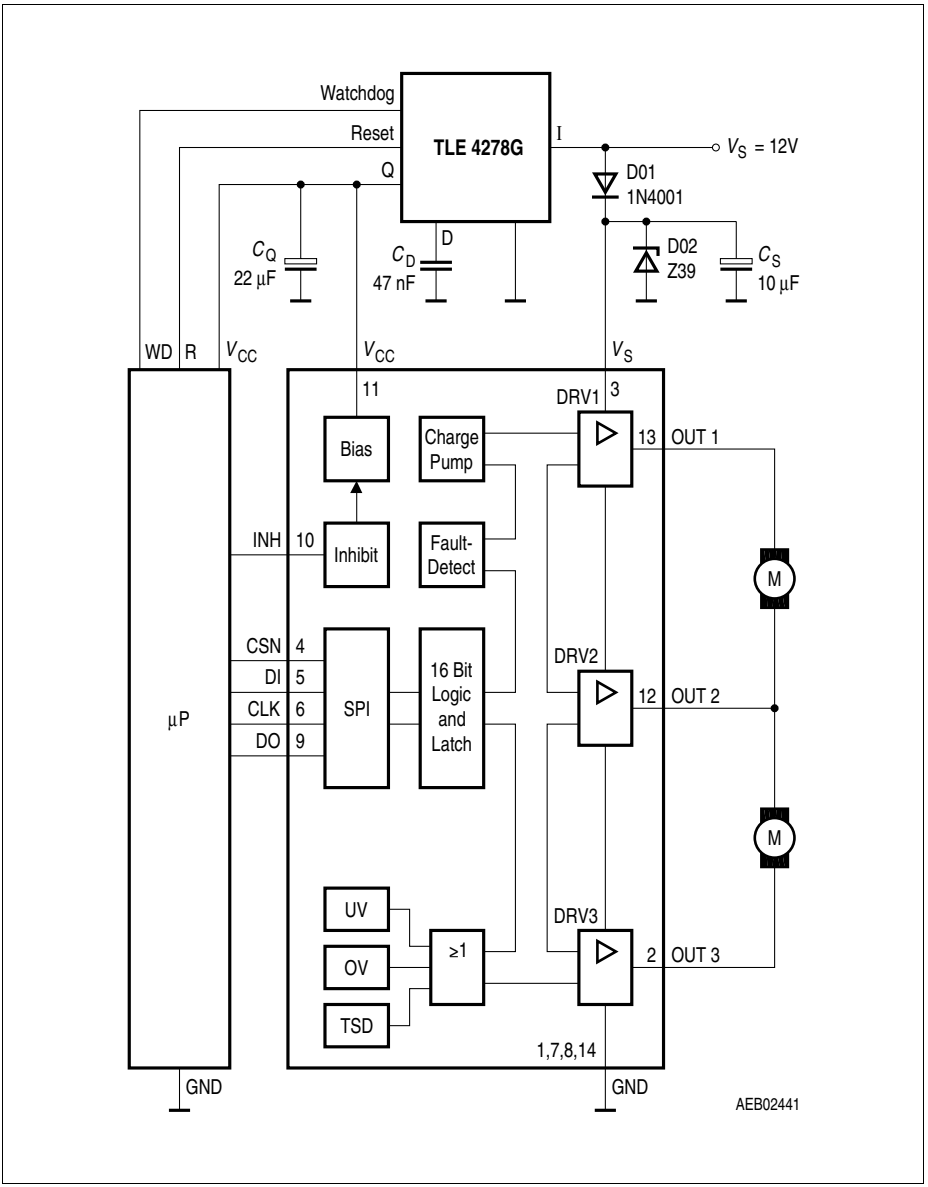

Figure 9 Application Circuit

4 Package Outlines

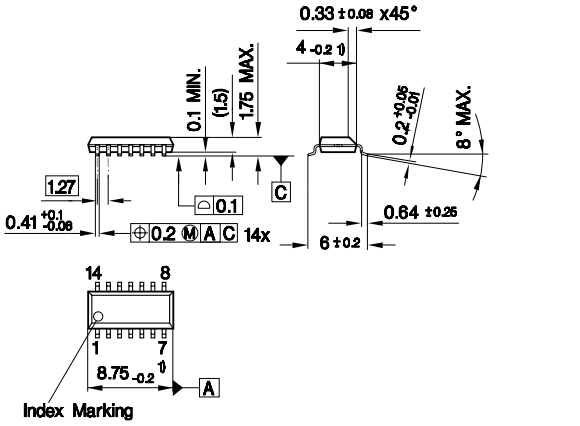

Figure 10 PG-DSO-14-35 (Plastic Dual Small Outline)

Green Product (RoHS compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

You can find all of our packages, sorts of packing and others in our Infineon Internet Page “Products”: **http://www.infineon.com/products**.

SMD = Surface Mounted Device

Dimensions in mm

Revision History

Version	Date	Changes
Rev. 1.1	2007-09-12	RoHS-compliant version of the TLE 6208-3 G • All pages: Infineon logo updated • Page 1: “added AEC qualified” and “RoHS” logo, “Green Product (RoHS compliant)” and “AEC qualified” statement added to feature list, package name changed to RoHS compliant versions, package picture updated, ordering code removed • Page 20: Package name changed to RoHS compliant versions, “Green Product” description added • Page 21-22: added Revision History and Legal Disclaimer

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