Dual Channel, High IP3, 100 MHz to 6 GHz Active Mixer

ADL5802

FEATURES

Power conversion gain of 1.6 dB
Wideband RF, LO, and IF ports
SSB noise figure of 11 dB
Input IP3 of 28 dBm
Input P1dB of 12 dBm
Typical LO drive of 0 dBm
Low LO leakage
Single supply operation: 5 V @ 240 mA
Exposed paddle, 4 mm × 4 mm, 24-lead LFCSP package

APPLICATIONS

Cellular base station receivers
Main and diversity receiver designs
Radio link downconverters

FUNCTIONAL BLOCK DIAGRAM

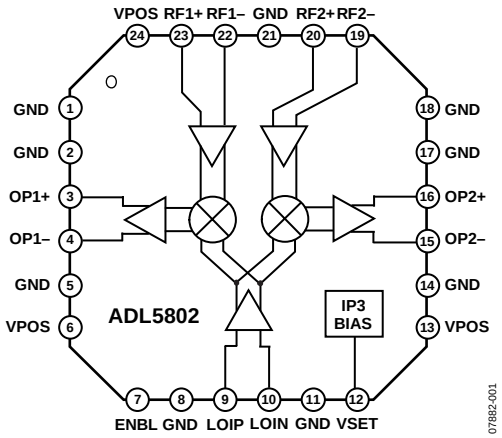

Figure 1.

GENERAL DESCRIPTION

The ADL5802 uses high linearity, double-balanced, active mixer cores with integrated LO buffer amplifiers to provide high dynamic range frequency conversion from 100 MHz to 6 GHz. The mixers benefit from a proprietary linearization architecture that provides enhanced input IP3 performance when subject to high input levels. A bias adjust feature allows the input linearity, SSB noise figure, and dc current to be optimized using a single control pin. The high input linearity allows the device to be used in demanding cellular applications where in-band blocking signals may otherwise result in degradation in dynamic performance. The balanced active mixer arrangement provides superb LO to RF and LO to IF leakage, typically better than −30 dBm.

The IF outputs are designed for a 200 Ω source impedance and provide a typical voltage conversion gain of 7.6 dB when loaded into a 200 Ω load.

The ADL5802 is fabricated using a SiGe high performance IC process. The device is available in a compact 4 mm × 4 mm, 24-lead LFCSP package and operates over a −40°C to +85°C temperature range. An evaluation board is also available.

Rev. 0

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REVISION HISTORY

11/09—Revision 0: Initial Version

SPECIFICATIONS

V_S = 5 V, VSET = 4 V, T_A = 25°C, f_{LO} = (f_{RF} − 153) MHz, LO power = 0 dBm, Z_0[1] = 50 Ω, unless otherwise noted.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
RF INPUT INTERFACE					
Return Loss	Tunable to >20 dB over a limited bandwidth		18		dB
Input Impedance			50		Ω
RF Frequency Range		100		6000	MHz
OUTPUT INTERFACE					
Output Impedance	Differential impedance, f = 200 MHz		240		Ω
IF Frequency Range	Can be matched externally to 3000 MHz	LF		600	MHz
DC Bias Voltage[2]	Externally generated	4.75	V_S	5.25	V
LO INTERFACE					
LO Power		−10	0	+10	dBm
Return Loss			18		dB
Input Impedance			50		Ω
LO Frequency Range		100		6000	MHz
POWER INTERFACE					
Supply Voltage		4.75	5	5.25	V
Quiescent Current	Resistor programmable		220	300	mA
Disable Current	ENBL pin low		170		mA
Enable Time	Time from ENBL pin low to power-up		182		ns
Disable Time	Time from ENBL pin high to power-down		28		ns
DYNAMIC PERFORMANCE at f_{RF} = 900 MHz/1900 MHz					
Power Conversion Gain[3]	f_{RF} = 900 MHz		1.5		dB
	f_{RF} = 1900 MHz		1.6		dB
Voltage Conversion Gain[4]	f_{RF} = 900 MHz		7.5		dB
	f_{RF} = 1900 MHz		7.6		dB
SSB Noise Figure	f_{CENT} = 900 MHz		10		dB
	f_{CENT} = 1900 MHz		11		dB
SSB Noise Figure Under Blocking[5]	f_{CENT} = 900 MHz		18		dB
	f_{CENT} = 1900 MHz		22		dB
Input Third Order Intercept[6]	f_{CENT} = 890 MHz		26		dBm
	f_{CENT} = 1890 MHz		28		dBm
Input Second Order Intercept[7]	f_{CENT} = 890 MHz		60		dBm
	f_{CENT} = 1890 MHz		45		dBm
Input 1 dB Compression Point	f_{RF} = 900 MHz		12		dBm
	f_{RF} = 1900 MHz		12		dBm
LO to IF Output Leakage	Unfiltered IF output		−35		dBm
LO to RF Input Leakage			−30		dBm
RF to IF Output Isolation			25		dBc
RFI1 to RFI2 Channel Isolation			45		dBc
IF/2 Spurious[8]	0 dBm input power, f_{RF} = 900 MHz		−68		dBc
IF/3 Spurious[8]	0 dBm input power, f_{RF} = 900 MHz		−67		dBc
IF/2 Spurious[8]	0 dBm input power, f_{RF} = 1900 MHz		−53		dBc
IF/3 Spurious[8]	0 dBm input power, f_{RF} = 1900 MHz		−59		dBc
DYNAMIC PERFORMANCE at f_{RF} = 2500 MHz[9]					
Power Conversion Gain[10]			−0.5		dB
Voltage Conversion Gain[4]			5.67		dB
SSB Noise Figure			11.5		dB
SSB Noise Figure Under Blocking[11]	f_{CENT} = 2145 MHz		18		dB
Input Third Order Intercept[6]	f_{CENT} = 2500 MHz		30		dBm

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
Input Second Order Intercept[7]	f_{CENT} = 2500 MHz		47		dBm
Input 1 dB Compression Point			13		dBm
LO to IF Output Leakage	Unfiltered IF output		36		dBm
LO to RF Input Leakage			31		dBm
RF to IF Output Isolation			26		dBc
RFI1 to RFI2 Channel Isolation			42		dBc
IF/2 Spurious[8]	0 dBm input power		−52		dBc
IF/3 Spurious[8]	0 dBm input power		−56		dBc
DYNAMIC PERFORMANCE at f_{RF} = 3500 MHz[12]					
Power Conversion Gain[13]			−0.5		dB
Voltage Conversion Gain[4]			5.5		dB
SSB Noise Figure			12.5		dB
SSB Noise Figure Under Blocking[14]	f_{CENT} = 3500 MHz		18		dB
Input Third Order Intercept[5]	f_{CENT} = 3500 MHz		25		dBm
Input Second Order Intercept[7]	f_{CENT} = 3500 MHz		39		dBm
Input 1 dB Compression Point			13		dBm
LO to IF Output Leakage	Unfiltered IF output		33		dBm
LO to RF Input Leakage			28		dBm
RF to IF Output Isolation			31		dBc
RFI1 to RFI2 Channel Isolation			39		dBc
IF/2 Spurious[8]	0 dBm input power		−46		dBc
IF/3 Spurious[8]	0 dBm input power		−63		dBc
DYNAMIC PERFORMANCE at f_{RF} = 5500 MHz[15]					
Power Conversion Gain[16]			−3		dB
Voltage Conversion Gain[4]			5.67		dB
SSB Noise Figure			14		dB
SSB Noise Figure Under Blocking[17]	f_{CENT} = 5800 MHz		17		dB
Input Third Order Intercept[5]	f_{CENT} = 5500 MHz		23		dBm
Input Second Order Intercept[7]	f_{CENT} = 5500 MHz		35		dBm
Input 1 dB Compression Point			13		dBm
LO to IF Output Leakage	Unfiltered IF output		42		dBm
LO to RF Input Leakage			27		dBm
RF to IF Output Isolation			50		dBc
RFI1 to RFI2 Channel Isolation			33		dBc
IF/2 Spurious[8]	0 dBm input power		−49		dBc
IF/3 Spurious[8]	0 dBm input power		−64		dBc

[1] Z_0 is the characteristic impedance assumed for all measurements and the PCB.
[2] Supply voltage must be applied from an external circuit through choke inductors.
[3] Excluding 4:1 IF port transformer (TC4-1W+), RF and LO port transformers (TC1-1-13M+), and PCB loss.
[4] Z_{SOURCE} = 50 Ω, differential; Z_{LOAD} = 200 Ω, differential 5 dBm; Z_{SOURCE} is the impedance of the source instrument; Z_{LOAD} is the load impedance at the output.
[5] $f_{RF1} = f_{CENT}$, $f_{BLOCKER} = (f_{CENT} - 5)$ MHz, $f_{LO} = (f_{CENT} - 153)$ MHz, blocker level = 0 dBm.
[6] $f_{RF1} = (f_{CENT} - 1)$ MHz, $f_{RF2} = f_{CENT}$, $f_{LO} = (f_{CENT} - 153)$ MHz, each RF tone at −10 dBm.
[7] $f_{RF1} = f_{CENT}$, $f_{RF2} = (f_{CENT} + 100)$ MHz, $f_{LO} = (f_{CENT} - 153)$ MHz, each RF tone at −10 dBm.
[8] For details, see the Spur Performance section.
[9] V_S = 5 V, VSET = 4.5 V, T_A = 25°C, $f_{LO} = (f_{RF} - 211)$ MHz, LO power = 0 dBm, Z_0 = 50 Ω.
[10] Excluding 4:1 IF port transformer (TC4-1W+), RF and LO port transformers (2500BL14M050), and PCB loss.
[11] $f_{RF1} = f_{CENT}$, $f_{BLOCKER} = (f_{CENT} - 5)$ MHz, $f_{LO} = (f_{CENT} - 235)$ MHz, blocker level = 0 dBm.
[12] V_S = 5 V, VSET = 5 V, T_A = 25°C, $f_{LO} = (f_{RF} - 153)$ MHz, LO power = 0 dBm, Z_0 = 50 Ω.
[13] Including 4:1 IF port transformer (TC4-1W+), RF and LO port transformers (3600BL14M050), and PCB loss.
[14] $f_{RF1} = f_{CENT}$, $f_{BLOCKER} = (f_{CENT} - 5)$ MHz, $f_{LO} = (f_{CENT} - 153)$ MHz, blocker level = −20 dBm.
[15] V_S = 5 V, VSET = 4.8 V, T_A = 25°C, $f_{LO} = (f_{RF} - 380)$ MHz, LO power = 0 dBm, Z_0 = 50 Ω.
[16] Including 4:1 IF port transformer (TC4-1W+), RF and LO port transformers (5400BL15B050), and PCB loss.
[17] $f_{RF1} = f_{CENT}$, $f_{BLOCKER} = (f_{CENT} - 5)$ MHz, $f_{LO} = (f_{CENT} - 300)$ MHz, blocker level = −20 dBm.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Supply Voltage, VPOS	5.5 V
VSET, ENBL	5.5 V
OP1+, OP1−, OP2+, OP2−	5.5 V
RF Input Power	20 dBm
Internal Power Dissipation	1.6 W
θ_{JA} (Exposed Paddle Soldered Down)[1]	26.5°C/W
θ_{JC} (at Exposed Paddle)	8.7°C/W
Maximum Junction Temperature	150°C
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C

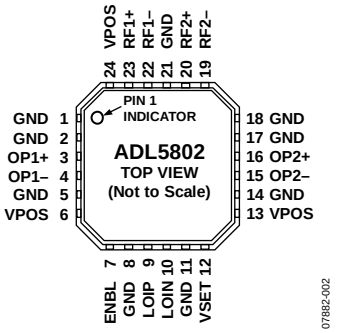
[1] As measured on the evaluation board. For details, see the Evaluation Board section.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES
1. THERE IS AN EXPOSED PADDLE THAT MUST BE SOLDERED TO GROUND.

Figure 2. Pin Configuration

Table 3. Pin Function Descriptions

Pin No.	Mnemonic	Function
1, 2, 5, 8, 11, 14, 17, 18, 21	GND	Device Common (DC Ground).
3, 4	OP1+, OP1−	Channel 1 Mixer Differential Output Terminals. Bias must be applied through pull-up choke inductors or the center tap of the IF transformer.
6, 13, 24	VPOS	Positive Supply Voltage. 5.0 V nominal.
7	ENBL	Device Enable. Pull low or leave disconnected to enable the device; pull high to disable the device.
9, 10	LOIP, LOIN	Differential LO Input Terminals. Internally matched to 50 Ω; must be ac-coupled.
12	VSET	High Input IP3 Bias Control. For high input IP3 performance, apply ~4 V to 5 V. Improved noise figure (NF) performance and lower supply current can be set by applying ~2 V to 3 V to the VSET pin. A resistor can be connected to the supply to raise the voltage, whereas a resistor to GND lowers the voltage.
15, 16	OP2−, OP2+	Channel 2 Mixer Differential Output Terminals. Bias must be applied through pull-up choke inductors or the center tap of the IF transformer.
19, 20	RF2−, RF2+	Differential RF Input Terminals for Channel 2. Internally matched to 50 Ω; must be ac-coupled.
22, 23	RF1−, RF1+	Differential RF Input Terminals for Channel 1. Internally matched to 50 Ω; must be ac-coupled.
	EPAD	Exposed Paddle. Must be soldered to ground.

TYPICAL PERFORMANCE CHARACTERISTICS

DOWNCONVERTER MODE USING A BROADBAND BALUN

V_S = 5 V, T_A = 25°C, VSET = 4 V, IF = 153 MHz, as measured using a typical circuit schematic with low-side local oscillator (LO), unless otherwise noted. Insertion loss of input and output baluns (TC1-1-13M+, TC4-1W+) is extracted from the gain measurement.

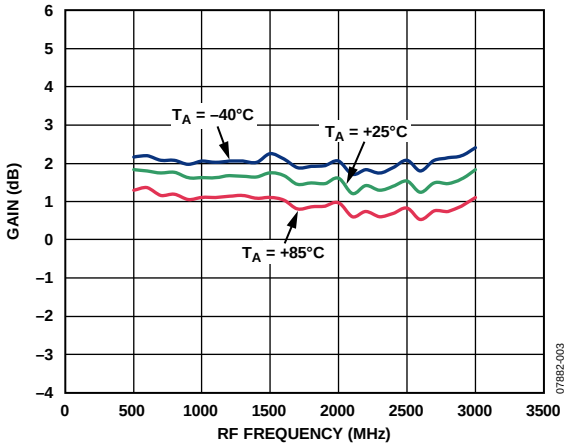


Figure 3. Power Conversion Gain vs. RF Frequency

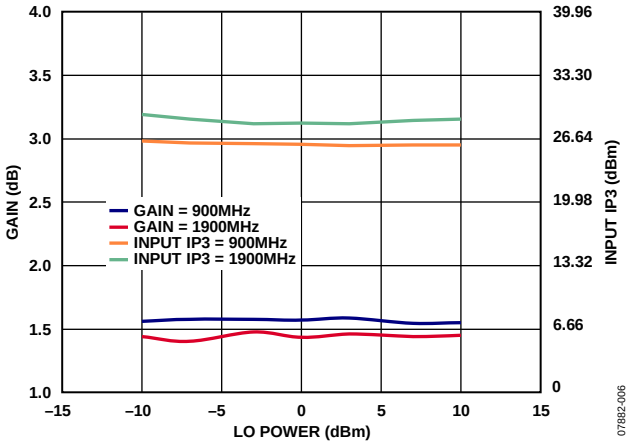


Figure 6. Power Conversion Gain and Input IP3 vs. LO Power

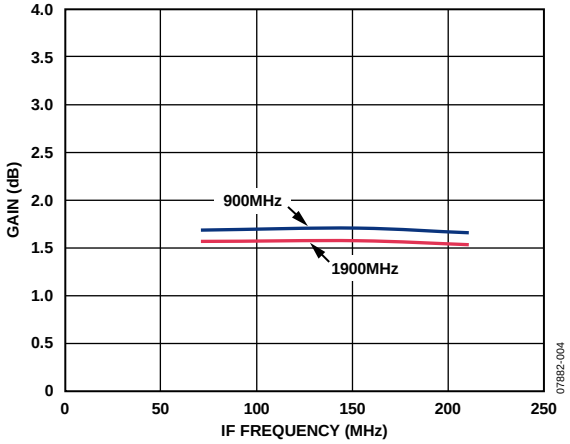


Figure 4. Power Conversion Gain vs. IF Frequency

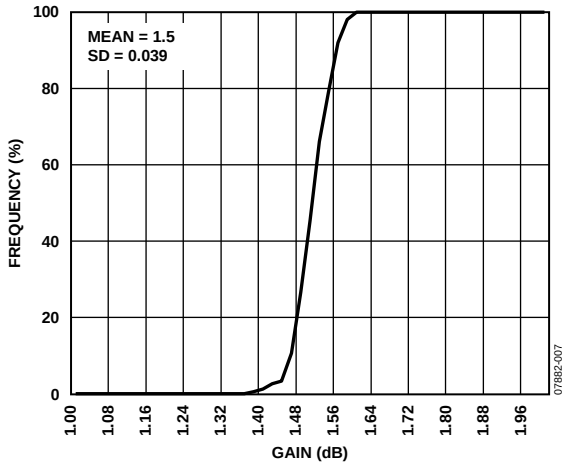


Figure 7. Power Conversion Gain Distribution

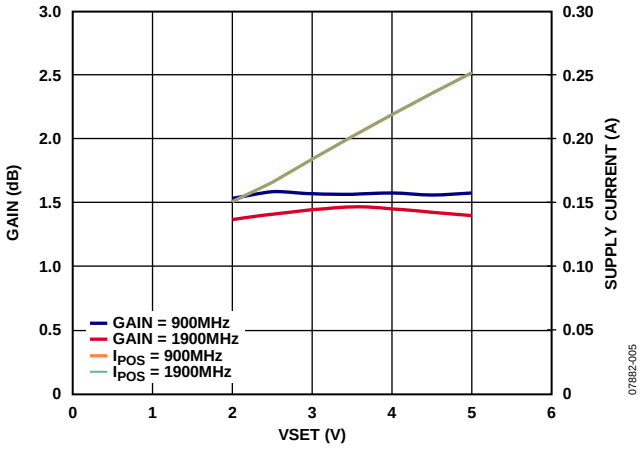


Figure 5. Power Conversion Gain and I_{POS} vs. VSET

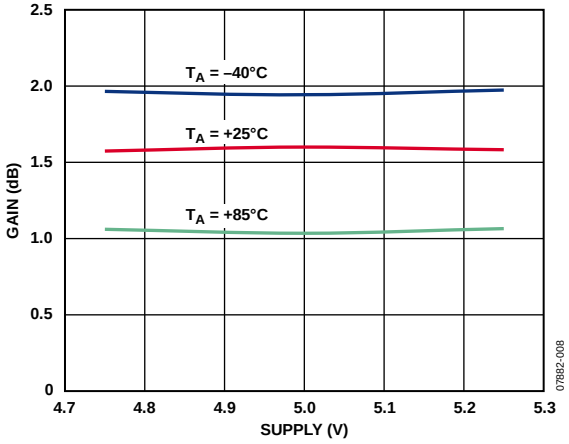


Figure 8. Power Conversion Gain vs. Supply Voltage

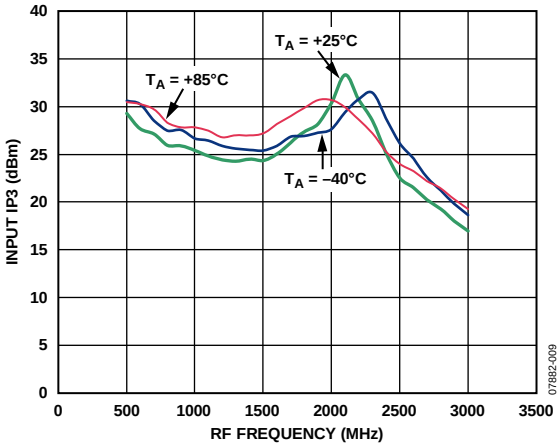


Figure 9. Input IP3 vs. RF Frequency

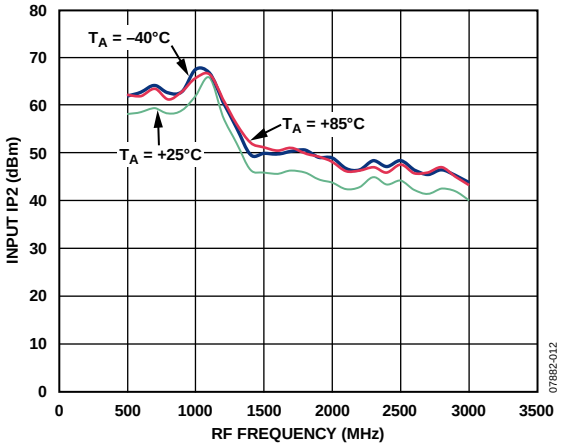


Figure 12. Input IP2 vs. RF Frequency

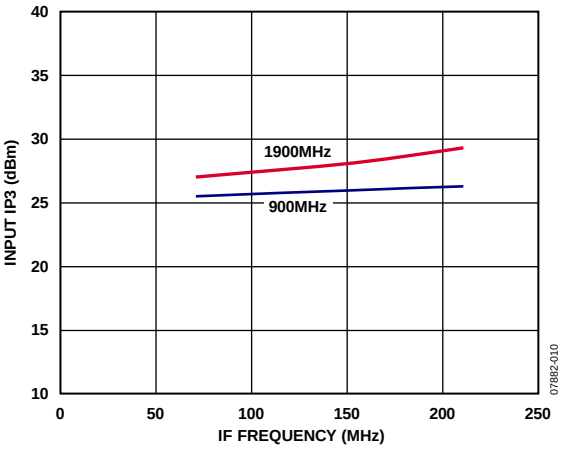


Figure 10. Input IP3 vs. IF Frequency

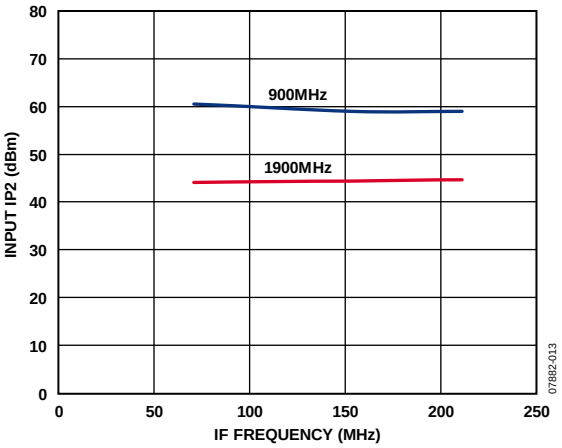


Figure 13. Input IP2 vs. IF Frequency

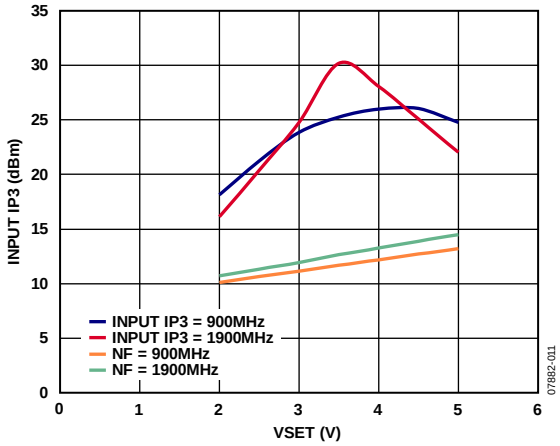


Figure 11. Input IP3, Noise Figure vs. VSET

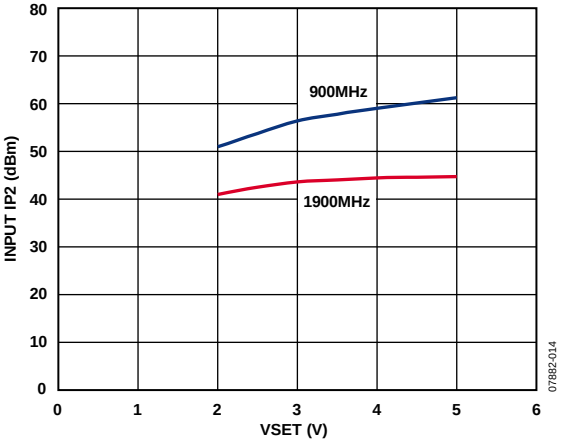


Figure 14. Input IP2 vs. VSET

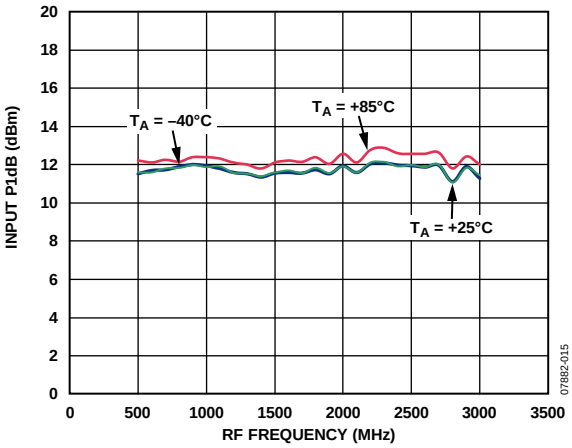


Figure 15. Input P1dB vs. RF Frequency

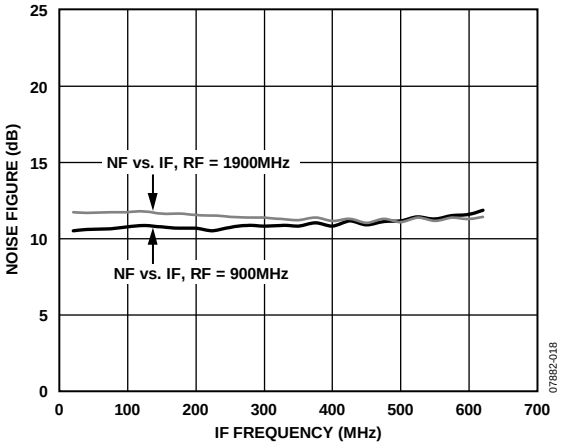


Figure 18. SSB Noise Figure vs. IF Frequency

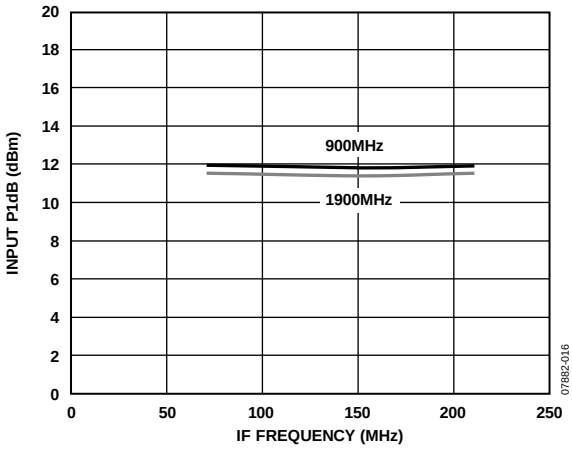


Figure 16. Input P1dB vs. IF Frequency

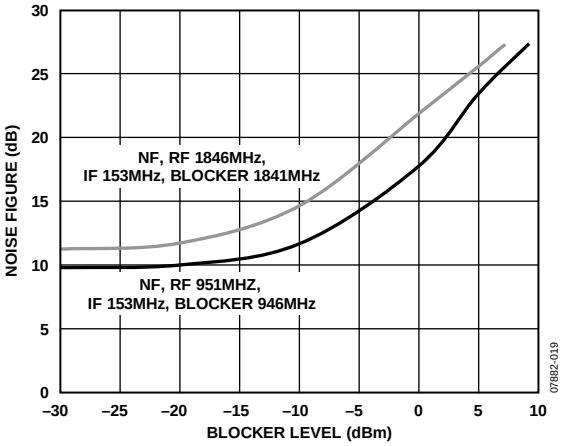


Figure 19. SSB Noise Figure vs. Blocker Level

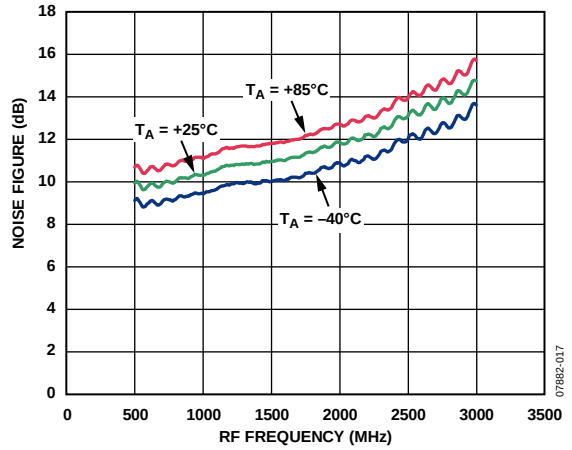


Figure 17. SSB Noise Figure vs. RF Frequency

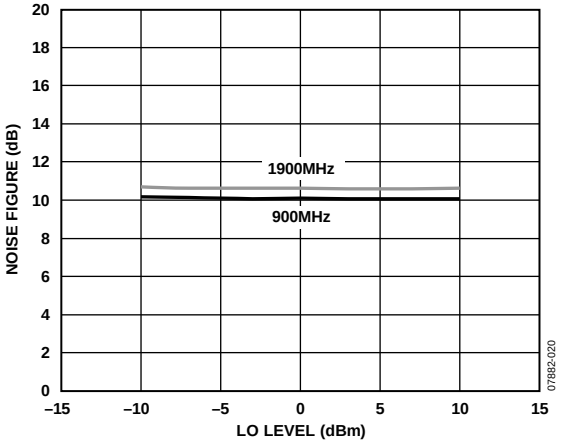


Figure 20. SSB Noise Figure vs. LO Drive

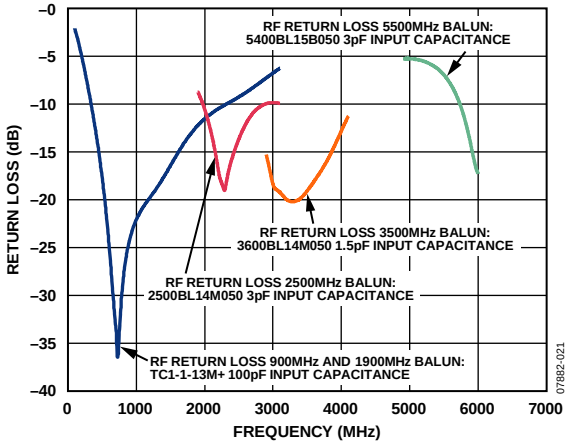


Figure 21. RF Return Loss Measured Differentially at the RF Port

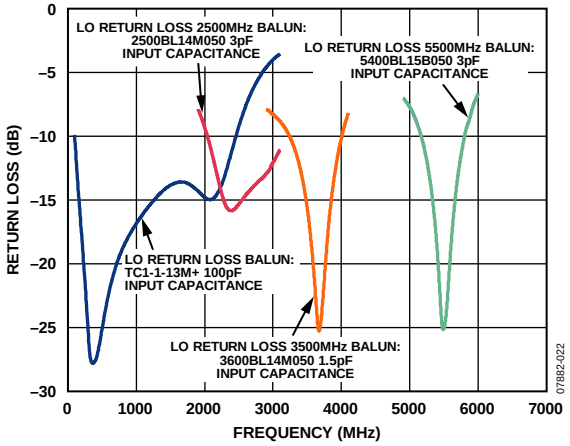


Figure 22. LO Return Loss Measured Differentially at the LO Port

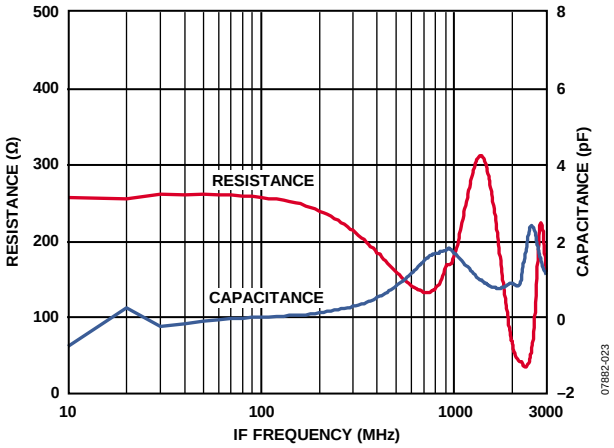


Figure 23. IF Differential Output Impedance (R Parallel C Equivalent)

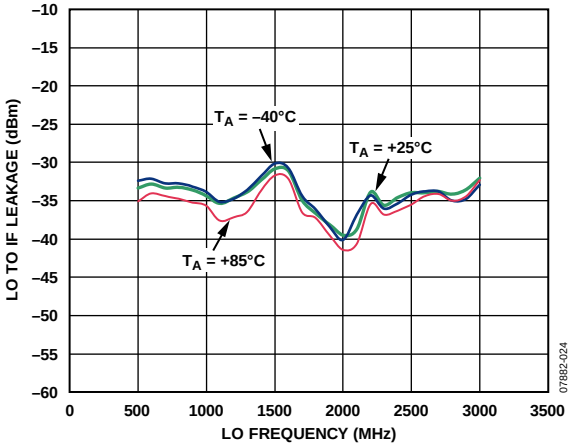


Figure 24. LO to IF Leakage vs. LO Frequency

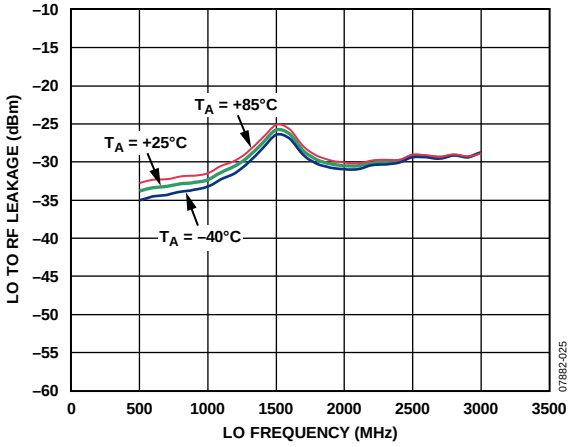


Figure 25. LO to RF Leakage vs. LO Frequency

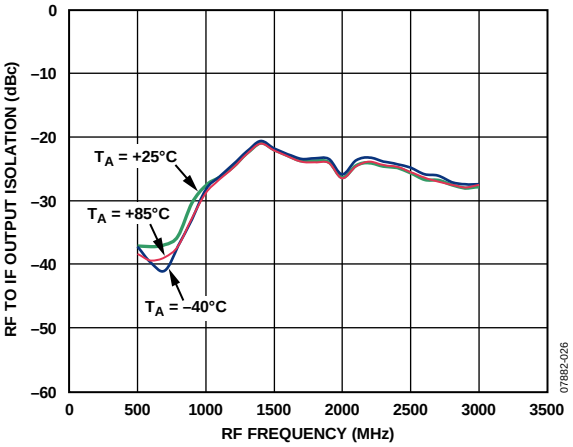


Figure 26. RF to IF Output Isolation vs. RF Frequency

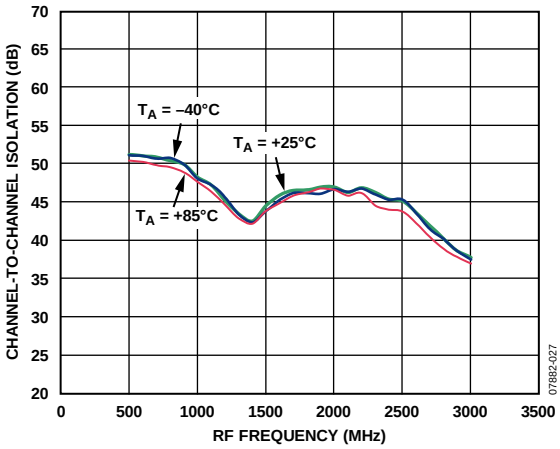


Figure 27. RF Channel Isolation

DOWNCONVERTER MODE USING A JOHANSON 2.7 GHZ BALUN

V_S = 5 V, T_A = 25°C, VSET = 4.5 V, IF = 211 MHz, as measured using a typical circuit schematic with low-side LO, unless otherwise noted. Insertion loss of input and output baluns (2500BL14M050, TC4-1W+) is included in the gain measurement.

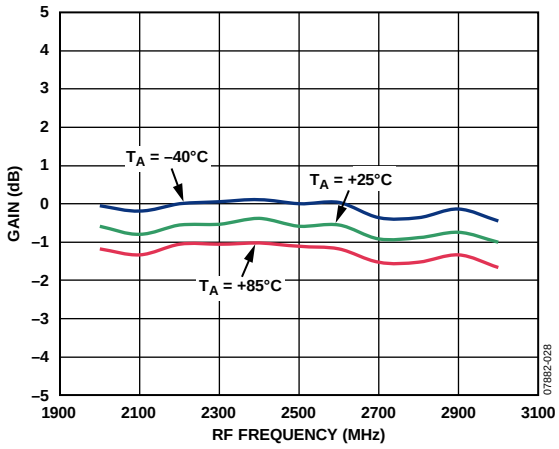


Figure 28. Power Conversion Gain vs. RF Frequency

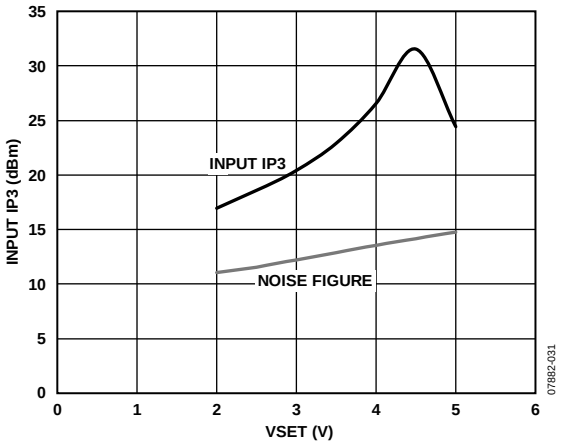


Figure 31. Input IP3, Noise Figure vs. VSET

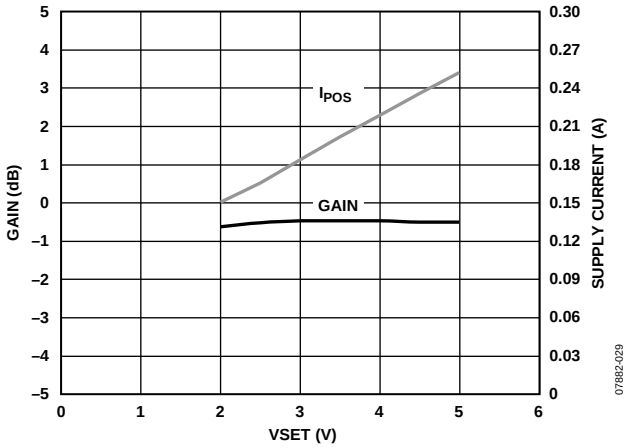


Figure 29. Power Conversion Gain and I_{POS} vs. VSET

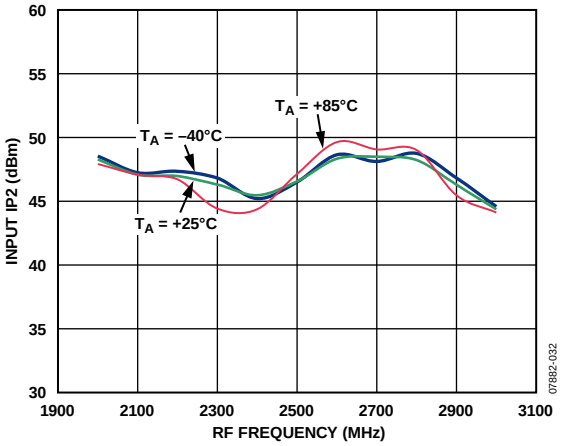


Figure 32. Input IP2 vs. RF Frequency

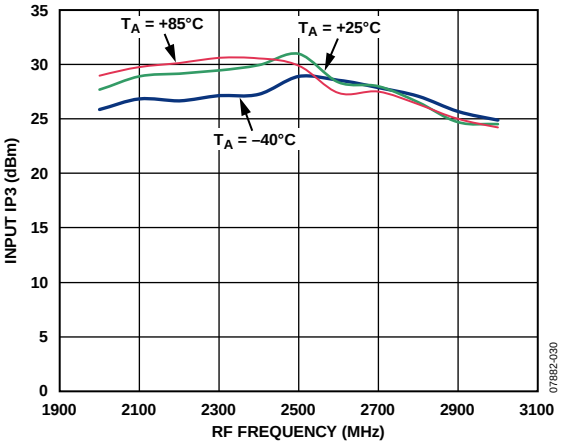


Figure 30. Input IP3 vs. RF Frequency

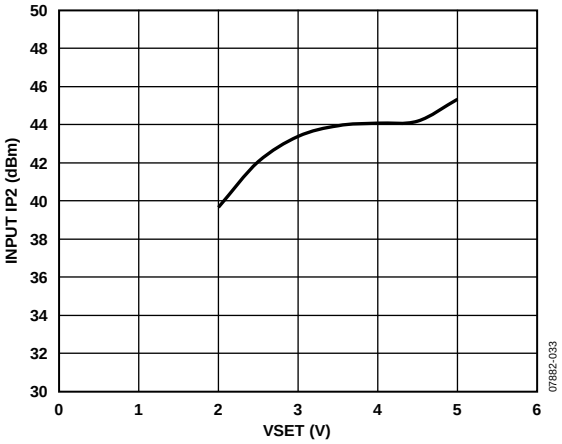


Figure 33. Input IP2 vs. VSET

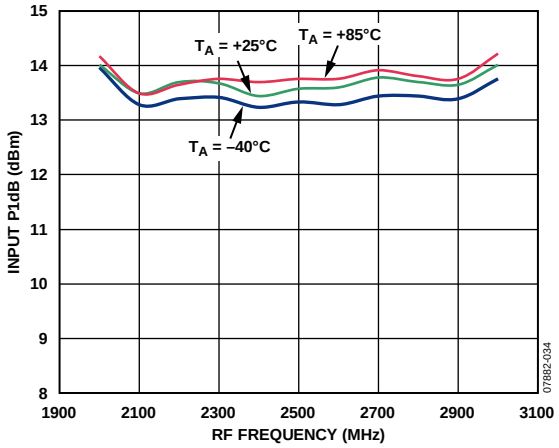


Figure 34. Input P1dB vs. RF Frequency

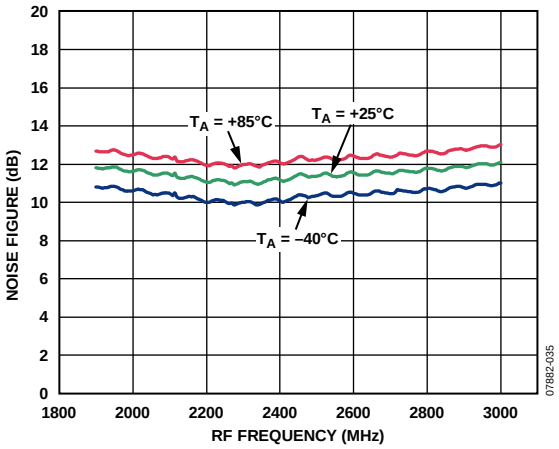


Figure 35. SSB Noise Figure vs. RF Frequency

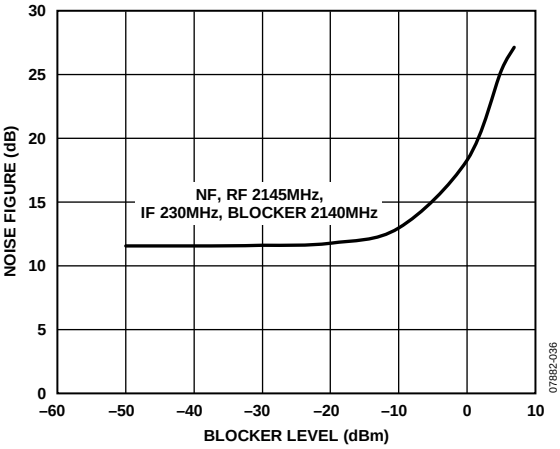


Figure 36. SSB Noise Figure vs. Blocker Level

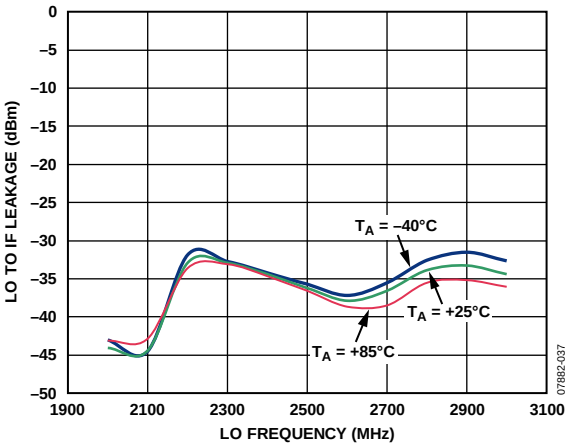


Figure 37. LO to IF Leakage vs. LO Frequency

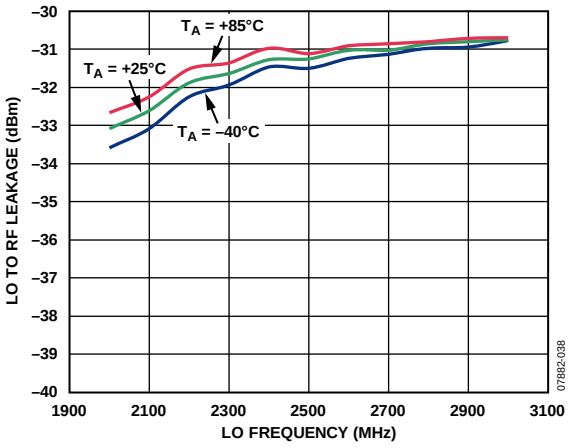


Figure 38. LO to RF Leakage vs. LO Frequency

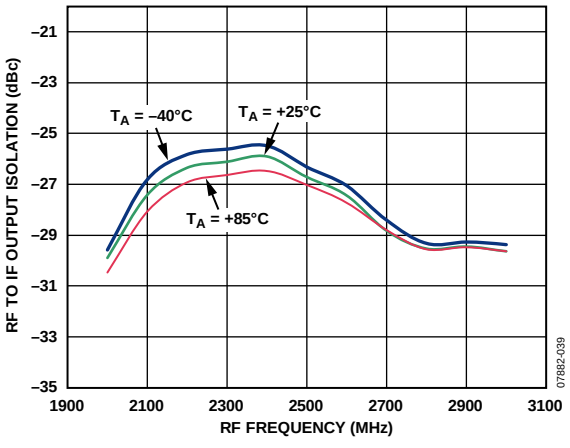


Figure 39. RF to IF Output Isolation vs. RF Frequency

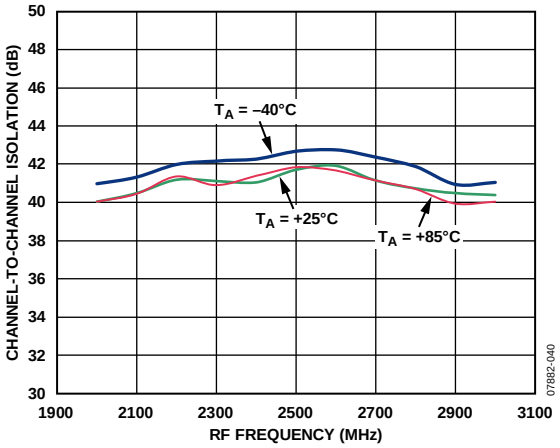


Figure 40. RF Channel Isolation

DOWNCONVERTER MODE USING A JOHANSON 3.5 GHZ BALUN

V_S = 5 V, T_A = 25°C, VSET = 5 V, IF = 153 MHz, as measured using a typical circuit schematic with low-side LO, unless otherwise noted. Insertion loss of input and output baluns (3600BL14M050, TC4-1W+) is included in the gain measurement.

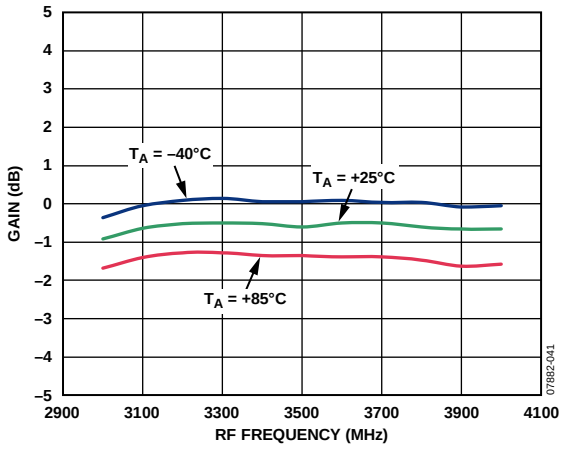


Figure 41. Power Conversion Gain vs. RF Frequency

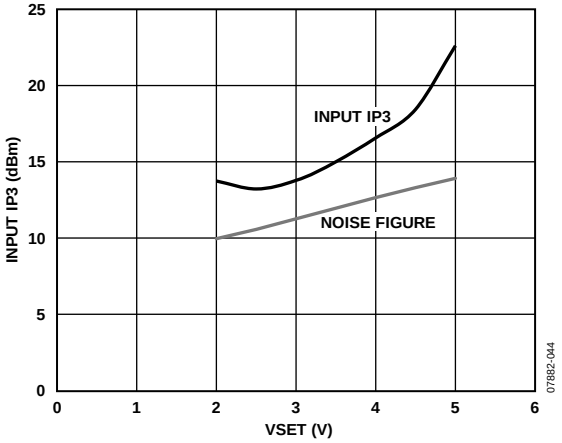


Figure 44. Input IP3, Noise Figure vs. VSET

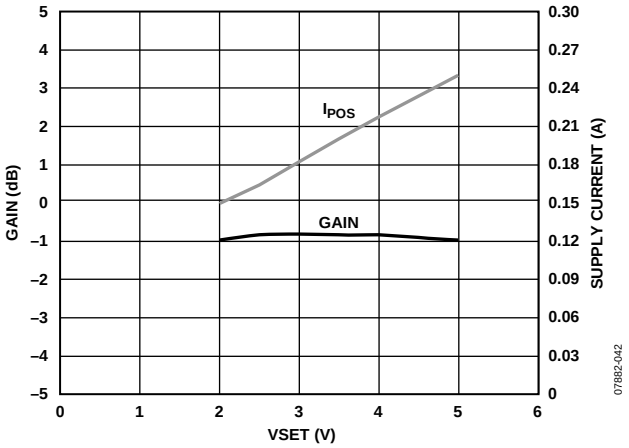


Figure 42. Power Conversion Gain and I_{POS} vs. VSET

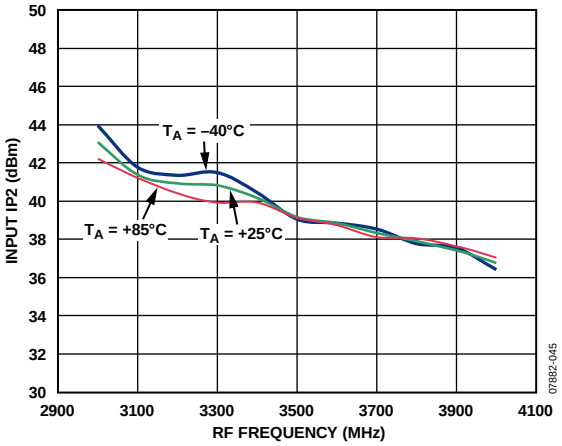


Figure 45. Input IP2 vs. RF Frequency

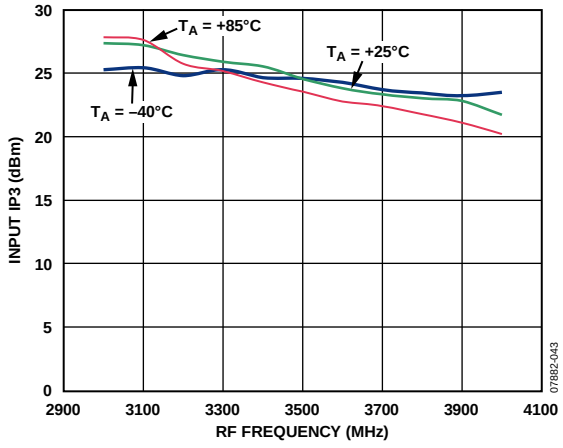


Figure 43. Input IP3 vs. RF Frequency

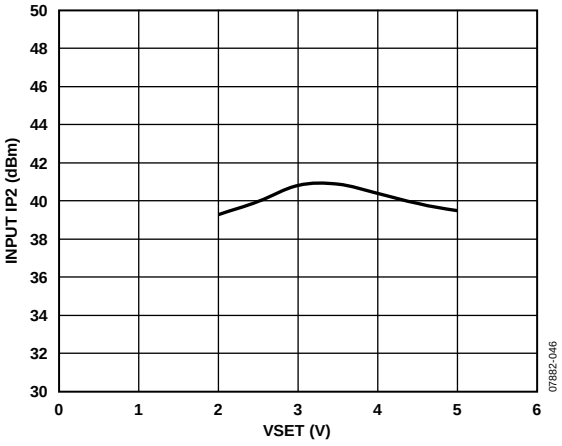


Figure 46. Input IP2 vs. VSET

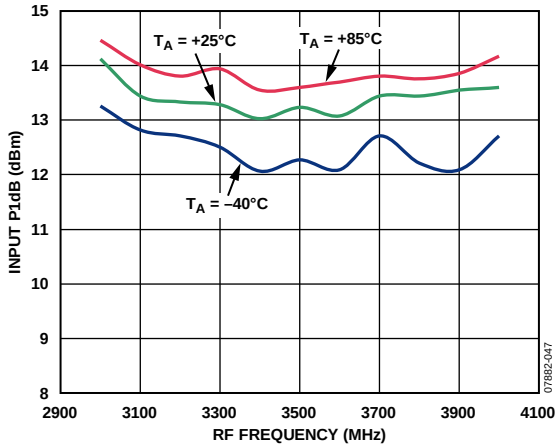


Figure 47. Input P1dB vs. RF Frequency

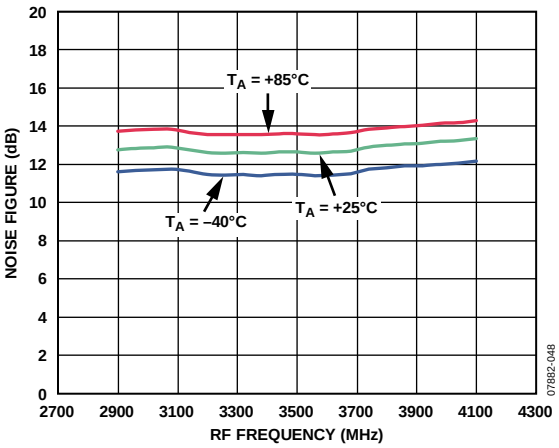


Figure 48. SSB Noise Figure vs. RF Frequency

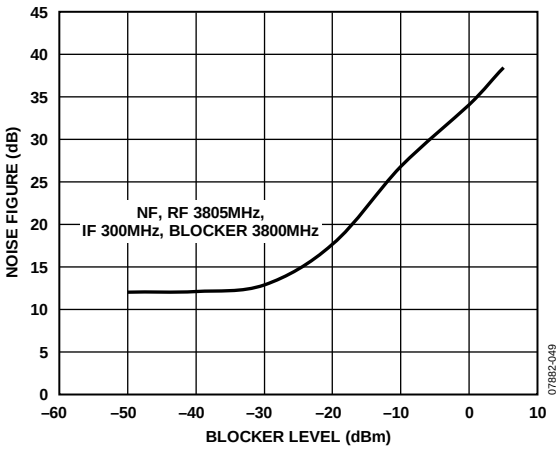


Figure 49. SSB Noise Figure vs. Blocker Level

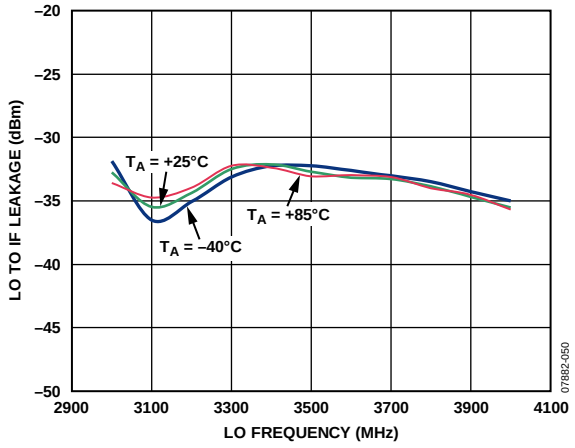


Figure 50. LO to IF Leakage vs. LO Frequency

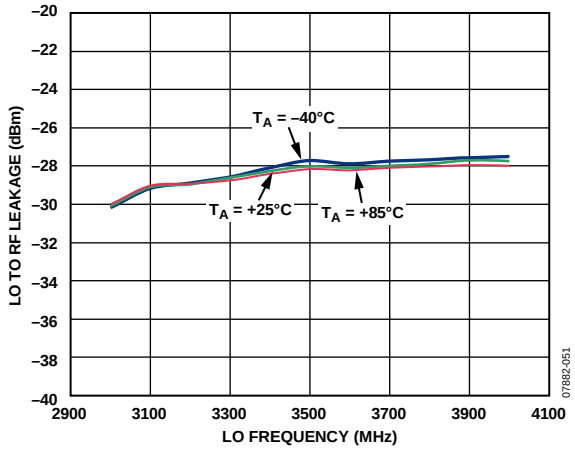


Figure 51. LO to RF Leakage vs. LO Frequency

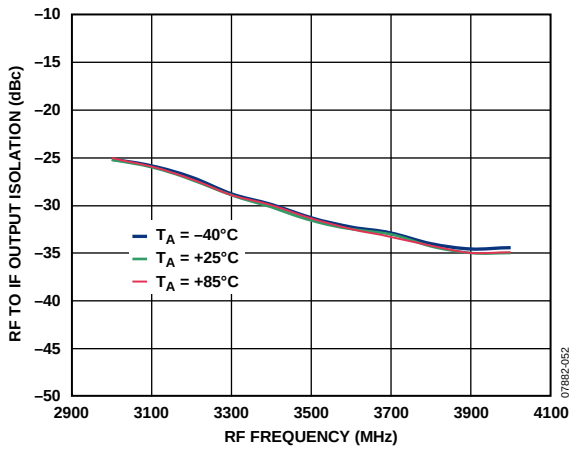


Figure 52. RF to IF Output Isolation vs. RF Frequency

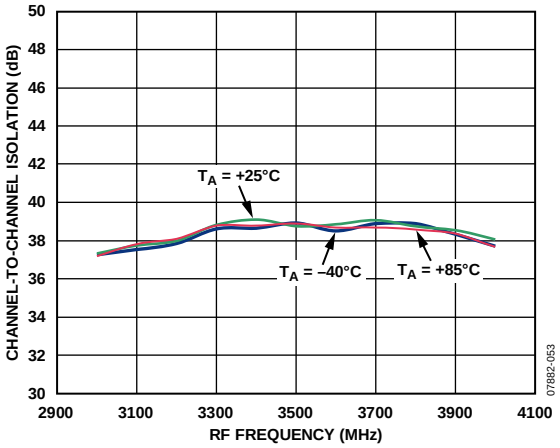


Figure 53. RF Channel Isolation

DOWNCONVERTER MODE USING A JOHANSON 5.7 GHZ BALUN

V_S = 5 V, T_A = 25°C, VSET = 4.8 V, IF = 380 MHz, as measured using a typical circuit schematic with low-side LO, unless otherwise noted. Insertion loss of input and output baluns (5400BL15B050, TC4-1W+) is included in the gain measurement.

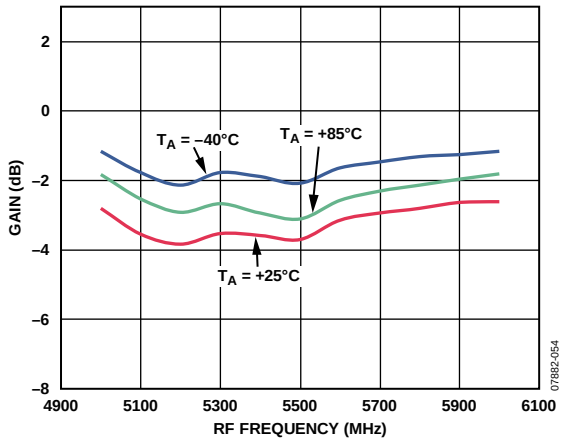


Figure 54. Power Conversion Gain vs. RF Frequency

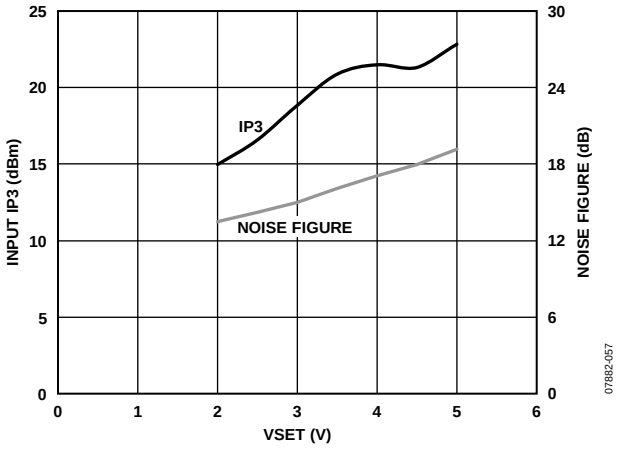


Figure 57. Input IP3, Noise Figure vs. VSET

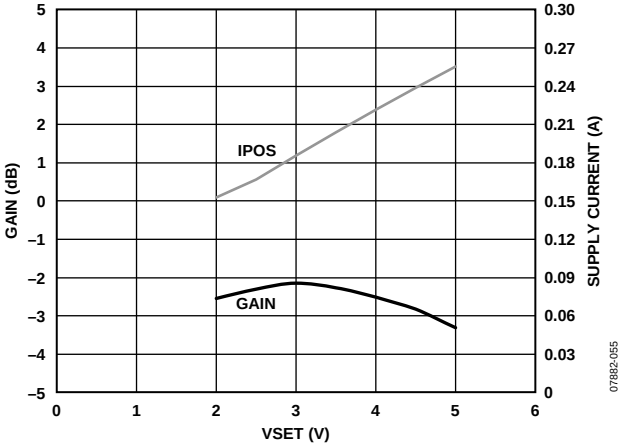


Figure 55. Power Conversion Gain and I_{POS} vs. VSET

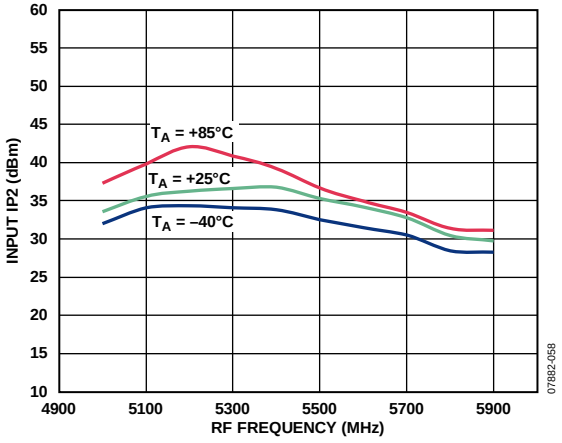


Figure 58. Input IP2 vs. RF Frequency

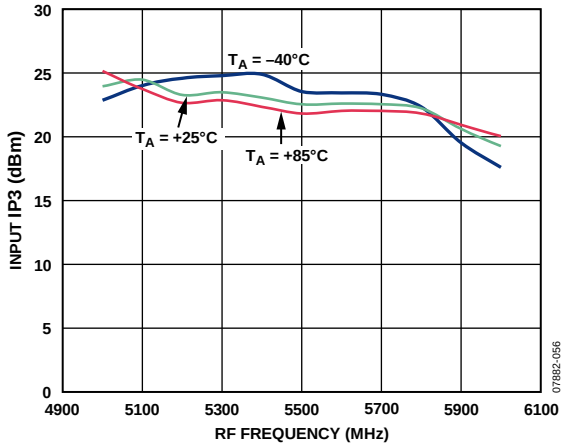


Figure 56. Input IP3 vs. RF Frequency

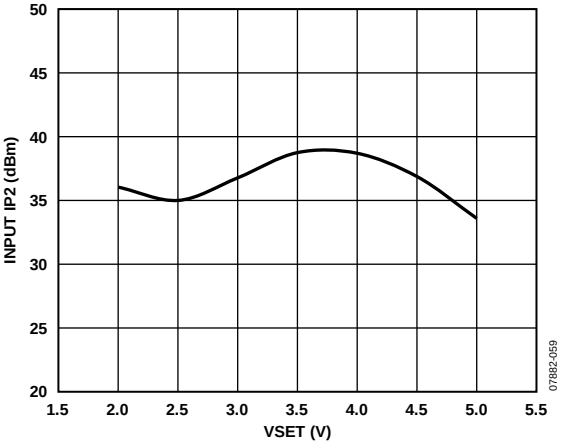


Figure 59. Input IP2 vs. VSET

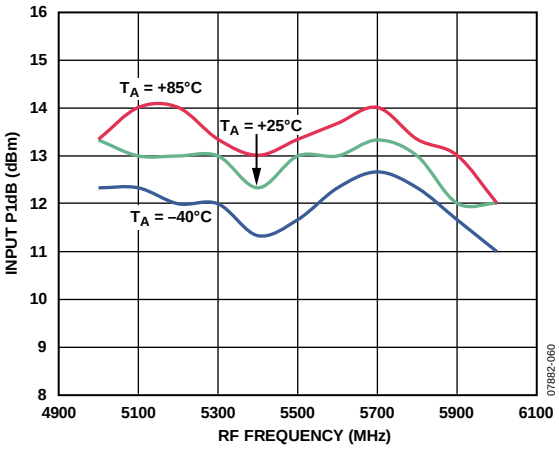


Figure 60. Input P1dB vs. RF Frequency

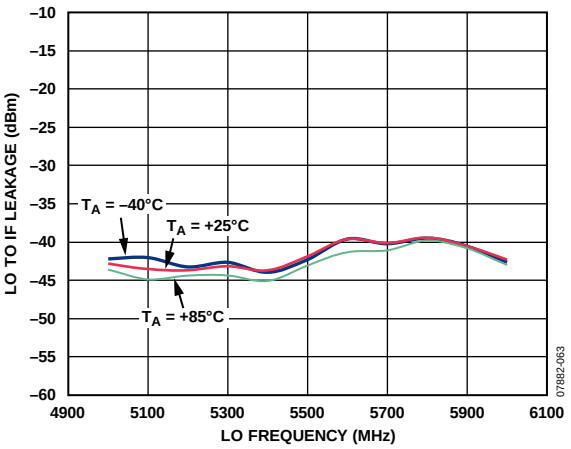


Figure 63. LO to IF Leakage vs. LO Frequency

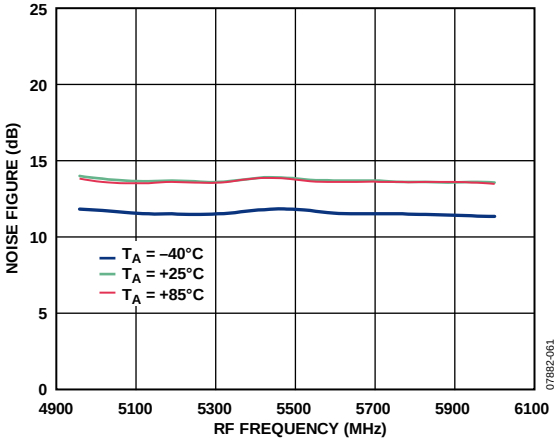


Figure 61. SSB Noise Figure vs. RF Frequency

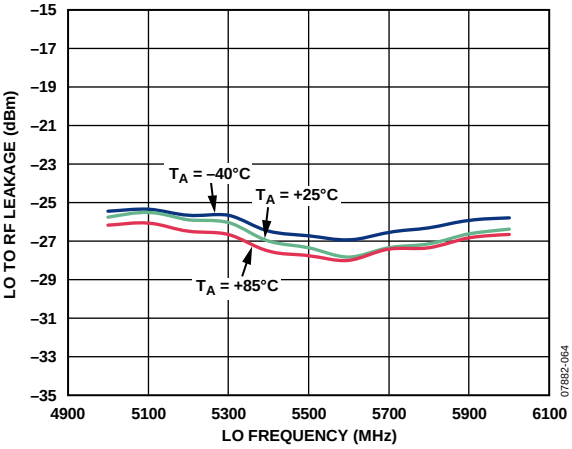


Figure 64. LO to RF Leakage vs. LO Frequency

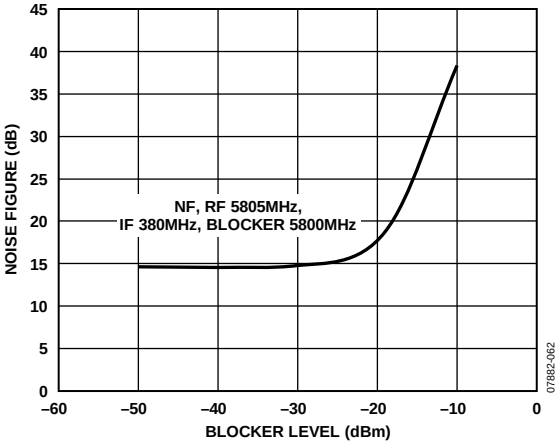


Figure 62. SSB Noise Figure vs. Blocker Level

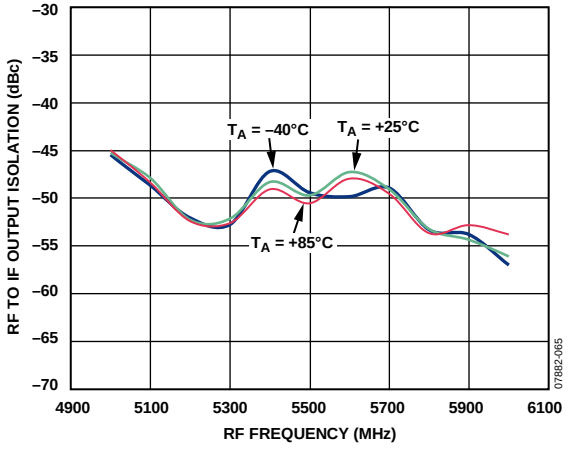


Figure 65. RF to IF Output Isolation vs. RF Frequency

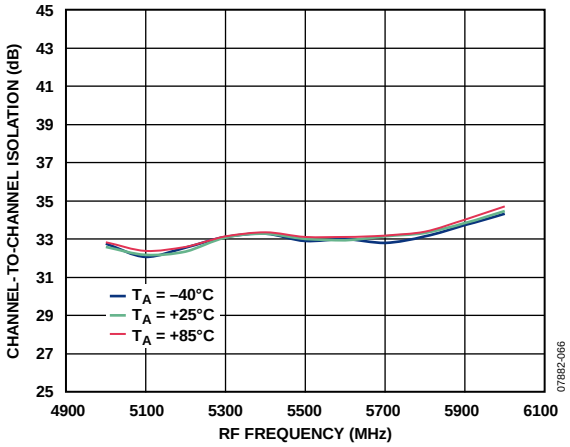


Figure 66. RF Channel Isolation

SPUR PERFORMANCE

All spur tables are (N × f_{RF}) − (M × f_{LO}) and were measured using the standard evaluation board (see the Evaluation Board section). Mixer spurious products are measured in decibels relative to the carrier (dBc) from the IF output power level. Data was measured for frequencies less than 6 GHz only. The typical noise floor of the measurement system is −100 dBm.

900 MHz Performance

V_S = 5 V, VSET = 4 V, T_A = 25°C, RF power = 0 dBm, LO power = 0 dBm, f_{RF} = 900 MHz, f_{LO} = 703 MHz, Z_0 = 50 Ω.

		M														
		0	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**
N	**0**		−35.9	−25.5	−47.3	−27.4	−51.5	−37.5	−62.1	−47.5						
	1	−34.3	0.0	−46.3	−19.8	−64.3	−30.0	−75.6	−45.0	−67.8	−55.3					
	2	−49.1	−69.2	−68.2	−61.6	−68.7	−80.7	−67.5	−88.1	−79.1	−82.6	−91.5	≤100			
	3	−86.7	−79.6	≤100	−67.3	−98.0	−71.0	≤100	−86.3	≤100	≤100	≤100	−98.4	≤100		
	4	−91.8	≤100	−96.4	≤100	≤100	≤100	≤100	≤100	≤100	≤100	≤100	≤100	≤100	≤100	
	5	≤100	≤100	≤100	≤100	≤100	≤100	≤100	≤100	≤100	≤100	≤100	≤100	≤100	≤100	≤100
	6	≤100	≤100	≤100	≤100	≤100	≤100	≤100	≤100	≤100	≤100	≤100	≤100	≤100	≤100	≤100
	7		≤100	≤100	≤100	≤100	≤100	≤100	≤100	≤100	≤100	≤100	≤100	≤100	≤100	≤100
	8			≤100	≤100	≤100	≤100	≤100	≤100	≤100	≤100	≤100	≤100	≤100	≤100	≤100
	9				≤100	≤100	≤100	≤100	≤100	≤100	≤100	≤100	≤100	≤100	≤100	≤100
	10						≤100	≤100	≤100	≤100	≤100	≤100	≤100	≤100	≤100	≤100
	11							≤100	≤100	≤100	≤100	≤100	≤100	≤100	≤100	≤100
	12								≤100	≤100	≤100	≤100	≤100	≤100	≤100	≤100
	13										≤100	≤100	≤100	≤100	≤100	≤100
	14											≤100	≤100	≤100	≤100	≤100
	15												≤100	≤100	≤100	≤100

2090 MHz Performance

V_S = 5 V, VSET = 4 V, T_A = 25°C, RF power = 0 dBm, LO power = 0 dBm, f_{RF} = 2090 MHz, f_{LO} = 1842 MHz, Z_0 = 50 Ω.

		M														
		0	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**
N	**0**		−43.0	−23.7	−52.9											
	1	−26.8	0.0	−59.6	−42.2	−80.5										
	2	−59.8	−71.9	−53.8	−67.5	−68.2	−84.1									
	3		−67.6	−97.6	−59.3	−92.2	−79.3	≤100								
	4			≤100	≤100	−93.7	−97.8	≤100	≤100							
	5				≤100	≤100	−96.1	≤100	≤100	≤100						
	6					≤100	≤100	≤100	≤100	≤100	≤100	≤100				
	7						≤100	≤100	≤100	≤100	≤100	≤100	≤100			
	8							≤100	≤100	≤100	≤100	≤100	≤100	≤100		
	9								≤100	≤100	≤100	≤100	≤100	≤100	≤100	
	10										≤100	≤100	≤100	≤100	≤100	≤100
	11											≤100	≤100	≤100	≤100	≤100
	12												≤100	≤100	≤100	≤100
	13													≤100	≤100	≤100
	14														≤100	≤100
	15															≤100

2600 MHz Performance

V_S = 5 V, VSET = 4.5 V, T_A = 25°C, RF power = 0 dBm, LO power = 0 dBm, f_{RF} = 2600 MHz, f_{LO} = 2350 MHz, Z_0 = 50 Ω.

		M														
		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14
N	0		−37.9	−31.5												
	1	−27.5	0.0	−62.6	−36.3											
	2	−75.5	−59.7	−52.2	−65.8	−68.8										
	3		−75.0	−88.7	−56.3	−86.8	−90.5									
	4			≤100	≤100	−82.5	−92.1	≤100								
	5				≤100	≤100	−94.4	≤100	≤100	≤100						
	6						≤100	≤100	≤100	≤100	≤100					
	7							≤100	≤100	≤100	≤100	≤100				
	8								≤100	≤100	≤100	≤100	≤100			
	9									≤100	≤100	≤100	≤100	≤100		
	10										≤100	≤100	≤100	≤100	≤100	
	11											≤100	≤100	≤100	≤100	≤100
	12												≤100	≤100	≤100	≤100
	13													≤100	≤100	≤100
	14														≤100	≤100
	15															

3500 MHz Performance

V_S = 5 V, VSET= 5 V, T_A = 25°C, RF power = 0 dBm, LO power = 0 dBm, f_{RF} = 3500 MHz, f_{LO} = 3800 MHz, Z_0 = 50 Ω.

		M														
		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14
N	0		−43.0	−23.7	−52.9											
	1	−26.8	0.0	−59.6	−42.2	−80.5										
	2	−59.8	−71.9	−53.8	−67.5	−68.2	−84.1									
	3		−67.6	−97.6	−59.3	−92.2	−79.3	≤100								
	4			≤100	≤100	−93.7	−97.8	≤100	≤100							
	5				≤100	≤100	−96.1	≤100	≤100	≤100						
	6					≤100	≤100	≤100	≤100	≤100	≤100	≤100				
	7						≤100	≤100	≤100	≤100	≤100	≤100	≤100			
	8							≤100	≤100	≤100	≤100	≤100	≤100	≤100		
	9								≤100	≤100	≤100	≤100	≤100	≤100	≤100	
	10										≤100	≤100	≤100	≤100	≤100	≤100
	11											≤100	≤100	≤100	≤100	≤100
	12												≤100	≤100	≤100	≤100
	13													≤100	≤100	≤100
	14														≤100	≤100
	15															≤100

5800 MHz Performance

V_S = 5 V, VSET= 4.8 V, T_A = 25°C, RF power = −10 dBm, LO power = 0 dBm, f_{RF} = 5800 MHz, f_{LO} = 5600 MHz, Z_0 = 50 Ω.

		M														
		0	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**
N	**0**		−28.3													
	1	−63.6	0.0	−80.5												
	2			−48.6	−92.6											
	3				−64.2	−98.7										
	4					−90.5	−98.3									
	5						≤100	−99.4								
	6							−81.6	−98.0							
	7								−87.2	−95.9						
	8									−84.0	−99.5					
	9										≤100	≤100				
	10											≤100	≤100			
	11												≤100	≤100		
	12													≤100	−99.6	
	13														≤100	−99.8
	14															≤100
	15															

CIRCUIT DESCRIPTION

The ADL5802 provides two double-balanced active mixers. These mixers are designed for a 50 Ω input impedance and a 200 Ω output impedance. Both are driven from a common local oscillator (LO) amplifier. The RF inputs and LO outputs are differential, providing maximum usable bandwidth at the input and output ports. The LO also operates with a 50 Ω input impedance and can, optionally, be operated differentially or single-ended. The input, output, and LO ports can be operated over an exceptionally wide frequency range. The ADL5802 can be configured as a downconvert mixer or as an upconvert mixer.

The ADL5802 can be divided into the following sections: the local oscillator (LO) amplifier and splitter, the RF voltage-to-current (V-to-I) converter, the mixer cores, the output loads, and the bias circuit. A simplified block diagram of the device is shown in Figure 67. The LO block generates a pair of differential LO signals to drive two mixer cores. The RF input is converted into current by the V-to-I converters that then feed into the two mixer cores. The internal differential load of the mixers is designed for a wideband 200 Ω output impedance from the mixer. Reference currents to each section are generated by the bias circuit, which can be enabled or disabled using the ENBL pin. A detailed description of each section of the ADL5802 follows.

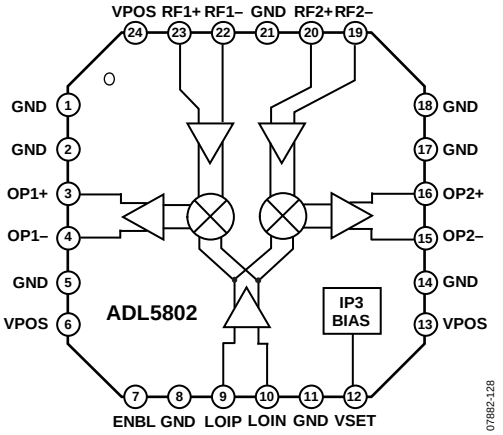


Figure 67. ADL5802 Block Diagram

LO AMPLIFIER AND SPLITTER

The LO input is amplified using a broadband LNA and is then split and followed by separate LO limiting amplifiers. The LNA input impedance is nominally 50 Ω. The LO is designed to accommodate a wide range of LO input power levels. The LO input is conditioned by the series of amplifiers to provide a well controlled and limited LO swing to the mixer core, resulting in excellent IP3. The LO circuit exhibits low additive noise, resulting in an excellent mixer noise figure and output noise under RF blocking. For optimal performance, the LO inputs should be driven differentially but at lower frequencies; single-ended drive is acceptable.

RF VOLTAGE TO CURRENT (V-TO-I) CONVERTER

The differential RF input signal is applied to a voltage-to-current converter that converts the differential input voltage to output currents. The V-to-I converter provides a 50 Ω input impedance. The V-to-I section bias current can be adjusted up or down using the VSET pin. Adjusting the current up improves IP3 and P1dB input but degrades SSB NF. Adjusting the current down improves SSB NF but degrades IP3 and P1dB input. The conversion gain remains nearly constant over a wide range of VSET pin settings, allowing the part to be adjusted dynamically without affecting the conversion gain. The current adjustment can be made by connecting a resistor from the VSET pin to the positive supply to increase the bias current or from the VSET pin to ground to decrease the bias current. The VSET pin impedance is approxi-mately 675 Ω in series with two diodes and an internal current source.

MIXER CORES

The ADL5802 has two double-balanced mixers that use high performance SiGe NPN transistors. These mixers are based on the Gilbert cell design of four cross-connected transistors.

MIXER LOAD

Each mixer load is designed to use a pair of 100 Ω resistors connected to the positive supply. This provides a 200 Ω differential output resistance. The mixer output should be pulled to the positive supply externally using a pair of RF chokes or using an output transformer with the center tap connected to the positive supply. It is possible to exclude these components when the mixer core current is low, but both P1dB and IP3 are then reduced.

The mixer load output can operate from direct current (dc) up to approximately 500 MHz into a 200 Ω load. For upconversion applications, the mixer load can be matched using off-chip matching components. Transmit operation up to 2 GHz is possible. See the Applications Information section for matching circuit details.

BIAS CIRCUIT

A band gap reference circuit generates the reference currents used by the mixers. The bias circuit can be enabled and disabled using the ENBL pin. If the ENBL pin is grounded or left open, the part is enabled. Pulling the ENBL pin high shuts off the bias circuit and disables the part. However, the ENBL pin does not alter the current in the LO section and, therefore, does not provide a true power-down feature. Certain configurations may require the VSET pin to be connected to the positive supply through a resistor. This will result in an increased mixer core current. Unless this resistor to positive supply is removed, bias current will continue to be supplied to the mixer core.

APPLICATIONS INFORMATION

BASIC CONNECTIONS

The ADL5802 features dual channel mixers with a common local oscillator (LO). The mixer is designed to translate between radio frequencies (RF) and intermediate frequencies (IF). For both upconversion and downconversion applications, RF1+ (Pin 23), RF1− (Pin 22), RF2+ (Pin 20), and RF2− (Pin 19) must be configured as the input interfaces. OP1+ (Pin 3), OP1− (Pin 4), OP2+ (Pin 16), and OP2− (Pin 15) must be configured as the output interfaces. Figure 68 illustrates the basic connections for ADL5802 operation.

RF AND LO PORTS

The RF and LO input ports are designed for differential input impedance of approximately 50 Ω. Figure 69 and Figure 70 illustrate the RF and LO interfaces, respectively. It is recommended that each of the RF and LO differential ports be driven through a balun for optimum performance. It is also necessary to ac-couple both RF and LO ports with the proper size capacitors. Table 4 lists the recommended components for various RF frequency bands. The characterization data is available in the Typical Performance Characteristics section.

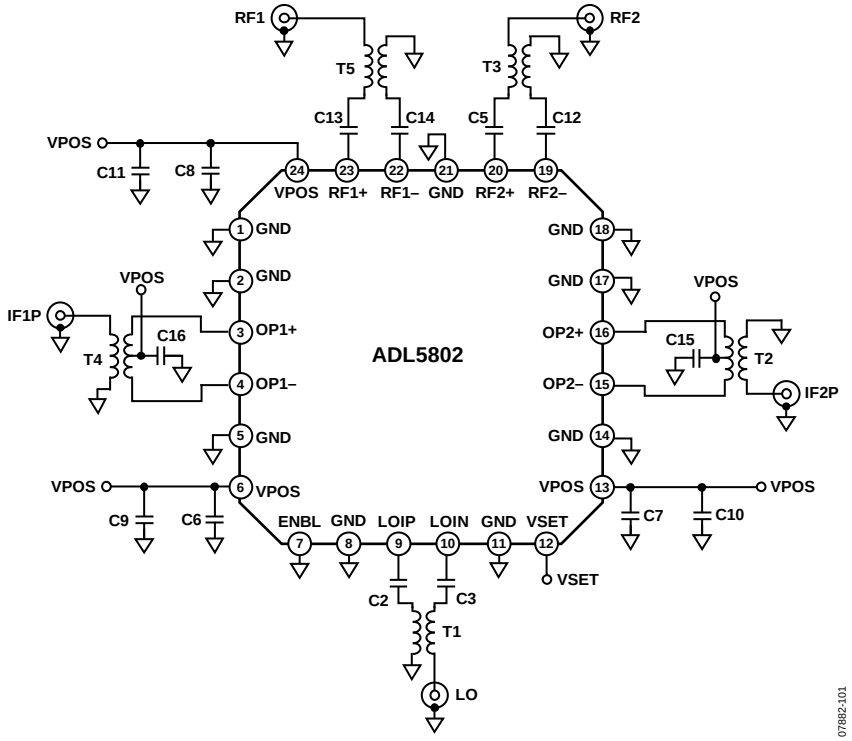


Figure 68. Basic Connections Schematic

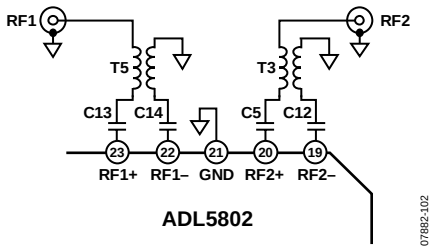


Figure 69. ADL5802 RF Interface

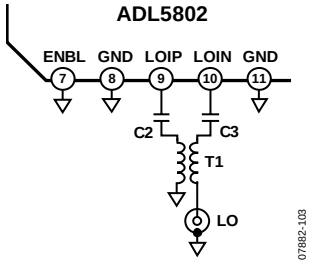


Figure 70. ADL5802 LO Interface

Table 4. Suggested Components for the RF and LO Interfaces

RF and LO Frequency	T1, T3, T5	C2, C3, C5, C12, C13, C14
900 MHz	Mini-Circuits® TC1-1-13M+	100 pF
1900 MHz	Mini-Circuits TC1-1-13M+	100 pF
2500 MHz	Johanson Technology 2500BL14M050	3 pF
3500 MHz	Johanson Technology 3600BL14M050	1.5 pF
5500 MHz	Johanson Technology 5400BL15B050	3 pF

IF PORT

The IF port features an open-collector differential output interface. It is necessary to bias the open collector outputs using one of the schemes presented in Figure 71 and Figure 72.

Figure 71 shows the use of center-tapped impedance transformers. The turns ratio of the transformer should be selected to provide the desired impedance transformation. In the case of a 50 Ω load impedance, a 4:1 impedance ratio transformer should be used to transform the 50 Ω load into a 200 Ω differential load at the IF output pins.

Figure 72 shows a differential IF interface where pull-up choke inductors are used to bias the open-collector outputs. The shunting impedance of the choke inductors used to couple dc current into the mixer core should be large enough at the IF frequency of operation so as not to load down the output current before it reaches the intended load. Additionally, the dc current handling capability of the selected choke inductors must be at least 45 mA. The self-resonant frequency of the selected choke inductors must be higher than the intended IF frequency. A variety of suitable choke inductors is commercially available from manufacturers such as Coilcraft and Murata. An impedance transforming network may be required to transform the final load impedance to 200Ω at the IF outputs.

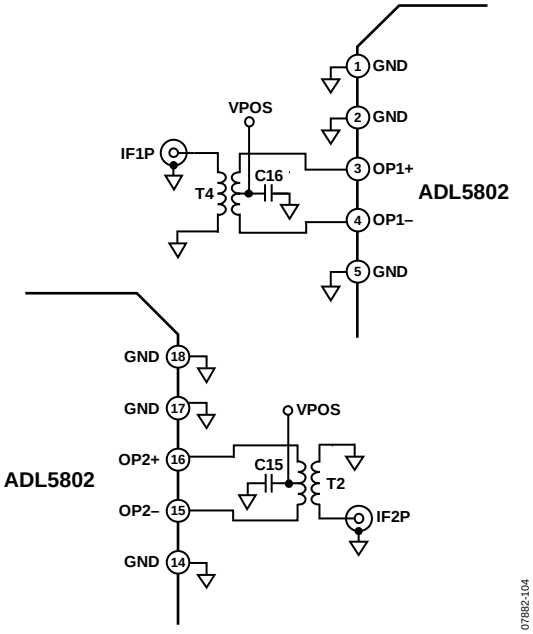


Figure 71. Biasing the IF Port Open-Collector Outputs Using a Center-Tapped Impedance Transformer

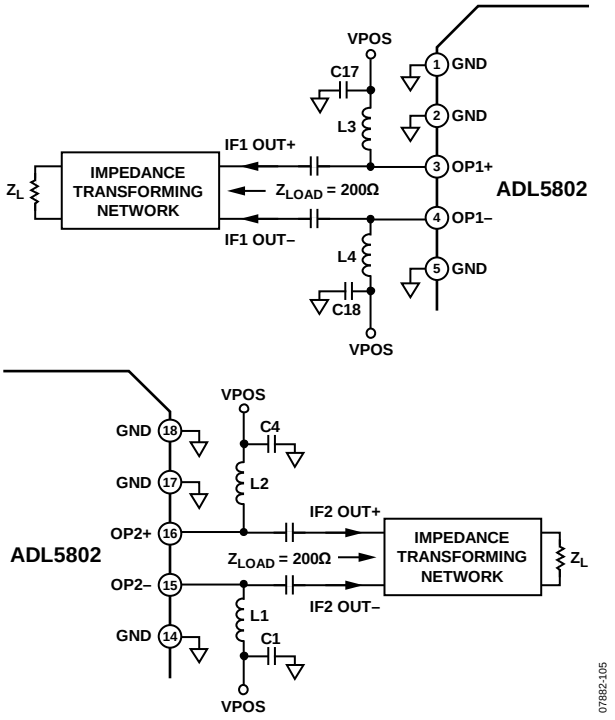


Figure 72. Biasing the IF Port Open-Collector Outputs Using Pull-Up Choke Inductors

EVALUATION BOARD

An evaluation board is available for the ADL5802. The standard evaluation board is fabricated using Rogers® RO3003 material. Each of the RF, LO, and IF ports is configured for single-ended signaling via a balun transformer. The schematic for the evaluation board is shown in Figure 73. Table 5 describes the various configuration options for the evaluation board. Layout for the board is shown in Figure 74 and Figure 75.

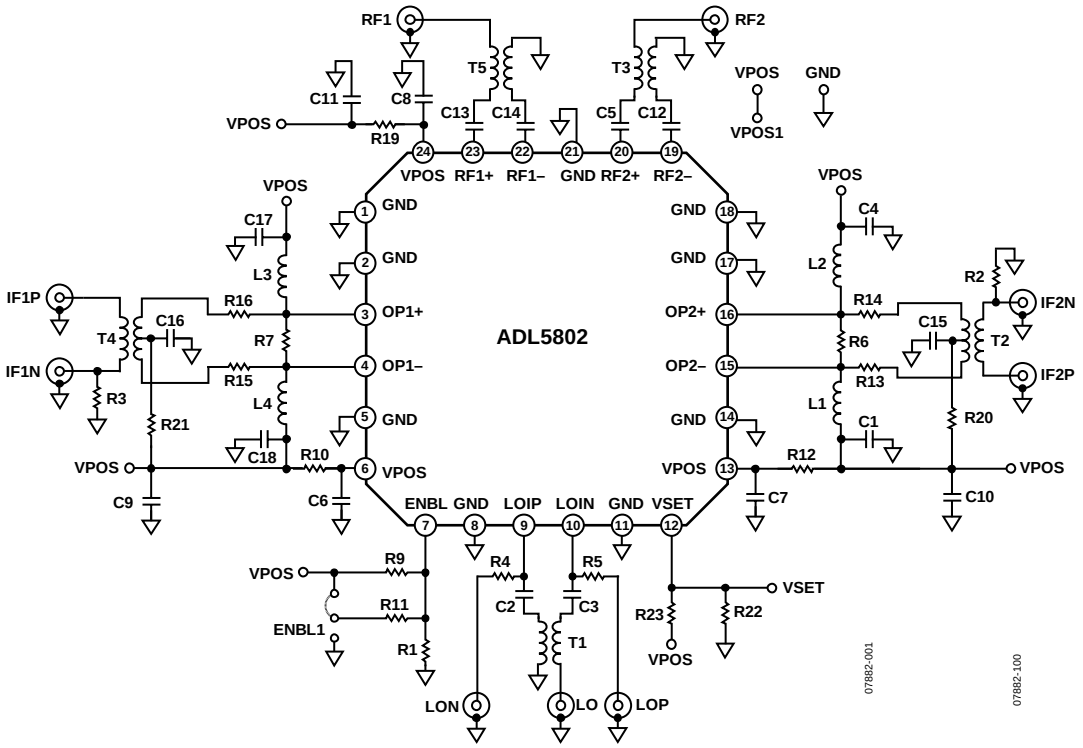


Figure 73. Evaluation Board Schematic

Table 5. Evaluation Board Configuration

Components	Function	Default Conditions
C1, C4, C6, C7, C8, C9, C10, C11, C17, C18, R10, R12, R19, R20, R21	Power supply decoupling. Nominal supply decoupling consists of a 0.01 µF capacitor to ground in parallel with 10 pF capacitors to ground, positioned as close to the device as possible. Series resistors are provided for enhanced supply decoupling using optional ferrite chip inductors.	C6, C7, C8 = 10 pF (size 0402) C9, C10, C11 = 0.01 µF (size 0402) C1, C4, C17, C18 = open (size 0402) R10, R12, R19, R20, R21 = 0 Ω (size 0402)
C5, C12, C13, C14, T3, T5, RF1, RF2	RF Channel 1 and RF Channel 2 input interfaces. Input channels are ac-coupled through C5, C12, C13, and C14. T3 and T4 are 1:1 baluns used to interface to the 50 Ω differential inputs.	C5, C12, C13, C14 = 100 pF (size 0402) T3, T5 = TC1-1-13M+ (Mini-Circuits)
C15, C16, L1, L2, L3, L4, R2, R3, R6, R7, R13, R14, R15, R16, R20, R21, T2, T4, IF1, IF2	IF Channel 1 and IF Channel 2 output interfaces. The 200 Ω open-collector IF output interfaces are biased through the center taps of T2 and T4 4:1 impedance transformers. C15 and C16 provide local bypassing with R20 and R21 available for additional supply bypassing. R6, R7, R13, R14, R15, and R16 are provided for IF filtering and matching options.	C15, C16 = 100 pF (size 0402) L1, L2, L3, L4 = open (size 0805) R2, R3, R13, R14, R15, R16, R20, R21 = 0 Ω (size 0402) R6, R7 = open (size 0402) T2, T4 = TC4-1W+ (Mini-Circuits)
C2, C3, R4, R5, T1, LO	LO interface. C2 and C3 provide ac coupling for the local oscillator input. T1 is a 1:1 balun to allow single-ended interfacing to the differential 50 Ω local oscillator input.	C2, C3 = 1 nF (size 0402) R4, R5 = open (size 0402) T1 = TC1-1-13M+ (Mini-Circuits)
R1, R9, R11, ENBL1	Enable interface. The ADL5802 can be disabled using the 3-pin ENBL1 header. The ENBL pin is pulled up to VPOS through R9. R1 is provided as an optional termination for the high impedance enable interface. If desired, the ENBL pin can be driven by an external source through the ENBL SMA connector.	R9 = 10 kΩ (size 0402); R1, R11 = open (size 0402) Or R1 = 10 kΩ (size 0402);R9, R11 = open (size 0402) Or R11 = 10 kΩ (size 0402); R1, R9 = open (size 0402) ENBL1 = 3-pin header and shunt

Components	Function	Default Conditions
R22, R23, VSET	VSET bias control. R22 and R23 form an optional resistor divider network between VPOS and GND, allowing for a fixed bias setting. See the Typical Performance Characteristics section to choose the recommended VSET control voltage for the desired frequency band.	R22, R23 = open (size 0402)
EPAD (EP)	Exposed paddle. Must be soldered to ground.	

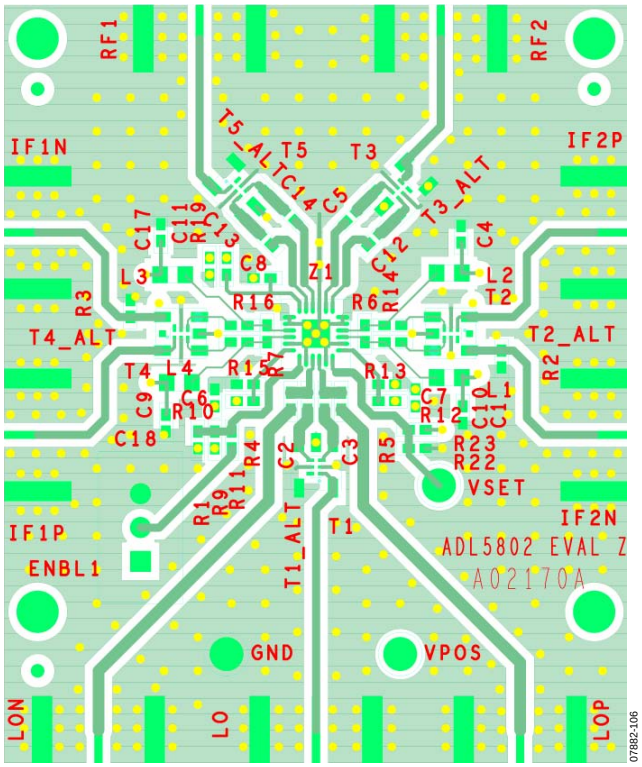


Figure 74. Evaluation Board Top Layer

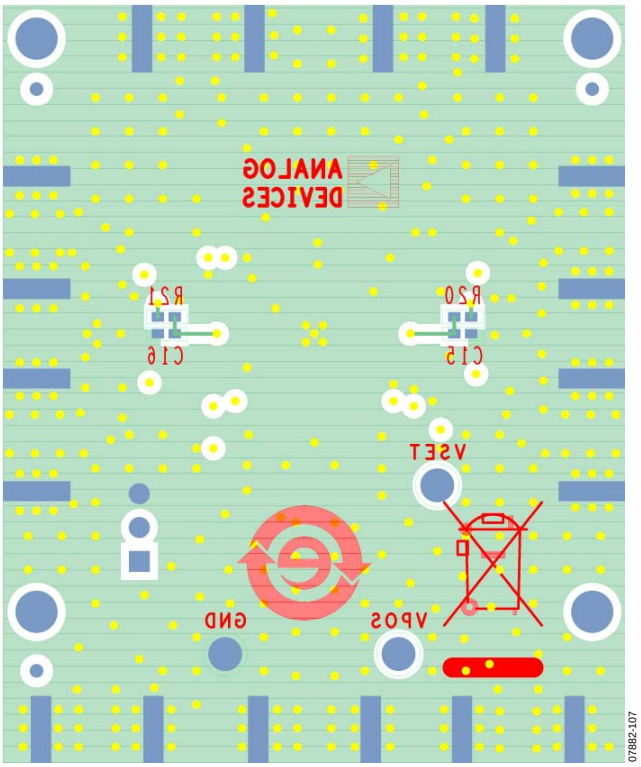


Figure 75. Evaluation Board Bottom Layer

OUTLINE DIMENSIONS

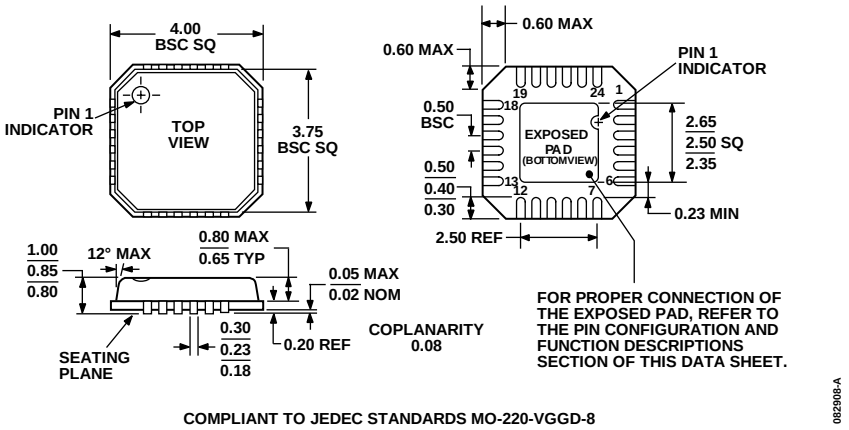


Figure 76. 24-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
4 mm × 4 mm Body, Very Thin Quad
(CP-24-3)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option	Ordering Quantity
ADL5802ACPZ-R7[1]	−40°C to +85°C	24-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-24-3	1,500 per Reel
ADL5802-EVALZ[1]		Evaluation Board		1

[1] Z = RoHS Compliant Part.

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