iC-GF

IO-Link TRANSCEIVER

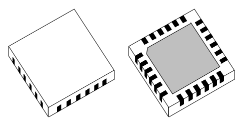
FEATURES

- IO-Link compliant slave transceiver
- Dual channel switches, configurable for high-side, low-side and push-pull operation with tristate function
- Configuration via pins or SPI interface
- Switches are current limited
- Switches, iC supply and feedback channel are protected against reverse polarity
- Output current of up to 150 mA per channel
- Parallel connection of both channels possible
- The channels can be inverted for antivalent output
- Sensor communication request function (IO-Link wake-up)
- Wide supply voltage range of 9 to 30 V
- Sensor parametrisation via a feedback channel (up to 30 V)
- Switching converters and linear regulators for 3.3/5 V voltage generation
- Error detection with hysteresis with excess temperature, overload and undervoltage
- Driver shut-down on all errors
- Error signalling at two open-collector outputs

APPLICATIONS

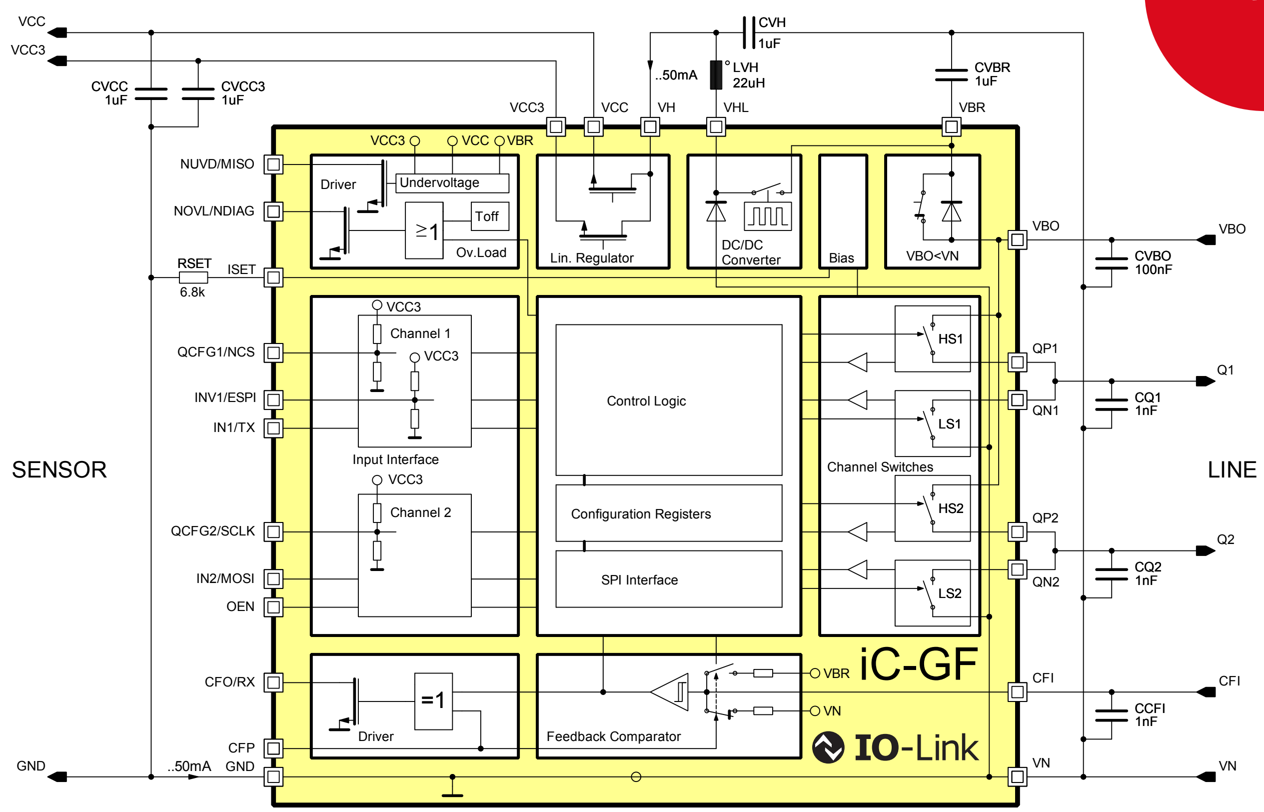
- IO-Link slaves
- I/O sensor interface
- Digital sensors
- Light barriers
- Proximity switches

PACKAGES



QFN24 4 mm x 4 mm

BLOCK DIAGRAM



Copyright © 2009 iC-Haus

DESCRIPTION

iC-GF is a fully IO-Link compliant transceiver iC with two independent switching channels which enables digital sensors to drive peripheral elements, such as programmable logic controllers (PLC) and relays, for example. All functions are controlled either by pins or via SPI interface, with extended functionality and configurability in SPI mode.

The output switches can be configured for push-pull, high-side or low-side operation and share a common tri-state function (separate tri-state switching in SPI mode). The switches are designed to cope with high driver currents of at least 100 mA (RSET = 6.8 kΩ), are current limited and also short-circuit-proof in that they shut down with excessive temperature or overload. The output current limit can be easily set with a resistor at pin ISET.

The protective overload feature is accomplished in a way so that capacitive loads can be switched with low repeat rates without the protective circuitry cutting in. In the event of excess temperature an error message is generated immediately.

Errors are signalled by two open-collector outputs: NOVL (for excess temperature and overloads) and NUVD (for low voltage at VBR or VCC resp. VCC3). The output switches are shut down with all types of errors.

To avoid error signalling during power-up, the output switches remain at high impedance for ca. 50 ms.

In SPI mode, the chip acts as an SPI slave and allows function configuration via register access. It also features a diagnostic register and supports *communication requests* (= IO-Link *wake-up*) at pin CFI, which generate interrupt signals at pin NDIAG.

The pins on the 24 V line side of the sensor interface (VBO, QP1, QN1, QP2, QN2, VN and CFI) are protected against reverse polarity. This makes any external reverse polarity protection diodes superfluous.

iC-GF features an integrated switching converter which generates voltages VCC (5 V) and VCC3 (3.3 V) with the aid of two downstream linear regulators. For *medium* currents the inductor may as well be replaced by a resistor (e.g. 170 Ω), resulting though in a considerably less efficiency. If only a low current is required inductor LVH may be omitted completely; the linear regulators are then powered directly by VBR.

The switching regulator comes equipped with a spread spectrum oscillator to reduce interferences.

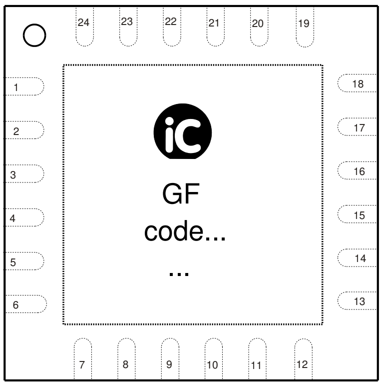
Input INV1 permits the input signal at channel 1 (IN1) to be inverted and if left unconnected, switches the chip into SPI mode.

The connected sensor can be parametrised using the feedback channel with a high voltage input (CFI → CFO).

CONTENTS

PACKAGES QFN24 4 mm x 4 mm to JEDEC Standard

PIN CONFIGURATION QFN24 4 mm x 4 mm



PIN FUNCTIONS

No.	Name	Function
1	ISET	Reference Current for current limitation of driver outputs
2	INV1	Inverting Input Channel 1
	ESPI	Enable SPI (pin open)
3	IN1	Input Channel 1
	TX	Transmission Input (SPI mode)
4	QCFG1	Configuration Input Channel 1
	NCS	Chip Select (SPI mode)

PIN FUNCTIONS

No.	Name	Function
5	QCFG2	Configuration Input Channel 2
	SCLK	Serial Clock (SPI mode)
6	IN2	Input Channel 2
	MOSI	Master Output Slave Input (SPI mode)
7	OEN	Output Enable Input
8	NOVL	Overload Error Output
	NDIAG	Diagnosis Output (SPI mode)
9	NUVD	Undervoltage Error Output
	MISO	Master Input Slave Output (SPI mode)
10	CFO	Feedback Channel Output
	RX	Transmission Output (SPI mode)
11	CFP	Configuration Input Feedback Channel
12	CFI	Feedback Channel Input
13	QP2	High Side Switch Output Channel 2
14	QN2	Low Side Switch Output Channel 2
15	VN	Ground
16	QN1	Low Side Switch Output Channel 1
17	QP1	High Side Switch Output Channel 1
18	VBO	Power Supply
19	VBR	Power Supply for switching converter
20	VHL	Inductor Switching Converter
21	VH	Input Linear Regulators
22	VCC	5 V Sensor Supply
23	VCC3	3.3 V Sensor Supply
24	GND	Sensor Ground

The *Thermal Pad* is to be connected to a Ground Plane (VN) on the PCB.
Only pin 1 marking on top or bottom defines the package orientation (iC-GF label and coding is subject to change).

ABSOLUTE MAXIMUM RATINGS

Beyond these values damage may occur; device operation is not guaranteed. Absolute Maximum Ratings are no operating conditions! Integrated circuits with system interfaces, e.g. via cable accessible pins (I/O pins, line drivers) are per principle endangered by injected interferences, which may compromise the function or durability. The robustness of the devices has to be verified by the user during system development with regards to applying standards and ensured where necessary by additional protective circuitry. By the manufacturer suggested protective circuitry is for information only and given without responsibility and has to be verified within the actual system with respect to actual interferences.

Item No.	Symbol	Parameter	Conditions	Min.	Max.	Unit
G001	VBO	Power Supply at VBO	Referenced to lowest voltage of VN, VBR, QP1, QN1, QP2, QN2, CFI, VH, VHL Referenced to highest voltage of VN, VBR, QP1, QN1, QP2, QN2, CFI, VH, VHL	 -36	36 	V V
G002	I(VBO)	Current in VBO		-10	600	mA
G003	VBR	Voltage at VBR	Referenced to lowest voltage of VN, VBO, QP1, QN1, QP2, QN2, CFI, VH, VHL Referenced to highest voltage of VN, VBO, QP1, QN1, QP2, QN2, CFI, VH, VHL	 -36	36 	V V
G004	I(VBR)	Current in VBR		-10	600	mA
G005	Cl(VBR)	Capacitive load at VBR			3.3	µF
G006	V(VH)	Voltage at VH	Referenced to lowest voltage of VN, VBR, VBO, QP1, QN1, QP2, QN2, CFI, VHL Referenced to highest voltage of VN, VBR, VBO, QP1, QN1, QP2, QN2, CFI, VHL	 -36	36 	V V
G007	I(VH)	Current in VH		-5	70	mA
G008	V(VHL)	Voltage at VHL	Referenced to lowest voltage of VN, VBR, VBO, QP1, QN1, QP2, QN2, CFI, VH Referenced to highest voltage of VN, VBR, VBO, QP1, QN1, QP2, QN2, CFI, VH	 -36	36 	V V
G009	I(VHL)	Current in VHL		-150	5	mA
G010	V(VN)	Voltage at GND vs. VN		-2	2	V
G011	I(VN)	Current in VN	VN < VBO VN > VBO	-500 -10	500 10	mA mA
G012	V()	Voltage at VCC, VCC3		-0.3	7	V
G013	I()	Current in VCC, VCC3		-50	10	mA
G014	V()	Voltage at QP1, QN1, QP2, QN2	Referenced to lowest voltage of VN, VBO, VBR, QP1, QN1, QP2, QN2, CFI, VH, VHL Referenced to highest voltage of VN, VBO, VBR, QP1, QN1, QP2, QN2, CFI, VH, VHL	 -36	36 	V V
G015	I()	Current in QP1, QP2		-400		mA
G016	I()	Current in QN1, QN2			400	mA
G017	V(CFI)	Voltage at CFI	Referenced to lowest voltage of VN, VBO, VBR, QP1, QN1, QP2, QN2, VH, VHL Referenced to highest voltage of VN, VBO, VBR, QP1, QN1, QP2, QN2, VH, VHL	 -36	36 	V V
G018	I(CFI)	Current in CFI		-4	4	mA
G019	V()	Voltage at INV1, QCFG1, QCFG2, IN1, IN2, OEN, CFP		-0.3	7	V
G020	I()	Current in INV1, QCFG1, QCFG2, IN1, IN2, OEN, CFP		-4	4	mA
G021	V()	Voltage at NOVL, NUVD, CFO		-0.3	7	V
G022	I()	Current in NOVL, NUVD, CFO		-5	20	mA
G023	V(ISET)	Voltage at ISET		-0.3	7	V
G024	I(ISET)	Current in ISET		-4	4	mA
G025	Vd()	ESD Susceptibility at all pins	HBM, 100 pF discharged through 1.5 kΩ		2	kV
G026	Tj	Junction Temperature		-40	150	°C
G027	Ts	Storage Temperature Range		-40	150	°C

All voltages are referenced to ground unless otherwise stated.
All currents into the device pins are positive; all currents out of the device pins are negative.

THERMAL DATA

Operating Conditions: VBO = 9...30 V (referenced to VN), Tj = -40...125 °C, RSET = 6.8 kΩ ±1%, unless otherwise stated

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
T01	Ta	Operating Ambient Temperature Range (extended range on request)		-40		85	°C
T02	Rthja	Thermal Resistance Chip/Ambient	Surface mounted, thermal pad soldered to ca. 2 cm² heat sink		30	40	K/W

All voltages are referenced to ground unless otherwise stated.
All currents into the device pins are positive; all currents out of the device pins are negative.

ELECTRICAL CHARACTERISTICS

Operating Conditions: VBO = 9...30 V (referenced to VN), Tj = -40...125 °C, RSET = 6.8 kΩ ±1%, unless otherwise stated

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Total Device							
001	VBO	Permissible Supply Voltage	Referenced to VN	9	24	30	V
002	I(VBO)	Supply Current in VBO	No load, VH conected to VBR, I(QP1) = I(QP2) = 0, QPx switched on			4.5	mA
003	Vs(VBR)	Saturation Voltage at VBR referenced to VBO	I(VBR) = 20mA I(VBR) = 50mA			0.8 1	V V
004	VH	Permissible Voltage at VH	VH > VHnr	8.4		30	V
005	I(VH)	Supply Current in VH	VH = 8 V, no load, I(VCC) = I(VCC3) = 0, V(OEN) = hi	1.5		3	mA
006	Vc()hi	Clamp Voltage hi at VBO, VBR vs. VN	I() = 10 mA	36			V
007	Vc()lo	Clamp Voltage lo at VBO, VBR vs. VN	I() = -10 mA			-36	V
008	Vc()hi	Clamp Voltage hi at QN1, QN2 vs. VN	I() = 1 mA, VBO > VN	36			V
009	Vc()lo	Clamp Voltage lo at QP1, QP2 vs. VBO	I() = -1 mA, VBO > VN			-36	V
010	Vc()hi	Clamp Voltage hi at VN, VBO, VBR, QP1, QN1, QP2, QN1, CFI, VH, VHL vs. lowest voltage of VN, VBO, VBR, QP1, QN1, QP2, QN1, CFI, VH, VHL	I() = 1 mA	36			V
011	Vc()hi	Clamp Voltage hi at VCC, VCC3, ISET, INV1, IN1, IN2, QCFG1, QCFG2, OEN, CFO, CFP, NOVL, NUVD	I() = 1 mA	7			V
012	Vc()lo	Clamp Voltage lo at VCC, VCC3, ISET, INV1, IN1, IN2, QCFG1, QCFG2, OEN, CFO, CFP, NOVL, NUVD	I() = -1 mA			-0.5	V
013	RGND	Resistance GND to VN			3	7	Ω
Low-Side Switch QN1, QN2							
101	Vs()lo	Saturation Voltage lo at QN1, QN2 vs. VN	RSET = 5.1 kΩ; I() = 100 mA I() = 50 mA I() = 10 mA			 1.2 0.65 0.3	 V V V
102	Isc()lo	Short-Circuit Current lo in QN1, QN2	RSET = 6.8 kΩ, V() = 3 V...VBO RSET = 5.1 kΩ, V() = 4 V...VBO	100 160	140 200	180 260	mA mA
103	Vol()on	Overload Detection Threshold on	QN1, QN2 lo → hi; referenced to GND	1.5		2.1	V
104	Vol()off	Overload Detection Threshold off	QN1, QN2 hi → lo; referenced to GND	1.5		1.8	V
105	Vol()hys	Overload Detection Threshold Hysteresis	Vol()hys = Vol()on − Vol()off	0.1			V
106	Ilk()	Leakage Current at QN1, QN2	OEN = lo; V(QN1, QN2) = VBO...VBO + 6 V V(QN1, QN2) = 0...VBO V(QN1, QN2) = -6...0 V V(QN1, QN2) = VBO − 36 V...-6 V	 0 0 -70 -200		 50 50 0 0	 µA µA µA µA
107	SR()	Slew Rate (switch off → on)	VBO = 30 V, Cl = 2.2 nF			45	V/µs
108	Imax()	Maximum Current in QN1, QN2	V(ISET) = 0 V, QNx > 3 V	170	300	440	mA
109	Ir()	Reverse Current in QN1, QN2	QNx activated; V(QNx) = -6 V	-300			µA
110	Iexc()	Excitation Current	NEXC = 0 (see Fig. 9)	300		540	mA
111	texc	Excitation Time	NEXC = 0 (see Fig. 9)	1.5		3.5	µs
112	tdead	Dead Time	Push-pull configuration, QNx activation delay after QPx deactivation (see Fig. 9)	1.2		2.8	µs

ELECTRICAL CHARACTERISTICS

Operating Conditions: VBO = 9...30 V (referenced to VN), Tj = -40...125 °C, RSET = 6.8 kΩ ±1%, unless otherwise stated

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
High-Side Switch QP1, QP2							
201	Vs()hi	Saturation Voltage hi vs. VBO	RSET = 5.1 kΩ; I() = -100 mA I() = -50 mA I() = -10 mA	 -1.4 -0.85 -0.35			 V V V
202	Isc()hi	Short-Circuit Current hi	RSET = 6.8 kΩ, V() = 0...VBO − 3 V RSET = 5.1 kΩ, V() = 0...VBO − 4 V	-230 -325	-150 -220	-100 -140	mA mA
203	Vol()on	Overload Detection Threshold on	QP1, QP2 hi → lo; referenced to VBO	-2.1		-1.5	V
204	Vol()off	Overload Detection Threshold off	QP1, QP2 lo → hi; referenced to VBO	-1.9		-1.4	V
205	Vol()hys	Overload Detection Threshold Hysteresis	Vol()hys = Vol()off − Vol()on	0.1			V
206	Ilk()	Leakage Current at QP1, QP2	OEN = lo; V(QP1, QP2) = -6...0 V V(QP1, QP2) = 0 V...VBO V(QP1, QP2) > VBO...VN + 30 V	 -100 -40 0		 0 0 100	 µA µA µA
207	SR()	Slew Rate (switch off → on)	VBO = 30 V, Cl = 2.2 nF			40	V/µs
208	Imax()	Maximum Current in QP1, QP2	V(ISET) = 0 V, VBO − QPx > 4 V	-520		-170	mA
209	Ir()	Reverse Current in QP1, QP2	QPx activated; V(QPx) = VBO...VBO + 6 V			1	mA
210	Iexc()	Excitation Current	NEXC = 0 (see Fig. 9)	-540		-300	mA
211	texc	Excitation Time	NEXC = 0 (see Fig. 9)	1.5		3.5	µs
212	tdead	Dead Time	Push-pull configuration, QPx activation delay after QNx deactivation (see Fig. 9)	1.2		2.8	µs
Short-Circuit/Overload Monitor							
301	toldly	Time to Overload Message (NOVL 1 → 0, outputs tri-state)	Permanent overload (see Fig. 6)	126	160	213	µs
302	tolcl	Time to Overload Message Reset (NOVL 0 → 1, outputs active)	No overload (see Fig. 6)	35	50	80	ms
303	tdscr	Time to Communication Request acknowledge	SPI mode, ENSCR = 1, QCFGx(1:0) = 01/10/11	70		90	µs
304	$tdnscr_{max}$	Maximum Time for no Communication Request acknowledge				40	µs
305	$tdnscr_{min}$	Minimum Time for no Communication Request acknowledge		151			µs
VBO Voltage Monitor							
401	VBOon	Turn-On Threshold VBO	Referenced to GND	8		9	V
402	VBOoff	Turn-Off Threshold VBO	Decreasing voltage VBO	7.3		8.5	V
403	VBOhys	Hysteresis	VBOhys = VBOon − VBOoff	200	500		mV
404	tuvdly	Time to Undervoltage Message (NUVD 1 → 0, switch tri-state)	Permanent undervoltage at VBR, VCC or VCC3	25		120	µs
405	tuvcl	Time to Undervoltage Message Reset (NUVD 0 → 1, switch active)	No undervoltage at VBR, VCC and VCC3 (see Fig. 6)	35	50	80	ms
Temperature Monitor							
501	Toff	Overtemperature Shutdown (NOVL 1 → 0, switch tri-state)	Increasing temperature Tj	130		165	°C
502	ton	Overtemperature Shutdown Reset Delay (NOVL 0 → 1, switch active)	Temperature Tj < Toff	35	50	80	ms
Inputs IN1/TX, IN2/MOSI, INV1/ENSPI, QCFG1/NCS, QCFG2/SCLK, OEN							
601	Vt()hi	Input Threshold Voltage hi at IN1/TX, IN2/MOSI, OEN, SCLK, NCS				2	V
602	Vt()lo	Input Threshold Voltage lo at IN1/TX, IN2/MOSI, OEN, SCLK, NCS		0.8			V

ELECTRICAL CHARACTERISTICS

Operating Conditions: VBO = 9...30 V (referenced to VN), Tj = -40...125 °C, RSET = 6.8 kΩ ±1%, unless otherwise stated

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
603	Vt()hys	Hysteresis at IN1/TX, IN2/MOSI, OEN, SCLK, NCS	Vt()hys = Vt()hi – Vt()lo	200	280		mV
604	Ipd()	Pull-Down Current at IN1/TX, IN2/MOSI	V() > 0.4 V	10		168	µA
605	Ipd()	Pull-Down Current at NCS, SCLK	SPI mode, V() > 0.4 V	10		40	µA
606	Ipd(OEN)	Pull-Down Current at OEN	V(OEN) > 0.4 V	1		6	µA
607	Vahi()	Input Threshold hi at QCFG1, QCFG2, INV1		52	64	69	%VCC3
608	Vahi()hys	Hysteresis hi at QCFG1, QCFG2, INV1		3		7	%VCC3
609	Valo()	Input Threshold lo at QCFG1, QCFG2, INV1		24	29	34	%VCC3
610	Valo()hys	Hysteresis lo at QCFG1, QCFG2, INV1		3		7	%VCC3
611	Voc()	Open Circuit Voltage at QCFG1, QCFG2, INV1		42	46.5	51	%VCC3
612	Ri()	Internal Resistance at QCFG1, QCFG2, INV1	Referenced to VCC3 Referenced to GND	40 40	85 85	190 190	kΩ kΩ
613	tsup()	Permissible Spurious Pulse Width at IN1/TX, IN2, INV1/ESPI	No activity triggered, DEFAULT mode or SPI mode with FCFG(1:0) = 10			2.5	µs
614	ttrig()	Required Pulse Width at IN1/TX, IN2, INV1/ESPI	Activity triggered, DEFAULT mode or SPI mode with FCFG(1:0) = 10	6			µs
615	tsup()	Permissible Spurious Pulse Width at QCFG1, QCFG2, OEN	No activity triggered, DEFAULT mode or SPI mode with FCFG(1:0) = 10			5	µs
616	ttrig()	Required Pulse Width at QCFG1, QCFG2, OEN	Activity triggered, DEFAULT mode or SPI mode with FCFG(1:0) = 10	12			µs
617	tpio	Propagation Delay IN1 → QP1, QN1 IN2 → QP2, QN2	INV1 = low or high, DEFAULT mode or SPI mode with FCFG(1:0) = 10	2.4		10	µs
Error Output NOVL/NDIAG, NUVD/MISO							
701	Vs()lo	Saturation Voltage lo at NOVL, NUVD	DEFAULT mode, I() = 1.0 mA			0.4	V
702	Vs()lo	Saturation Voltage lo at NDIAG	SPI mode, I() = 1.0 mA			0.4	V
703	Isc()lo	Short Circuit Current lo in NOVL, NUVD	DEFAULT mode, V() = 0.4 V...VCC	1.2		25	mA
704	Isc()lo	Short Circuit Current lo in NDIAG	SPI mode, V() = 0.4 V...VCC	1.2		25	mA
705	Ilk()	Leakage Current in NOVL, NUVD	DEFAULT mode, V() = 0 V...VCC, no error	-10		10	µA
706	Ilk()	Leakage Current in NDIAG	SPI mode, V() = 0 V...VCC, no error	-10		10	µA
707	Vs()hi	Saturation Voltage high at MISO	SPI mode, I(MISO) = -2 mA, Vs(MISO)hi = VCC3 – V(MISO)			0.4	V
708	Vs()lo	Saturation Voltage low at MISO	SPI mode, I(MISO) = 2 mA			0.4	V
709	Isc()hi	Short Circuit current hi in MISO	SPI mode, V(MISO) = 0...VCC3 – 0.4 V	-40			mA
710	Isc()lo	Short Circuit current lo in MISO	SPI mode, V(MISO) = 0.4 V...VCC3			90	mA
711	tr(MISO)	Rise Time	SPI mode, Cl(MISO) = 30 pF, 0 → 90%VCC3			22	ns
712	tf(MISO)	Fall Time	SPI mode, 100 → 10%VCC3			16	ns
Feedback Channel CFI to CFO/RX							
801	Vt1(CFI)hi	Input Threshold 1 hi at CFI	VBR < 18 V	59	66	74	%VBR
802	Vt1(CFI)lo	Input Threshold 1 lo at CFI	VBR < 18 V	44	50	56	%VBR
803	Vt2(CFI)hi	Input Threshold 2 hi at CFI	VBR > 18 V	10.5	11.3	12	V
804	Vt2(CFI)lo	Input Threshold 2 lo at CFI	VBR > 18 V	8.3	9	10.5	V
805	Vt()hys	Hysteresis at CFI	Vt(CFI)hys = Vt(CFI)hi – Vt(CFI)lo	1			V
806	Ipu(CFI)	Pull-Up Current at CFI	DEFAULT mode: CFP = hi, V(CFI) = 0...VBR – 3 V SPI mode: POL = 1, ENPUD = 1	-300		-40	µA

ELECTRICAL CHARACTERISTICS

Operating Conditions: VBO = 9...30 V (referenced to VN), Tj = -40...125 °C, RSET = 6.8 kΩ ±1%, unless otherwise stated

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
807	Ipd(CFI)	Pull-Down Current at CFI	DEFAULT mode: CFP = lo, V(CFI) = 3 V...VBR SPI mode: POL = 0, ENPUD = 1	40		300	µA
808	tpcf	Propagation Delay CFI → CFO/RX	V(CFO/RX) = 10 ↔ 90%	2.4		10	µs
809	Vs()lo	Saturation Voltage lo at CFO/RX	Open collector mode, I(CFO/RX) = 1.0 mA			0.4	V
810	Isc()lo	Short Circuit Current lo in CFO/RX	Open collector mode, V(CFO/RX) = 0.4 V...VCC	1.2		25	mA
811	Ilk()	Leakage Current at CFO/RX	Open collector mode, V(CFO/RX) = 0 V...VCC, CFO/RX = off	-10		10	µA
812	Vt(CFP)hi	Input Threshold Voltage hi at CFP				2	V
813	Vt(CFP)lo	Input Threshold Voltage lo at CFP		0.8			V
814	Vt(CFP)hys	Hysteresis at CFP	Vt(CFP)hys = Vt(CFP)hi – Vt(CFP)lo	200	280		mV
815	Ipd(CFP)	Pull-Down Current at CFP	V(CFP) = 0.4 V...Vt(CFP)lo V(CFP) > Vt(CFP)hi	30 10		168 40	µA µA
816	tsup(CFI)	Permissible Spurious Pulse Width at CFI	No activity triggered, DEFAULT mode or SPI mode with FCFI(1:0) = 01			2.5	µs
817	ttrig(CFI)	Required Pulse Width at CFI	Activity triggered, DEFAULT mode or SPI mode with FCFI(1:0) = 01	6			µs
818	tsup(CFP)	Permissible Spurious Pulse Width at CFP	No activity triggered			5	µs
819	ttrig(CFP)	Required Pulse Width at CFP	Activity triggered	12			µs
820	Ipd(CFI)+ Ilk(QPx)	Pull-Down Current at CFI plus leakage current at QPx	V(CFI) = 3 V...VBR, OEN = lo; DEFAULT mode: CFP = lo SPI mode: POL = 0, ENPUD = 1	20			µA
821	Vs(RX)hi	Saturation Voltage high at RX	SPI mode, ENOD = 0, I(RX) = -2 mA, Vs(RX)hi = VCC3 – V(RX)			0.4	V
822	Vs(RX)lo	Saturation Voltage low at RX	SPI mode, ENOD = 0, I(RX) = 2 mA			0.4	V
823	Isc(RX)hi	Short Circuit current hi in RX	SPI mode, ENOD = 0, V(RX) = 0...VCC3 – 0.4 V	-40			mA
824	Isc(RX)lo	Short Circuit current lo in RX	SPI mode, ENOD = 0, V(RX) = 0.4 V...VCC3			90	mA
825	tr(RX)	Rise Time at RX	SPI mode, ENOD = 0, CL(RX) = 30 pF, 0 → 90%VCC3			22	ns
826	tf(RX)	Fall Time at RX	SPI mode, ENOD = 0, CL(RX) = 30 pF, 100 → 10%VCC3			22	ns
Step Down Converter VHL, VH							
901	VHn	Nominal Voltage at VH	LVH = 22 µH, Ri(LVH) < 1.1 Ω, CVH = 1 µF, I(VH) = 0...50 mA	6.3	6.7	7.4	V
902	VHnr	Nominal Voltage at VH, LVH replaced by a resistor	R = 170 Ω, I(VH) = 0...10 mA	6.3		8.4	V
903	Ia(VHL)	max. DC Cut-Off Current in VHL		-200			mA
904	Va(VH)	Cut-Off Voltage at VH	Va(VH) > VHn	6.5	7.3	8.4	V
906	Vs(VHL)	Saturation Voltage at VHL vs. VBR	I(VHL) = -50 mA I(VHL) = -150 mA		0.5 1.5	1.1 3.0	V V
907	Vf(VHL)	Saturation Voltage at VHL vs. GND	Vf(VHL) = V(GND) – V(VHL); I(VHL) = -50 mA I(VHL) = -150 mA		 0.6 1.7	 1.5 2.9	 V V
908	Ilk(VHL)	Leakage Current at VHL	VHL = lo, V(VHL) = V(VH)	-20		20	µA
909	ηVH	Efficiency of VH switching regulator	I(VH) = 50 mA, Ri(LVH) < 1.1 Ω, V(VBR) = 12...30 V	70			%

ELECTRICAL CHARACTERISTICS

Operating Conditions: VBO = 9...30 V (referenced to VN), Tj = -40...125 °C, RSET = 6.8 kΩ ±1%, unless otherwise stated

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Series Regulator VCC							
A01	VCCn	Nominal Voltage at VCC	I(VCC) = -50...0 mA, VH = VHn	4.75	5	5.25	V
A02	CVCC	Required Capacitor at VCC vs. GND		150			nF
A03	RiCVCC	Maximum Permissible Internal Resisitance of capacitor at VCC				1	Ω
A04	VCCon	VCC Monitor Threshold hi		89		98	%VCCn
A05	VCCoff	VCC Monitor Threshold lo	Decreasing Voltage at VCC	80		90	%VCCn
A06	VCChys	Hysteresis	VCChys = VCCon – VCCoff	50	500		mV
Series Regulator VCC3							
B01	VCC3n	Nominal Voltage at VCC3	I(VCC3) = -50...0 mA, VH = VHn	3.1	3.3	3.5	V
B02	CVCC3	Required Capacitor at VCC3 vs. GND		150			nF
B03	RiCVCC3	Maximum Permissible Internal Resisitance of capacitor at VCC3				1	Ω
B04	VCC3on	VCC3 Monitor Threshold hi		89		98	% VCC3n
B05	VCC3off	VCC3 Monitor Threshold lo	Decreasing Voltage at VCC3	80		90	% VCC3n
B06	VCC3hys	Hysteresis	VCC3hys = VCC3on – VCC3off	50	200		mV
Oscillator							
C01	fos_{SS}	Spread Spectrum Oscillator Frequency	Average value from 64 clock cycles	0.88		1.5	MHz
C02	Tos_{SS}	Single Clock Cycle Periode (spread spectrum oscillator)		0.571		1.35	µs
C03	fos	Fixed Oscillator Frequency	 Tj = 27 °C	1.5 1.53		2.5 2.43	MHz MHz
Reference and Bias							
D01	V(ISET)	Voltage at ISET	Tj = 27 °C	1.12	1.24	1.29	V
D02	Isc(ISET)	Short Circuit Current in ISET	V(ISET) = 0 V, Tj = 27 °C	-0.55	-0.4	-0.28	mA
D03	rIbeg	Transmission Ratio for driver output current limitation	Imax(QP1) = Imax(QP2) = Imax(QN1) = Imax(QN2) = I(ISET) ∗ rIbeg, RSET = 5.1...20 kΩ		800		

OPERATING REQUIREMENTS: SPI Interface

Operating Conditions: VBO = 9...30 V (referenced to VN), Tj = -40...125 °C

Item No.	Symbol	Parameter	Conditions	Min.	Max.	Unit
I001	tsCCL	Setup Time: NCS hi → lo before SCLK lo → hi		15		ns
I002	tsDCL	Setup Time: MOSI stable before SCLK lo → hi		20		ns
I003	thDCL	Hold Time: MOSI stable after SCLK lo → hi		0		ns
I004	tCLh	Signal Duration SCLK hi		30		ns
I005	tCLl	Signal Duration SCLK lo		30		ns
I006	thCLC	Hold Time: NCS lo after SCLK lo → hi		0		ns
I007	tCSh	Signal Duration NCS hi		0		ns
I008	tpCLD	Propagation Delay: MISO stable after SCLK hi → lo		0	90	ns
I009	tpCSD	Propagation Delay: MISO high impedance after NCS lo → hi		0	25	ns
I010	f(SPI)	SPI Frequency			5	MHz

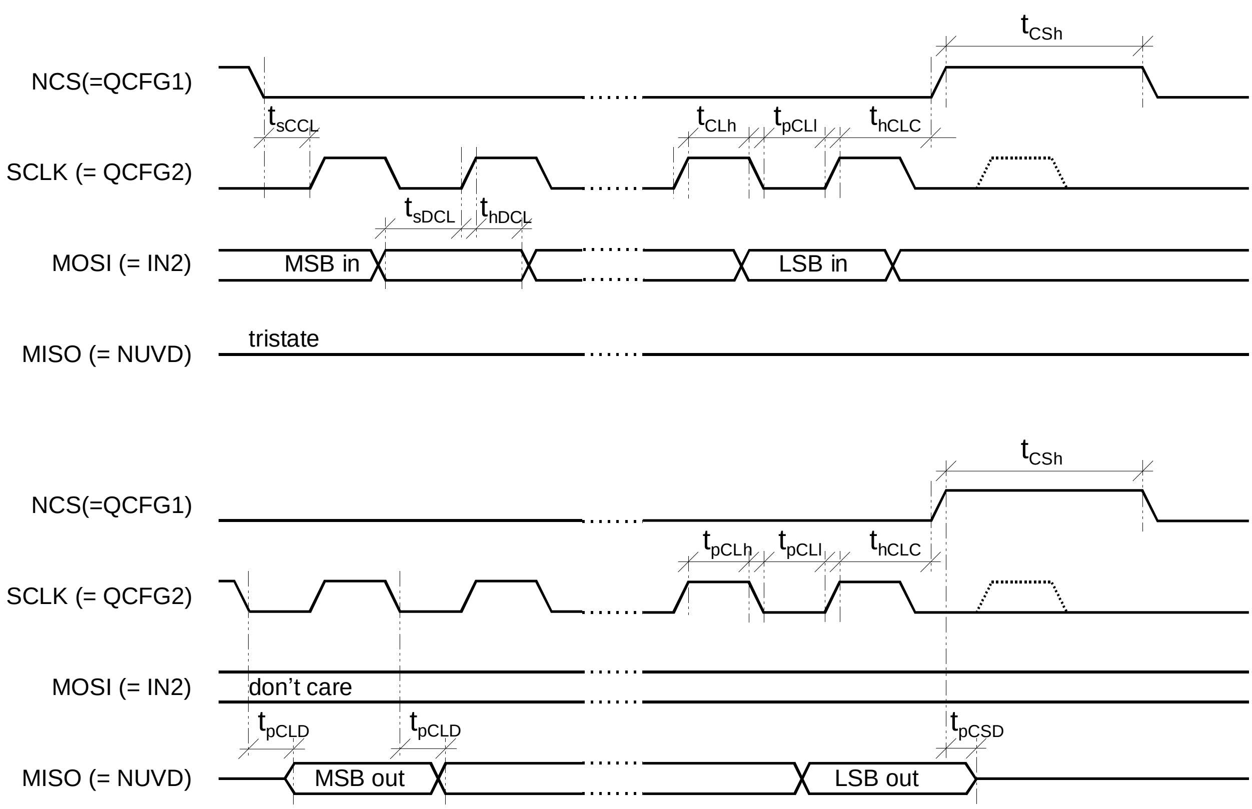


Figure 1: SPI write cycle (top) and read cycle (bottom)

DESCRIPTION OF FUNCTIONS

iC-GF has two independent switching channels which enables digital sensors to drive peripheral elements. They are designed to cope with high driver currents. The switches are reverse-polarity protected, feature a free-wheeling circuit for inductive loads and a saturation voltage minimising system.

Reverse polarity protection
The pins VBO, QPx, QNx, VN and CFI on the *line side* of the chip are reverse polarity protected. As far as the maximum voltage ratings are not exceeded, no possible supply combination at the *line side* pins can damage the chip.

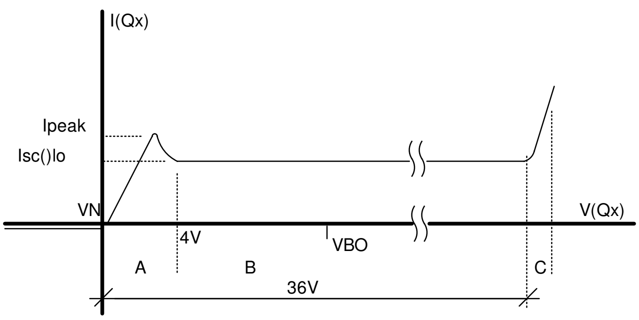


Figure 2: QNx characteristic when active

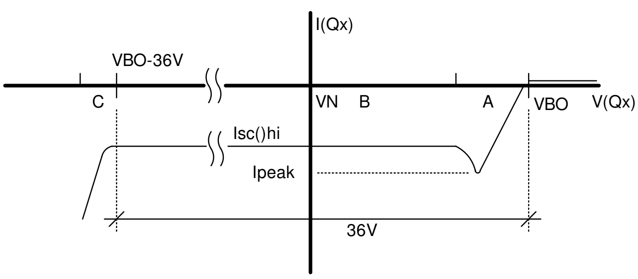


Figure 3: QPx characteristic when active

Output characteristics of Q1, Q2
The switching channels are current limited to a value set by the external resistor RSET (cf. Electrical Characteristics No. D03). If pin ISET is short circuited to GND, the current limitation will be set to a maximum value (cf. Electrical Characteristics Nos. 108, 208). The current limitation works only for voltages higher than 4 V at QNx resp. lower than VBO − 4 V at QPx. For smaller output voltages the current limitation is reduced in order to minimise the saturation voltages without increasing the power dissipation. Figures 2 and 3 show the characteristic of the switching channels when activated. Region "A" is the saturation range, where the current limitation is not fully active yet and region "B" is the current limited range. Region "C" corresponds to the free-wheeling circuit activated. The switching channels are designed so that QNx can only sink current and QPx can only source current (no reverse current).

Free-wheeling circuit for inductive loads
The free-wheeling circuit is always present and does not depend on the current output status. It is activated by voltages higher than 36 V at QNx referenced to VN or lower than -36 V at QPx referenced to VBO. In that case the correspondent channel will switch on without current limitation (see Figure 4).

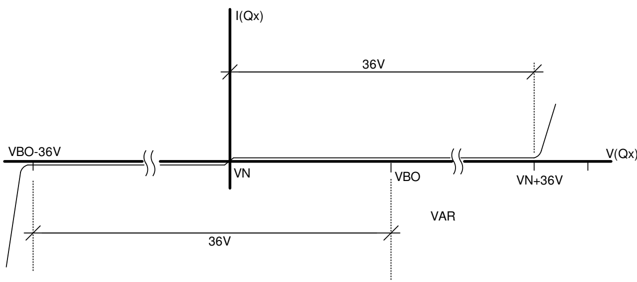


Figure 4: Free-wheeling characteristic

Dead time
In order to avoid current flow between high- and low-side switch in push-pull configuration, a dead time t_{dead} is implemented as shown in Figure 5 (cf. Electrical Characteristics Nos. 112 and 212).

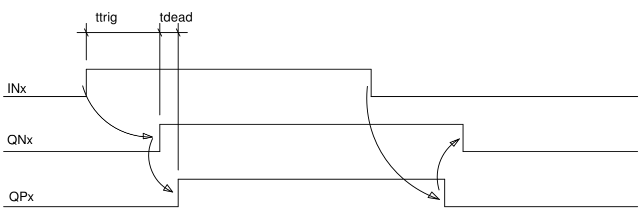


Figure 5: Propagation delay

Overload detection
To protect the device against excessive power dissipation due to high currents the switches are clocked if an overload occurs. If a short circuit is detected, i.e. if the voltage at the switch output overshoots or undershoots *Overload Detection Threshold off* (cf. Electrical Characteristics Nos. 104 and 204), the switches are shut down for a typical 50 ms (cf. Electrical Characteristics No. 302) and the current flow thus interrupted.

The level of power dissipation depends on the current and the time during which this current flows. A current which fails to trigger the overload detection is not critical; high current can also be tolerated for a short period and with low repeat rates. This is particularly important when switching capacitive loads (charge/discharge currents).

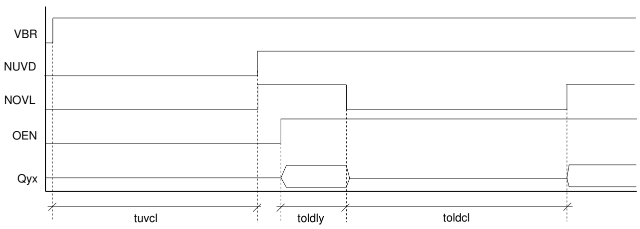


Figure 6: Permanent short circuit

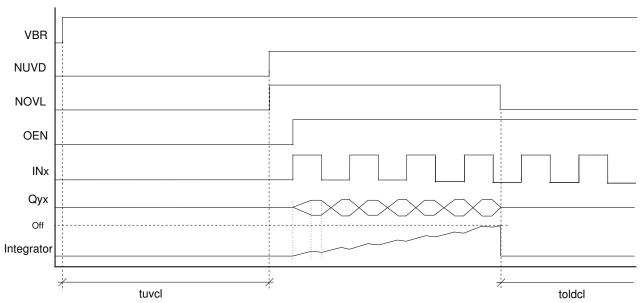


Figure 7: Overload

So that this is possible a shared back-end integrator follows the switches for the purpose of overload detection. This integrator is an 8-bit counter which is updated together with the oscillator clock. If an overload is detected on one channel the counter is incremented by 1; an overload on both channels increments the counter by 2. If no overload is apparent the counter is decremented by 1 every 10 clock pulses. A maximum duty cycle – without deactivation of the switches – of 1:10 results if one channel is overloaded. Only when this ratio is exceeded the counter can reach its maximum value, generating an error message at NOVL and deactivating the switches.

Undervoltage detection
iC-GF features two separate undervoltage detectors: voltage monitoring at VBO and voltage monitoring at VCC and VCC3. Both undervoltage detectors are filtered against spurious events smaller than 25 µs (cf. Electrical Characteristics No. 404). In case of a valid undervoltage event (longer than 25 µs) both QPx and QNx are unconditionally brought to high impedance for at least 35 ms (cf. Electrical Characteristics No. 405) resp. as long as the duration of the undervoltage situation.

Digital filtering at inputs
To obtain high noise immunity the pins QCFGx, INV1/ESPI, IN1/TX, IN2, OEN, CFI and CFP have a digital input filter. Figure 5 shows this filter time t_{trig} for INx (cf. Electrical Characteristics Nos. 613 to 616 and 816 to 819).

Feedback channel CFI–CFO
iC-GF implements a feedback channel which permits a communication from the *line side* to the *sensor side*. *High voltage* digital signals at CFI are converted into low voltage (open-collector) levels at CFO.

Spread spectrum oscillator
To reduce the electromagnetic interference generated by the switching converter (pin VHL) a *spread spectrum oscillator* has been introduced. Here the switch is not triggered by a fixed frequency but by a varying 32 step frequency mix. Generated interference is then distributed across the frequency spectrum with its amplitude reduced at the same time.

Configuration mode
Leaving pin INV1 unconnected (cf. Table 1) selects SPI mode for configuration. All functions implemented in DEFAULT mode are also available in SPI mode plus some additional functions, available in SPI mode only.

Mode Select	
INV1	MODE
L	DEFAULT
H	DEFAULT
Z	SPI

Table 1: Operating mode configuration

DEFAULT MODE

Enabling the switches

Setting pin OEN to low unconditionally disables all four output switches. Other functions of the chip (like the DC/DC converter or the feedback channel) remain enabled.

Configuring the switches

The functionality of the switches is determined by the pins QCFG1 and QCFG2. A voltage at QCFGx which is lower than Va()lo (cf. Figure 8) deactivates the relevant high-side switches; with a voltage higher than Va()hi the relevant low-side switches are deactivated. Both high-side and low-side switches are activated, when the pin is left open.

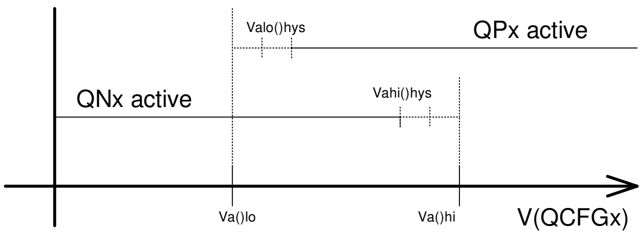


Figure 8: Levels at QCFG1/QCFG2 for switch configuration

CHANNEL 1					
IN1	QCFG1	INV1	OEN	QN1	QP1
X	X	X	L	off	off
L	Z	L	H	on	off
H	Z	L	H	off	on
L	Z	H	H	off	on
H	Z	H	H	on	off
L	H	L	H	off	off
H	H	L	H	off	on
L	H	H	H	off	on
H	H	H	H	off	off
L	L	L	H	off	off
H	L	L	H	on	off
L	L	H	H	on	off
H	L	H	H	off	off

Table 2: Function table Channel 1

CHANNEL 2				
IN2	QCFG2	OEN	QN2	QP2
X	X	L	off	off
L	Z	H	on	off
H	Z	H	off	on
L	H	H	off	off
H	H	H	off	on
L	L	H	off	off
H	L	H	on	off

Table 3: Function table Channel 2 (INV1 = H, L)

Tables 2 and 3 show the switch configuration for both channels, with respect to the input pins.

Feedback channel CFI–CFO configuration

The feedback channel CFI–CFO polarity can be configured via pin CFP (see table 4). This pin also sets the pull-up/down current at pin CFI.

FEEDBACK CHANNEL			
CFI	CFP	CFO	PULL at CFI pin
H	H	Z	UP
H	L	L	DOWN
L	H	L	UP
L	L	Z	DOWN

Table 4: Function table Feedback Channel

Undervoltage signalling

Undervoltage at VBO, VCC or VCC3 is signalled at pin NUVD. A valid undervoltage event is signalled at NUVD for at least 35 ms (cf. Electrical Characteristics No. 405) resp. as long as the duration of the undervoltage situation.

SPI MODE

In SPI mode the iC-GF is configured and operated using the on-chip registers. Additionally there is a status register, where chip events are logged. If any of the status bits is set to high, the low-active open-drain pin NDIAG is activated, e.g. for interrupt generation for micro controllers. The SPI mode is activated when the pin INV1 is left open and the filter time (cf. Electrical Characteristic No. 614) has elapsed. This enables communication with the iC-GF via an SPI protocol using pins MISO, MOSI, SCLK and NCS.

Switch enable

There are three different ways of enabling/disabling the output switches in SPI mode: *pin mode*, *register mode* and *mixed mode*. In *pin mode* (TXEN = "11") or *register mode* (TXEN = "00") the OEN pin acts as a common enable for both switching channels. The OEN register on the other hand enables or disables each switch separately.

Switch enable				
OEN pin	TXEN(1:0)	OEN(1:0)	Qx2	Qx1
0	00/11	XX	disabled	disabled
1	00/11	01	disabled	enabled
1	00/11	10	enabled	disabled
1	XX	11	enabled	enabled
X	XX	00	disabled	disabled
0	01	0X	disabled	disabled
0	01	1X	enabled	disabled
0	10	X0	disabled	disabled
0	10	X1	disabled	enabled
1	01	01	disabled	enabled
1	01	10	enabled	disabled
1	10	01	disabled	enabled
1	10	10	enabled	disabled

Table 5: Switch enable, QCFGx ≠ "00"

In *mixed mode* (TXEN = "01" or "10") the OEN pin acts as an enable only for the channel for which the TXEN bit is set to "1". The OEN register enables or disables each switching channel separately. Table 5 summarises these configurations.

Switch control

Each switch can be operated by the OUTD register or the input pin TX. The register TXEN selects register OUTD or the pin TX for switch control.

A "0" in the register TXEN sets the corresponding switch to be controlled by the relevant bit of the register OUTD.

TXEN(1:0)	Adr 0x00; Bit (5:4) R/W 01
x0	Channel 1 controlled by OUTD(0)
x1	Channel 1 controlled by TX
0x	Channel 2 controlled by OUTD(1)
1x	Channel 2 controlled by TX

Table 6: Transmit enable

OUTD(1:0)	Adr 0x00; Bit (1:0) R/W 00
x0	Channel 1: push-pull low resp. high/low-side off
x1	Channel 1: push-pull high resp. high/low-side on
0x	Channel 2: push-pull low resp. high/low-side off
1x	Channel 2: push-pull high resp. high/low-side on

Table 7: Output data with INV = "00"

Switch configuration

The configuration of the switches is determined by the registers QCFG1 and QCFG2; either as high-side, low-side, push-pull or high impedance (disabled).

QCFG1(1:0)	Adr 0x01; Bit (5:4) R/W 11
00	disabled
01	low-side switch
10	high-side switch
11	push-pull

Table 8: Switch configuration Channel 1

QCFG2(1:0)	Adr 0x01; Bit (7:6) R/W 11
00	disabled
01	low-side switch
10	high-side switch
11	push-pull

Table 9: Switch configuration Channel 2

INV inverts the corresponding switching channel.

INV(1:0)	Adr 0x03; Bit (5:4) R/W 00
x0	Switching channel 1 not inverted
x1	Switching channel 1 inverted
0x	Switching channel 2 not inverted
1x	Switching channel 2 inverted

Table 10: Invert Ouput

Table 11 summarises the above configurations for channel 1.

CHANNEL 1						
TXEN(0)	QCFG1(1:0)	TX	OUTD(0)	INV(0)	QN1	QP1
0	01	x	0	0	off	off
0	01	x	0	1	on	off
0	01	x	1	0	on	off
0	01	x	1	1	off	off
0	10	x	0	0	off	off
0	10	x	0	1	off	on
0	10	x	1	0	off	on
0	10	x	1	1	off	off
0	11	x	0	0	on	off
0	11	x	0	1	off	on
0	11	x	1	0	off	on
0	11	x	1	1	on	off
1	01	L	x	0	off	off
1	01	L	x	1	on	off
1	01	H	x	0	on	off
1	01	H	x	1	off	off
1	10	L	x	0	off	off
1	10	L	x	1	off	on
1	10	H	x	0	off	on
1	10	H	x	1	off	off
1	11	L	x	0	on	off
1	11	L	x	1	off	on
1	11	H	x	0	off	on
1	11	H	x	1	on	off

Table 11: Function table for channel 1 in SPI mode

FCFI(1:0)	Adr 0x02; Bit (1:0)	R/W 01
00	Filter disabled	
01	4 µs filtering (8 CLKs)	
10	7 µs filtering (14 CLKs)	
11	16 µs filtering (32 CLKs)	

Table 12: CFI filter configuration

FCFG(1:0)	Adr 0x02; Bit (3:2)	R/W 10
00	Filter disabled	
01	TX: 1.5 µs filtering (3 CLKs) OEN: 3 µs filtering (6 CLKs)	
10	TX: 4 µs filtering (8 CLKs) OEN: 8 µs filtering (16 CLKs)	
11	TX: 7.5 µs filtering (15 CLKs) OEN: 15 µs filtering (30 CLKs)	

Table 13: TX and OEN filter configuration

Digital filtering at inputs
The digital input filters can be configured with the register FCFG for pins TX and OEN and register FCFI for pin CFI. Figure 9 shows the filter time t_{trig} for TX (cf. Electrical Characteristics Nos. 613 to 616 and 816 to 819).

Excitation current
Using register NEXC an additional current I_{exc} can be activated for driving capacitive loads. Figure 9 shows the characteristic of one channel with the excitation current enabled (cf. Electrical Characteristics Nos. 110, 111, 210 and 211).

NEXC(1:0)	Adr 0x03; Bit (1:0)	R/W 11
x0	Excitation for channel 1 enabled	
x1	Excitation for channel 1 disabled	
0x	Excitation for channel 2 enabled	
1x	Excitation for channel 2 disabled	

Table 14: Excitation current configuration

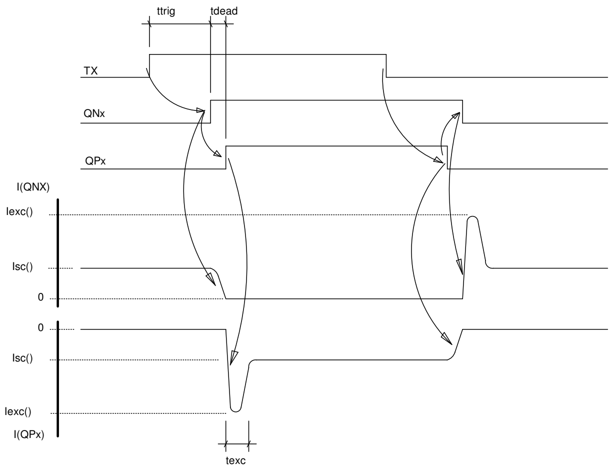


Figure 9: Dynamic characteristic

Feedback channel CFI–RX configuration
In SPI mode RX is a standard CMOS output, which can also be configured as an open-drain output, using the register bit ENOD (cf. Table 15).

ENOD	Adr 0x01; Bit (0) R/W 1
0	Push-pull output
1	Open-drain output

Table 15: RX configuration

The polarity of the feedback channel CFI–RX can be configured using register bit POL (cf. Table 16). Pin CFP has no function in SPI mode. The POL bit also controls the pull-up/down current at CFI. The INVPUD bit changes the polarity of the pull-up/down current at CFI independent of the other configurations. The pull-up/down current can be disconnected completely – if required – by means of register bit ENPUD (cf. Table 17).

POL	Adr 0x01; Bit (2) R/W 0
0	CFI hi → RX hi (ENOD = 0) resp. on (ENOD = 1) Pull-down current (ENPUD = 1, INVPUD = 0)
1	CFI hi → RX lo (ENOD = 0) resp. off (ENOD = 1) Pull-up current (ENPUD = 1, INVPUD = 0)

Table 16: Input polarity

ENPUD	Adr 0x01; Bit (3) R/W 1
0	CFI pull-up/down disabled
1	CFI pull-up/down enabled

Table 17: Enable pull-up/down

The state of the CFI pin (high or low) is mapped independent of POL to the register bit IND (see table 18). Changes at CFI can be logged in the status bit CFED (and signalled at pin NDIAG), if the bit ENCFD is set to high. The CFED bit is cleared after read.

IND	Adr 0x00; Bit (7) R
0	Input Signal at CFI is low
1	Input Signal at CFI is high

Table 18: CFI status

ENCFD	Adr 0x02; Bit (7) R/W 0
0	CFED Disabled
1	CFED Enabled

Table 19: Enable edge detection at CFI

Table 20 summarizes the behaviour of the feedback channel CFI in SPI mode.

Feedback channel CFI						
CFI	POL	INVPUD	IND	RX (ENOD = 0)	RX (ENOD = 1)	Current at CFI
0	0	0	0	0	off	down
1	0	0	1	1	on	down
0	1	0	0	1	on	up
1	1	0	1	0	off	up
0	0	1	0	0	off	up
1	0	1	1	1	on	up
0	1	1	0	1	on	down
1	1	1	1	0	off	down

Table 20: Function table of feedback channel CFI in SPI mode (ENPUD = 1)

Overload detection
In SPI mode the counter decrements of the overload detection can be programmed with the register DUTYC(1:0), resulting in different overload duty cycles at the switching channels. The maximum allowed over-

load time cannot be changed (cf. Electrical Characteristics No. 301), only the average value (duty cycle).

DUTYC(1:0)	Adr 0x03; Bit (3:2) R/W 10
00	Duty cycle of 1:4
01	Duty cycle of 1:8
10	Duty cycle of 1:10
11	Duty cycle of 1:15

Table 21: Overload detection duty cycle

Spread spectrum oscillator
In SPI mode the spread spectrum operation can be disabled with the register ENRND.

ENRND	Adr 0x02; Bit (4) R/W 1
0	Spread spectrum disabled
1	Spread spectrum enabled

Table 22: Spread spectrum oscillator

Pull-down currents
In SPI mode the pins NCS and SCLK do only have a pull-down current.

Undervoltage signalling
Undervoltage at VBO, VCC or VCC3 is signalled in the status register UVD. A valid undervoltage event is signalled for the duration of the undervoltage situation resp. for at least 35 ms (Electrical Characteristics No. 405). Only during this time, the undervoltage event is signalled in the status register UVD. It will also be signalled at pin NDIAG. Any confirmed undervoltage situation at VCC or VCC3 will reset the configuration register which will also be signalled in the status register INITR; this bit is cleared when read. The SPI interface is not affected by any of the undervoltage events and is still operable, provided that the supply level at VCC is high enough.

UVD(1:0)	Adr 0x04; Bit (7:6) R 00
00	No undervoltage detected
01	Undervoltage at VCC or VCC3
10	Undervoltage at VBO
11	Undervoltage at VBO and VCC/VCC3

Table 23: Undervoltage detection

Communication requests
The communication request function (IO-Link *wake-up*) allows interrupt signal generation by means of a well defined short-circuit on one of the switching channels. This requires the relevant switching channel (Q1 or Q2) to be connected to the feedback channel input CFI (see Figure 10). The communication request would be a contrasting pulse, forcing the selected line to a state different than the current one (short-circuit).

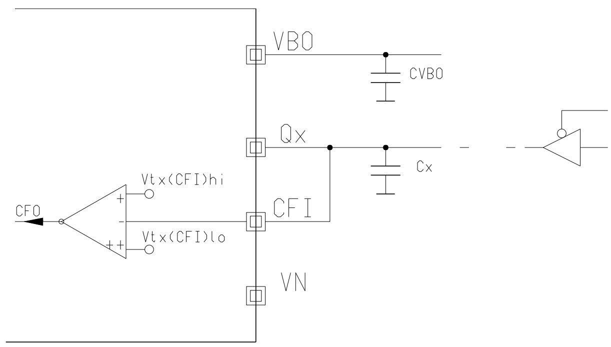


Figure 10: Communication request pulse generation

Bit ENSCR enables the communication request function. By default, communication requests are detected at channel 1 (Q1 connected to CFI). For detection at channel 2, the bit SCR2 must be set. As shown in Figure 11, a communication request is acknowledged when its duration is inside a defined window (cf. Electrical Characteristics No. 303). The relevant threshold voltages are given in the Electrical Characteristics Nos. 801, 802, 803 and 804. The example in Table 26 shows channel 1 used for communication request.

ENSCR	Adr 0x02; Bit (6) R/W 0
0	Communication request disabled
1	Communication request enabled

Table 24: Enable communication request

SCR2	Adr 0x02; Bit (5) R/W 0
0	Communication request in channel 1
1	Communication request in channel 2

Table 25: Communication request channel select

An acknowledged communication request will be logged in the status bit SCR and signalled at pin NDIAG. The communication request is not affected by the output disabling (neither by pin nor register OEN), but is disabled if the configuration in QCFGx is set to "00".

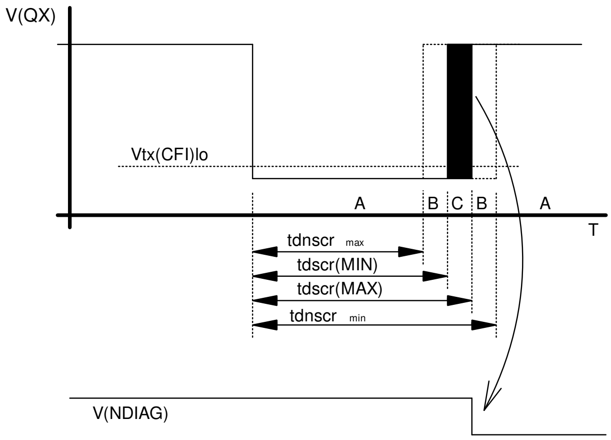


Figure 11: Communication request timing:
A: Communication request ignored
B: Uncertainty range
C: Communication request acknowledged

Sensor Communication request SCR		
OUTD(1:0)	QCFG1(1:0)	CFI (70...90 µs pulse)
x0	11	High
x1	11	Low
x0	10	High
x1	10	Low
x0	01	Low
x1	01	High

Table 26: Communication request at channel 1, OEN = 1, SCR2 = 0, ENSCR = 1, INVx = 0

SPI INTERFACE

The SPI interface uses the pins NCS, SCLK, MISO and MOSI. The protocol is shown in Figures 12 and 13. A communication frame consists of one addressing byte and one data byte. Bit 7 of the address byte is used for selecting a read (set to 1) or a write (set to 0) operation. The other bits are used for register addressing. It is possible to transmit several bytes consecutively, if the NCS signal is not reset and SCLK keeps clocking. The address is internally incremented after each transmitted byte. Once the address has reaches the last register (0x04), the following 3 increments will read and write dummy data. After that addressing will start again at 0x00. The required timing for the SPI signals during a communication is shown in Figure 1.

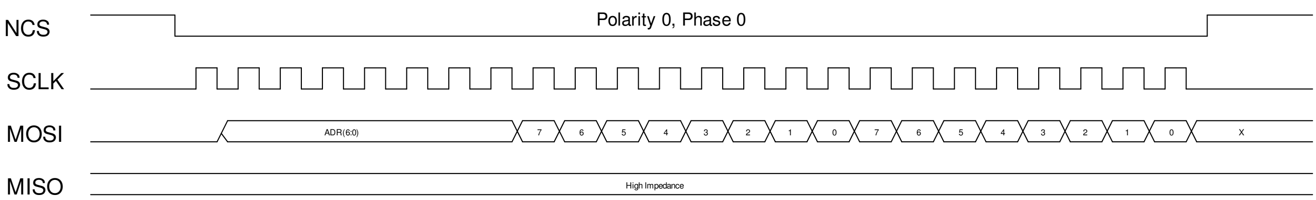


Figure 12: SPI write data

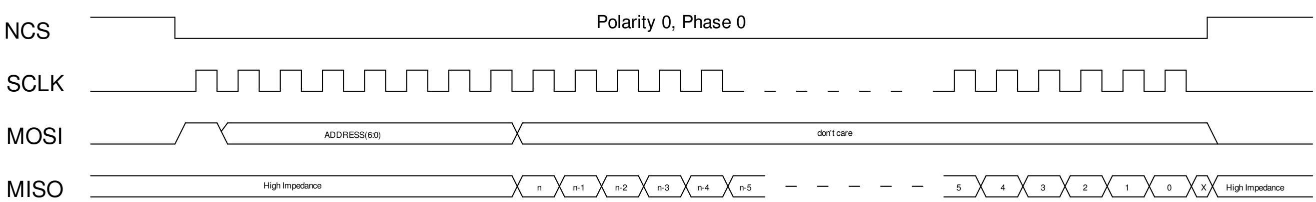


Figure 13: SPI read data

REGISTERS

Configuration overview
The configuration bytes are readable and writeable, with the exception of the IND bit (adr 0x00). The diagnostic register is read only. After reading, the bits CFED, INITRAM and WUD are reset. The bits OVT, OVL(1:0) and UVD(1:0) are set to high during the respective error condition and stay high for least 35 ms after the condition has been removed (Electrical Characteristics Nos. 302, 405). Tables 27, 28 and 29 show an overview of the registers, accessible in SPI mode.

Register	Address	Bits	Default	Description
DUTY	0x03	3:2	10	Duty cycle configuration for overload detection
ENCFD	0x02	7	0	Enable logging of changes at CFI
ENOD	0x01	0	1	Enable Open-Drain output at RX pin
ENPUD	0x01	3	1	Enable pull-up/down current at CFI pin
ENRND	0x02	4	1	Enable spread spectrum oscillator
ENSCR	0x02	6	0	Enable communication requests
FCFG	0x02	3:2	10	Filter configuration for TX and OEN
FCFI	0x02	1:0	01	Filter configuration for CFI
IND	0x00	7	R/O	CFI status (independent of POL), r/o
INV	0x03	5:4	00	Switching channel inversion
INVPUD	0x01	1	0	Invert pull-up/down configuration at CFI
NEXC	0x03	1:0	11	Enable excitation current for capacitive loads
OEN	0x00	3:2	11	Switching channel enable
OUTD	0x00	1:0	00	Output data for the switching channels
POL	0x01	2	0	Polarity inversion at CFI
QCFG1	0x01	5:4	11	Switching channel 1 configuration
QCFG2	0x01	7:6	11	Switching channel 2 configuration
TXEN	0x00	5:4	01	Channel control select (register or pin)
SCR2	0x02	5	0	Communication request channel selection

Table 27: Overview of the configuration registers

Register	Address	Bits	Description
INITR	0x04	0	Register reset
SCR	0x04	1	Communication request acknowledged
CFED	0x04	2	Change detection at CFI
OVT	0x04	3	Overtemperature
OVL(0)	0x04	4	Overload Channel 1
OVL(1)	0x04	5	Overload Channel 2
UVD(0)	0x04	6	Undervoltage VCC resp. VCC3
UVD(1)	0x04	7	Undervoltage VBO

Table 28: Overview of the diagnostic register (read only)

OVERVIEW

Adr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x00	IND		TXEN(1:0)		OEN(1:0)		OUTD(1:0)	
0x01	QCFG2(1:0)		QCFG1(1:0)		ENPUD	POL	INVPUD	ENOD
0x02	ENCFD	ENSCR	SCR2	ENRND	FCFG(1:0)		FCFI(1:0)	
0x03			INV(1:0)		DUTY(1:0)		NEXC(1:0)	
0x04	UVD(1:0)		OVL(1:0)		OVT	CFED	SCR	INITR

Table 29: Register layout

APPLICATION NOTES

Setup for medium and small currents at VCC/VCC3

For *medium* output currents at VCC/VCC3 the inductor of the switching converter may as well be replaced by a resistor (see Fig. 14), resulting though in a considerably less efficiency (power dissipation!) and an elevated noise level at VH and thus at VCC/VCC3.

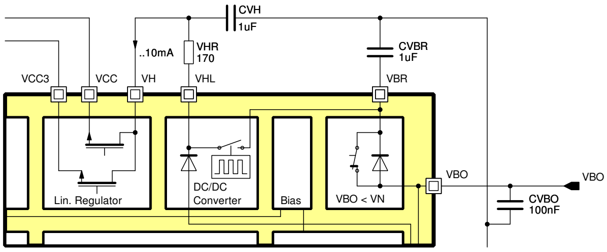


Figure 14: LVH replaced by a resistor

For *small* output currents the switching converter can be bypassed completely (see Fig. 15).

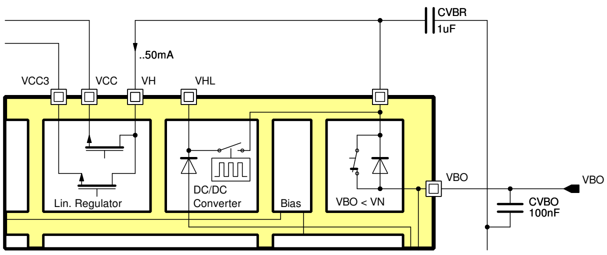


Figure 15: Switching converter bypassed

In extremely noisy environments, additional blocking capacitors (CEM1, CEM2) can be used to ensure SPI mode (see Fig. 16).

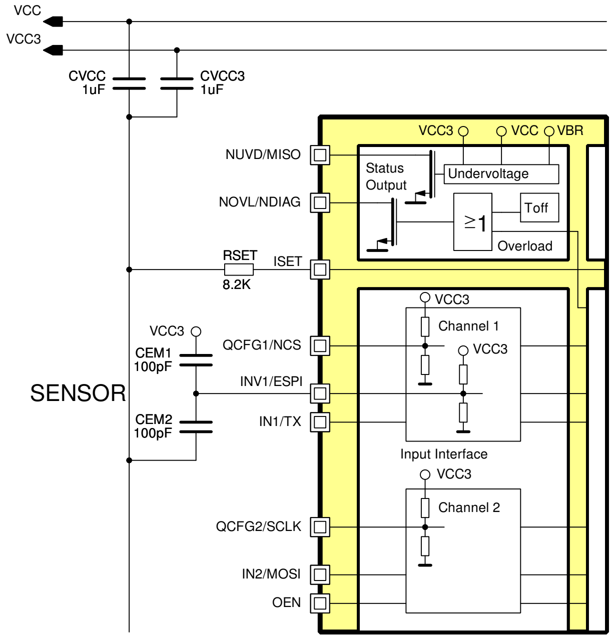


Figure 16: SPI Mode in extremely noisy environments

Output protection

Figures 17 to 20 show some common configurations with different wire counts and the respective additional protective circuitry against transients on the transmission line; suggested values as follows:

CQx:	1 nF
CCFI:	1 nF
CVBO:	100 nF
TVSx:	TVS diodes (eg. Vishay GSOT36C)

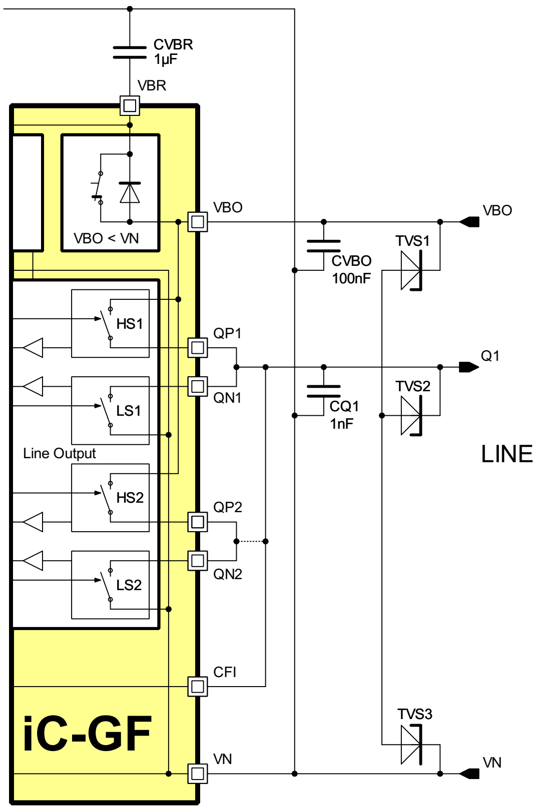


Figure 17: Three-wire interface with feedback (parallel operated channels optional)

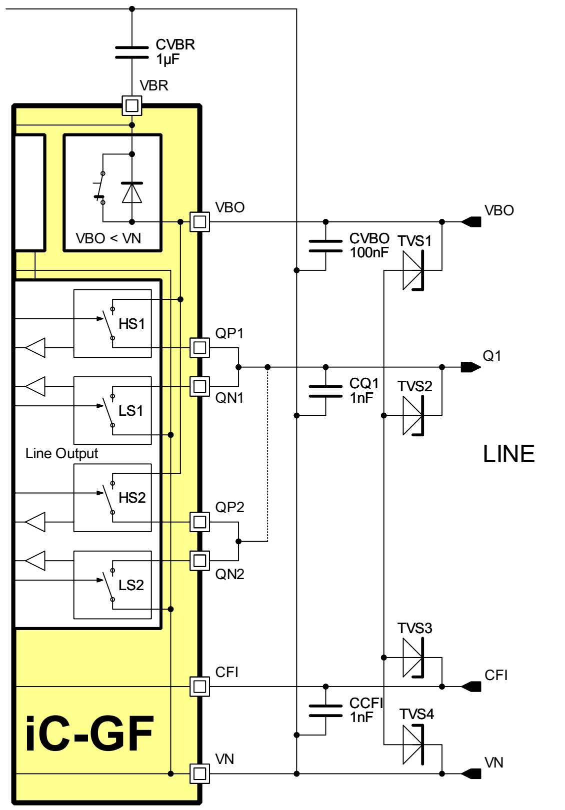


Figure 19: Four-wire interface with separate feedback (parallel operated channels optional)

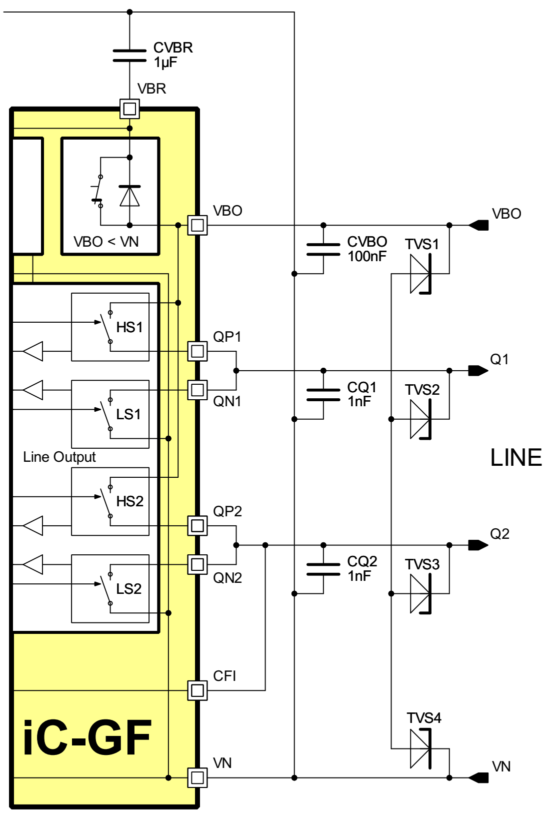


Figure 18: Four-wire interface with feedback at channel 2

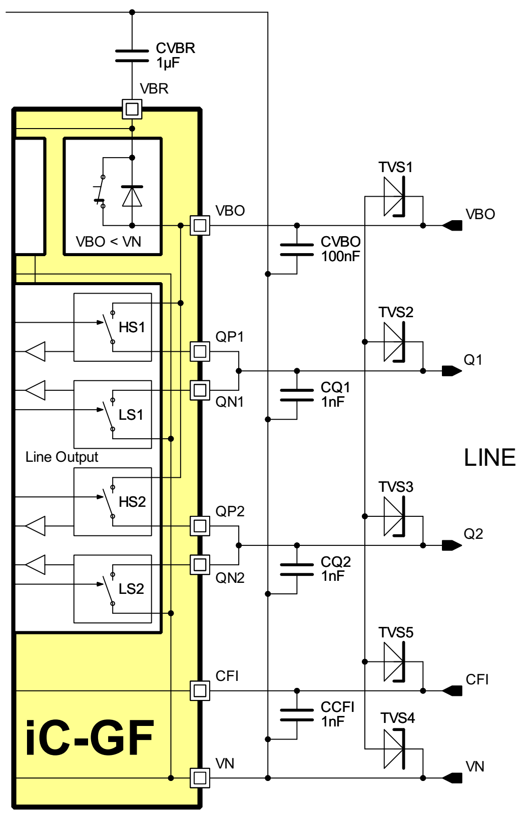


Figure 20: Five-wire interface

DEMO BOARD

iC-GF comes with a demo board for test purposes. Figures 21 and 22 show both the schematic and the component side of the demo board.

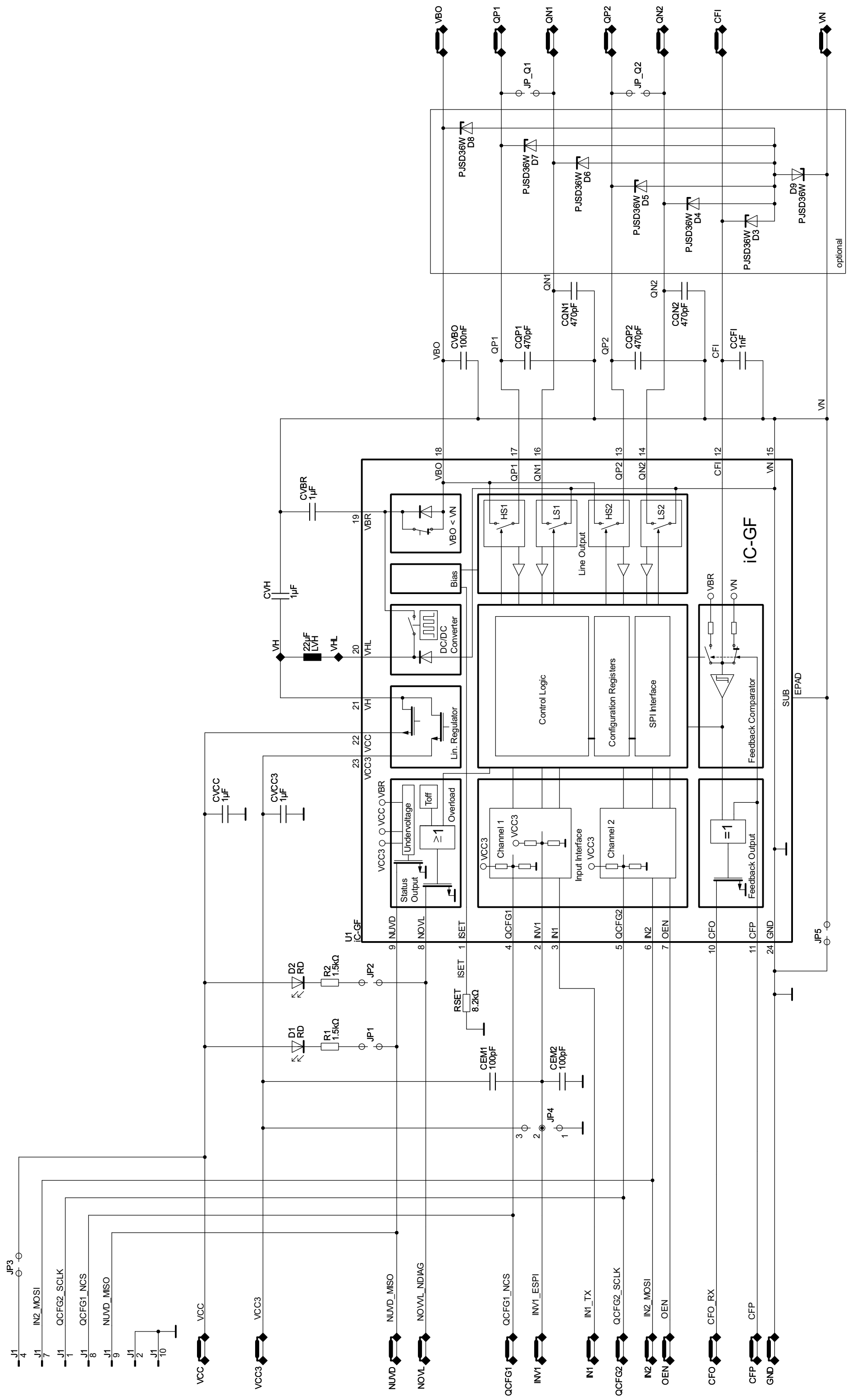


Figure 21: Schematic of the demo board

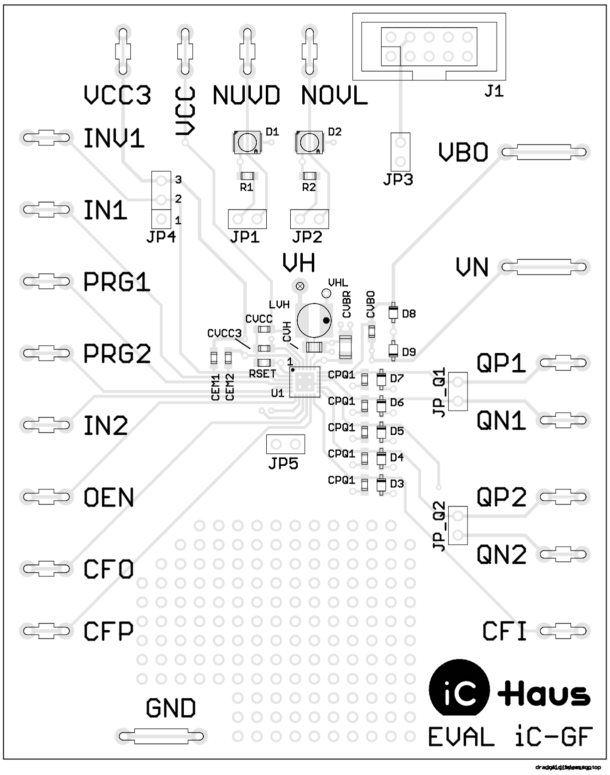


Figure 22: Demo board (component side)

iC-Haus expressly reserves the right to change its products and/or specifications. An Infoletter gives details as to any amendments and additions made to the relevant current specifications on our internet website www.ichaus.de/infoletter; this letter is generated automatically and shall be sent to registered users by email.
Copying – even as an excerpt – is only permitted with iC-Haus approval in writing and precise reference to source.
iC-Haus does not warrant the accuracy, completeness or timeliness of the specification on this site and does not assume liability for any errors or omissions in the materials. The data specified is intended solely for the purpose of product description. No representations or warranties, either express or implied, of merchantability, fitness for a particular purpose or of any other nature are made hereunder with respect to information/specification or the products to which information refers and no guarantee with respect to compliance to the intended use is given. In particular, this also applies to the stated possible applications or areas of applications of the product.
iC-Haus conveys no patent, copyright, mask work right or other trade mark right to this product. iC-Haus assumes no liability for any patent and/or other trade mark rights of a third party resulting from processing or handling of the product and/or any other use of the product.
As a general rule our developments, IPs, principle circuitry and range of Integrated Circuits are suitable and specifically designed for appropriate use in technical applications, such as in devices, systems and any kind of technical equipment, in so far as they do not infringe existing patent rights. In principle the range of use is limitless in a technical sense and refers to the products listed in the inventory of goods compiled for the 2008 and following export trade statistics issued annually by the Bureau of Statistics in Wiesbaden, for example, or to any product in the product catalogue published for the 2007 and following exhibitions in Hanover (Hannover-Messe).
We understand suitable application of our published designs to be state-of-the-art technology which can no longer be classed as inventive under the stipulations of patent law. Our explicit application notes are to be treated only as mere examples of the many possible and extremely advantageous uses our products can be put to.

ORDERING INFORMATION

Type	Package	Order Designation
iC-GF Evaluation Board	QFN24 4 mm x 4 mm (RoHS compliant)	iC-GF QFN24 iC-GF EVAL GF1D

For technical support, information about prices and terms of delivery please contact:

iC-Haus GmbH
Am Kuemmerling 18
D-55294 Bodenheim
GERMANY

Tel.: +49 (61 35) 92 92-0
Fax: +49 (61 35) 92 92-192
Web: http://www.ichaus.com
E-Mail: sales@ichaus.com

Appointed local distributors: http://www.ichaus.com/sales_partners