

# iC-LF1401

128x1 LINEAR IMAGE SENSOR



Rev B1, Page 1/10

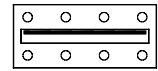
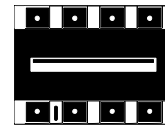
## FEATURES

- ◆ 128 active photo pixels of 56  $\mu\text{m}$  at a 63.5  $\mu\text{m}$  pitch (400 DPI)
- ◆ Integrating L-V conversion followed by a sample & hold circuit
- ◆ High sensitivity and uniformity over wavelength
- ◆ High clockrates of up to 5 MHz
- ◆ Only 128 clocks required for readout
- ◆ Shutter function enables flexible integration times
- ◆ Glitch-free analogue output
- ◆ Push-pull output amplifier
- ◆ 5 V single supply operation
- ◆ Can run off external bias to reduce power consumption
- ◆ Pin-to-pin compatible with TSL1401

## APPLICATIONS

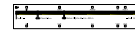
- ◆ Optical line image sensors
- ◆ CCD substitute

## PACKAGES



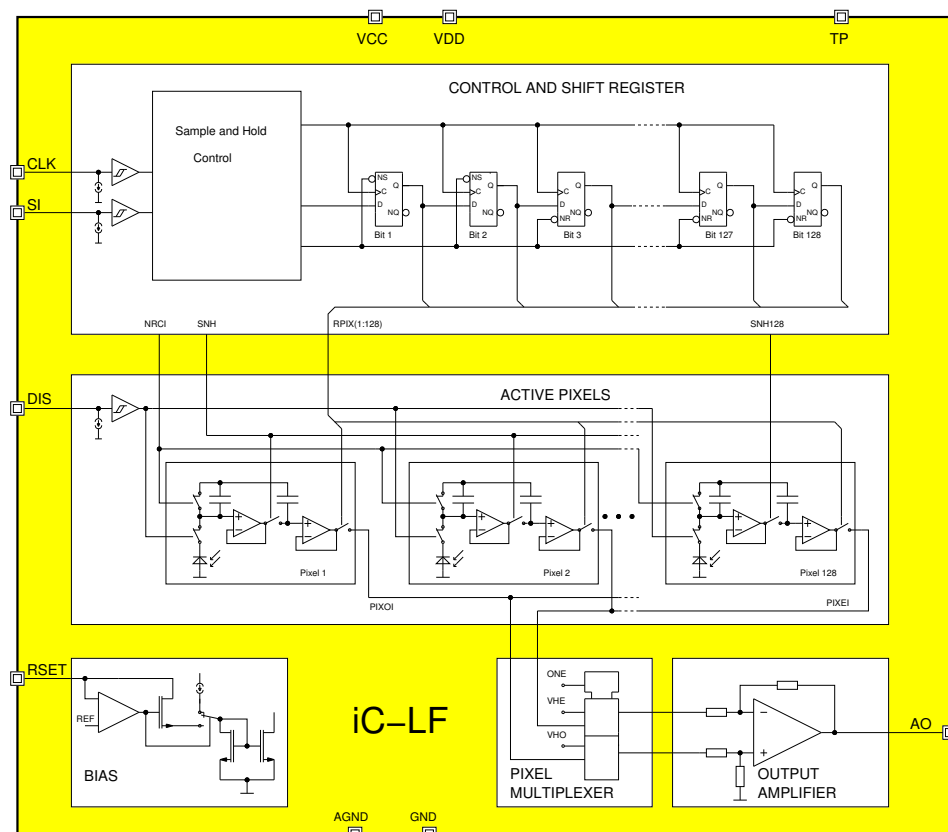
OLGA LF2C

OBGA™ LF3C



Die size (8.5 mm x 1.6 mm)

## BLOCK DIAGRAM



# iC-LF1401

128x1 LINEAR IMAGE SENSOR



Rev B1, Page 2/10

## DESCRIPTION

iC-LF1401 is an integrating light-to-voltage converter with a line of 128 pixels pitched at  $63.5\ \mu\text{m}$  (center-to-center distance). Each pixel consists of a  $56.4\ \mu\text{m} \times 200\ \mu\text{m}$  photodiode and an integration capacitor with a sample-and-hold circuit.

The integrated control logic makes operation very simple, with only a start and clock signal necessary. A third control input (DIS) enables the integration to be suspended at any time (electronic shutter).

When the start signal is given hold mode is activated for all pixels simultaneously with the next lead-

ing clock edge; starting with pixel 1 the hold voltages are switched in sequence to the push-pull output amplifier. The second clock pulse resets all integration capacitors and the integration period starts again in the background during the output phase. A run is complete after 128 clock pulses.

iC-LF1401 is suitable for high clock rates of up to 5 MHz. If this is not required the supply current can be reduced via the external bias setting (current into pin RSET).

# iC-LF1401

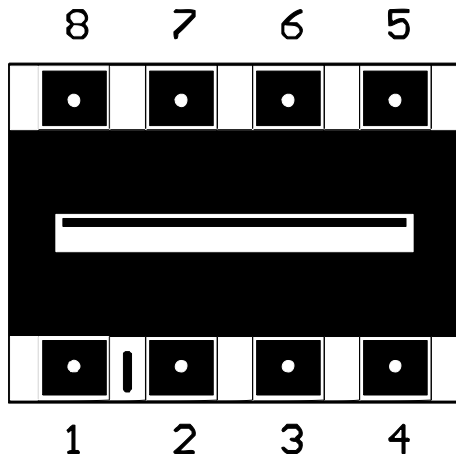
128x1 LINEAR IMAGE SENSOR



Rev B1, Page 3/10

## PACKAGES OLGA LF2C, OBGA™ LF3C

### PIN CONFIGURATION OLGA LF2C

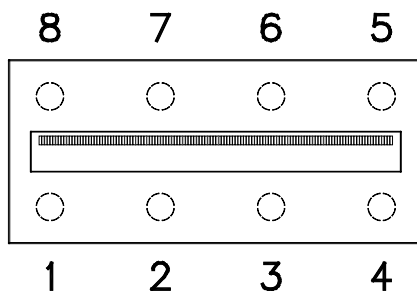


### PIN FUNCTIONS

#### No. Name Function

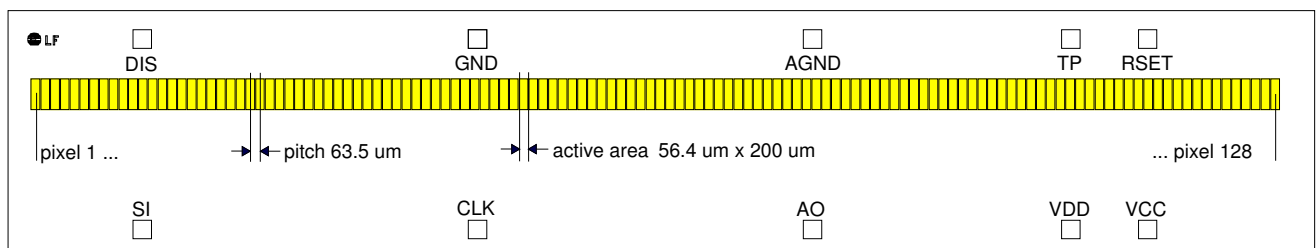
- |   |      |  |
|---|------|--|
| 1 | SI   | Start Integration Input  |
| 2 | CLK  | Clock Input  |
| 3 | AO   | Analogue Output  |
| 4 | VCC  | +5 V Supply Voltage  |
| 5 | RSET | Bias Current (connected to GND for internal bias = default; resistor from VCC to RSET for reduced current consumption) |
| 6 | AGND | Analogue Ground  |
| 7 | GND  | Digital Ground   |
| 8 | DIS  | Hold Integration Input   |

### PIN CONFIGURATION OBGA™ LF3C



## CHIP LAYOUT

Die size: 8.5 mm x 1.6 mm



# iC-LF1401

## 128x1 LINEAR IMAGE SENSOR



Rev B1, Page 4/10

### ABSOLUTE MAXIMUM RATINGS

Beyond these values damage may occur; device operation is not guaranteed.

| Item No. | Symbol | Parameter                             | Conditions   | Limits |           | Unit |
|----------|--------|---------------------------------------|--|--------|-----------|------|
|          |        |                                       |  | Min.   | Max.      |      |
| G001     | VDD    | Digital Supply Voltage                |  | -0.3   | 6         | V    |
| G002     | VCC    | Analog Supply Voltage                 |  | -0.3   | 6         | V    |
| G003     | V()    | Voltage at SI, CLK, DIS, RSET, TP, AO |  | -0.3   | VCC + 0.3 | V    |
| G004     | I()    | Current in RSET, TP, AO               |  | -10    | 10        | mA   |
| G005     | Vd()   | ESD Susceptibility at all pins        | MIL-STD-883, Method 3015, HBM 100 pF discharged through 1.5 kΩ |        | 2         | kV   |
| G006     | Tj     | Operating Junction Temperature        |  | -40    | 125       | °C   |
| G007     | Ts     | Storage Temperature Range             | see package specification                                      |        |           |      |

### THERMAL DATA

Operating Conditions: VCC = VDD = 5 V ±10 %

| Item No. | Symbol | Parameter   | Conditions                | Limits |      |      | Unit |
|----------|--------|---|---------------------------|--------|------|------|------|
|          |        |   |                           | Min.   | Typ. | Max. |      |
| T01      | Ta     | Operating Ambient Temperature Range (extended range on request) | see package specification |        |      |      |      |

All voltages are referenced to ground unless otherwise stated.

All currents into the device pins are positive; all currents out of the device pins are negative.

# iC-LF1401

## 128x1 LINEAR IMAGE SENSOR



Rev B1, Page 5/10

### ELECTRICAL CHARACTERISTICS

Operating Conditions: VCC = VDD = 5 V ±10 %, RSET = GND, Tj = -25...85 °C unless otherwise noted

| Item No.                            | Symbol     | Parameter  | Conditions  |         |      |      | Unit              |
|-------------------------------------|------------|--|---|---------|------|------|-------------------|
|                                     |            |  |   | Min.    | Typ. | Max. |                   |
| <b>Total Device</b>                 |            |  |   |         |      |      |                   |
| 001                                 | VDD        | Digital Supply Voltage Range                     |   | 4.5     |      | 5.5  | V                 |
| 002                                 | VCC        | Analog Supply Voltage Range                      |   | 4.5     |      | 5.5  | V                 |
| 003                                 | I(VDD)     | Supply Current in VDD                            | f(CLK) = 1 MHz  |         | 200  | 300  | µA                |
| 004                                 | I(VCC)     | Supply Current in VCC                            |   |         | 8    | 13   | mA                |
| 005                                 | Vc()hi     | Clamp Voltage hi at SI, CLK,DIS, TP, RSET        | Vc()hi = V() – V(VCC); I() = 1 mA                       | 0.3     |      | 1.8  | V                 |
| 006                                 | Vc()lo     | Clamp Voltage lo at SI, CLK,DIS, TP, RSET        | Vc()hi = V() – V(AGND); I() = -1 mA                     | -1.5    |      | -0.3 | V                 |
| 007                                 | Vc()hi     | Clamp Voltage hi at AO                           | Vc()hi = V(AO) – V(VCC); I(AO) = 1 mA                   | 0.3     |      | 1.5  | V                 |
| 008                                 | Vc()lo     | Clamp Voltage lo at AO, VCC, VDD, GND            | Vc()lo = V() – V(AGND); I() = -1 mA                     | -1.5    |      | -0.3 | V                 |
| <b>Photodiode Array</b>             |            |  |   |         |      |      |                   |
| 201                                 | A()        | Radiant Sensitive Area                           | 200 µm x 56.40 µm per Pixel                             | 0.01128 |      |      | mm <sup>2</sup>   |
| 202                                 | S(λ)max    | Spectral Sensitivity                             | λ = 680 nm  |         | 0.5  |      | A/W               |
| 203                                 | λar        | Spectral Application Range                       | S(λar) = 0.25 x S(λ)max                                 | 400     |      | 980  | nm                |
| <b>Analogue Output AO</b>           |            |  |   |         |      |      |                   |
| 301                                 | Vs()lo     | Saturation Voltage lo                            | I() = 1 mA  |         |      | 0.5  | V                 |
| 302                                 | Vs()hi     | Saturation Voltage hi                            | Vs()hi = VCC – V(), I() = -1 mA                         |         |      | 1    | V                 |
| 303                                 | K          | Sensitivity                                      | λ = 680 nm, package OLGA LF2C                           |         | 2.88 |      | V/pWs             |
| 304                                 | V0()       | Offset Voltage                                   | integration time 1 ms, no illumination                  |         | 400  | 800  | mV                |
| 305                                 | ΔV0()      | Offset Voltage Deviation during integration mode | ΔV0() = V(AO)t1 – V(AO)t2, Δt = t2 – t1 = 1 ms          | -250    |      | 50   | mV                |
| 306                                 | ΔV()       | Signal Deviation during hold mode                | ΔV() = V(AO)t1 – V(AO)t2, Δt = t2 – t1 = 1 ms           | -150    |      | 150  | mV                |
| 307                                 | tp(CLK-AO) | Settling Time                                    | CI(AO) = 10 pF, CLK lo → hi until V(AO) = 0.98 x V(VCC) |         |      | 200  | ns                |
| 308                                 | PRNU       | Pixel Response Nonuniformity                     | V(AO) = 2 V   |         |      | ±5*  | %                 |
| 309                                 | INL        | Integral Nonlinearity                            | V(AO) = 1...3.5 V                                       |         | ±1   |      | %                 |
| 310                                 | Vnoise(AO) | Output Noise Voltage                             | V(AO) = 2 V   |         | 2    |      | mV <sub>RMS</sub> |
| 311                                 | DR         | Dynamic Range†                                   | V(AO) <sub>max</sub> = 3.5 V                            |         | 62   |      | dB                |
| <b>Power-On Reset</b>               |            |  |   |         |      |      |                   |
| 801                                 | VCCon      | Power-On Release by VCC                          |   |         |      | 4.4  | V                 |
| 802                                 | VCCoff     | Power-Down Reset by VCC                          |   | 1       |      |      | V                 |
| 803                                 | VCChys     | Hysteresis                                       | VCChys = VCCon – VCCoff                                 | 0.4     | 1    | 2    | V                 |
| <b>Bias Current Adjust RSET</b>     |            |  |   |         |      |      |                   |
| 901                                 | Ibias()    | Permissible External Bias Current                |   | 20      |      | 100  | µA                |
| 902                                 | Vref       | Reference Voltage                                | I(RSET) = Ibias   | 2.5     | 3    | 3.5  | V                 |
| <b>Input Interface SI, CLK, DIS</b> |            |  |   |         |      |      |                   |
| B01                                 | Vt()hi     | Threshold Voltage hi                             | see Fig. 2  | 1.4     |      | 1.8  | V                 |
| B02                                 | Vt()lo     | Threshold Voltage lo                             | see Fig. 2  | 0.9     |      | 1.2  | V                 |
| B03                                 | Vt()hys    | Hysteresis                                       | Vt()hys = Vt()hi – Vt()lo, see Fig. 2                   | 300     |      | 800  | mV                |
| B04                                 | I()        | Pull-Down Current                                |   | 10      | 30   | 50   | µA                |
| B05                                 | fclk       | Permissible Clock Frequency                      |   |         |      | 5    | MHz               |

\* Projected values by sample characterization

†  $DR = 20 \times \log \frac{V(AO)_{max} - V(AO)_{min}}{V_{noise(AO)}}$

### OPTICAL CHARACTERISTICS: Diagrams

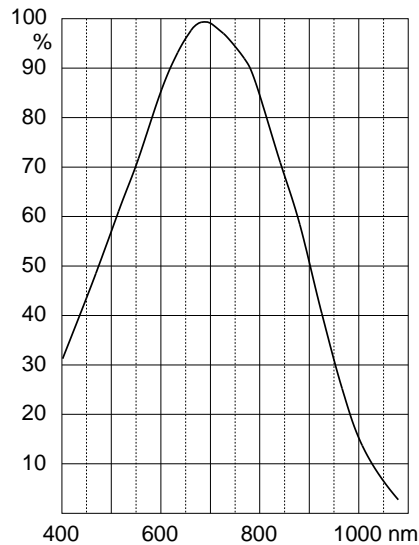


Figure 1: Relative spectral sensitivity

### OPERATING REQUIREMENTS: Logic

Operating Conditions:  $V_{CC} = V_{DD} = 5V \pm 10\%$ ,  $T_j = -25 \dots 85^\circ C$   
 input levels  $lo = 0 \dots 0.45V$ ,  $hi = 2.4V \dots V_{CC}$ , see Fig. 2 for reference levels

| Item No. | Symbol | Parameter   | Conditions | Fig. | Min.   Max. |      | Unit |
|----------|--------|---|------------|------|-------------|------|------|
|          |        |   |            |      | Min.        | Max. |      |
| I001     | tset   | Setup Time:<br>SI stable before CLK lo $\rightarrow$ hi |            | 3    | 50          |      | ns   |
| I002     | thold  | Hold Time:SI stable after CLK lo $\rightarrow$ hi       |            | 3    | 50          |      | ns   |

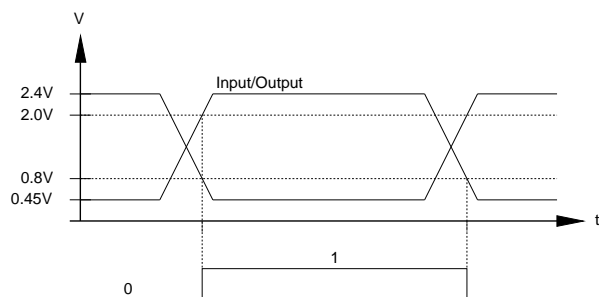


Figure 2: Reference levels

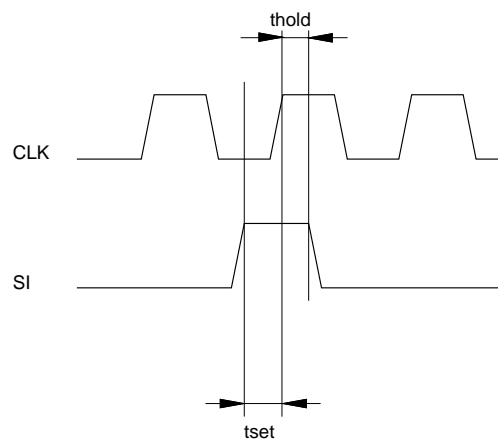


Figure 3: Timing diagram

**DESCRIPTION OF FUNCTIONS**

**Normal operation**

Following an internal power-on reset the integration and hold capacitors are discharged and the sample and hold circuit is set to sample mode. A high signal at SI and a rising edge at CLK triggers a readout cycle and with it a new integration cycle.

In this process the hold capacitors of pixels 1 to 127 are switched to hold mode immediately (SNH = 1),

with pixel 128 (SNH128 = 1) following suit one clock pulse later. This special procedure allows all pixels to be read out with just 128 clock pulses. The integration capacitors are discharged by a one clock long reset signal (NRCI = 0) which occurs between the 2<sup>nd</sup> and 3<sup>rd</sup> falling edge of the readout clock pulse (cf. Figure 4). After the 127 pixels have been read out these are again set to sample mode (SNH = 0), likewise for pixel 128 one clock pulse later (SNH128 = 0).

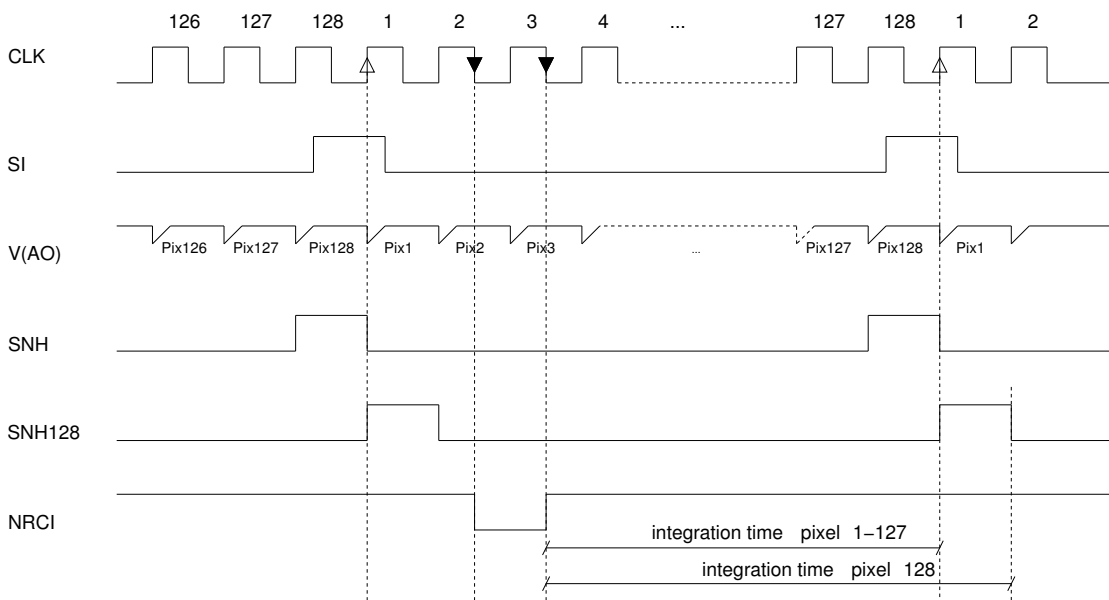


Figure 4: Readout cycle and integration sequence

If prior to the 128<sup>th</sup> clock pulse a high signal occurs at SI the present readout is halted and immediately reinitiated with pixel 1. In this instance the hold ca-

pacitors retain their old value i.e. hold mode prevails (SNH/SNH128 = 0).

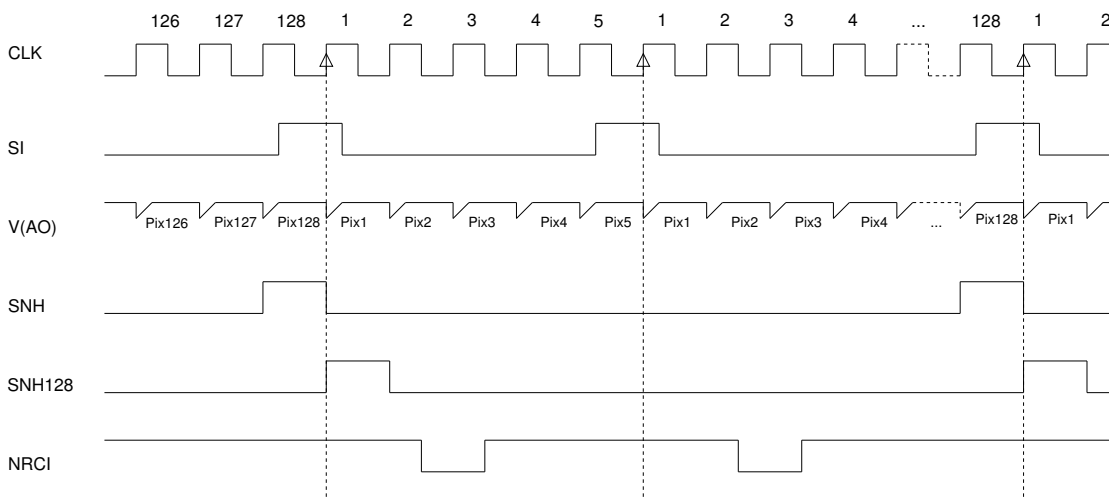


Figure 5: Restarting a readout cycle

With more than 128 clock pulses until the next SI signal, pixel 1 is output without entering hold mode; the output voltage tracks the voltage of the pixel 1 integration capacitor.

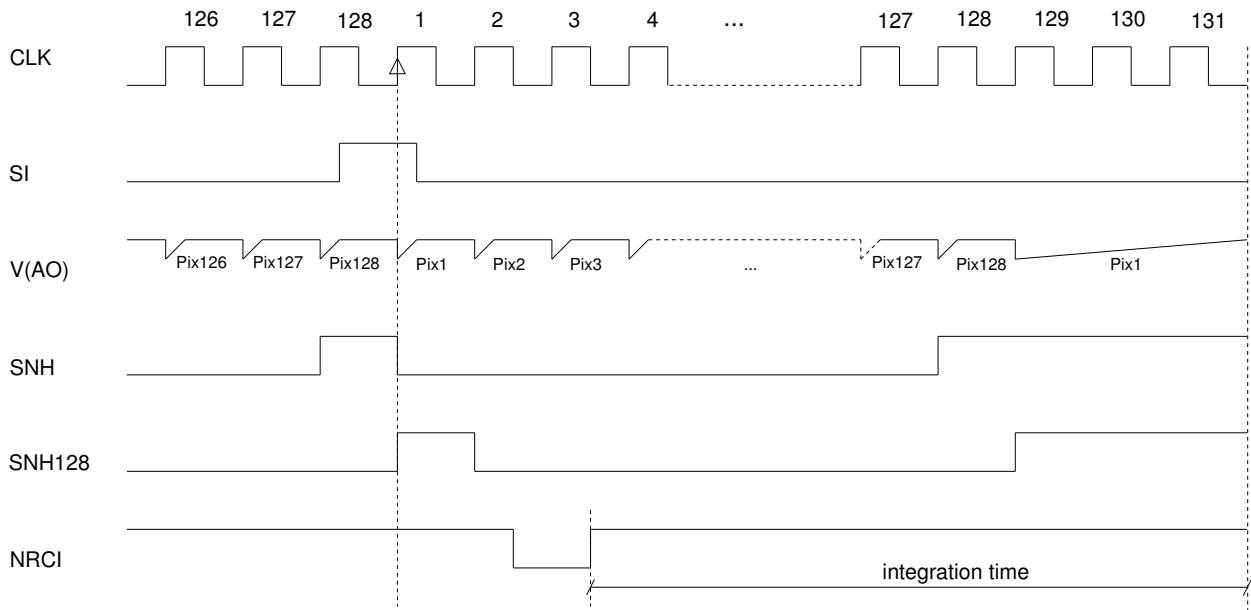


Figure 6: Clock pulse continued without giving a new integration start signal

### Operation with the shutter function

Integration can be suspended at any time via pin DIS, i.e. the photodiodes are disconnected from their corresponding integration capacitor when DIS is high and

the current integration capacitor voltages are maintained. If this pin is open or switched to GND the pixel photocurrents are summed up by the integration capacitors until the next successive SI signal follows.

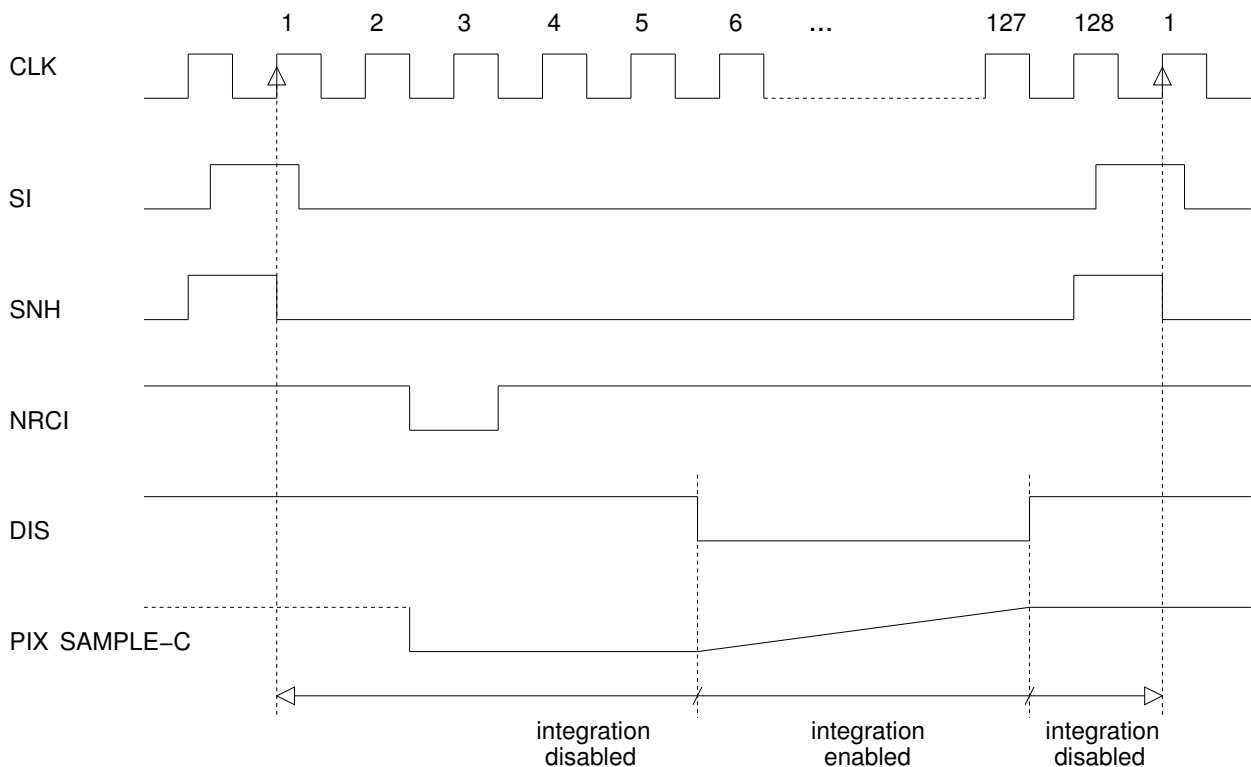


Figure 7: Defining the integration time via shutter input DIS



# iC-LF1401

128x1 LINEAR IMAGE SENSOR



Rev B1, Page 9/10

## External bias current setting

In order to reduce the power consumption of the device an external reference current can be supplied to pin RSET which reduces the maximum readout frequency,

however. To this end a resistor must be connected from VCC to RSET. If this pin is not used, it should be connected to GND.

This specification is for a newly developed product. iC-Haus therefore reserves the right to change or update, without notice, any information contained herein, design and specification; and to discontinue or limit production or distribution of any product versions. Please contact iC-Haus to ascertain the current data.

Copying – even as an excerpt – is only permitted with iC-Haus approval in writing and precise reference to source.

iC-Haus does not warrant the accuracy, completeness or timeliness of the specification on this site and does not assume liability for any errors or omissions in the materials. The data specified is intended solely for the purpose of product description. No representations or warranties, either express or implied, of merchantability, fitness for a particular purpose or of any other nature are made hereunder with respect to information/specification or the products to which information refers and no guarantee with respect to compliance to the intended use is given. In particular, this also applies to the stated possible applications or areas of applications of the product.

iC-Haus conveys no patent, copyright, mask work right or other trade mark right to this product. iC-Haus assumes no liability for any patent and/or other trade mark rights of a third party resulting from processing or handling of the product and/or any other use of the product.

As a general rule our developments, IPs, principle circuitry and range of Integrated Circuits are suitable and specifically designed for appropriate use in technical applications, such as in devices, systems and any kind of technical equipment, in so far as they do not infringe existing patent rights. In principle the range of use is limitless in a technical sense and refers to the products listed in the inventory of goods compiled for the 2008 and following export trade statistics issued annually by the Bureau of Statistics in Wiesbaden, for example, or to any product in the product catalogue published for the 2007 and following exhibitions in Hanover (Hannover-Messe).

We understand suitable application of our published designs to be state-of-the-art technology which can no longer be classed as inventive under the stipulations of patent law. Our explicit application notes are to be treated only as mere examples of the many possible and extremely advantageous uses our products can be put to.

# iC-LF1401

128x1 LINEAR IMAGE SENSOR



Rev B1, Page 10/10

## ORDERING INFORMATION

| Type  | Package                      | Order Designation                                |
|-------|------------------------------|--|
| iC-LF | OLGA LF2C<br>OBGA™ LF3C<br>- | iC-LF OLGA LF2C<br>iC-LF OBGA LF3C<br>iC-LF chip |

For technical support, information about prices and terms of delivery please contact:

**iC-Haus GmbH**  
Am Kuemmerling 18  
D-55294 Bodenheim  
GERMANY

**Tel.: +49 (61 35) 92 92-0**  
**Fax: +49 (61 35) 92 92-192**  
**Web: <http://www.ichaus.com>**  
**E-Mail: [sales@ichaus.com](mailto:sales@ichaus.com)**

Appointed local distributors: [http://www.ichaus.de/support\\_distributors.php](http://www.ichaus.de/support_distributors.php)