V1.0 July 2009

TDA 5150

Multichannel / Multiband Transmitter

Multichannel / Multiband RF Transmitter for 300-928 MHz bands

On-chip, high resolution fractional-N synthesizer and
Sigma-Delta modulator with ASK, FSK, GFSK options

Wireless Control

Never stop thinking.

Edition July 2009

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TDA 5150
Revision History: V1.0

Previous Version:	**V0.94** issued January 2009
	New issue

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1 Product Description

1.1 Overview

The TDA 5150 is a low cost and easy to implement, multi-channel ASK/FSK/GFSK RF transmitter for the 300-320 MHz, 425-450 MHz, 863 - 928 MHz frequency bands with low power consumption and RF-output power of up to +10 dBm.

The IC offers a high level of integration and needs only a few external components, such as a crystal, blocking capacitors and the necessary matching elements between the power amplifier output and the antenna.

On-chip antenna tuning capacitors are implemented.

An integrated high-resolution sigma-delta fractional-N PLL synthesizer covers all of the above listed frequency bands, using the same crystal for reference frequency generation.

The configurable digital modulator allows precise FSK modulation and Gaussian shaping (GFSK), which contributes to reduction of occupied bandwidth.

The output power of the integrated class-C RF power amplifier can be controlled over the SPI bus and if necessary, downsized (reduced) in digital steps.

ASK shaping option contributes to reduced harmonics and minimized spectral splatter.

The data encoder supports NRZ, Manchester, Bi-Phase, and Miller encoding.

The device is fully configureable via the 3-wire Serial Peripheral Interface (SPI).

1.2 Features

- High resolution Sigma-Delta fractional-N PLL synthesizer (frequency step size down to 7 Hz)
- Multiband/Multichannel capability for the 300-320 MHz, 425-450 MHz and 863-928 MHz bands
- Modulation types ASK (OOK) with ASK shaping, FSK (CPFSK) and GFSK
- Multi-channel and channel hopping capability, 4 register banks for fast Tx frequency switching
- Configurable via 3-wire serial interface bus (SPI)
- Manchester, Bi-Phase, and Miller encoding, on-chip PRBS9 scrambler
- Continuos checking of chip status by Fail-Safe mechanism
- Transparent and synchronized RF modulation mode
- Programmable clock divider output
- Configurable output power level from -10 dBm to +10 dbm, in 2 dB nominal steps
- Supply voltage range 1.9 V - 3.6 V, 2 low battery detection thresholds, preset to 2.4V and 2.1V
- Low supply current (Sleep Mode < 0.8 µA, RF transmission 9 mA @ +5 dBm)
- ESD protection up to +/- 4 kV on all pins
- Operating temperature range -40°C to +85°C
- Green Package TSSOP-10

1.3 Applications

- Short range wireless data transmission
- Remote keyless entry transmitters
- Remote control units
- Wireless alarm systems
- Remote metering
- Garage door openers

1.4 Order Information

Type	Ordering Code	Package
TDA 5150	SP000300415	PG-TSSOP-10

1.5 Key Features overview

1.5.1 Typical Application Circuit

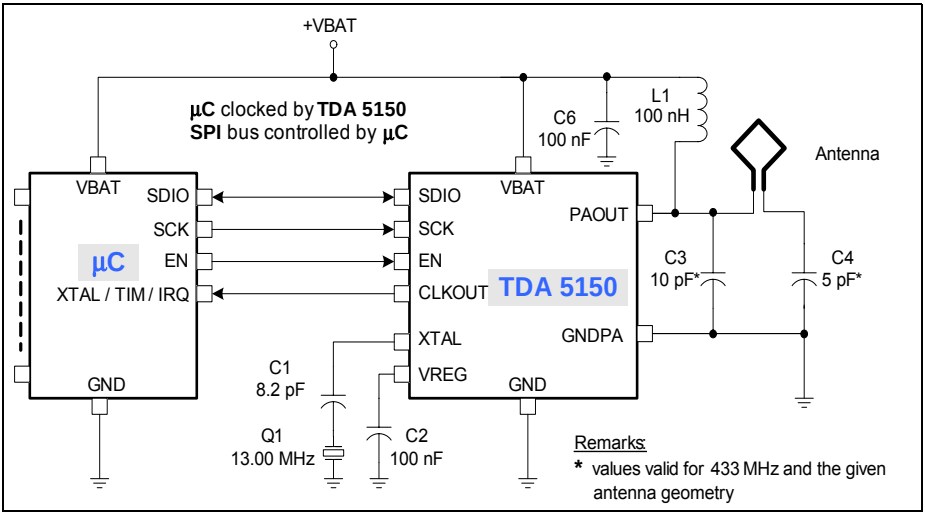


Figure 1 Minimum component count application circuit

The TDA 5150 application circuit shown demonstrates the ease and simplicity of an intelligent transmitter implementation. The µC configures the TDA5150 via 3-wire SPI, the SDIO line is used at the same time to transfer data on SPI bus and as digital data input into the RF modulator. The CLKOUT line may be used as clock source for the µC or as a timer for bitrate generation.

The matching shown is an example for a loop antenna application. Different antenna types (electrical monopole or dipole, magnetic loop etc.) as well as different layout versions might require component values which can differ from those given in above example. The antenna geometry has a major influence on the antenna impedance and consequently on the component values in the matching network.

1.5.2 Sigma-Delta fractional-N PLL with High Resolution

This type of PLL offers a multitude of advantages compared to fixed, integer division ratio PLLs.

In the reference oscillator circuit the same crystal can be used for all of the RF bands and frequencies (for example a 13 MHz crystal).

Dedicated crystals for each frequency are no longer required.

However by choice of crystal frequency a phenomenon, known as occurrence of fractional-N spurs must be kept in mind. The phenomenon and the countermeasures which should be taken to avoid it are described in detail in **Chapter 2.4.6.1**.

The PLL allows a direct (G)FSK modulation for reduced spurs and harmonics with high accuracy and resolution compared to legacy transmitters using crystal pulling for FSK modulation.

Synthesizer resolution down to 7 Hz for carrier frequency and FSK deviation allows fine tuning, correction of crystal tolerances and for temperature drift.

1.5.3 Reduction of Spurs and Occupied Bandwidth

The direct FSK modulation and in addition the Gaussian FSK (GFSK) reduces spurs and occupied bandwidth. Bandwidth reduction is exemplified below

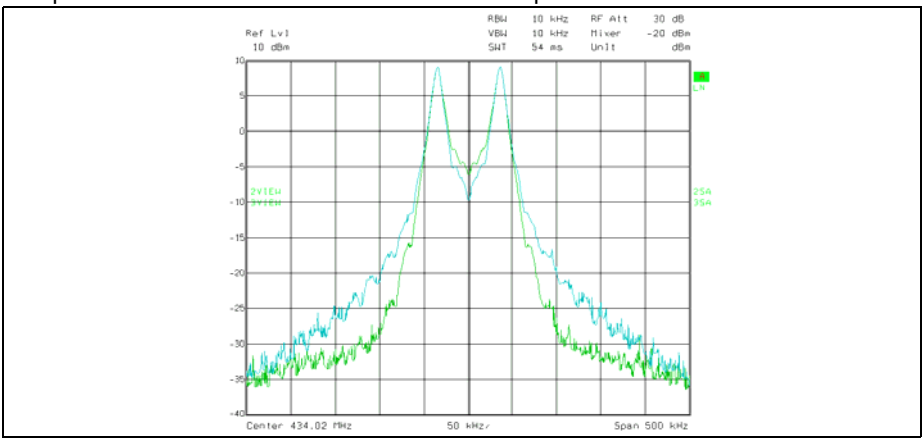


Figure 2 Spectrum of RF-signals with equal frequency deviations (± 35kHz), same 20kBit/s datarate and encoding (NRZ). Blue plot corresponds to FSK modulation and green to GFSK. Observe the difference in terms of occupied bandwidth between the signals.

1.5.4 Asynchronous and Synchronous Transmission

TDA 5150 offers a simple asynchronous transmission mode (transparent modulation), whereby after the configuration word is downloaded into the transmitter's SFRs (via SPI bus) the data bitstream is output on the SDIO line and fed into the transmitter's RF modulator.

The CLKOUT signal can be used either as clock line for host µC or, alternatively, as timer base (flag) for bitrate generator (this last function should be implemented in µC).

In this mode, the bitrate is solely imposed and controlled by the µC software.

GFSK modulation and ASK shaping options are allowed in Asynchronous Mode.

In Synchronous Transmission Mode the bitrate is solely under the transmitter's control and fully timed by the TDA 5150. The CLKOUT is used to alert the µC about the request for next databit.

The µC may have a higher allowable processing delay tolerance, typically the duration of 1/2 bit, before sending the corresponding bit via SDIO line to transmitter.

Usage of data encoding option is allowed in Synchronous Mode.

1.5.5 Integrated Data Encoder

TDA 5150 comprises a Data Encoder which automatically generates encoded data from a regular (NRZ) bitstream. The supported data encoding modes are:

- Manchester code
- Differential Manchester code
- Bi-phase space code
- Bi-phase mark code
- Miller code (Delay modulation)
- NRZ
- Scrambling (PRBS9 generator)

All the encoded bitstreams can be level inverted (as part of the encoding option). The scrambling module (PRBS9 generator) is intended to be used for generation of pseudo-random data patterns (rather for Tx test scopes) or for basic level data encryption.

1.5.6 Fail-Safe Mechanism

The Transmitter Status Register reports about failures such as: Brownout event, PLL lock error, VCO auto-calibration error and Register Parity error.

The Register Parity is a special safety feature. Each SFR (Special Function Register) has an extra parity bit which is automatically calculated and stored during a SFR write operation. During transmitter active state these parity bits, belonging to SFR content are continuously recalculated and compared against the stored values. Changes in the contents of writable SFRs without write command generate an SFR error event and an error flag is set.

To prevent erroneous transmissions (on wrong frequency or with erroneous modulation parameters, altered payload etc.) the activation of Fail-Safe mechanism is coupled with deactivation (switching off) of the RF Power Amplifier stages.

This additional feature inhibits the transmission if errors occur, thus preventing the transmission of erroneous datagrams or on false frequency

For details see the associated SFR description, and their interaction with the Fail-Safe Mechanism, as described in **Chapter 2.4.10**.

1.5.7 TESEUS - Configuration and Evaluation Tool

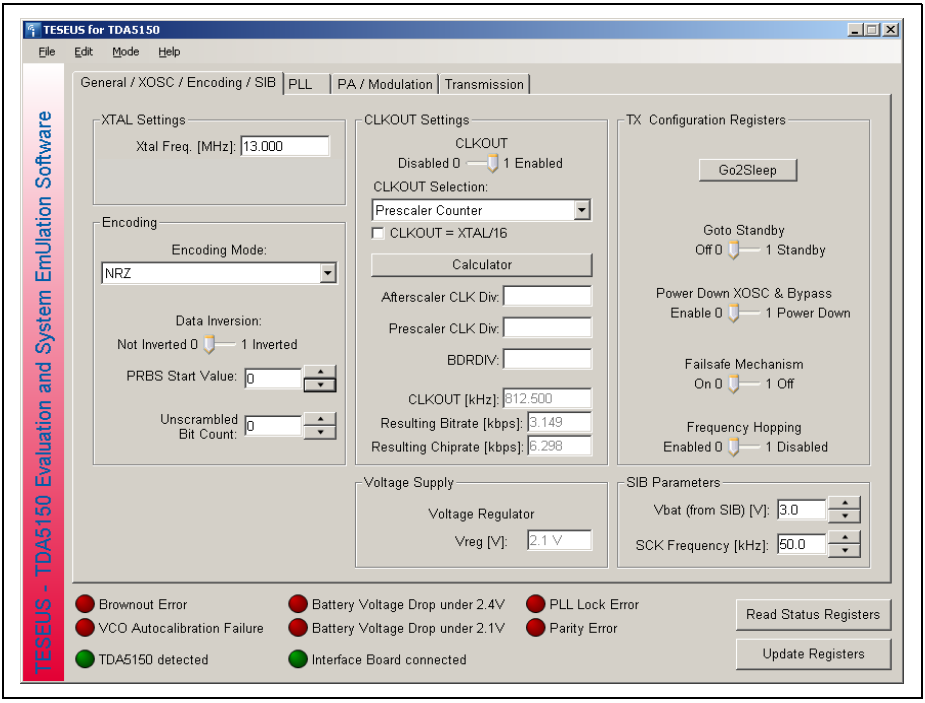


Figure 3 TESEUS - First Tab of User Interface screen

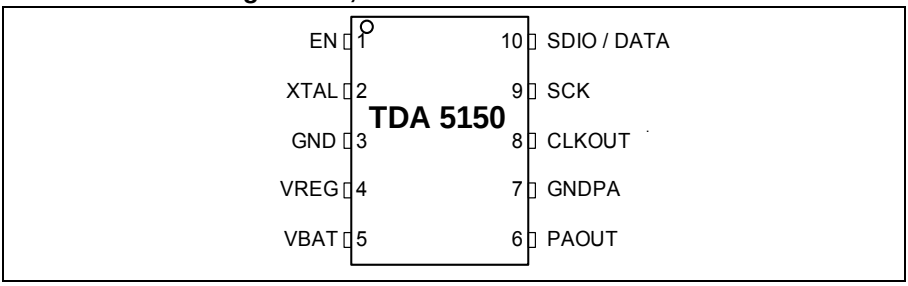
TESEUS is a user-friendly, comfortable tool, suitable for generation of TDA 5150 configurations and testing them using a TDA 5150 Evaluation Board. Configurations can be automatically converted into register lists and implemented in C-code.

The pattern to be transmitted is written into a datagram- or TX file. A commented example TX file can be generated by TESEUS. This file might be edited using a standard text file editor, if changes of the transmit parameters and data patterns are required.

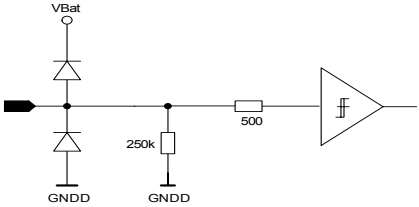
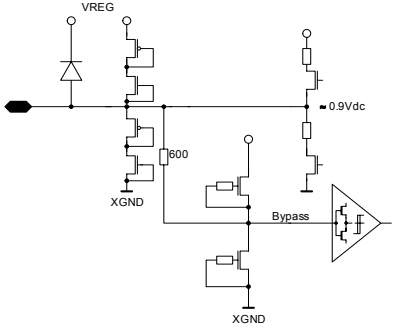
Note: for further details please consult the ***TESEUS User's Manual*** document.

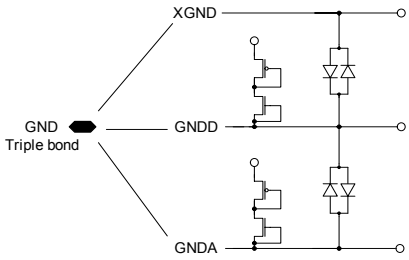
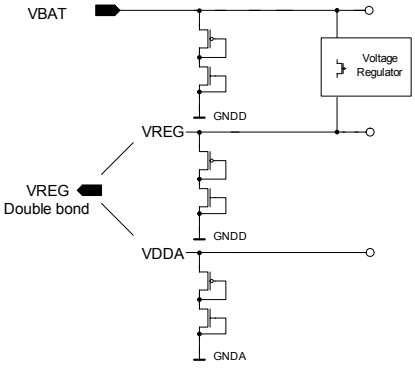
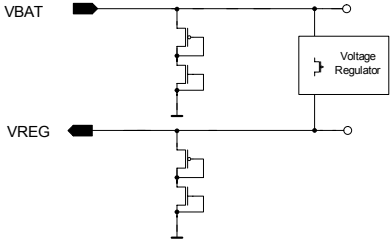
2 TDA 5150 Functional Description

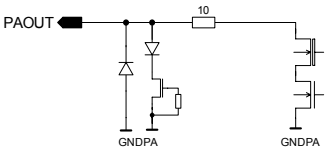
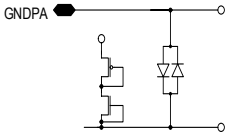
2.1 PIN Configuration, Pin-out

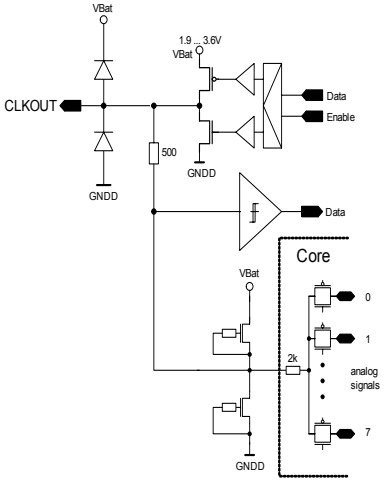


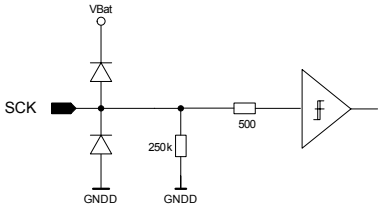
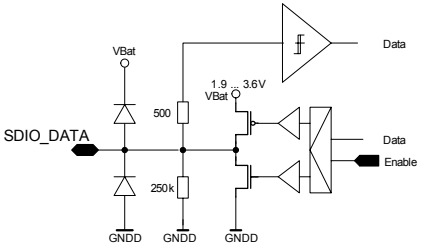
2.2 Pin Definition and Pin Functionality

Pin No.	Name	Pin Type	Equivalent I/O Schematic	Function
1	EN	Digital Input		Enable 3-wire bus
2	XTAL	Analog Input		Crystal Oscillator

Pin No.	Name	Pin Type	Equivalent I/O Schematic	Function
3	GND	Supply		Power supply ground
4	VREG	Analog Output		Voltage Regulator output
5	VBAT	Supply		Power supply (+)

Pin No.	Name	Pin Type	Equivalent I/O Schematic	Function
6	PAOUT	RF-PA Output		RF Power Amplifier Output (open drain)
7	GNDPA	Analog GND		RF Power Amplifier Ground return

Pin No.	Name	Pin Type	Equivalent I/O Schematic	Function
8	CLKOUT	Digital Output		Programmable Divided Clock

Pin No.	Name	Pin Type	Equivalent I/O Schematic	Function
9	SCK	Digital Input		Clock 3-wire bus
10	SDIO	Digital Input/ Output		Data 3-wire bus

2.3 Functional Block Diagram

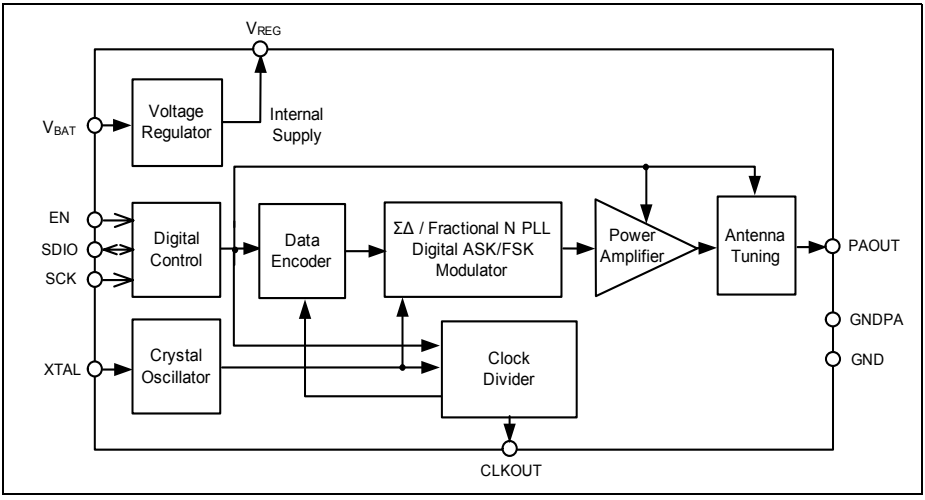


Figure 4 TDA 5150 Block Diagram

TDA 5150 is an SPI configurable fully integrated ASK/FSK/GFSK RF transmitter for the 300-320 MHz, 425-450 MHz and 863-928 MHz frequency bands. The input datastream, applied to the digital SDIO line is transposed and appears as modulated RF-signal, at the output of the integrated RF power amplifier. Signal encoding and spectrum is in accordance with the chosen modulation type (i.e ASK, FSK or GFSK) and encoding scheme.

TDA 5150 contains following major blocks which extend the functionality compared to legacy RF transmitters:

- An on-chip voltage regulator is delivering 2.1 V nominal supply voltage for the transmitter's functional units. In addition, the battery voltage is monitored and battery low and brown out flags are set, if a critical supply voltage drop event occurs.
- For avoidance of erroneous transmissions, the brownout flag is coupled with the RF Power Amplifier state control. If a brownout or critical voltage drop event occurs, the RF Power Amplifier is automatically switched off, as part of the Fail-Safe philosophy. The mechanism is explained in detail in **Chapter 2.4.8.5**
- The crystal oscillator and the associated clock divider(s) generate the required clock signals. There is an output line (CLKOUT) which may be used to clock a host µC, or for bit rate generation.
- A digital control logic, accessible for user via the SPI bus allows flexible and fast (re)configuration. At the same time it offers a simple but powerful Fail-Safe mechanism, which enhances the reliability of transmissions

- The data encoder synchronizes the bitstream to be transmitted with the internal bit clock. It supports different types of Manchester and Bi-Phase encodings and is able to generate PRBS9 pseudo-random patterns. The internal data encoder can be bypassed, allowing transmissions in direct (transparent) mode.
- The core element of the transmitter is the sigma-delta fractional-N PLL Synthesizer, used for carrier frequency control and as part of the digital modulator as well. It covers the frequency bands 300-320 MHz, 425-450 MHz and 863-928 MHz with outstanding frequency resolution. Only one, fixed frequency crystal (e.g. 13 MHz) is required for reference frequency generation. The synthesizer is characterized by short settling time. It is also used as direct FSK modulator, and together with a Gaussian filter, implemented by means of lookup table offers the functionality of a direct GFSK modulator.
- The integrated Power Amplifier is able to deliver up to +10dBm output power into a 50 Ω load (usually the antenna) via an external impedance matching network. In addition there are integrated capacitors, connected between GND and the RF-PA output, over SFR controlled on/off switches. These capacitors are elements of a software controlled antenna tuner. They may be used to fine-tune (adjust) the PA-output to Load matching network impedance, and thus to maintain good VSWR values over a wider frequency band. This is particularly useful if the transmitter is operated not only on a single frequency but in a given frequency band.

2.4 Functional Description

2.4.1 Special Function Registers

TDA 5150 is configurable by programming the Special Function Register bank (abbreviated SFRs) via the SPI interface.

Terminology and notations related to TDA5150 SFR set, list of symbols and programming restrictions are given in **Chapter 22 Register Terminology**.

Detailed description of SFR map, programming, usage and content explanations are found in the following chapters (§2.4.x.x and §2.5.x.x). See also **Chapter 2.5.1 SFR Register List**.

2.4.2 Power Supply Circuit

An internal **voltage regulator** generates a constant supply voltage (2.1V nominal) for most of the analog and digital blocks.

An external capacitor (100nF nominal value) connected between VREG (pin 4) and GND (pin 3) is necessary to guarantee stable functionality of the regulator.

The regulated voltage on VREG pin is not adjustable by user and it is not allowed to connect any additional, external loads to this pin, but the above mentioned decoupling capacitor.

In **STANDBY** state, a special, low-power voltage regulator is activated, which is supplying only the SPI bus interface, the SFR registers and the system controller.

In order to further reduce the current consumption, and keeping in mind that leakage currents can steeply increase by high temperatures, an additional low-power state, denoted **SLEEP** was defined. In this state most of the digital part is disconnected from the regulator (VREG). Only the SPI bus interface remains active. As a consequence, further power saving is achieved, but register content is lost by entering this mode.

See **Chapter 2.4.9 Operating Modes** for further informations.

2.4.2.1 Brownout Detector

A **Brownout Detector** (abbreviated **BOD**) is integrated into the TDA 5150 transmitter.

Brownout is a condition where the supply voltage drops below a certain threshold level. By brownout events the integrity of SFRs can not be guaranteed, even if the dropout's duration is very short.

During active states, BOD monitors the VREG pin; during **STANDBY**, it monitors VBAT and VREG supply lines.

Table 1 BOD Thresholds

Description		Monitored @	min	max
Brownout Detection Level—Active State	VBDR	VREG	1.7 V	1.8 V
Brownout Detection Level—StandBy State	VPDBR	VREG & VBAT	0.7 V	1.7 V

If the BOD detects a brownout, the Power Amplifier is switched off and the SFRs are reset. The device is then forced to restart from the Power Up Reset condition. This ensures that the device is always in a well-defined logic state.

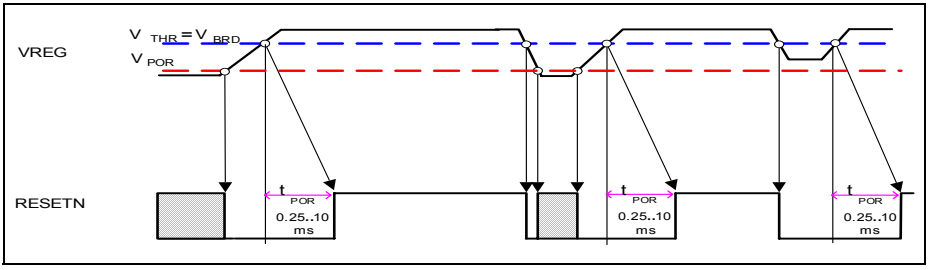


Figure 5 Power-on Reset/Brownout Detector

Brownout is indicated by bit BROUTERR (0x01.2) within SFR *TXTSTAT* (0x01).

Note: The BOD itself can not be used to guarantee the correct operation of analog sections, where the minimum operating voltage is defined to be 1.9 V; as this is larger than the maximum BOD voltage. In other words, in case of a supply voltage drop, the voltage region which is critical for reliable operation of the analog sections (min 1.9V) is reached before the brownout detector triggers (between 1.8..1.7V).

See also **Chapter 4.2** for operating voltage limits.

2.4.2.2 Low Battery Detector

TDA 5150 has an embedded **Low Battery Detector** (**LBD**) block. In active modes, **LBD** monitors the voltage on VBAT supply line (pin 5). **LBD** has two activation thresholds, set to 2.4 V and 2.1 V. The status regarding supply voltage below threshold events can be updated by reading from SFR *TXSTAT*, bits 4 and 5 (0x01.5:4). These LBD flags are cleared after every transmission start. The LBD might be used as early warning for low battery voltage state (but before the battery voltage is dropping below the critical value, which renders normal operation capability).

2.4.2.3 SFRs related to Supply Voltage monitoring

ADDR 0x01		TXSTAT—Transmitter Status Register					
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	n.u.	LBD_2V1	LBD_2V4	VAC_FAIL	BROUTERR	PARERR	PLLLDER
/	/	r/0	r/0	c/0	c/1	c/0	c/0

Bit 7	1		Set to 1, mandatory
Bit 5	LBD_2V1		battery low detected, threshold at 2.1 V -
Bit 4	LBD_2V4		battery low detected, threshold at 2.4 V
Bit 3	reserved		Don't care
Bit 2	BROUTERR		Brown out event
Bit 1	PARERR		Parity error
Bit 0	PLLLDER		PLL lock detector error

LBD_2V1	Battery voltage drop below 2.1 V detected if **1** - in standby mode, bit is invalid
LBD_2V4	Battery voltage drop below 2.4 V detected if **1** - in standby mode, bit is invalid
BROUTERR	Brownout event detected if **1**
PARERR	Parity error detected if **1**
PLLLDERR	PLL lock error detected if **1**

2.4.3 Digital Control (3-wire SPI Bus)

The control interface is a 3-wire Serial Peripheral Interface (SPI), which is used for device control and data transmission.

2.4.3.1 SPI Pin Description

- **EN - enable input** with embedded pull-down resistor. High level on EN input enables the SPI transmission. The rising edge of the EN signal triggers the selection of the active SCK edge (for the consequent data transfer, until the EN line goes again in low state) and transmission/ sampling of data between the device and the microcontroller can start. For details refer to **Figure 6** and **Figure 7**.
- **SDIO - 3-state input/output** This bidirectional line is used for data transfer between the TDA 5150 and external host (usually a µC). On-chip pull-down resistor is connected to this pin

- **SCK - clock input** pin with embedded pull-down resistor. If SCK is at low level while EN goes high, the incoming SDIO data is sampled by falling edge of the SCK and the output SDIO data is set by the rising edge of SCK. Contrariwise, If SCK is at high level when EN goes high, the SDIO data is sampled with the rising edge of the SCK clock and output on SDIO by falling edge of the SCK clock. For details refer to **Figure 6** and **Figure 7**.

SPI commands are started by the rising edge on the EN line and terminated by the falling edge on EN.

The available Burst Write mode allows configuration of several SFRs within one block access, without cycling the EN line Low - High - Low for each individual byte. By keeping the EN line at High level, subsequent bytes could be sent, and the byte address counter is autoincremented, thus speeding up the transfer on the SPI bus.

A self-explaining diagram is found here: **Chapter 9 Timing Diagrams of 3-wire SPI**.

The active edge of SCK (during SPI commands) is programmable, and it is determined by the level on SCK line at the moment of activation of the EN line (rising edge on EN).

If SCK is low at that moment, the incoming SDIO data will be sampled with the falling edge of SCK, and output by rising edge of SCK (see **Figure 6** below)..

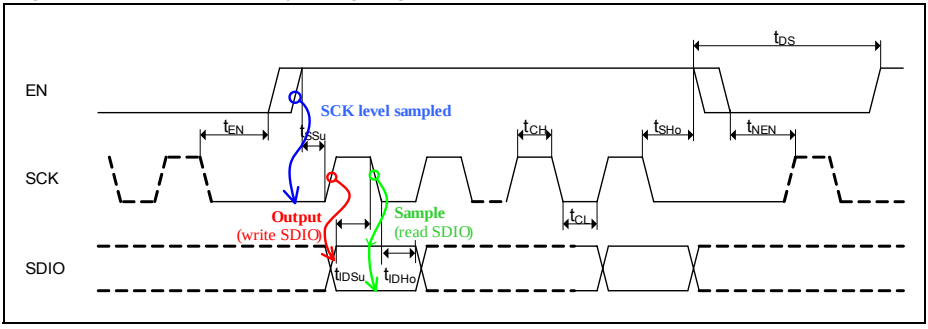


Figure 6 SPI Timing — SCK low at rising edge of EN

If SCK is high during occurrence of rising edge on EN, incoming SDIO data is sampled with the rising edge on SCK, and output by falling edge of SCK, as illustrated in **Figure 7**.

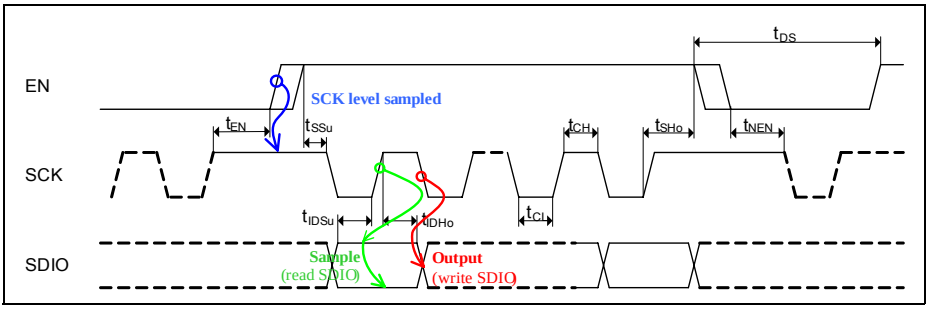


Figure 7 SPI Timing — SCK high at rising edge of EN

2.4.3.2 SPI XOR Checksum

The SPI block includes a safety feature for checksum calculation. This is achieved by means of XOR operation between the address and the data during write operation of SFR registers. The checksum is in fact the XOR of the data 8-bitwise after every 8 bits of the SPI write command. The calculated checksum value is then automatically written into SFR *SPICHKSUM* (0x00) and can be compared with the expected value.By executing a read operation of SFR *SPICHKSUM* (0x00) the register content is automatically cleared (after read). Read access to any of the other readable SFRs does not influence the SFR *SPICHKSUM*.

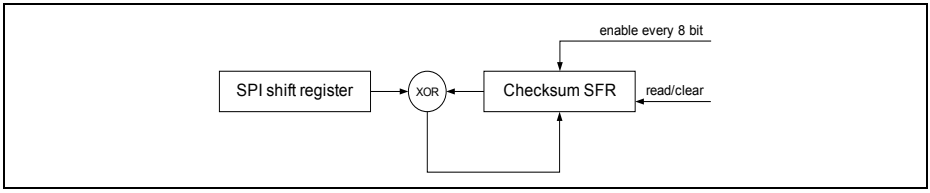


Figure 8 Generating the Checksum of SFRs, block diagram

Example:

Write to SFR address 0x04, data 0x02, address 0x05, data 0x01

Bytes transmitted via SPI	Result in Checksum Register
0000 0100	0000 0100
0000 0010	0000 0110
0000 0101	0000 0011
0000 0001	0000 0010

After writing into the registers, content of checksum SFR *SPICHKSUM* (0x00) will be 0x02.

2.4.3.3 Command Byte Structure

First byte of each SPI sequence is the **Command Byte**, with the following structure:

Function Code		Command Byte Configuration					
C1	C0	Address					
x	x	A5	A4	A3	A2	A1	A0

The first 2 bits **C1, C0** of the Command Byte are the function code field**.**

They define the command to be performed, according to the following table:

C1	C0	Function Code Configuration Bits
0	0	**Write** data into SFR register <A5:A0> field contains the SFR register's address There are 2 possible write modes (controlled by state of EN line): 1. write to a single address 2. burst mode write (with address auto increment)
0	1	**Read** data from SFR, <A5:A0> points to register address
1	0	**Reserved** (do not use)
1	1	**Transmit Command Byte** Bits <A5:A0>within this byte define the transmission parameters (see **Chapter 2.4.3.4 Transmit Command** for command fields).

The **Write / Read Command** bytes are used for device control. Bit fields <A5:A0> within **Command Byte** are used to specify the addressed SFR register.An overview and register map is given in **Chapter 2.5.1 SFR Register List**.

There are two ways to program the SFR registers:

1. by sending a Write command individually, for each register which should be written.
2. by sending a Burst Write command, which allows sequential programming.

Attention: Writing to address space beyond the valid SFR address range [0x04 - 0x27] is prohibited, and may lead to system malfunction.

2.4.3.4 Transmit Command

The **Transmit Command Byte** is used for **data transmission**. It precedes the datagram to be transmitted. The Transmit Command Byte format is described in the following table:

C1	C0	Transmit Command Configuration		
		Bit	**Function**	**Value, description**
1	1	A	Data sync	0: off 1: on (at the same time Bit C - Encoding must be set also to 1 -->int. Encoding)
1	1	B	PA mode	0: PA off at the falling edge of EN (synchronized with bit-rate if bit A is high) 1: SDIO/DATA is latched at the falling edge of EN, PA stays on, TX data are kept constant. After the time-out of 65536 / f_{sys} which is ~5 ms for a 13 MHz crystal, PA and PLL are switched off.
1	1	C	Encoding	0: off 1: on (selects SFR register for encoding Bit A must be also set to1 -->Data sync)
1	1	D	Pwr. level/ ModSetting	0: selects **PowerLevel/Modulation Setting1** 1: selects **Power Level/Modulation Setting2**
1	1	<E,F>	Frequency selection	0 (00): selects frequency channel **A** 1 (01): selects frequency channel **B** 2 (10): selects frequency channel **C** 3 (11): selects frequency channel **D** (for description of frequency channels **A**..**D** programming see **Chapter 2.4.11.3 Channel Hopping**)

Note: After the last configuration bit for a new transmission was sent, a break of at least 100 µs must be provided in order to achieve PLL settling and lock on the selected channel frequency.

2.4.3.5 Timing Diagrams

In the following timing diagrams the 4 possible SPI commands are shown. The examples are valid for the case of SCK is low when EN line goes from Low into High (rising edge).

Therefore the incoming SDIO data is sampled at the falling edge of SCK, and data is output on SDIO line by the rising edge of SCK signal.

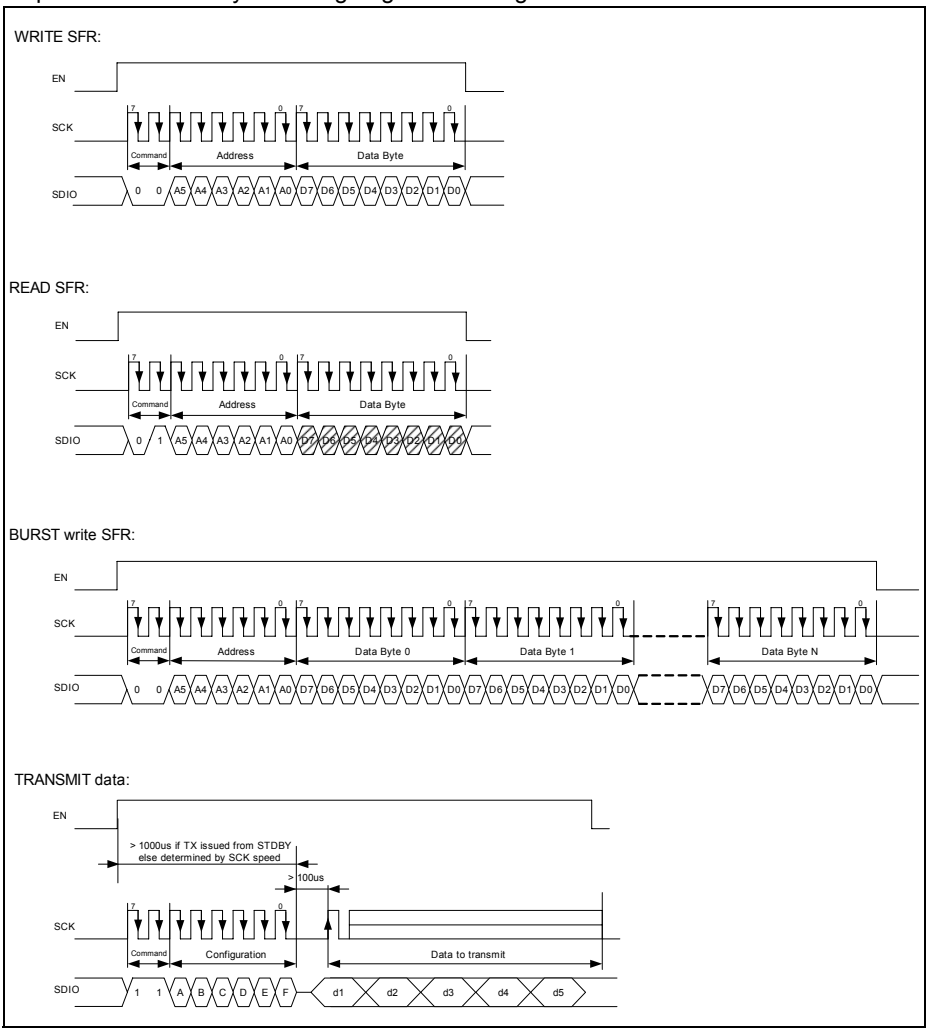


Figure 9 Timing Diagrams of 3-wire SPI

Note: In order to minimize cross-talk between SDIO and SCK lines, it is recommended to keep the SCK either Low or High, but avoid transitions during RF transmission.

Previous **Chapter 2.4.3.4 Transmit Command** gives an in-depth overview of Transmit Command structure.

2.4.4 Data Encoder

The **Data Encoder** is used in the so-called Synchronous Transmission Mode.

A description of this transmission mode is found in **Chapter 2.4.11.2 Synchronous Transmission**.

In Synchronous Transmission Mode the Encoder has to be used. If no specific encoding of SDIO data shall be done, select NRZ as encoding scheme.

Definition: ´bit-rate´ is the number of transmitted bits per second and expressed in [bits/sec]. Besides NRZ all the other implemented encoding methods split a single bit into two elementary parts, the so-called chips. Therefore we also talk about a chip-rate, which is an “n” multiple of the data-rate.

For NRZ (which means no extra encoding) n =1 (data-rate = chip-rate), and for all other implemented encoding methods n = 2, or the chip-rate is twice the bit-rate.

The TDA 5150 supports the following encoding types:

- Manchester code
- Differential Manchester code
- Bi-phase space code
- Bi-phase mark code
- Miller code (Delay modulation)
- NRZ
- Scrambling (PRBS9 generator)

All encoded bitstreams can be level inverted (as part of the encoding option)

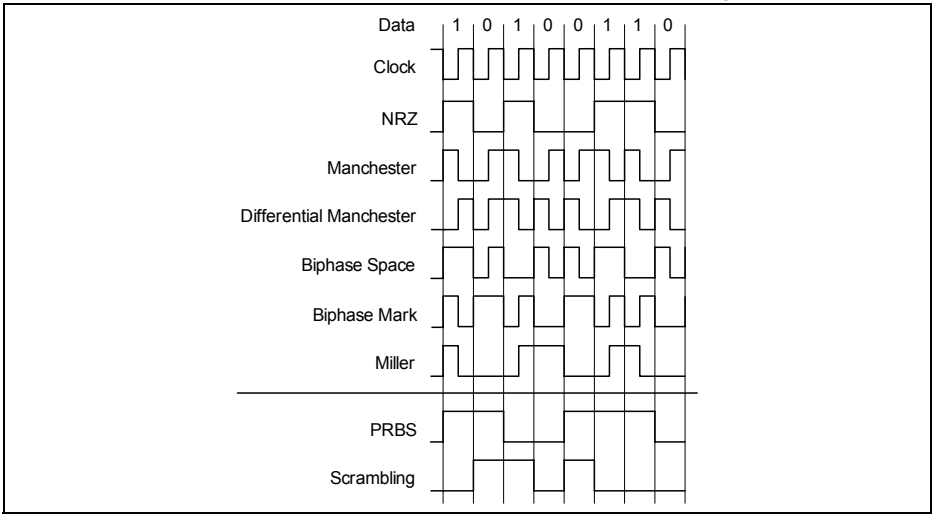


Figure 10 Coding Schemes

The Data Encoder option is enabled by bit C of Transmit Command (Data Encoder enabled if bit C=1). See also **Chapter 2.4.3.4 Transmit Command** for command structure. If the Data Encoder is enabled, bit A must to be set for Synchronous Transmission Mode as well (Bit A=1 and Bit C=1, this last to enable encoding).

The selection of encoding mode is done via bits ENCODE (0x05.2:0) of SFR *TXCFG1*. (0x05). At the same time bit INVERT (0x05.3) of the same SFR enables the inversion of an already encoded bit stream.

The encoding activation entry point can be configured in SFR *ENCCNT* (0x27).

By initializing the SFR *ENCCNT* (0x27) with 0x00, already the first bit is encoded. If for example ENCCNT = 0x10, the first 16 bits should remain unencoded. This method allows to keep the first N bits unencoded within a datagram (in fact plain NRZ), followed by encoded bits (of the same datagram).The encoding scheme is selected by bit-field ENCMODE (0x05.2:0) of SFR *TXCFG1*.

2.4.4.1 PRBS9 Generator, Data Scrambler

TDA 5150 contains a PRBS9 generator, suitable for generation of pseudo-random NRZ data patterns.The PRBS9 datastream satisfies (in general lines) the requirements for random distribution (even if longer PRBS polynomials come closer to “true” random distribution) and therefore it can be useful for Transmitter RF tests, for instance by measurement of the “Occupied RF Bandwidth”.

In addition the generated PRBS9 pattern can be XOR’ed with a real data pattern sent by the microcontroller and this way “scramble” this data pattern.

Attention: The data scrambling functionality is intended to enhance the clock recovery performance of the Receiver Station. It is not suitable, as stand-alone encryption method for security applications!

PRBS9 is a well known standard in the class of pseudo-random patterns, and is implemented within the TDA 5150 by a subpart with following block diagram:

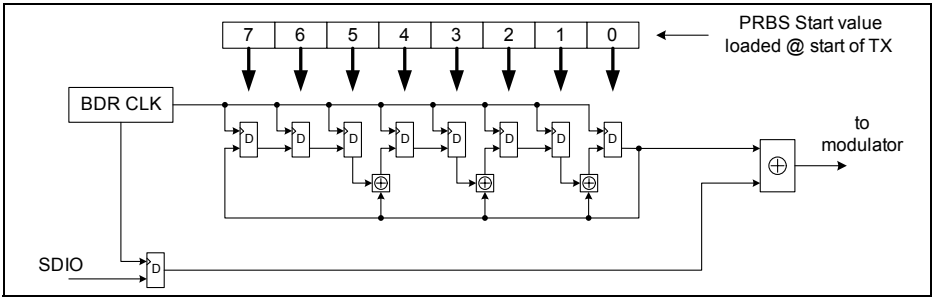


Figure 11 PRBS9 Generator and Data Scrambler

The feedback branches within the PRBS9 generator are fixed (as shown above), but the PRBS generation can be influenced by SFR configuration in the following manner:

- A start value for the PRBS9 Generator can be programmed in SFR *PRBS Start Value* (0x08). The reset value is 0xAB (10101011). Choice of 0x00 as start value is not allowed, because the output of PRBS9 Generator should “lock” and will never go in High. The PRBS Start Value is loaded into the PRBS9 Generator at the start of each transmission.
- If the Data Scrambler is used, the start of scrambling can be configured in SFR *ENCCNT* (0x27). If *ENCCNT* is 0, already the first bit is XOR’ed with PRBS9. If for example ENCCNT = 0x10, the first 16 bits stay unscrambled. This is necessary if a data frame should have always the same wake up and synchronization part, but the payload should be pseudo-random for sensitivity measurements or to enhance the clock recovery on the receiver side.

2.4.4.2 SFRs related to Transmitter Configuration and Data Encoding

ADDR 0x05	TXCFG1—Transmitter Configuration Register 1						
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
GO2SLEEP	ASKFSK2	ASKFSK1	ASKSLOPE	INVERT	ENCMODE	ENCMODE	ENCMODE
cw/0	w/0	w/1	w/0	w/0	w/1	w/0	w/1

Bit 3	INVERT		Data inversion
Bit <2:0>	ENCMODE		Encoding mode bit <2:0>

INVERT	Encoded data inversion enable				
	0: data not inverted			**1**: data inverted	
ENCMODE	Encoding mode, code selection (3 bits)				
	000: Manchester	**010**: Biphase Space	**100**: Miller (Delay)	**110**: Scrambling (PRBS)	
	001: Differential Manchester	**011**: Biphase Mark	**101**: NRZ	**111**: not used (data =0)	

ADDR 0x08	PRBS—PRBS Start Value						
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PRBS	PRBS	PRBS	PRBS	PRBS	PRBS	PRBS	PRBS
w/1	w/0	w/1	w/0	w/1	w/0	w/1	w/1

Bit <7:0>	PRBS		PRBS start value bit <7:0>

PRBS	PRBS start value (8 bits), the PRBS generator uses this value as a starting value after each transmission beginning

ADDR 0x27		ENCCNT - Encoding start bit counter					
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ENCCNT	ENCCNT	ENCCNT	ENCCNT	ENCCNT	ENCCNT	ENCCNT	ENCCNT
w/0	w/0	w/0	w/0	w/0	w/0	w/0	w/0
Bit <7:0>	ENCCNT			Encoding start bit counter bit <7:0>			
ENCCNT	Sets the number of bits on start of a telegram which shall be sent unencoded or unscrambled before encoder/scrambler is switched on. This feature is used e.g. for send of unscrambled synchronization patterns first, followed by encoded payload.						

2.4.5 Crystal Oscillator and Clock Divider

The Crystal Oscillator is a single pin, negative-impedance-converter type oscillator (**NIC**), and provides the reference frequency for the phase locked loop and clock signal for the sigma delta modulator.

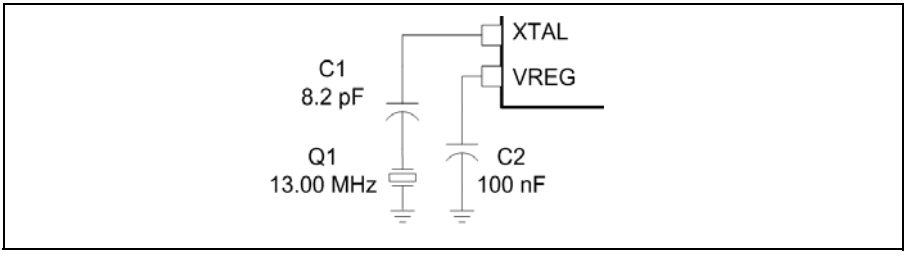


Figure 12 Oscillator Circuit

The allowed crystal frequencies are in [12..14] MHz range. A load capacitor (C1) is connected in series with the crystal. The value of the load capacitor depends on crystal parameters and - at some extent even the parasitic capacitance of the PCB layout has a slight, but measurable influence. The shown values are exemplifications, and valid for the crystal used on IFX evaluation board. Please refer also to the crystal oscillator parameters listed in **Chapter 4 Electrical Characteristics** to select a suitable crystal type.

Theoretically any crystal frequency, within the frequency range specified above, can be used. In practice this freedom is limited by the occurrence of so-called Fractional Spurs. (See also **Chapter 2.4.6.1 Fractional Spurs** for details). To avoid this unwanted effect,

the crystal frequency must be chosen in such way, that the division ratio:

PLL division factor = (RF carrier frequency) / (crystal frequency)

gives a fractional part (the part behind the decimal point) between 0.1 and 0.9.

For example a 13.56MHz crystal should not be used for 868MHz (resulting PLL division factor is 64.012 and the fractional part, equaling 0.012 is smaller then 0.1).

In addition the RF frequencies used for the FSK deviation must not cross the PLL division factor integer line (lower and higher FSK frequencies have different PLL division factors). This criterion is automatically fulfilled if and when the rule, stated above for the fractional part is fulfilled.

2.4.5.1 The Bit-Rate Generator

The TDA 5150 is able to generate a bit (or chip) clock by dividing the signal frequency output by the crystal oscillator.

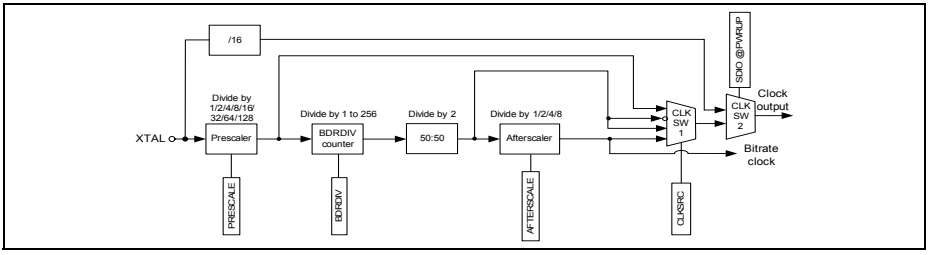


Figure 13 Bit-Rate Divider

In Asynchronous Transmission Mode the bitrate clock can be routed to CLKOUT pin and used by the µC as timer signal for bitrate generation.

In Synchronous Transmission Mode the bitrate clock is in addition used internally, for synchronization of the incoming bitstream.

The bitrate or chiprate is calculated according to the formula:

$$bitrate = \frac{f_{XOSC}}{PRESCALE \times (BDRDIV + 1) \times 2 \times AFTERSCALE}$$

2.4.5.2 The Clock Output

The TDA 5150 offers a **clock output** signal **(CLKOUT)**, derived from the crystal frequency. It can be used as source for system clock of a µC or as bit (chip) clock to control the data rate as already described.

Different stages of the bit-rate divider can be routed to CLKOUT, as well as the output of the XTAL / 16 divider according to following rules:

- If SDIO = 0 when EN goes High, the output clock chosen as XTAL/16 by default.

- If SDIO = 1 when EN goes High, the output clock is selected as imposed by settings of SFR *CLKOUTCFG* (0x06). This is the configurator register for Clock pre- and afterscaler. Detailed description of the bit-fields is given in next **Chapter 2.4.5.3 SFRs related to Crystal Oscillator and Clock Divide**

If enabled, the CLKOUT starts toggling when the swing amplitude on crystal oscillator output reaches a certain threshold.

If disabled, no clock signal is output on CLKOUT, but it delivers a rising edge pulse and stays high, signalizing that the crystal oscillator output already reached a stable level

*Note: If the CLKOUT line is used as system clock for a µC, keep in mind that in Synchronous Transmission Mode the delivered frequency is not highly stable in phase (it is affected by jitter), due to the fact that the related counters are synchronized with each Transmit Command. The reasons for it and the synchronization procedure itself are explained in **Chapter 2.4.11.2 Synchronous Transmission**.*

2.4.5.3 SFRs related to Crystal Oscillator and Clock Divide

r

ADDR 0x06		CLKOUTCFG - Clock Pre- and Post-scaler					
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CLKSRC	CLKSRC	AFTERSCAIE	AFTERSCALE	PRESCALE	PRESCALE	PRESCALE	CLKOUTENA
w/0	w/0	w/0	w/0	w/1	w/0	w/0	w/1

Bit <7:6>	CLKSRC		Clock source selection bit <1:0> 00: after prescaler, 01: after BRDIV counter 10: after BRDIV counter inverted, 11: after afterscaler
Bit <5:4>	AFTERSCALE		Afterscaler selection bit <1:0> divide by 2^AFTERSCALE
Bit <3:1>	PRESCALE		Prescaler selection bit <2:0> divide by 2^PRESCALE
Bit 0	CLKOUTENA		0 if CLKOUT disabled. In this case CLKOUT goes High after crystal oscillator achieves stable level 1 if clock output enabled

ADDR 0x07		BDRDIV—Bit-rate Divider					
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
BDRDIV	BDRDIV	BDRDIV	BDRDIV	BDRDIV	BDRDIV	BDRDIV	BDRDIV
w/1	w/0	w/0	w/0	w/0	w/0	w/0	w/0

Bit <7:0>	BDRDIV		BDRDIV divider bit <7:0>

2.4.6 Sigma-Delta fractional-N PLL Block

The **Sigma-Delta fractional-N PLL** contained on-chip is the core piece of the transmitter.

The advantage of a fractional-N PLL is that not only integer multiples of the crystal frequencies [N * f_{XTAL}] can be generated, but also values of N-multiples plus a fractional part.

Part of the PLL is a VCO (Voltage Controlled Oscillator) running at a center frequency of approximately 1.8 GHz. The VCO frequency is divided at first by 2 in a prescaler block with fixed division ratio. It is then further divided by 1, 2 or 3 in the band select divider block, the resulting frequency equaling the transmitter's RF output frequency.

This RF signal is then further divided in a multimodulus divider block down to a frequency which is in same range as those of the reference signal's, input from the reference oscillator (i.e the crystal oscillator).

The reference oscillator's frequency and the VCO's subdivided frequency, input from multimodulus divider are compared in a phase detector. On the output of the phase detector an error signal, proportional to the phase difference of the two, above mentioned signals is obtained. The phase-error signal is converted to a bipolar current by the charge pump and then fed into the loop filter (integrator).

The output of this integrator controls the VCO frequency via the tuning voltage and so closing the loop.

The multimodulus divider is able to switch between different dividing factors. Thus it is possible e.g. to divide by 2.5 by first dividing by 2, than by 3, followed by 2 again, and so on. The dividing factor is defined by the Sigma-Delta Modulator.

2.4.6.1 Fractional Spurs

Due to the behavior of Sigma-Delta PLLs, spurs are generated at frequencies close to the integer multiples of the reference frequency. These spurs are named **Fractional Spurs**. It is therefore recommended to use PLL division ratios (output RF frequency divided by crystal oscillator frequency) with fractional parts between 0.1 and 0.9, or in other words, the crystal frequency should be chosen in such way to yield for fractional part of the PLL division ratio values between 0.1 and 0.9.

2.4.6.2 Voltage Controlled Oscillator (VCO)

The Voltage Controlled Oscillator runs at approximately 1.8 GHz. This is 2, 4, or 6 times the desired RF output frequency, dependent on the frequency band settings.

To trim out production tolerances of the VCO, a VCO Auto Calibration mechanism (VAC) is implemented and runs automatically during each start up of the PLL. First a fixed, internal voltage is applied to the VCO, and the generated RF frequency is divided by 4 (or 8 for 868/915 MHz bands). The positive transitions are then counted during 32 system clock cycles. The result is compared to a configured number, derived from the desired RF frequency value (as the formula shows). The VCO is then automatically fine-tuned, before an RF transmission starts.

$$VAC\_CTR<8:0> = \frac{PLLINT<6:0> + \frac{PLLFRAC<20:0>+0.5}{2^{21}-0.5}}{(ISMB<1>+1)\times 4} \times VAC\_NXOSC<5:0>$$

where:

- VAC_CTR<8:0> has to be calculated according the formula above. It contains the optimal number of positive transitions to which the VAC-counter result is compared.

- PLLINT <6:0> and PLLFRAC <20:0> PLL divider SFRs used to define the desired RF frequency.
- ISMB<1> MSB of SFR register ISMB<1:0>, for band selection.
- VAC_NXOSC<5:0> always set to 32 decimal or 0x20, number of elapsed system clocks time (duration) used for VAC counting.

2.4.6.3 Loop Filter Bandwidth

In order to provide a high grade of flexibility by choice of modulation parameters, a PLL with programable bandwidth have been implemented in the TDA5150.

The damping resistor(s), part of the active Loop Filter in PLL can be selected by means of a 3 bit control field designated PLLBWTRIM in the SFR register *PLLBW* (0x25.6:4).

Aiming the minima of RF-energy leaking into the adjacent channel(s) and/or out of band transmissions, the PLL bandwidth should be set as narrow as possible, but not less then 1.5.. 2 times the chip rate, if FSK or GFSK modulation is used.

For NRZ encoding the chip rate and data- or bit rate are the same. For all other coding schemes like Manchester or Bi-Phase etc. each bit is represented by two chips. Therefore the chip rate is the double of the bit rate for all encoding schemes, implemented in the TDA5150 encoder, excepting NRZ.

The chip rate is not influenced by the fact whether the encoding is done by the on-chip Data Encoder or is realized externally.

In order to maintain loop stability within the PLL and for optimum performance, following chargepump settings should be used, correlated with loop filter damping:

Table 2 PLL recommended settings

Loop filter damping resistor selection			Chargepump settings and resulting current					Resulting nominal PLL BW	Notes
PLLBW TRIM			**CPTRIM**				CP_current	[kHz]	
Bit2	Bit1	Bit0	Bit3	Bit2	Bit1	Bit0	[uA]		
0	0	0	*	*	*	*	*	*	not recommended
0	0	1	1	1	1	1	40	410	
0	1	0	1	1	0	0	32.5	375	
0	1	1	1	0	0	1	25	335	
1	0	0	0	1	1	0	17.5	270	
1	0	1	0	1	0	0	12.5	230	
1	1	0	0	0	1	0	7.5	175	
1	1	1	0	0	0	1	5	150	

2.4.6.4 PLL Dividers, RF Carrier Frequency

The divider chain contains a fixed divider by 2 (prescaler), a band select divider, dividing by 1 for the 915 and 868 MHz bands, by 2 for the 434 MHz band, and by 3 for the 315 MHz band. The divider ratio of this block is controlled by the field SMB0/1 of SFR *TXCFG0* (0x04.3:2).This band selection block is followed by the Multi-Modulus Divider, which is controlled by the Sigma-Delta Modulator. The RF frequency is set in the PLL Integer and PLL Fractional SFRs. Up to 4 different frequencies may be preconfigured in the same band (Frequency Registers A, B, C, D) and finally the active channel selected through the Transmit Command. This allows fast channel switching or hopping, without the need of downloading the complete reconfiguration dataset into the corresponding SFRs (i.e the new PLL settings).

The RF frequency f_{RF} is derived from the crystal frequency.

$$f_{RF} = f_{XOSC} \times \left(PLLINT<6:0> + \frac{PLLFRAC<20:0> + \mathbf{0.5}}{2^{21} - \mathbf{0.5}} \right)$$

For the **315 MHz** and **433 MHz** bands (ISMB<1> = 0) PLLINT bit 6 is not used and only values from 15 to 43 are valid.

For the **868 MHz** and **915 MHz** bands (ISMB<1> = 1) all PLLINT bits are used and values between 54 and 84 are valid.

2.4.6.5 SFRs related to Sigma-Delta fractional-N PLL Block

ADDR 0x04		**TXCFG0—Transmitter Configuration Register 0**					
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
GO2STDBY	reserved	reserved	FSOFF	ISMB	ISMB	reserved	reserved
cw/0	w/0	w/0	w/0	w/0	w/1	w/1	w/0
Bit 7	GO2STDBY	**1:** activate STANDBY					
Bit 6	FSOFF	**1:** activate FAILSAFE					
Bit <3:2>	ISMB			RF frequency band bits			
ISMB		ISM band selection (2-bits)					
		00: MHz 300-320	**01**: MHz 425-450	**10**: MHz 863-870	**11**: MHz 902-928		

ADDR 0x09, 0x0D, 0x11, 0x15	PLLINT*n*—PLL MM Integer Value Channel A, B, C, D *n*: Channel A, B, C, D

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
n.u.	PLLINT*n*	PLLINT*n*	PLLINT*n*	PLLINT*n*	PLLINT*n*	PLLINT*n*	PLLINT*n*
/	w/1	w/0	w/0	w/0	w/0	w/0	w/0

Bit <6:0>	PLLINT*n*		Integer division ratio bit <6:0>

PLLINT*n*	Multi-modulus divider integer offset value (7 bits) for Channel **A**, **B**, **C**, and **D**

ADDR 0x0A, 0x0E, 0x12, 0x16	PLLFRAC*n*0—PLL Fractional Division Ratio *n*: Channel A, B, C, D (byte 0)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PLLFRAC*n*0	PLLFRAC*n*0	PLLFRAC*n*0	PLLFRAC*n*0	PLLFRAC*n*0	PLLFRAC*n*0	PLLFRAC*n*0	PLLFRAC*n*0
w/0	w/0	w/0	w/0	w/0	w/0	w/0	w/0

Bit <7:0>	PLLFRAC*n*0		Fractional division ratio bit <7:0>

PLLFRAC*n*0	Synthesizer channel frequency value (21 bits, bits < 7:0 >), Fractional division ratio for Channel **A**, **B**, **C**, and **D**

ADDR 0x0B, 0x0F, 0x13, 0x17	PLLFRAC*n*1—PLL Fractional Division Ratio *n*: Channel A, B, C, D (byte 1)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PLLFRAC*n*1	PLLFRAC*n*1	PLLFRAC*n*1	PLLFRAC*n*1	PLLFRAC*n*1	PLLFRAC*n*1	PLLFRAC*n*1	PLLFRAC*n*1
w/0	w/0	w/0	w/0	w/0	w/0	w/0	w/0

Bit <7:0>	PLLFRAC*n*1		Fractional division ratio bit <15:8>

PLLFRAC*n*1	Synthesizer channel frequency value (21 bits, bits < 15:8 >), fractional division ratio for Channel **A**, **B**, **C**, and **D**

ADDR 0x0C, 0x10, 0x14, 0x18		PLLFRAC*n*2—PLL Fractional Division Ratio *n*: Channel A, B, C, D (byte 2)					
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
n.u.	n.u.	reserved	PLLFRAC*n*2	PLLFRAC*n*2	PLLFRAC*n*2	PLLFRAC*n*2	PLLFRAC*n*2
/	/	w/0	w/1	w/0	w/0	w/0	w/0

Bit 5	reserved		Set always to 0
Bit <4:0>	PLLFRAC*n*2		Fractional division ratio bit <20:16>

PLLFRAC*n*2	Synthesizer channel frequency value (21 bits, bits < 20:16 >), fractional division ratio for Channel **A**, **B**, **C**, and **D**

2.4.7 Digital FSK/GFSK Modulator

The TDA 5150 uses an integrated **direct FSK Modulator** for generation of RF-signals. By this method, and assuming NRZ data encoding, a positive frequency deviation (relative to nominal carrier frequency) occurs for a logical "1" of the already encoded data, and a negative frequency deviation for a logical "0" if the data inversion bit INVERT in SFR *TXCFG1* (0x05.3) is 0 (inversion OFF).

If the inversion function is active (INVERT bit is set to 1), the frequency shift directions are inverted (i.e. negative frequency deviation for logical "1" of input data and positive deviation for “0”) for the same NRZ data stream.

*Note: if an encoding scheme other then NRZ is choosen, then data bits are decomposed in elementary chips, as shown in **Figure 10** and above two statements regarding input data inversion state (on/off) versus frequency shift direction are true, but apply instead of input data bit, to the resulting chips.*

The two frequencies, corresponding to positive and negative frequency shift are directly associated with specific divider numbers.

The modulation is achieved by switching between these two divider numbers and it takes effect under the control of data signal state (and encoding scheme, if other then NRZ).

The above described (divider ratio switching) method is called direct FSK modulation.

With direct FSK modulation a well controlled frequency shift can be achieved and the pullability of the crystal in the reference frequency oscillator circuit is no issue anymore, like by the classical FSK, where usually a reactance does “pull” the crystal frequency.

Also a data shaping is realized in digital domain, as Gaussian filtered FSK (GFSK) and can be enabled by setting the GFBYP bit of SFR *GFXOSC* (0x1E.3) to 0.

The GFSK modulation can further reduce the occupied RF bandwidth versus FSK modulation.

The ASK or FSK modulation type is selected by a bit-field in SFR *TXCFG1* (0x05). There are two possible setups, denoted **ModulationSetting1**, and **ModulationSetting2**. A field within **Transmit Command** Byte (referenced as bit D in **Transmit Command** byte) selects one of the two settings as active. This allows for fast commutation between modulation parameters without additional (re)configuration and repeated register downloads. See also **Chapter 2.4.3.4 Transmit Command** for details.

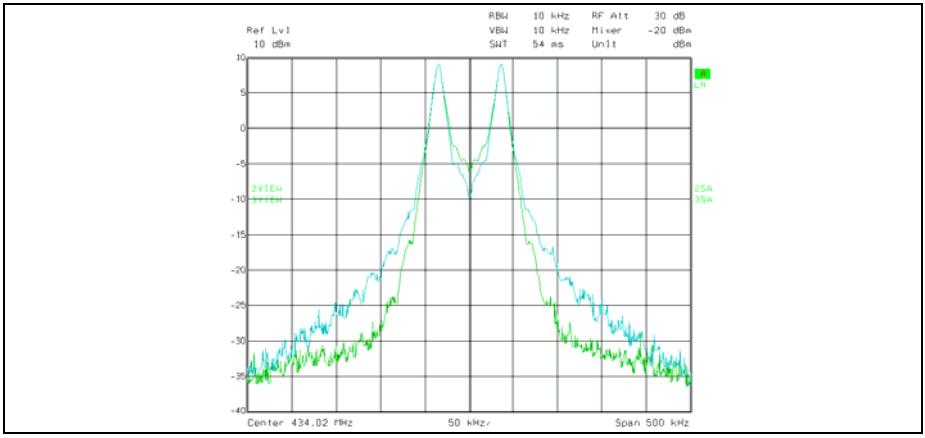


Figure 14 Spectrum for FSK and Gaussian FSK (GFSK) modulated RF-signals, both with 20 kbit/s datarate and ± 35 kHz FSK deviation. Blue plot corresponds to FSK and green plot to GFSK modulation.

The **frequency deviation** is configured using the bits FDEF<4:0> and FDEVSCALE<2:0> in the SFR *FDEV*(0x1C.7:0) and is calculated as follows:

$$\Delta f_{RF} = f_{XOSC} \times \frac{190 \times FDEV<4:0> \times \frac{2^{FDEVSCALE<2:0>}}{64} + 0.5}{2^{21} - 0.5}$$

Note that the FSK deviation is referenced to the center frequency. This means, that the spacing between the two FSK frequencies, is twice the FSK deviation.

The pulse-shaping Gaussian Filter used for GFSK can be disabled if regular FSK is used. In ASK mode the filter is always switched off. For ASK mode a power-sloping mechanism is available and described in detail in **Chapter 2.4.8 Power Amplifier, ASK Modulator**.

The Gaussian shaping is defined as a number of fixed frequency steps (transitions) between the 2 FSK frequencies, corresponding to Low and High, or 0 and 1 on the modulator input. It is understood that the steps are counted over one edge of the data chip. Ideally these 16 steps are distributed over the complete data chip length, which means there are 16 gaussian filter steps per chip or N_{GF} = 16. Selecting N_{GF} > 16 will reduce the shaping effect and selecting N_{GF} < 16 will cause a reduction of signal information, with minimal positive effect on the obtained RF spectrum.

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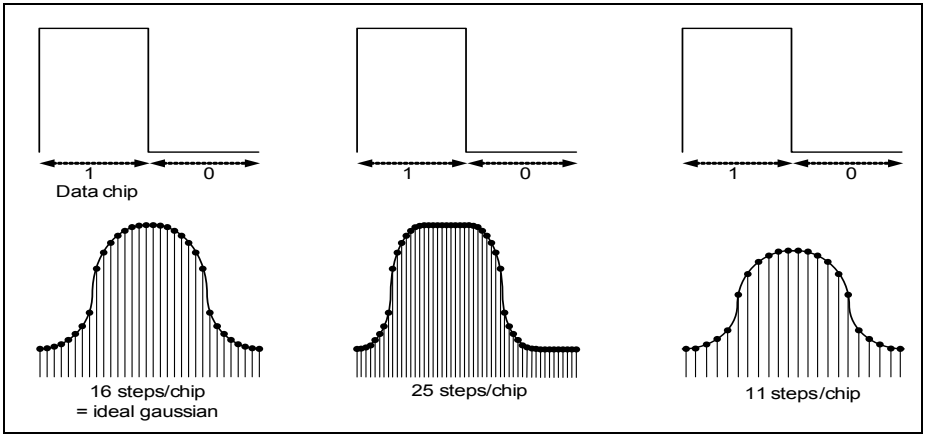

Figure 15 Influence of the Gaussian Divider on Data Shaping

The content of GFDIV is calculated as follows:

$$GFDIV = \frac{f_{XOSC}}{chiprate \times N_{GF}} - 1$$

It is recommended to program the **GFDIV** register in such way, that the GF divider **NGF** is 16 times the chip-rate. This allows optimum Gaussian filtering.

2.4.7.1 SFRs related to digital FSK / GFSK Modulator

ADDR 0x1C	FDEV—Frequency Deviation						
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
FDEVSCALE	FDEVSCALE	FDEVSCALE	FDEV	FDEV	FDEV	FDEV	FDEV
w/1	w/1	w/0	w/1	w/1	w/1	w/1	w/1

Bit <7:5>	FDEVSCALE		Frequency deviation scaling bit <2:0>
Bit <4:0>	FDEV		Frequency deviation bit <4:0>

FDEVSCALE	Scaling of the frequency deviation (3 bits)				
	000: divide by 64	**001**: divide by 32	**010**: divide by 16	**011**: divide by 8	
	100: divide by 4	**101**: divide by 2	**110**: divide by 1	**111**: multiply by2	
FDEV	Frequency deviation value (5 bits), defines the multiplication value for the output data from the Gaussian filter (0-31)				

ADDR 0x1D	GFDIV—Gaussian Filter Divider Value						
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
GFDIV	GFDIV	GFDIV	GFDIV	GFDIV	GFDIV	GFDIV	GFDIV
w/0	w/0	w/0	w/0	w/1	w/0	w/0	w/0

Bit <7:0>	GFDIV		Gaussian filter divider bit <7:0>

GFDIV	Gaussian filter clock divider value (11 bits, bits < 7:0 >), defines the sampling ratio of the Gaussian filter; typically this value is set such that the GF divider N_{GF} is 16 x chip-rate (for ideal Gaussian filtering) **Note:** bits < 10:8> are contained in **GFXOSC** register **ADDR(0x1E)**

ADDR 0x1E		GFXOSC—Gaussian Filter Configuration					
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
FHBLANK	reserved	reserved	reserved	GFBYP	GFDIV	GFDIV	GFDIV
w/0	w/1	w/1	w/1	w/1	w/0	w/0	w/0

Bit 7	FHBLANK						
Bit 3	GFBYP			Gaussian filter bypass			
Bit <2:0>	GFDIV			Gaussian filter divider bit <10:8>			

FHBLANK	Frequency Hopping disable (defines the jump from the TX_TIMEOUT state)		
	0: enable (jump to TX_ON state) **1**: disable (jump to PLL_ON state)		
GFBYP	Gaussian filter bypass: **0**: GF enabled **1**: GF bypassed		
GFDIV		Gaussian filter clock divider value (11 bits, bits < 10:8 >), defines the sampling ratio of the Gaussian filter, typically this value is set such that the GF divider is 16 x chip-rate (for ideal Gaussian filtering) **Note:** bits < 7:0> are contained in **GFDIV** register **ADDR(0x1D)**	

2.4.8 Power Amplifier, ASK Modulator

The RF signal, generated by VCO and under the control of the Sigma-Delta fractional-N PLL is fed to a group of class-C Power Amplifier stages, before being transmitted. The Power Amplifier (PA) includes an output power control, ASK sloping, switchable capacitors for antenna fine tuning and an auto switch -off mechanism, as part of the Fail-Safe system. If critical supply voltage or frequency error events occur, the Fail-Safe mechanism switches off the PA, thus preventing erroneous transmissions...

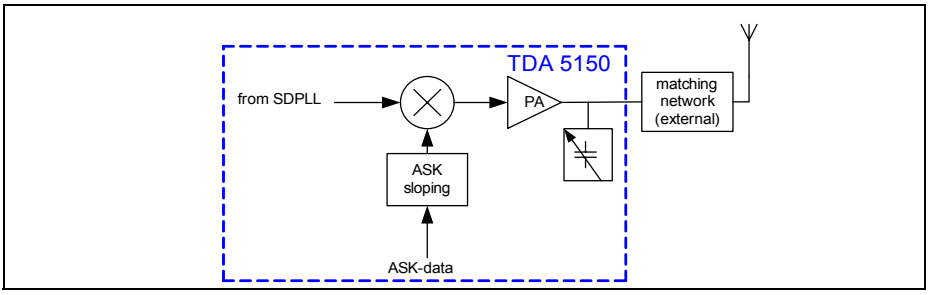

Figure 16 Transmitter Blocks

In FSK or GFSK mode, the PA is always ON during the transmission's duration.
By ASK mode, the SDPLL delivers a continuous RF signal to the PA. The PA is switched ON and OFF, according the data signal to be transmitted. Additionally there is an ASK sloping mechanism, which switches the different power stages ON (and OFF) in a well determined sequence, correlated with the transitions on data signal line. This power ramping procedure minimizes out-of band transients and spectral splatter.

2.4.8.1 PA Output Power Programming

The PA comprises 11 elementary cells in parallel. Each one is a class-C amplifier.

The cells are grouped in three PA blocks.

PA Block 0 is composed of 9 stages, PA Block 1 and PA Block 2 are strong single stages. Each PA Block can be individually enabled and disabled to optimize power consumption and efficiency in an output power subrange. The overall 11 PA stages allow control of the RF output power in 11 steps over a range of 20 dB. The PA can be switched OFF by disabling all the 11 stages.

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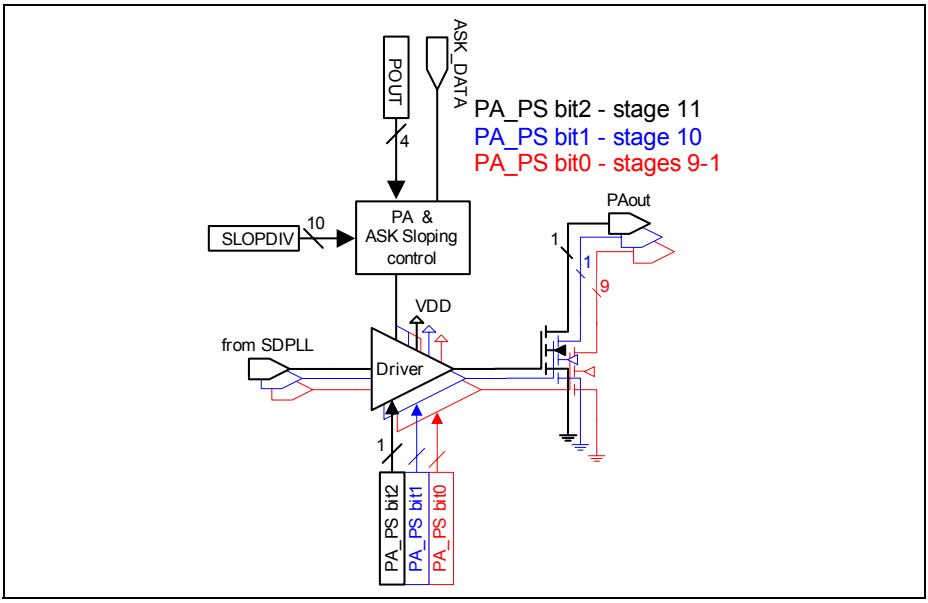

Figure 17 PA Core with Output Power Control

Two independent PA power level settings can be configured. With the Transmit Command the PA power level is selected together with the modulation setting. This means, either power level 1 AND modulation type 1 or power level 2 AND modulation type 2 are selected, according to Modulation Setting 1 or Modulation Setting 2 field in Transmit Configuration byte.

The 3 PA Blocks are enabled by PA_PS1 and PA_PS2 bits within SFR *POWCFG0* (0x1A). The bits PA_PS1 do enable the PA blocks for power level 1 and bits PA_PS2 are used for power level 2.

Enabling the 3 PA Blocks offers following typical PA ranges (note that the PA output power depends also on the external matching circuit, at a quite large extent):

- PA_PS bit0=1: 5dBm matched; Pout = +5dBm down to -10dBm, 9 PA Stages
- PA_PS bit1=1: 8dBm matched; Pout = +8dBm down to -10dBm, 10 PA Stages
- PA_PS bit2=1:10dBm matched; Pout = +10dBm down to -10dBm, 11 PA Stages

In addition to enabling the PA Blocks, the 11 PA stages have to be configured. This is achieved by setting the bit-fields POUT1 (0x1B.3:0) for power level 1 and POUT2 (0x1B.7:4) for power level 2 in SFR *POWCFG1* (0x1B) (POUTn=0 means that the PA is effectively OFF).

The output impedance of the PA depends on the number of PA stages used. The external antenna matching must be done for the impedance related to the highest number of used PA stages, or in other words, for the use-case of highest RF output power.If the desired output power is +10dBm for instance, the antenna should be matched for the case of all the11 PA Stages active. In the same way, if the output power requirement is for +5dBm, the antenna should be matched assuming that 9 PA Stages are used and active. Supposed the matching network have been set up for the PA impedance bound to +10dBm output power (all 11 PA Stages active), it is reasonable to expect some degree of mismatch and efficiency loss by operation in +5dBm RF power mode.

2.4.8.2 ASK Modulation and ASK Sloping

The ASK or FSK modulation is selected by SFR *TXCFG1* (0x05). There are two possible setups, designated **ModulationSetting1**, and **ModulationSetting2**. The bit D of Transmit Command Byte selects the active setting. This allows switching between the two modulation setups, without any further register configuration. See also

Chapter 2.4.3.4 Transmit Command

ASK modulation is realized by switching the PA Stages ON and OFF in accordance with data signal to be transmitted.

On-chip ASK Sloping capability is provided within TDA 5150. This means that instead of switching all PA Stages at the same time, they are switched ON one after the other in a configurable time sequence.The power sloping is controlled by SFR SLOPDIV (0x19.7:0).

The register content is equal with the number of reference oscillator cycles elapsed until the next PA stage is switched ON or OFF.

Note: For optimum shaping effect, it is recommended to match the number of sloping steps to the required maximum output power and consequently to the maximum number of stages which might be used.

2.4.8.3 Duty Cycle Control

The control of Duty Cycle leads to control of the averaged RF output power (by changing the conductive angle of the power amplifier) and contributes to further reduction of the current consumption. It is worth to be noted, that the decreasing conduction angle values lead to decrease of power consumption, but due to the short and high-amplitude current pulses the level of RF harmonics (on $n*f_{carrier}$ frequencies) tends to rise.

Proper measures (filtering) must be taken to maintain harmonics level rejection.

If Duty Cycle control option is enabled, nominal values of 27%, 33%, 39% and 44% can be programmed. If disabled, the default value of 50% applies for Duty Cycle.

The Duty Cycle Control is accessible through the bits DCCCONF (0x1F.5:4) of SFR *ANTTDCC* (0x1F).See **Chapter DCCCONF** for details.

In the 315 MHz band the DCCCONF and DCCDISABLE bits are ignored and the optimized (and predefined) value of 33% Duty Cycle is superimposed

2.4.8.4 Antenna Tuning

A block of 4 switchable capacitors is paralleled with the PA output. The Antenna Tuning option can be useful for fine-tuning the PA to Load matching network, and thus to obtain a better antenna performance in a wider frequency band. This feature is useful by multichannel applications, for maintaining antenna matching close to the optimum. The tuning capacitors can be switched ON / OFF individually and the control of the switches is implemented in SFR *TUNETOP* (0x1F).

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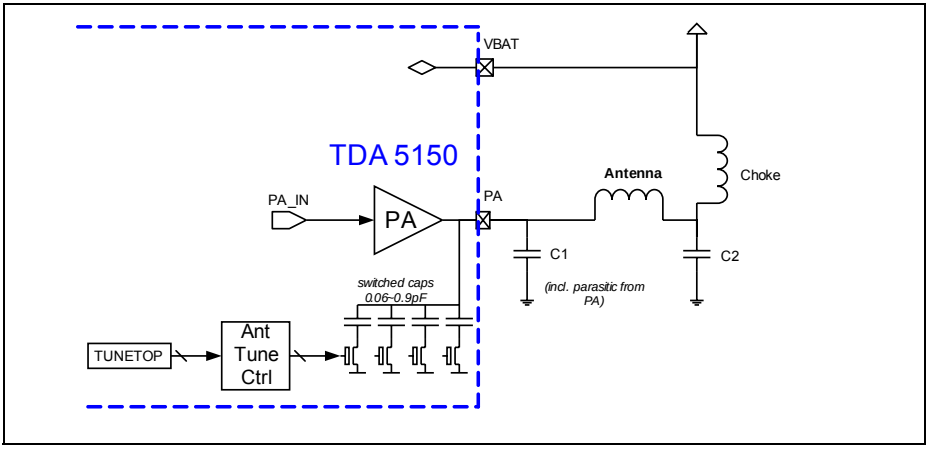

Figure 18 PA Antenna Tuning and Matching

The 4 switched capacitors have different values of typically 60 fF, 120 fF, 240 fF and 480 fF, giving an overall maximum capacitance of about 0.9 pF.

Note: Due to the low Q Factor of the switched capacitors at the higher frequencies, the device´s current consumption tends to increase when this feature is used in the 868 MHz and 915 MHz frequency bands.

2.4.8.5 Fail-Safe PA Switch Off

To prevent erroneous transmissions (on wrong frequency or with erroneous modulation parameters, altered payload etc.) the activation of Fail-Safe mechanism is coupled with deactivation (switching off) of the RF Power Amplifier stages. If critical errors occur, the Fail-Safe mechanism incorporated in the TDA5150 is activated, provided the detection enable bit is armed (i.e. bit FSOFF in SFR *TXCFG0* (0x04.4) is 0).

Observe that this corresponds to the after-reset state. In other words, by exiting the reset state, the Fail-Safe detection is already armed, but it can be deactivated anytime by changing its control bit state to High (bit FSOFF=1 (0x04.4)) or rearmed, by setting it to Low.

If the detection is armed, RF Power Amplifier drivers are automatically switched OFF in case of an error, to prevent erroneous transmissions.

This happens if at least one of the following events occurs:

- Parity error in the SFRs
- Brownout event (event sensed by the brown-out detector BOD)
- PLL lock failure is detected (event sensed by the lock detector LD)

If the detection is disabled, the error flags in *Transmitter Status Register* (0x01) still keep track of error status (i.e. they are set, if an error occurs) but the RF Power Amplifier is not switched off by the error flag(s) set condition (i.e. the RF-PA continues to transmit despite error until the transmission is terminated as a normal, error-free one).

Refer to *Transmitter Status Register* (0x01) description and Fail-Safe Flags, explained in next **Chapter 2.4.8.6 SFRs related to RF Power Amplifier and ASK Modulator**.

2.4.8.6 SFRs related to RF Power Amplifier and ASK Modulator

ADDR 0x04	TXCFG0—Transmitter Configuration Register 0						
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
GO2STDBY	reserved	reserved	FSOFF	ISMB	ISMB	reserved	reserved
cw/0	w/0	w/0	w/0	w/0	w/1	w/1	w/0
Bit 4	FSOFF		Fail-Safe mechanism: 0 enabled, 1 turned off				

ADDR 0x05	TXCFG1—Transmitter Configuration Register 1						
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
GO2SLEEP	ASKFSK2	ASKFSK1	ASKSLOPE	INVERT	ENCMODE	ENCMODE	ENCMODE
cw/0	w/0	w/1	w/0	w/0	w/1	w/0	w/1
Bit 4	ASKSLOPE		ASK sloping: 0 disable, 1 enable				

ADDR 0x19	SLOPEDIV —ASK Sloping Clock Divider						
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SLOPEDIV	SLOPEDIV	SLOPEDIV	SLOPEDIV	SLOPEDIV	SLOPEDIV	SLOPEDIV	SLOPEDIV
w/1	w/0	w/0	w/0	w/0	w/0	w/0	w/0
Bit <7:0>	SLOPEDIV		ASK sloping clock divider bit <7:0>				
SLOPEDIV	ASK sloping clock division ratio (10 bits, bits < 7:0 >), defines the timing of the ASK signal shaping using PA power stage switching						
	Range:		from **0x000**: SLOPEDIV = 1		to **0x3FF**: SLOPEDIV = 1024		

ADDR 0x1A	POWCFG0—PA Output Power Configuration Register 0						
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PA_PS2	PA_PS2	PA_PS2	PA_PS1	PA_PS1	PA_PS1	SLOPEDIV	SLOPEDIV
w/0	w/0	w/0	w/0	w/0	w/0	w/0	w/0

Bit <7:5>	PA_PS2		PA output blocks setting 2 bit <2:0>
Bit <4:2>	PA_PS1		PA output blocks setting 1 bit <2:0>
Bit <1:0>	SLOPEDIV		ASK sloping clock divider bit <9:8>

PA_PS2	Individual control of the 3 PA blocks, setting 2 (3-bits)					
	0: disabled	**1**: enabled	Bit(0) ==> PA block 0	Bit(1) ==> PA block 1	Bit(2) ==> PA block 2	
PA_PS1	Individual control of the 3 PA blocks, setting 1(3-bits)					
	0: disabled	**1**: enabled	Bit(0) ==> PA block 0	Bit(1) ==> PA block 1	Bit(2) ==> PA block 2	
SLOPEDIV	ASK sloping clock division ratio (10 bits, bits < 9:8 >), defines the frequency of the ASK signal shaping using PA power stage switching					
	Range:		from **0x000**: SLOPEDIV = 1		to **0x3FF**: SLOPEDIV = 1024	

ADDR 0x1B	POWCFG1—PA Output Power Configuration Register 1						
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
POUT2	POUT2	POUT2	POUT2	POUT1	POUT1	POUT1	POUT1
w/0	w/0	w/0	w/0	w/0	w/0	w/0	w/0

Bit <7:4>	POUT2		Output power setting 2 bit <3:0>
Bit <3:0>	POUT1		Output power setting 1 bit <3:0>

POUT2	PA output power setting 2 (4 bits), defines the number of enabled PA stages		
	Range:	from **0x0**: POUT2 = 0	to **0xB**: POUT2 = 11 > **0xB**: POUT2 = 11
POUT1	PA output power setting 1 (4 bits), defines the number of enabled PA stages		
	Range:	from **0x0**: POUT1 = 0	to **0xB**: POUT1 = 11 > **0xB**: POUT1 = 11

ADDR 0x1F			ANTTDCC—Antenna Tuning and Duty Cycle Configurations				
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
reserved	DCC DISABLE	DCCCONF	DCCCONF	TUNETOP	TUNETOP	TUNETOP	TUNETOP
w/0	w/0	w/1	w/0	w/0	w/0	w/0	w/0

Bit 7	reserved		Always use 0
Bit 6	DCCDISABLE		Duty cycle control disable
Bit <5:4>	DCCCONF		Duty cycle control delay configuration bit <1:0>
Bit 3:0	TUNETOP		Antenna tuning top capacitor bit <3:0>

DCCDISABLE	Duty cycle control disable (must be 0 for ISMB=0)					
	0 enabled			1 disabled (delay = 0ps)		
DCCCONF	Duty cycle control delay configuration (ISMB = 1/2/3, for ISMB = 0 => delay = 0 ps)					
	00: 43% (69/35/33 ps)	01: 39% (207/104/98 ps)	10: 35% (346/173/164 ps)	11: 31% (484/242/230 ps)		
TUNETOP	Antenna tuning top capacitor selection (4-bits):					
	Individual switch of capacitor banks		**0**: switched off		**1**: switched on	
	Bit(0) ==> 60 fF	Bit(1) ==> 120 fF	Bit(2) ==> 240 fF	Bit(3) ==> 480 fF		

2.4.9 Operating Modes

TDA 5150 has 3 main operating modes: **SLEEP**, **STANDBY**, **TRANSMIT** and 2 temporary modes: **XOSC_ENABLE** and **PLL_ENABLE**.

2.4.9.1 SLEEP Mode

SLEEP is the lowest power consumption mode. Most of the internal blocks, excepting the SPI interface are powered down and consequently the content of SFRs is going lost. Therefore the SFR bank requires a full reprogramming after exiting SLEEP mode.

The SPI interface stays active and is supplied via the Low Power Voltage Regulator while in SLEEP mode.

The SPI interface is able to detect bus non-idle conditions and it will wake up the transmitter if the EN pin is taken high and at least 3 pulses are applied to SCK pin.

Observe that this last wakeup condition is automatically fulfilled during communication over the transmitter's SPI-bus, assuming a standard, SPI-bus protocol is used.

SLEEP mode is entered:

- after a GO2SLEEP command execution, i.e by taking the EN pin to Low preceded by setting of the GO2SLEEP bit in SFR *TXCFG1* (0x05.7) to 1. This bit will be cleared automatically on WAKEUP (i.e. on exiting the SLEEP state). There is a small latency after the trailing edge of signal on EN pin (of 2 f_{sys} cycles) the time taken to close down internal blocks.

SLEEP mode is left if the EN line is set to High level and there is clock activity (at least 3 pulses) on the SCK line. The conjunction of these 2 conditions will wake up the transmitter and thus SLEEP Mode will be exited.

In SLEEP mode:

- Only the low power voltage regulator is ON
- Only the SPI interface is powered
- POR is ON
- BOD is in low power mode (inaccurate threshold)
- All other blocks are OFF.
- Power supply for digital core and SFR data is disconnected. As a consequence, SFR register content is lost.

2.4.9.2 STANDBY Mode (Data Retention Mode)

STANDBY is a low power mode, but with higher consumption as SLEEP mode, due to the fact that the SFRs are still supplied in this mode.

STANDBY is entered:

- whenever the EN line is low (no SPI communication), and the time-out count of 65536/ f_{sys} periods have been elapsed
- after a GO2STANDBY command execution (setting the GO2STANDBY bit in SFR *TXCFG0* (0x04.7) followed by taking the EN pin to Low (EN=0).

In STANDBY Mode:

- Only the low power voltage regulator is ON
- SPI, SFR container, and System Controller are supplied - data can be read into and from the chip.
- POR is ON
- BOD is in low-power mode (inaccurate threshold)
- Data consistency of SFR container is monitored by means of parity bits

All other blocks are OFF.

2.4.9.3 TRANSMIT Mode

This mode is automatically entered during a transmit command. PLL and PA are active i this mode. TRANSMIT is left, with the falling edge of the EN line, when bit B in the Transmit Command is 0. Otherwise TDA 5150 remains in the transmit mode with PA and PLL in ON state, until the time-out of 65536 / f_{sys} occurs (around ~5 ms for a 13 MHz reference clock).

- Normal voltage regulator is ON
- POR is ON
- BOD is ON
- XOSC is ON
- PLL is ON
- PA is ON

2.4.9.4 XOSC_ENABLE Mode

This is a temporary mode after power up, entered whenever SLEEP or STANDBY mode is left (by a rising edge of the EN line). This mode is automatically entered while SFRs are programmed. XOSC_ENABLE is left by GO2SLEEP, GO2STANDBY commands, by the ~5 ms time-out to enter automatically STANDBY, or by a transmit command.

- Normal voltage regulator is ON
- POR is ON
- BOD is ON
- XOSC is ON
- Clock divider is ON
- PLL and PA are OFF

2.4.9.5 PLL_ENABLE Mode

This is a temporary mode during a transmit command, when the PLL is already activated, but the PA is not switched ON yet.

- Normal voltage regulator is ON
- POR is ON
- BOD is ON
- XOSC is ON
- PLL is ON, PA is OFF

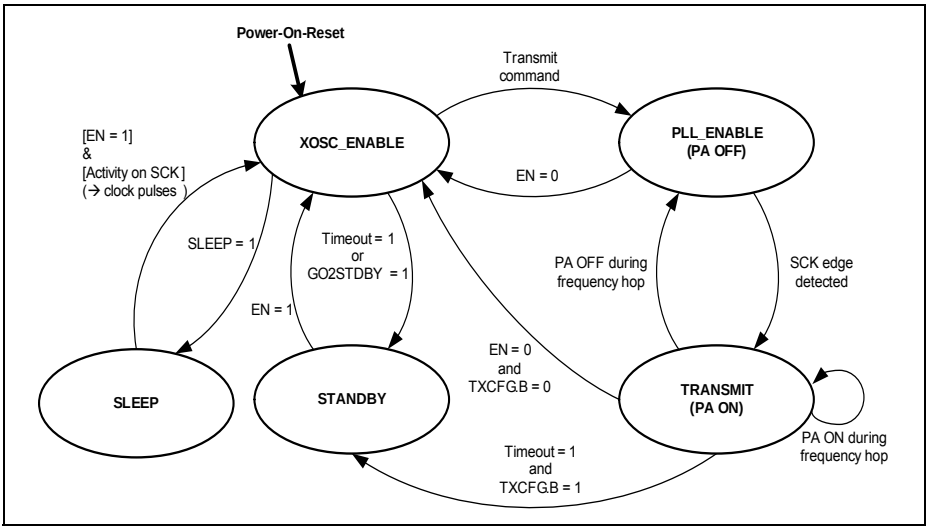

Figure 19 Simplified State Diagram of the TDA 5150

2.4.9.6 SFRs related to Operating Modes

ADDR 0x04		TXCFG0—Transmitter Configuration Register 0					
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
GO2STDBY	reserved	reserved	FSOFF	ISMB	ISMB	reserved	reserved
cw/0	w/0	w/0	w/0	w/0	w/1	w/1	w/0
Bit 7	GO2STDBY		**1:** go to StandBy, (cleared after 1 is written)				

ADDR 0x05		TXCFG1—Transmitter Configuration Register 1					
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
GO2SLEEP	ASKFSK2	ASKFSK1	ASKSLOPE	INVERT	ENCMODE	ENCMODE	ENCMODE
cw/0	w/0	w/1	w/0	w/0	w/1	w/0	w/1
Bit 7	GO2SLEEP		**1:** go to Sleep **Note:** after execution of this command all SFR content is lost				

2.4.10 Fail-Safe Mechanism and Status Register

2.4.10.1 Fail-Safe Flags

The status of the TDA 5150 is continuously monitored during active state. The integrated Fail-Safe mechanism includes:

- Brownout Error—generates an internal reset, whenever the voltage drops below the specific threshold. The brownout error flag is set, to allow recognition of a brownout event.The flag can be red via SPI bus.
- Parity Error— There is a single parity bit for each SFR register, which is updated each time the SFR register is written. Following this update, the parity for each register is calculated and checked against this bit continuously. If there is a mismatch in any of the registers, the error flag is set. The content of all SFRs is monitored and the parity checked even during **STANDBY** state.
- PLL Lock Error—is monitored after the transmission start. If the PLL loses the phase-locked state during transmission, the related flag is set.

The Fail-Safe status of the chip is stored and available via the SFR *Transmitter Status Register* (0x01).If a failure condition occurs, a flag is set and latched via previously mentioned SFR.Even if the condition which led to the event occurrence is no longer true, the “set” state of the Fail-Safe bits is kept, and cleared only by the Transmitter Status Register read operation. See also **Chapter 2.5.2** for detailed SFR register map.

Preservation of above described Fail-Safe Flag bits in SFR Transmitter Status Register provides a feedback to user about the failure root cause - if any error occurred.

If the Transmit Fail-Safe mechanism FSOFF in SFR *TXCFG0* (0x04) is enabled (set to 1) and one of the Fail-Safe flags is set, the PA is disabled thus preventing further transmission.

It is highly recommended to read the SFR *Transmitter Status Register* (0x01) before- and after a transmission (clear error flags, if any and check for error-free transmission).

2.4.10.2 Low Battery Monitor

The low-battery detector monitors the supply voltage on Pin 5 (VBAT). If the voltage drops below 2.4 V, a corresponding flag is set and the threshold is switched automatically to 2.1 V. If this new threshold is also reached due to further voltage drop, the 2.1 V flag bit is set in addition to the 2.4 V flag. These Fail-Safe flags are automatically cleared after each transmission start, and content is not preserved like for Brownout Error, Parity Error and PLL Lock Error bits.

Summary:

- LBD_2V4 set if battery voltage drops below 2.4 V
- LBD_2V1 set if battery voltage drops below 2.1 V

2.4.10.3 SFRs related to Supply Voltage monitoring

ADDR 0x01		TXSTAT—Transmitter Status Register					
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	n.u.	LBD_2V1	LBD_2V4	VAC_FAIL	BROUTERR	PARERR	PLLLDER
/	/	r/0	r/0	c/0	c/1	c/0	c/0

Bit 7	1		Set to 1, mandatory
Bit 5	LBD_2V1		Low battery detected at 2.1 V -
Bit 4	LBD_2V4		Low battery detected at 2.4 V
Bit 3	reserved		Don’t care
Bit 2	BROUTERR		Brown out event
Bit 1	PARERR		Parity error
Bit 0	PLLLDER		PLL lock detector error

LBD_2V1	Battery voltage drop below 2.1 V detected if **1** - in standby mode, bit is invalid
LBD_2V4	Battery voltage drop below 2.4 V detected if **1** - in standby mode, bit is invalid
BROUTERR	Brownout event detected if **1**
PARERR	Parity error detected if **1**
PLLLDERR	PLL lock error detected if **1**

2.4.11 RF Data Transmission

The procedure of RF Transmission starts by rising the EN line (pin 1) high. STANDBY or SLEEP Mode are exited, and the crystal oscillator started. The crystal oscillator requires maximum 1 ms to start up. During this time the TDA 5150 can be already reconfigured, because the SPI block does not require the system clock. Before transmission the *Transmitter Status Register* (0x01) should be read (to clear bits set by previous errors, if any). Every transmission starts with the Transmit Command:

C1	C0	Transmit Command Configuration		
		Bit	**Function**	**Value, description**
1	1	A	Data sync	0: off 1: on (at the same time Bit C - Encoding must be set also to 1 -->int. Encoding)
1	1	B	PA mode	0: PA off at the falling edge of EN (synchronized with bit-rate if bit A is high) 1: SDIO/DATA is latched at the falling edge of EN, PA stays on, TX data are kept constant. After the time-out of 65536 / f_{sys} which is ~5 ms for a 13 MHz crystal, PA and PLL are switched off.
1	1	C	Encoding	0: off 1: on (selects SFR register for encoding Bit A must be also set to1 -->Data sync)
1	1	D	Pwr. level/ ModSetting	0: selects **PowerLevel/Modulation Setting1** 1: selects **Power Level/Modulation Setting2**
1	1	<E,F>	Frequency selection	0 (00): selects frequency channel **A** 1 (01): selects frequency channel **B** 2 (10): selects frequency channel **C** 3 (11): selects frequency channel **D** (for description of frequency channels **A**..**D** programming see **Chapter 2.4.11.3 Channel Hopping**)

The Transmit Command byte is sent via SPI, and identified by the first two bits, designated C0 and C1. These two bits are mandatory set to1.

The following 6 bits, designated bit A.. bit F, specify the transmission details.

- A: Synchronous (1) or asynchronous (0) transmission, details are described later in this chapter.

- B: If 0, the PA is switched off by the falling edge of the EN line. If 1, the SDIO line is latched with the falling edge of EN, the PA stays active, continuing to transmit according to the latched SDIO state. After a time-out duration of 65536 / f_{sys} (~5 ms for a 13 MHz reference clock), both the PA and PLL are switched off if no other SPI command starts a new transmission. This feature helps to keep the transmitter sending, despite the fact that the EN line is pulled to Low state, normally a stop condition for Transmitter. Pulling the EN line to (Low) in between SPI command blocks is required by SPI protocol, if commands are not sent in burst mode.
- C: If C=0, the Encoder is not used. If C=1, the Encoder is used as configured in the *Transmitter Configuration Register 1,* bits ENCMODE (0x05.2:0).
- D: Switch between two subsets of transmission parameters, referenced as **PowerLevel/Modulation Setting *n***. Each subset contains 3 bit-fields for control of:
  - modulation type (ASK or FSK)
  - RF-PA block activation (3 blocks are available, may be switched ON/OFF individually)
  - RF-PA output power

– Modulation type (ASK or FSK) is controlled by bit-field ASKFSK1:2 (0x05.6:5) of the SFR *Transmitter Configuration Register 1* (0x05). The modulation type selection is done individually for each of the two transmission settings (steered by bit D=0 or D=1), with choice between ASK and FSK modulation. The settings are not coupled, i.e one could be set for ASK modulation and the other for FSK for example. Further, if FSK is chosen as modulation type, enabling of Gaussian filtering is another option - but not mandatory. See also **Chapter 2.4.4.2 SFRs related to Transmitter Configuration and Data Encoding**.

– RF-PA block activation, controlled by bit-fields PA_PS1 (0x1A.4:2) respectively PA_PS2 (0x1A.7:5) of the SFR *Output Power Configuration Register 0*, (0x1A) for the two transmission settings

– RF-PA output power selection, controlled by the bit-fields POUT1 (0x1B.3:0) respectively POUT2 (0x1B.7:4) of the SFR *Output Power Configuration Register 1*, (0x1B) for the two transmission settings

– If D=0, following fields are selected: [ASKFSK1, together with PA_PS1 and POUT1]. If D=1, following fields are selected: [ASKFSK2, together with PA_PS2 and POUT2].

- E, F RF Frequency selection as configured in PLL MM Integer Value registers A/B/C/D (0x09/0x0D/0x11/0x15) and the PLL Fractional Division Ratio registers A/B/C/D (0x0A:0x0C/0x0E:0x10/0x12:0x14/0x16:0x18.

After the transmit command have been sent, the SCLK line has to stay low for at least 100 µs (i.e settling time of the PLL). A rising edge of the SCLK line after this brake activates the PA and starts the transmission. The digital data is input into the transmitter via the SDIO line and transposed into modulated RF signal, without regard on the state of SCLK line (which could be Low or High).

To keep crosstalk between SCLK and SDIO at minimum level, it is recommended to keep SCLK at a steady level, instead of toggling it (usually by the uC).

2.4.11.1 Asynchronous Transmission

In Asynchronous Transmission Mode (also referred as Transparent Mode), the data on SDIO is directly input into modulator and converted into RF carrier.There is no internal synchronization with the bit-rate clock.The CLKOUT programmed to the proper bit-rate (or a multiple of it) may be used by the host to time and shift (into SDIO line) the bits to be transmitted.

The Encoder and Scrambler can not be used and are automatically bypassed.

It is not recommended to use GFSK in conjunction with Asynchronous Transmission Mode, as the frequency steps are timed with 1/16 of the bit-rate (chip-rate) clock. Timing differences between the internal bit-rate clock and the µC may cause unwanted jitter in the transmission. GFSK modulation is intended to be used in conjunction with Synchronous Transmission Mode.

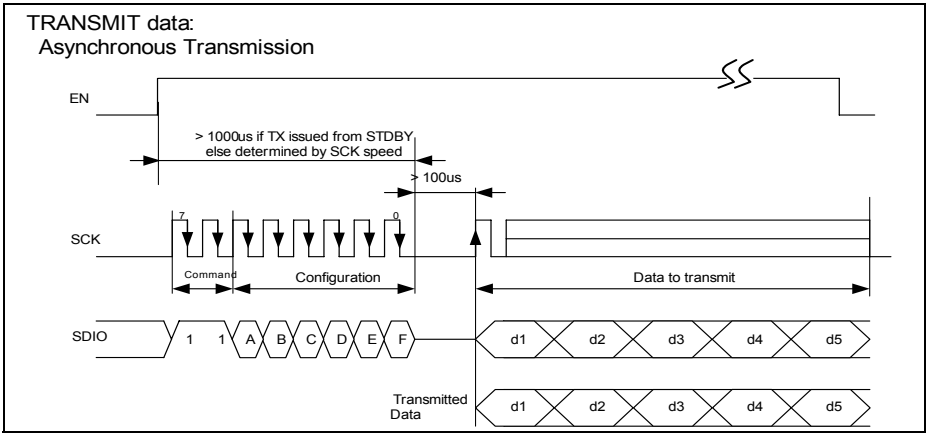

Figure 20 Asynchronous Transmission

Setting the EN line (pin 1) to low terminates the RF-transmission.

2.4.11.2 Synchronous Transmission

In the Synchronous Transmission Mode the transmit data is latched with the falling edge of the internal bit clock, and thus synchronized. The bit clock at the CLKOUT has to be used by the µC to time the bits which are transmitted, e.g. on interrupt basis.

The Encoder has to be enabled. If the bits shall not be encoded, select NRZ as generic Encoder scheme. See **Chapter 2.4.4 Data Encoder**.

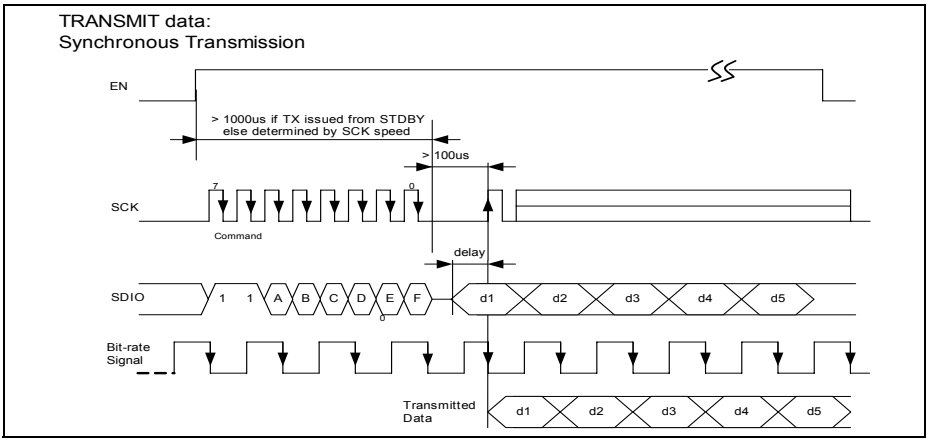

Figure 21 Synchronous Transmission

Synchronous transmission is the recommended user mode. Encoding can be used, this mode is preferred for GFSK. At the same time SW implementation is easier, because the setting of the next data bit on SDIO is triggered by interrupt (CLKOUT line) and timing inacuracies e.g. caused by interrupt reaction latency are compensated / neutralized by the synchronization.

2.4.11.3 Channel Hopping

TDA 5150 offers the possibility for usage of up to 4 preconfigured RF channels, called A, B, C, and D frequency channels. The preconfiguration assumes proper programming PLL's Multi-Modulus Integer Value registers A/B/C/D (0x09/0x0D/0x11/0x15) and the PLL Fractional Division Ratio registers A/B/C/D (0x0A:0x0C/0x0E:0x10/0x12:0x14/0x16:0x18. Bit-filed <E:F> in Transmit Command is used for frequency channel selection. Thus it is possible to quickly switch between RF frequency channels, without reconfiguration (assuming channels A...D have been preconfigured in advance).

Any frequency hop inside the band requires a new Transmit Command and100 µs idle time for the PLL to perform the VCO Auto Calibration and to settle (achieve locked state).

For frequency hops to frequencies not more than 1 MHz apart from the frequency on which the VCO Auto Calibration was performed, it is possible to skip the VCO Auto Calibration and thus to reduce the PLL settling time to 20µs instead of 100µs. In this case it is allowed to start the transmission, triggered by a rising edge on the SCK line, by waiting for only 20 µs after the Transmit Command was completed.

The VCO Auto Calibration can be skipped by setting the bit FHBLANK (0x1E.7) in SFR *GFXOSC* (0x1E) to 1.

There should be no more than 4 consecutive jumps without VCO Auto Calibration during transmissions.

If bit B of the Transmit Command is set, the PA will stay active, until the time-out condition is reached (i.e. for a duration of 65536 / f_{sys} corresponding to ~5 ms for a 13 MHz reference clock)

2.4.11.4 SFRs related to Channel Hopping

ADDR 0x1E		**GFXOSC—Gaussian Filter Configuration**					
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
FHBLANK	reserved	reserved	reserved	GFBYP	GFDIV	GFDIV	GFDIV
w/0	w/1	w/1	w/1	w/1	w/0	w/0	w/0

Bit 7	FHBLANK		Frequency Hopping VAC Disable

FHBLANK	Frequency Hopping, enable/disable VCO Auto Calibration for Channel Hopping	
	0: enable VCO Auto Calibration (default)	**1**: Skip VCO Auto Calibration for frequency hops <1MHz

2.5 Digital Control (SFR Registers)

2.5.1 SFR Register List

The SFRs (Special Function Registers) are used to configure TDA 5150 and to read out certain information e.g. the transmitter status.

There are complete SFRs, as well as register bits in SFRs, called “Reserved”. These SFRs and register bits used in the production process. The SFRs and bits have to be configured with their default value as shown in the **Chapter 2.5.2 SFR Detailed Descriptions**

Table 3 SFR Register List

Register Name	Register Description	Address
SPICHKSUM	SPI Checksum register	0x00
TXSTAT	Transmitter status register	0x01
TXCFG0	Transmitter configuration register 0	0x04
TXCFG1	Transmitter configuration register 1	0x05
CLKOUTCFG	Clock pre- and after-scaler	0x06
BDRDIV	BDRDIV divider	0x07
PRBS	PRBS start value	0x08
PLLINTA	PLL MM integer value Channel A	0x09
PLLFRACA0	PLL fractional division ratio Channel A (byte 0)	0x0A
PLLFRACA1	PLL fractional division ratio Channel A (byte 1)	0x0B
PLLFRACA2	PLL fractional division ratio Channel A (byte 2)	0x0C
PLLINTB	PLL MM integer value Channel B	0x0D
PLLFRACB0	PLL fractional division ratio Channel B (byte 0)	0x0E
PLLFRACB1	PLL fractional division ratio Channel B (byte 1)	0x0F
PLLFRACB2	PLL fractional division ratio Channel B (byte 2)	0x10
PLLINTC	PLL MM integer value Channel C	0x11
PLLFRACC0	PLL fractional division ratio Channel C (byte 0)	0x12
PLLFRACC1	PLL fractional division ratio Channel C (byte 1)	0x13
PLLFRACC2	PLL fractional division ratio Channel C (byte 2)	0x14
PLLINTD	PLL MM integer value Channel D	0x15
PLLFRACD0	PLL fractional division ratio Channel D (byte 0)	0x16

PLLFRACD1	PLL fractional division ratio Channel D (byte 1)	0x17
PLLFRACD2	PLL fractional division ratio Channel D (byte 2)	0x18
SLOPEDIV	ASK sloping clock divider low	0x19
POWCFG0	PA output power configuration register 0	0x1A
POWCFG1	PA output power configuration register 1	0x1B
FDEV	Frequency deviation	0x1C
GFDIV	Gaussian filter divider value	0x1D
GFXOSC	Gaussian filter configuration	0x1E
ANTTDCC	Antenna tuning and Duty Cycle configurations	0x1F
RES1	Reserved	0x20
VAC0	VAC configuration 0	0x21
VAC1	VAC configuration 1	0x22
VACERRTH	VCA error threshold	0x23
CPCFG	Charge pump configuration	0x24
PLLBW	PLL bandwidth configuration	0x25
RES2	Reserved	0x26
ENCCNT	Encoding start bit counter	0x27

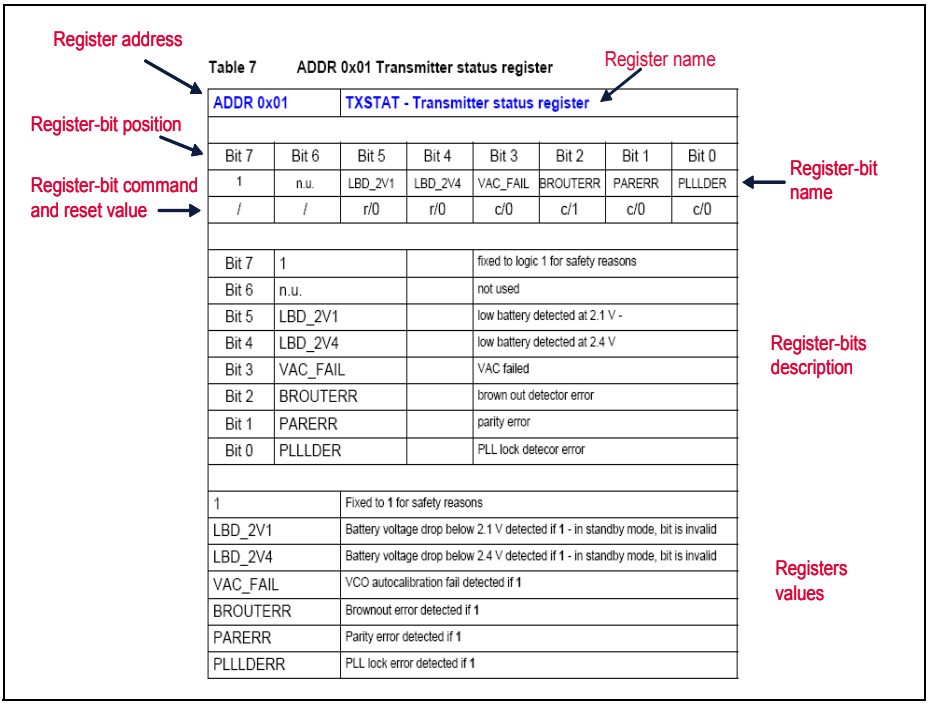

Table 7 ADDR 0x01 Transmitter status register

ADDR 0x01	TXSTAT - Transmitter status register						
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	n.u.	LBD_2V1	LBD_2V4	VAC_FAIL	BROUTERR	PARERR	PLLLDER
/	/	r/0	r/0	c/0	c/1	c/0	c/0

Bit 7	1		fixed to logic 1 for safety reasons
Bit 6	n.u.		not used
Bit 5	LBD_2V1		low battery detected at 2.1 V -
Bit 4	LBD_2V4		low battery detected at 2.4 V
Bit 3	VAC_FAIL		VAC failed
Bit 2	BROUTERR		brown out detector error
Bit 1	PARERR		parity error
Bit 0	PLLLDER		PLL lock detecor error

1	Fixed to **1** for safety reasons
LBD_2V1	Battery voltage drop below 2.1 V detected if **1** - in standby mode, bit is invalid
LBD_2V4	Battery voltage drop below 2.4 V detected if **1** - in standby mode, bit is invalid
VAC_FAIL	VCO autocalibration fail detected if **1**
BROUTERR	Brownout error detected if **1**
PARERR	Parity error detected if **1**
PLLLDERR	PLL lock error detected if **1**

Figure 22 Register Terminology

Register-bit command terminology

r	read register	\0	default to 0	\1	default to 1
w	write register	\0	default to 0	\1	default to 1
c	clear-after-write register	\0	default to 0 after clear	\1	default to 1 after clear

Important notice: It is mandatory to maintain the default values, as specified in the register tables for all reserved SFRs or reserved bits in SFRs

Table 4 Register Bit Map Configuration

Register	Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SPICHKSUM	0x00	SPICHKSUM	SPICHKSUM	SPICHKSUM	SPICHKSUM	SPICHKSUM	SPICHKSUM	SPICHKSUM	SPICHKSUM
TXSTAT	0x01	1	n.u.	LBD_2V1	LBD_2V4	VAC_FAIL	BROUTERR	PARERR	PLLLDERR
TXCFG0	0x04	GO2STDBY	reserved	reserved	FSOFF	ISMB	ISMB	reserved	reserved
TXCFG1	0x05	GO2SLEEP	ASKFSK2	ASKFSK1	ASKSLOPE	INVERT	ENCMODE	ENCMODE	ENCMODE
CLKOUTCFG	0x06	CLKSRC	CLKSRC	AFTERSCALE	AFTERSCALE	PRESCALE	PRESCALE	PRESCALE	CLKOUTENA
BDRDIV	0x07	BDRDIV	BDRDIV	BDRDIV	BDRDIV	BDRDIV	BDRDIV	BDRDIV	BDRDIV
PRBS	0x08	PRBS	PRBS	PRBS	PRBS	PRBS	PRBS	PRBS	PRBS
PLLINTA	0x09	n.u.	PLLINTA	PLLINTA	PLLINTA	PLLINTA	PLLINTA	PLLINTA	PLLINTA
PLLFRACA0	0x0A	PLLFRACA0	PLLFRACA0	PLLFRACA0	PLLFRACA0	PLLFRACA0	PLLFRACA0	PLLFRACA0	PLLFRACA0
PLLFRACA1	0x0B	PLLFRACA1	PLLFRACA1	PLLFRACA1	PLLFRACA1	PLLFRACA1	PLLFRACA1	PLLFRACA1	PLLFRACA1
PLLFRACA2	0x0C	n.u.	n.u.	FRACCOMPA	PLLFRACA2	PLLFRACA2	PLLFRACA2	PLLFRACA2	PLLFRACA2
PLLINTB	0x0D	n.u.	PLLINTB	PLLINTB	PLLINTB	PLLINTB	PLLINTB	PLLINTB	PLLINTB
PLLFRACB0	0x0E	PLLFRACB0	PLLFRACB0	PLLFRACB0	PLLFRACB0	PLLFRACB0	PLLFRACB0	PLLFRACB0	PLLFRACB0
PLLFRACB1	0x0F	PLLFRACB1	PLLFRACB1	PLLFRACB1	PLLFRACB1	PLLFRACB1	PLLFRACB1	PLLFRACB1	PLLFRACB1
PLLFRACB2	0x10	n.u.	n.u.	FRACCOMPB	PLLFRACB2	PLLFRACB2	PLLFRACB2	PLLFRACB2	PLLFRACB2
PLLINTC	0x11	n.u.	PLLINTC	PLLINTC	PLLINTC	PLLINTC	PLLINTC	PLLINTC	PLLINTC
PLLFRACC0	0x12	PLLFRACC0	PLLFRACC0	PLLFRACC0	PLLFRACC0	PLLFRACC0	PLLFRACC0	PLLFRACC0	PLLFRACC0
PLLFRACC1	0x13	PLLFRACC1	PLLFRACC1	PLLFRACC1	PLLFRACC1	PLLFRACC1	PLLFRACC1	PLLFRACC1	PLLFRACC1
PLLFRACC2	0x14	n.u.	n.u.	FRACCOMPC	PLLFRACC2	PLLFRACC2	PLLFRACC2	PLLFRACC2	PLLFRACC2
PLLINTD	0x15	n.u.	PLLINTD	PLLINTD	PLLINTD	PLLINTD	PLLINTD	PLLINTD	PLLINTD
PLLFRACD0	0x16	PLLFRACD0	PLLFRACD0	PLLFRACD0	PLLFRACD0	PLLFRACD0	PLLFRACD0	PLLFRACD0	PLLFRACD0
PLLFRACD1	0x17	PLLFRACD1	PLLFRACD1	PLLFRACD1	PLLFRACD1	PLLFRACD1	PLLFRACD1	PLLFRACD1	PLLFRACD1
PLLFRACD2	0x18	n.u.	n.u.	FRACCOMPD	PLLFRACD2	PLLFRACD2	PLLFRACD2	PLLFRACD2	PLLFRACD2
SLOPEDIV	0x19	SLOPEDIV	SLOPEDIV	SLOPEDIV	SLOPEDIV	SLOPEDIV	SLOPEDIV	SLOPEDIV	SLOPEDIV
POWCFG0	0x1A	PA_PS2	PA_PS2	PA_PS2	PA_PS1	PA_PS1	PA_PS1	SLOPEDIV	SLOPEDIV
POWCFG1	0x1B	POUT2	POUT2	POUT2	POUT2	POUT1	POUT1	POUT1	POUT1
FDEV	0x1C	FDEVSCALE	FDEVSCALE	FDEVSCALE	FDEV	FDEV	FDEV	FDEV	FDEV
GFDIV	0x1D	GFDIV	GFDIV	GFDIV	GFDIV	GFDIV	GFDIV	GFDIV	GFDIV
GFXOSC	0x1E	FHBLANK	reserved	reserved	reserved	GFBYP	GFDIV	GFDIV	GFDIV
ANTTDCC	0x1F	DCCVBYP	DCCDISABLE	DCCCONF	DCCCONF	TUNETOP	TUNETOP	TUNETOP	TUNETOP
RES1	0x20	n.u.	reserved	reserved	reserved	reserved	reserved	reserved	reserved
VAC0	0x21	VAC_CTR	VAC_CTR	VAC_CTR	VAC_CTR	VAC_CTR	VAC_CTR	VAC_CTR	VAC_CTR
VAC1	0x22	n.u.	VAC_NXOSC	VAC_NXOSC	VAC_NXOSC	VAC_NXOSC	VAC_NXOSC	VAC_NXOSC	VAC_CTR
RES2	0x23	reserved	reserved	reserved	reserved	reserved	reserved	reserved	reserved
CPCFG	0x24	n.u.	reserved	reserved	reserved	CPTRIM	CPTRIM	CPTRIM	CPTRIM
PLLBW	0x25	reserved	PLLBWTRIM	PLLBWTRIM	PLLBWTRIM	reserved	reserved	reserved	reserved
RES3	0x26	reserved	reserved	reserved	reserved	reserved	reserved	reserved	reserved
ENCCNT	0x27	ENCCNT	ENCCNT	ENCCNT	ENCCNT	ENCCNT	ENCCNT	ENCCNT	ENCCNT

2.5.2 SFR Detailed Descriptions

ADDR 0x00	SPICHKSUM—SPI Checksum Register						
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SPICHKSUM	SPICHKSUM	SPICHKSUM	SPICHKSUM	SPICHKSUM	SPICHKSUM	SPICHKSUM	SPICHKSUM
c/0	c/0	c/0	c/0	c/0	c/0	c/0	c/0

Bit <7:0>	SPICHKSUM		SPI checksum bit <7:0>

SPICHKSUM	Readout and clear the SPI checksum (8-bits), generated by each write to SFR register

ADDR 0x01	TXSTAT—Transmitter Status Register						
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	n.u.	LBD_2V1	LBD_2V4	VAC_FAIL	BROUTERR	PARERR	PLLLDER
/	/	r/0	r/0	c/0	c/1	c/0	c/0

Bit 7	1		Mandatory to keep set (1)
Bit 5	LBD_2V1		battery low detected at 2.1 V -
Bit 4	LBD_2V4		battery low detected at 2.4 V
Bit 3	reserved		Don't care
Bit 2	BROUTERR		Brown out detector error
Bit 1	PARERR		Parity error
Bit 0	PLLLDER		PLL lock detector error

LBD_2V1	Battery voltage drop below 2.1 V detected if **1** NOTE: bit invalid in standby mode.
LBD_2V4	Battery voltage drop below 2.4 V detected if **1** NOTE: bit invalid in standby mode
BROUTERR	Brownout error detected if **1**
PARERR	Parity error detected if **1**
PLLLDERR	PLL lock error detected if **1**

ADDR 0x04		TXCFG0—Transmitter Configuration Register 0					
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
GO2STDBY	reserved	reserved	FSOFF	ISMB	ISMB	reserved	reserved
cw/0	w/0	w/0	w/0	w/0	w/1	w/1	w/0

Bit 7	GO2STDBY		Go to StandBy
Bit 6	reserved		Reserved, set 0
Bit 5	reserved		Reserved, set to 0
Bit 4	FSOFF		Fail-Safe mechanism turned off
Bit <3:2>	ISMB		RF frequency band bit <1:0>
Bit 1	reserved		Reserved, set to 1
Bit 0	reserved		Reserved, set to 0

GO2STDBY	Put the chip in STDBY mode (look at the detailed state diagram), cleared after 1 is written				
FSOFF	Fail-Safe mechanism				
	0: on			**1**:off	
ISMB	ISM band selection (2-bits)				
	00: MHz 300-320	**01**: MHz 425-450	**10**: MHz 863-870	**11**: MHz 902-928	

For the reserved **registers**, it is mandatory to retain always the **default** values.

ADDR 0x05	TXCFG1—Transmitter Configuration Register 1						
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
GO2SLEEP	ASKFSK2	ASKFSK1	ASKSLOPE	INVERT	ENCMODE	ENCMODE	ENCMODE
cw/0	w/0	w/1	w/0	w/0	w/1	w/0	w/1

Bit 7	GO2SLEEP		Go to Sleep
Bit <6:5>	ASKFSK2:1		[ASK / FSK setting 2] and [ASK / FSK setting 1]
Bit 4	ASKSLOPE		ASK sloping enable
Bit 3	INVERT		Data inversion
Bit <2:0>	ENCMODE		Encoding mode bit <2:0>

GO2SLEEP	Set the chip into SLEEP mode (look at the detailed state diagram), cleared after 1 is written				
ASKFSK2:1	[ASK / FSK modulation switch setting 2] and [ASK / FSK modulation switch setting 1]				
	0: ASK			**1**: FSK	
ASKSLOPE	ASK sloping enable				
	0: disable			**1**: enable	
INVERT	Encoded data inversion enable				
	0: data not inverted			**1**: data inverted	
ENCMODE	Encoding mode, code selection (3 bits)				
	000: Manchester	**010**: Biphase Space	**100**: Miller (Delay)	**110**: Scrambling (PRBS)	
	001: Differential Manchester	**011**: Biphase Mark	**101**: NRZ	**111**: not used (data =0)	

ADDR 0x06	CLKOUTCFG - Clock Pre- and Post-scaler						
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CLKSRC	CLKSRC	AFTERSCALE	AFTERSCALE	PRESCALE	PRESCALE	PRESCALE	CLKOUTENA
w/0	w/0	w/0	w/0	w/1	w/0	w/0	w/1

Bit <7:6>	CLKSRC		Clock source selection bit <1:0>
Bit <5:4>	AFTERSCALE		Post scaler selection bit <1:0>
Bit <3:1>	PRESCALE		Pre scaler selection bit <2:0>
Bit 0	CLKOUTENA		Enable clock output

CLKSRC	Clock output selection (2-bits)				
	00: prescaler clock	**01**: BDRDIV counter clock	**10**: inverted BDRDIV counter clock	**11**: afterscaler clock	
AFTERSCALE	Post-scaler clock divider selection (2 bits)				
	00: divide by 1	**01**: divide by 2	**10**: divide by 4	**11**: divide by 8	
PRESCALE	Pre-scaler clock divider selection (3-bits)				
	000: divide by 1	**001**: divide by 2	**010**: divide by 4	**011**: divide by 8	
	100: divide by 16	**101**: divide by 32	**110**: divide by 64	**111**: divide by 128	
CLKOUTENA	Clock output enable				
	0: disable, instead of clock, the Crystal Oscillator stable signal causes a rising edge on CLKOUT			**1**: enabled	
	Enabled also automatically, when default clocking (f_{SYS}/16) is used, when the SDI input is low at the rising edge of the EN after power up				

ADDR 0x07		BDRDIV—Bit-rate Divider					
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
BDRDIV	BDRDIV	BDRDIV	BDRDIV	BDRDIV	BDRDIV	BDRDIV	BDRDIV
w/1	w/0	w/0	w/0	w/0	w/0	w/0	w/0

Bit <7:0>	BDRDIV		BDRDIV divider bit <7:0>

BRDRDIV	Along with the pre-scaler and the post-scaler, Bit-rate clock divider value (8 bits), defines the data bit-rate, according to following formula.		
	Range:	from **0x00**: BDRDIV = 0	to **0xFF**: BDRDIV = 255
	Formula to calculate the bit-rate: $$bitrate = \frac{f_{XOSC}}{PRESCALE \times (BDRDIV + 1) \times 2 \times AFTERSCALE}$$		

ADDR 0x08		PRBS—PRBS Start Value					
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PRBS	PRBS	PRBS	PRBS	PRBS	PRBS	PRBS	PRBS
w/1	w/0	w/1	w/0	w/1	w/0	w/1	w/1

Bit <7:0>	PRBS		PRBS start value bit <7:0>

PRBS	PRBS start value (8 bits), the PRBS generator uses this as a starting value after each transmission beginning

ADDR 0x09			PLLINTA—PLL MM Integer Value Channel A				
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
n.u.	PLLINTA	PLLINTA	PLLINTA	PLLINTA	PLLINTA	PLLINTA	PLLINTA
/	w/1	w/0	w/0	w/0	w/0	w/0	w/0
Bit <6:0>	PLLINTA			Integer division ratio bit <6:0>			
PLLINTA	Multi-modulus divider integer offset value (7 bits) for **Channel A**						

ADDR 0x0A			PLLFRACA0—PLL Fractional Division Ratio Channel A (byte 0)				
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PLLFRACA0	PLLFRACA0	PLLFRACA0	PLLFRACA0	PLLFRACA0	PLLFRACA0	PLLFRACA0	PLLFRACA0
w/0	w/0	w/0	w/0	w/0	w/0	w/0	w/0
Bit <7:0>	PLLFRACA0			Fractional division ratio bit <7:0>			
PLLFRACA0	Synthesizer channel frequency value (21 bits, bits < 7:0 >), fractional division ratio for **Channel A**						

ADDR 0x0B			PLLFRACA1—PLL Fractional Division Ratio Channel A (byte 1)				
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PLLFRACA1	PLLFRACA1	PLLFRACA1	PLLFRACA1	PLLFRACA1	PLLFRACA1	PLLFRACA1	PLLFRACA1
w/0	w/0	w/0	w/0	w/0	w/0	w/0	w/0
Bit <7:0>	PLLFRACA1			Fractional division ratio bit <15:8>			
PLLFRACA1	Synthesizer channel frequency value (21 bits, bits < 15:8 >), fractional division ratio for **Channel A**						

ADDR 0x0C	PLLFRACA2—PLL Fractional Division Ratio Channel A (byte 2)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
n.u.	n.u.	reserved	PLLFRACA2	PLLFRACA2	PLLFRACA2	PLLFRACA2	PLLFRACA2
/	/	w/0	w/1	w/0	w/0	w/0	w/0

Bit 5	reserved		Reserved, set to 0
Bit <4:0>	PLLFRACA2		Fractional division ratio bit <20:16>

PLLFRACA2	Synthesizer channel frequency value (21 bits, bits < 20:16 >), fractional division ratio for **Channel A**

ADDR 0x0D	PLLINTB—PLL MM Integer Value Channel B

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
n.u.	PLLINTB	PLLINTB	PLLINTB	PLLINTB	PLLINTB	PLLINTB	PLLINTB
/	w/1	w/0	w/0	w/0	w/0	w/0	w/0

Bit <6:0>	PLLINTB		Integer division ratio bit <6:0>

PLLINTB	Multi-modulus divider integer offset value (7 bits) for **Channel B**

ADDR 0x0E	PLLFRACB0—PLL Fractional Division Ratio Channel B (byte 0)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PLLFRACB0	PLLFRACB0	PLLFRACB0	PLLFRACB0	PLLFRACB0	PLLFRACB0	PLLFRACB0	PLLFRACB0
w/0	w/0	w/0	w/0	w/0	w/0	w/0	w/0

Bit <7:0>	PLLFRACB0		Fractional division ratio bit <7:0>

PLLFRACB0	Synthesizer channel frequency value (21 bits, bits < 7:0 >), fractional division ratio for **Channel B**

ADDR 0x0F	PLLFRACB1—PLL Fractional Division Ratio Channel B (byte 1)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PLLFRACB1	PLLFRACB1	PLLFRACB1	PLLFRACB1	PLLFRACB1	PLLFRACB1	PLLFRACB1	PLLFRACB1
w/0	w/0	w/0	w/0	w/0	w/0	w/0	w/0

Bit <7:0>	PLLFRACB1		Fractional division ratio bit <15:8>

PLLFRACB1	Synthesizer channel frequency value (21 bits, bits < 15:8 >), fractional division ratio for **Channel B**

ADDR 0x10	PLLFRACB2—PLL Fractional Division Ratio Channel B (byte 2)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
n.u.	n.u.	reserved	PLLFRACB2	PLLFRACB2	PLLFRACB2	PLLFRACB2	PLLFRACB2
/	/	w/0	w/1	w/0	w/0	w/0	w/0

Bit 5	reserved		Reserved, set to 0
Bit <4:0>	PLLFRACB2		Fractional division ratio bit <20:16>

PLLFRACB2	Synthesizer channel frequency value (21 bits, bits < 20:16 >), fractional division ratio for **Channel B**

ADDR 0x11	PLLINTC—PLL MM Integer Value Channel C

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
n.u.	PLLINTC	PLLINTC	PLLINTC	PLLINTC	PLLINTC	PLLINTC	PLLINTC
/	w/1	w/0	w/0	w/0	w/0	w/0	w/0

Bit <6:0>	PLLINTC		Integer division ratio bit <6:0>

PLLINTC	Multi-modulus divider integer offset value (7 bits) for **Channel C**

ADDR 0x12			PLLFRACC0—PLL Fractional Division Ratio Channel C (byte 0)				
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PLLFRACC0	PLLFRACC0	PLLFRACC0	PLLFRACC0	PLLFRACC0	PLLFRACC0	PLLFRACC0	PLLFRACC0
w/0	w/0	w/0	w/0	w/0	w/0	w/0	w/0
Bit <7:0>	PLLFRACC0			Fractional division ratio bit <7:0>			
PLLFRACC0	Synthesizer channel frequency value (21 bits, bits < 7:0 >), fractional division ratio for **Channel C**						

ADDR 0x13			PLLFRACC1—PLL Fractional Division Ratio Channel C (byte 1)				
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PLLFRACC1	PLLFRACC1	PLLFRACC1	PLLFRACC1	PLLFRACC1	PLLFRACC1	PLLFRACC1	PLLFRACC1
w/0	w/0	w/0	w/0	w/0	w/0	w/0	w/0
Bit <7:0>	PLLFRACC1			Factional division ratio bit <15:8>			
PLLFRACC1	Synthesizer channel frequency value (21 bits, bits < 15:8 >), fractional division ratio for **Channel C**						

ADDR 0x14		PLLFRACC2—PLL Fractional Division Ratio Channel C (byte 2)					
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
n.u.	n.u.	reserved	PLLFRACC2	PLLFRACC2	PLLFRACC2	PLLFRACC2	PLLFRACC2
/	/	w/0	w/1	w/0	w/0	w/0	w/0
Bit 5	reserved		Reserved, set to 0				
Bit <4:0>	PLLFRACC2		Factional division ratio bit <20:16>				
PLLFRACC2	Synthesizer channel frequency value (21 bits, bits < 20:16 >), fractional division ratio for **Channel C**						

ADDR 0x15		PLLINTD—PLL MM Integer Value Channel D					
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
n.u.	PLLINTD	PLLINTD	PLLINTD	PLLINTD	PLLINTD	PLLINTD	PLLINTD
/	w/1	w/0	w/0	w/0	w/0	w/0	w/0
Bit <6:0>	PLLINTD		Integer division ratio bit <6:0>				
PLLINTD	Multi-modulus divider integer offset value (7 bits) for **Channel D**						

ADDR 0x16		PLLFRACD0—PLL Fractional Division Ratio Channel D (byte 0)					
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PLLFRACD0	PLLFRACD0	PLLFRACD0	PLLFRACD0	PLLFRACD0	PLLFRACD0	PLLFRACD0	PLLFRACD0
w/0	w/0	w/0	w/0	w/0	w/0	w/0	w/0
Bit <7:0>	PLLFRACD0		Fractional division ratio bit <7:0>				
PLLFRACD0	Synthesizer channel frequency value (21 bits, bits < 7:0 >), fractional division ratio for **Channel D**						

ADDR 0x17			PLLFRACD1—PLL Fractional Division Ratio Channel D (byte 1)				
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PLLFRACD1	PLLFRACD1	PLLFRACD1	PLLFRACD1	PLLFRACD1	PLLFRACD1	PLLFRACD1	PLLFRACD1
w/0	w/0	w/0	w/0	w/0	w/0	w/0	w/0
Bit <7:0>	PLLFRACD1			Fractional division ratio bit <15:8>			
PLLFRACD1	Synthesizer channel frequency value (21 bits, bits < 15:8 >), fractional division ratio for **Channel D**						

ADDR 0x18			PLLFRACD2—PLL Fractional Division Ratio Channel D (byte 2)				
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
n.u.	n.u.	reserved	PLLFRACD2	PLLFRACD2	PLLFRACD2	PLLFRACD2	PLLFRACD2
/	/	w/0	w/1	w/0	w/0	w/0	w/0
Bit 5	reserved			Reserved			
Bit <4:0>	PLLFRACD2			Fractional division ratio bit <20:16>			
PLLFRACD2	Synthesizer channel frequency value (21 bits, bits < 20:16 >), fractional division ratio for **Channel D**						

ADDR 0x19		SLOPEDIV —ASK Sloping Clock Divider					
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SLOPEDIV	SLOPEDIV	SLOPEDIV	SLOPEDIV	SLOPEDIV	SLOPEDIV	SLOPEDIV	SLOPEDIV
w/1	w/0	w/0	w/0	w/0	w/0	w/0	w/0
Bit <7:0>	SLOPEDIV			ASK sloping clock divider bit <7:0>			
SLOPEDIV	ASK sloping clock division ratio (10 bits, bits < 7:0 >), defines the slope of the ASK signal shaping using PA power stage switching						
	Range:			from **0x000**: SLOPEDIV = 1		to **0x3FF**: SLOPEDIV = 1024	

ADDR 0x1A		POWCFG0—PA Output Power Configuration Register 0					
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PA_PS2	PA_PS2	PA_PS2	PA_PS1	PA_PS1	PA_PS1	SLOPEDIV	SLOPEDIV
w/0	w/0	w/0	w/0	w/0	w/0	w/0	w/0
Bit <7:5>	PA_PS2			PA output blocks setting 2 bit <2:0>			
Bit <4:2>	PA_PS1			PA output blocks setting 1 bit <2:0>			
Bit <1:0>	SLOPEDIV			ASK sloping clock divider bit <9:8>			
PA_PS2	Individual control of the 3 PA blocks, setting 2 (3-bits)						
	0: disabled	**1**: enabled		Bit(0) ==> PA block 0	Bit(1) ==> PA block 1	Bit(2) ==> PA block 2	
PA_PS1	Individual control of the 3 PA blocks, setting 1(3-bits)						
	0: disabled	**1**: enabled		Bit(0) ==> PA block 0	Bit(1) ==> PA block 1	Bit(2) ==> PA block 2	
SLOPEDIV	ASK sloping clock division ratio (10 bits, bits < 9:8 >), defines the frequency of the ASK signal shaping using PA power stage switching						
	Range:			from **0x000**: SLOPEDIV = 1		to **0x3FF**: SLOPEDIV = 1024	

ADDR 0x1B		POWCFG1—PA Output Power Configuration Register 1					
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
POUT2	POUT2	POUT2	POUT2	POUT1	POUT1	POUT1	POUT1
w/0	w/0	w/0	w/0	w/0	w/0	w/0	w/0

Bit <7:4>	POUT2		Output power setting 2 bit <3:0>
Bit <3:0>	POUT1		Output power setting 1 bit <3:0>

POUT2	PA output power setting 2 (4 bits), defines the number of enabled PA stages		
	Range:	from **0x0**: POUT2 = 0	to **0xB**: POUT2 = 11 > **0xB**: POUT2 = 11
POUT1	PA output power setting 1 (4 bits), defines the number of enabled PA stages		
	Range:	from **0x0**: POUT1 = 0	to **0xB**: POUT1 = 11 > **0xB**: POUT1 = 11

ADDR 0x1C		FDEV—Frequency Deviation					
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
FDEVSCALE	FDEVSCALE	FDEVSCALE	FDEV	FDEV	FDEV	FDEV	FDEV
w/1	w/1	w/0	w/1	w/1	w/1	w/1	w/1

Bit <7:5>	FDEVSCALE		Frequency deviation scaling bit <2:0>
Bit <4:0>	FDEV		Frequency deviation bit <4:0>

FDEVSCALE	Scaling of the frequency deviation (3 bits)				
	000: divide by 64	**001**: divide by 32	**010**: divide by 16	**011**: divide by 8	$value = \frac{2^{FDEVSCALE}}{64}$
	100: divide by 4	**101**: divide by 2	**110**: divide by 1	**111**: multiply by2	
FDEV	Frequency deviation value (5 bits), defines the multiplication value for the output data from the Gaussian filter (0-31)				

ADDR 0x1D		GFDIV—Gaussian Filter Divider Value					
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
GFDIV	GFDIV	GFDIV	GFDIV	GFDIV	GFDIV	GFDIV	GFDIV
w/0	w/0	w/0	w/0	w/1	w/0	w/0	w/0
Bit <7:0>	GFDIV			Gaussian filter divider bit <7:0>			
GFDIV	Gaussian filter clock divider value (11 bits, bits < 7:0 >), defines the sampling ratio of the Gaussian filter; typically this value is set such that the GF divider N_{GF} is 16 x chip-rate (for ideal Gaussian filtering) $$GFDIV = \frac{f_{XOSC}}{chiprate \times NGF} - 1$$						

Note: it is recommended to program the **GFDIV** register in such way, that the GF divider **N_{GF}** is 16 times the chip-rate. This allows optimum Gaussian filtering.

ADDR 0x1E		GFXOSC—Gaussian Filter Configuration					
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
FHBLANK	reserved	reserved	reserved	GFBYP	GFDIV	GFDIV	GFDIV
w/0	w/1	w/1	w/1	w/1	w/0	w/0	w/0

Bit 7	FHBLANK		Frequency Hopping VAC Disable
Bit <6:4>	reserved		Reserved, set all bits to 1
Bit 3	GFBYP		Gaussian filter bypass
Bit <2:0>	GFDIV		Gaussian filter divider bits <10:8>

FHBLANK	Frequency Hopping, enable/disable VCO Auto Calibration for Channel Hopping		
	0: enable VCO Auto Calibration (default)		**1**: Skip VCO Auto Calibration for frequency hops <1MHz
GFBYP	Gaussian filter bypass:	**0**: GF enabled	**1**: GF bypassed
GFDIV		Gaussian filter clock divider value (11 bits, bits < 10:8 >), defines the sampling ratio of the Gaussian filter, typically this value is set such that the GF divider is 16 x chiprate (for ideal Gaussian filtering) $$GFDIV = \frac{f_{XOSC}}{chiprate \times \mathbf{16}} - \mathbf{1}$$	

ADDR 0x1F	ANTTDCC—Antenna Tuning and Duty Cycle Configurations

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
reserved	DCC DISABLE	DCCCONF	DCCCONF	TUNETOP	TUNETOP	TUNETOP	TUNETOP
w/0	w/0	w/1	w/0	w/0	w/0	w/0	w/0

Bit 7	reserved		Reserved, set to 0
Bit 6	DCCDISABLE		Duty cycle control disable
Bit <5:4>	DCCCONF		Duty cycle control delay configuration bit <1:0>
Bit 3:0	TUNETOP		Antenna tuning top (PAOUT pin) bit <3:0>

DCCDISABLE	Duty cycle control disable (must be 0 for ISMB=0)					
	0 enabled			1 disabled (delay = 0ps)		
DCCCONF	Duty cycle control delay configuration (ISMB = 1/2/3, for ISMB = 0 => delay = 0 ps)					
	00: 43% (69/35/33 ps)	01: 39% (207/104/98 ps)	10: 35% (346/173/164 ps)	11: 31% (484/242/230 ps)		
TUNETOP	Antenna tuning top capacitor selection (4-bits):					
	Individual switch of capacitor banks		**0**: switched off		**1**: switched on	
	Bit(0) ==> 60 fF	Bit(1) ==> 120 fF	Bit(2) ==> 240 fF	Bit(3) ==> 480 fF		

ADDR 0x20	RES1—Reserved

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
n.u.	reserved	reserved	reserved	reserved	reserved	reserved	reserved
/	w/1	w/0	w/0	w/1	w/1	w/0	w/0

Bit <7:0>	reserved		Reserved, set bits <6,3,2> to 1 and bits <5, 4, 1, 0> to 0

.

ADDR 0x21	VAC0—VAC Configuration 0						
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
VAC_CTR	VAC_CTR	VAC_CTR	VAC_CTR	VAC_CTR	VAC_CTR	VAC_CTR	VAC_CTR
w/1	w/1	w/0	w/0	w/1	w/0	w/0	w/0
Bit <7:0>	VAC_CTR			VAC frequency counter value bit <7:0>			
VAC_CTR	VCO autocalibration FAST counter (~100 MHz) compare value (9 bits, bits< 7:0 >)						

ADDR 0x22	VAC1—VAC Configuration 1						
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
n.u.	reserved	reserved	reserved	reserved	reserved	reserved	VAC_CTR
/	w/1	w/0	w/0	w/0	w/0	w/0	w/0
Bit 7	n.u.			Not used			
Bit <6:1>	reserved			Reserved, set bit 6 to 1, bits <5:1> to 0			
Bit 0	VAC_CTR			VAC frequency counter value bit 8			
VAC_CTR	VCO autocalibration FAST counter (~100 MHz) compare value (9 bits, bit 8)						

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ADDR 0x23	RES2						
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
reserved	reserved	reserved	reserved	reserved	reserved	reserved	reserved
w/0	w/0	w/0	w/0	w/0	w/0	w/0	w/0
Bit <7:0>	reserved			Reserved, set to 0			

ADDR 0x24	CPCFG—Charge Pump Configurations						
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
n.u.	reserved	reserved	reserved	CPTRIM	CPTRIM	CPTRIM	CPTRIM
/	w/0	w/1	w/0	w/0	w/1	w/0	w/0

Bit <6:4>	reserved		Reserved
Bit <3:0>	CPTRIM		Charge pump current trimming bit <3:0>

CPTRIM	Charge pump current trimming (4-bits):			
	Range:	from **0x00**: current = 2.5 µA	to **0xF**. current = 40 µA	step: 2.5 µA

*Note: **CPTRIM** bits must be set correlated with PLLBW bits, otherwise loop instability may occur*

ADDR 0x25	PLLBW— PLL Bandwidth Configuration						
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
reserved	PLLBW TRIM	PLLBW TRIM	PLLBW TRIM	reserved	reserved	reserved	reserved
w/1	w/1	w/0	w/1	w/1	w/0	w/0	w/0

Bit 7	reserved		reserved
Bit <6:4>	PLLBWTRIM		Trim bandwidth of the PLL loop filter bit <2:0>
Bit <3:0>	reserved		reserved

PLLBWTRIM	Trim bandwidth of the PLL loop filter (3 bits):			
	Range:	from **0x0**: BW = 300 kHz	to **0x7**: BW = 90 kHz	step: 30 kHz

Note: PLLBW must be set together with CPTRIM according to following table:

PLLBWTRIM [kHz]	90	120	150	180	210	240	270
CPTRIM [µA]	5	7.5	12.5	17.5	25	32.5	40

.

ADDR 0x26			RES3—Reserved				
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
reserved	reserved	reserved	reserved	reserved	reserved	reserved	reserved
w/1	w/1	w/0	w/0	w/0	w/0	w/0	w/0
Bit <7:0>	reserved		Reserved, set bits <7:6> to 1, and bits <5:0> to 0				

.

ADDR 0x27			ENCCNT - Encoding start bit counter				
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ENCCNT	ENCCNT	ENCCNT	ENCCNT	ENCCNT	ENCCNT	ENCCNT	ENCCNT
w/0	w/0	w/0	w/0	w/0	w/0	w/0	w/0
Bit <7:0>	ENCCNT		Encoding start bit counter bit <7:0>				
ENCCNT	Sets the number of bits on start of a telegram which shall be sent unencoded or unscrambled before encoder/scrambler is switched on. This feature is used e.g. to be able to send unscrambled synchronization patterns first.						

3 Applications

3.1 Simple application schematics example

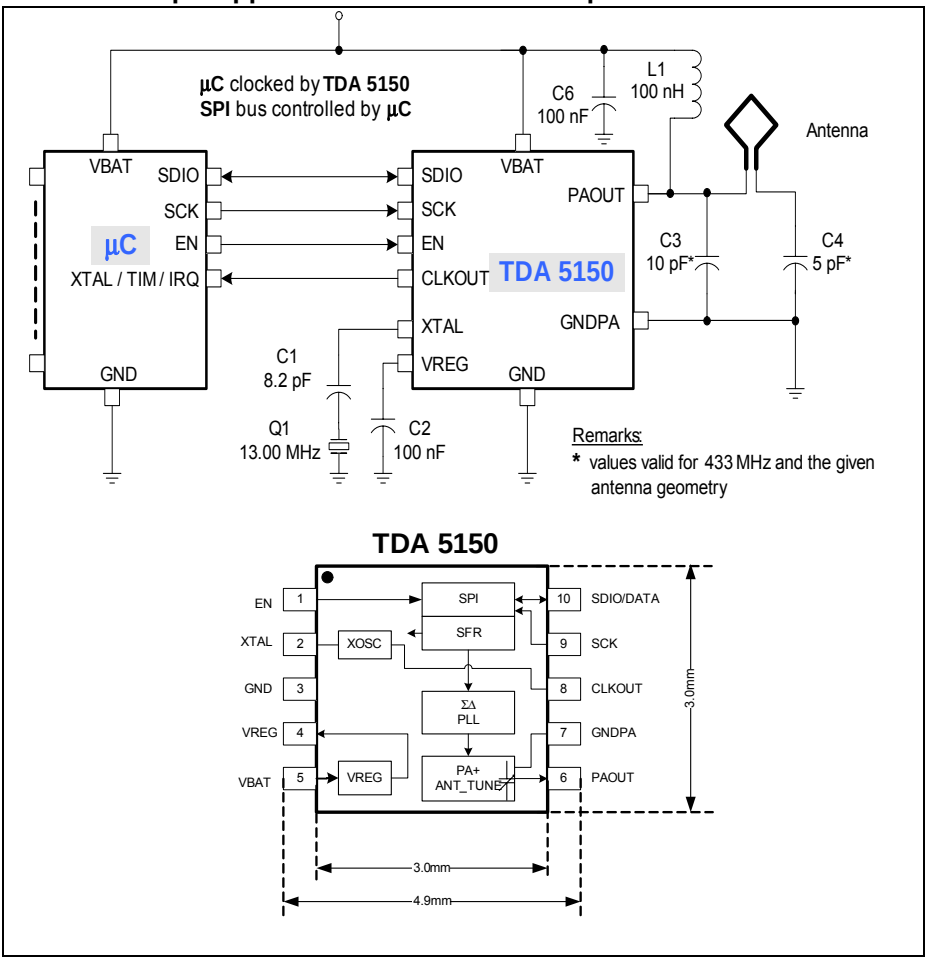

Figure 23 Simple application example with reduced Bill of Materials

3.2 Infineon Evaluation Board V1.1

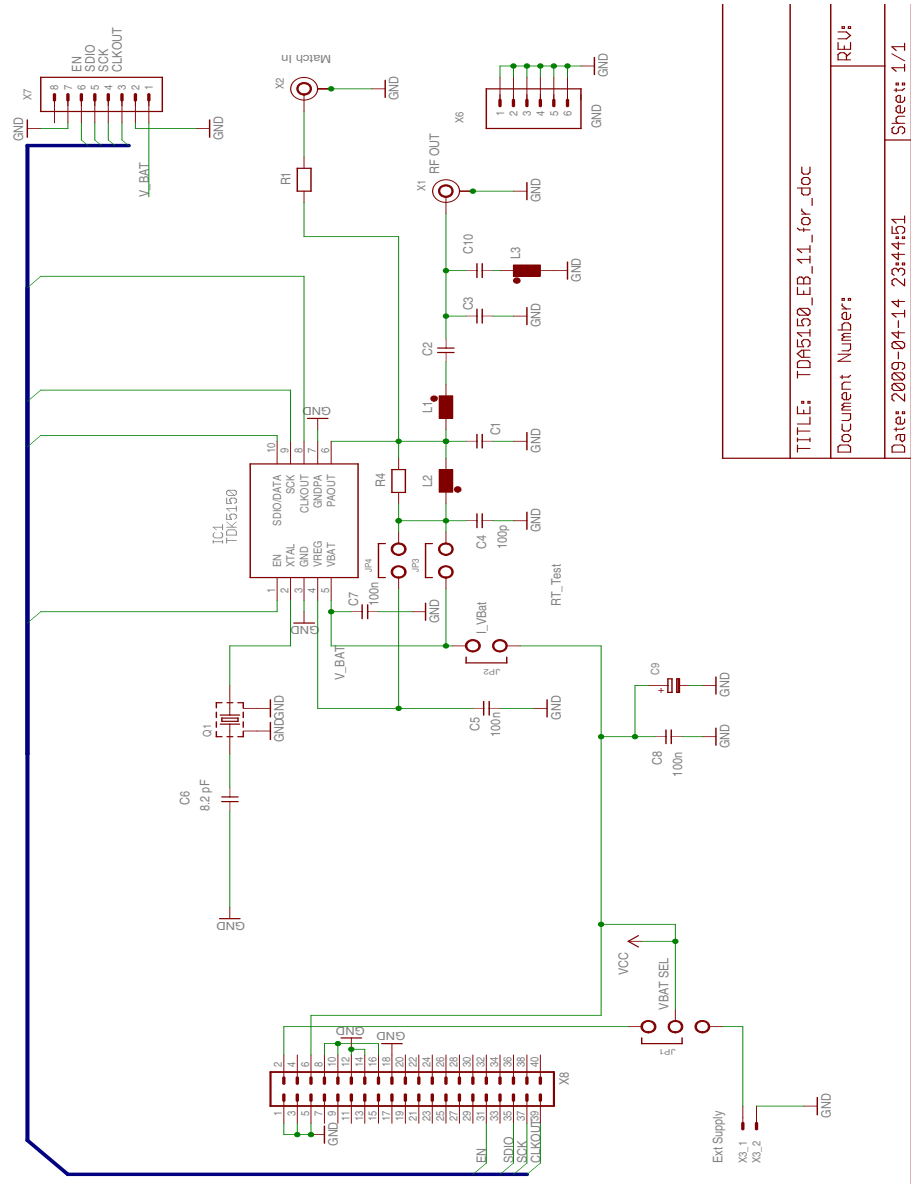

Figure 24 Infineon Evaluation Board schematics (E.B. V1.1 board version)

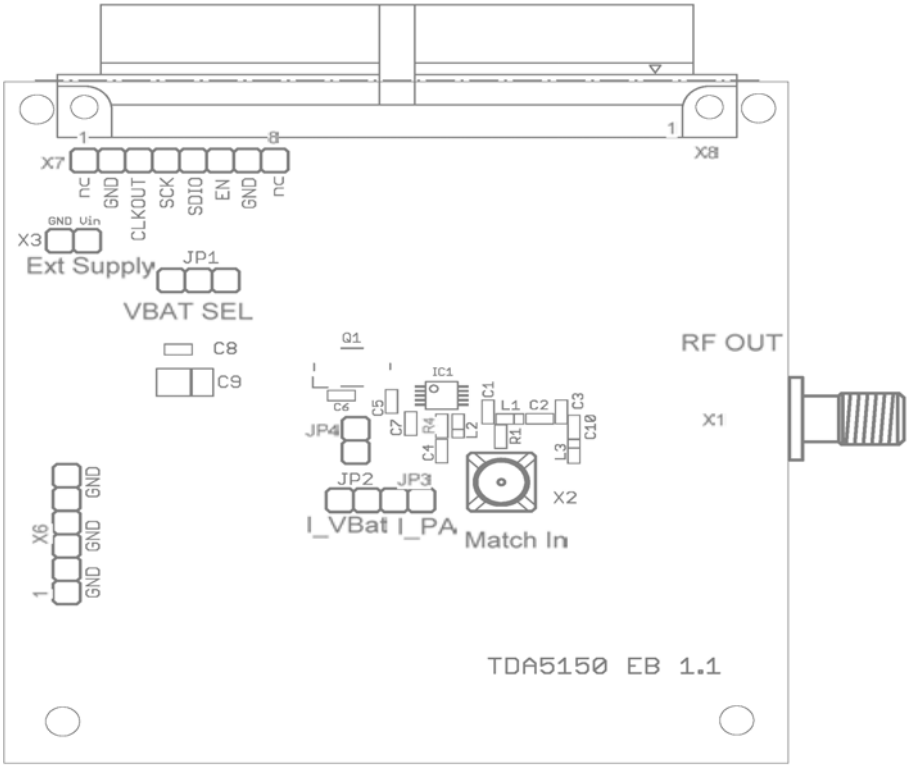

Figure 25 Component placement on Infineon Evaluation Board (V1.1, top side)

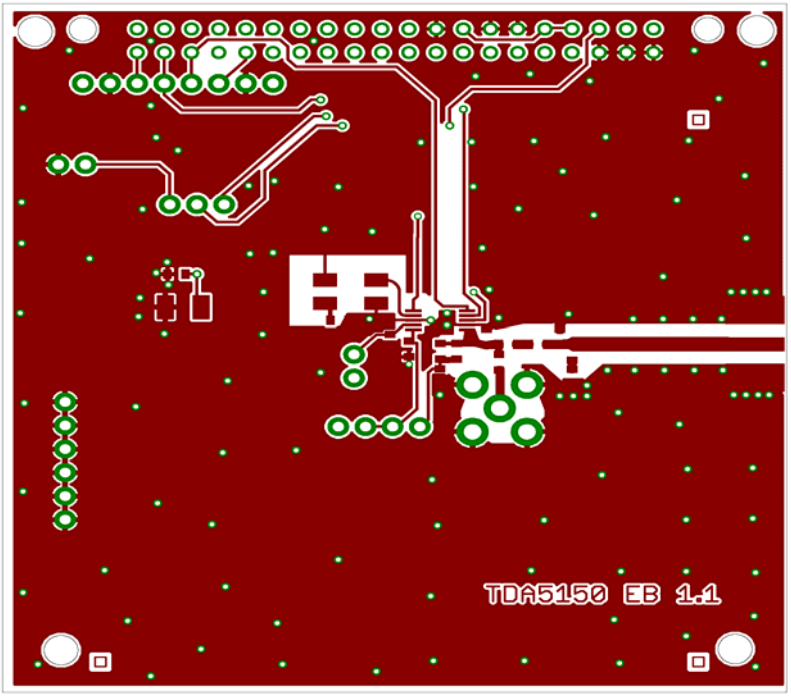

Figure 26 Infineon Evaluation Board V1.1 top side, copper layer

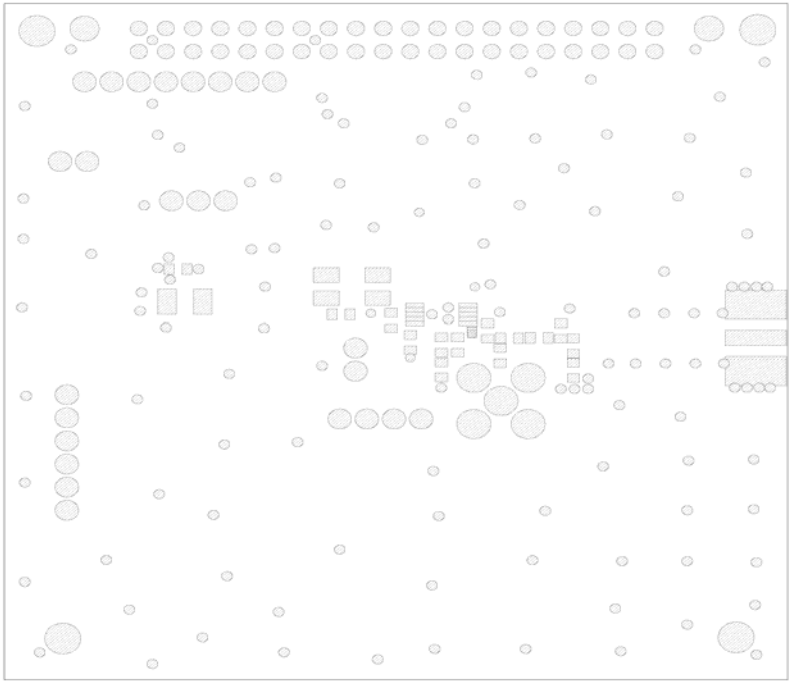

Figure 27 Infineon Evaluation Board V1.1 top side, solder mask

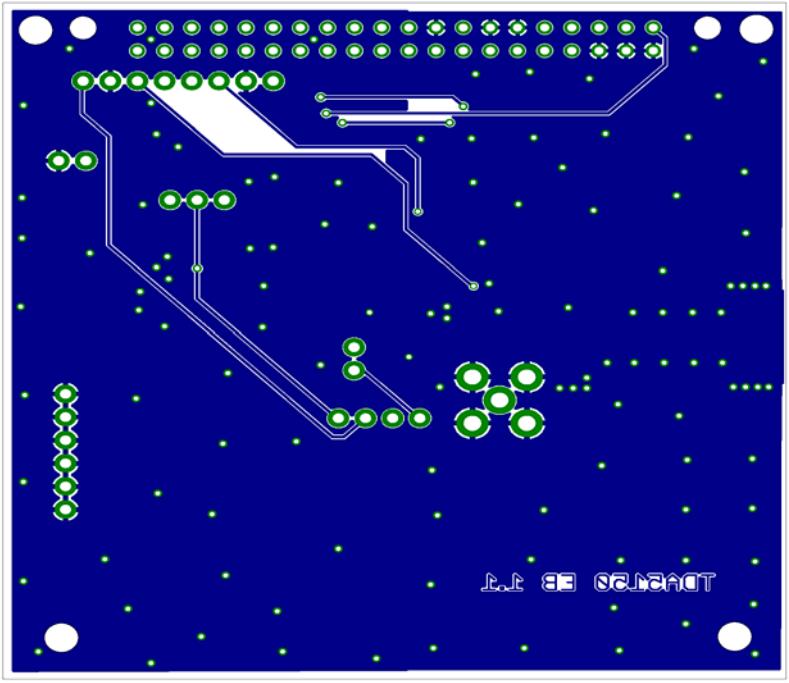

Figure 28 Infineon Evaluation Board V1.1 bottom side, copper layer

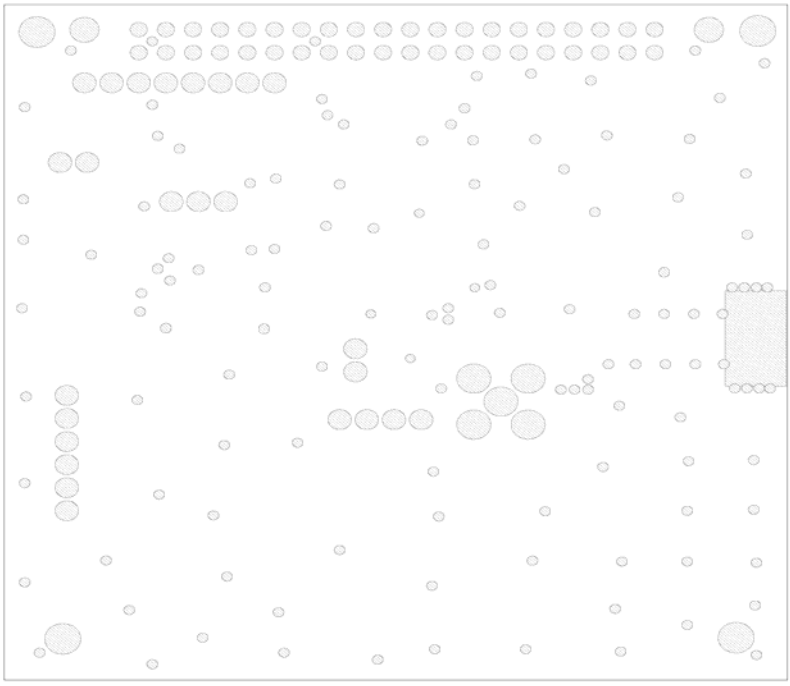

Figure 29 Infineon Evaluation Board V1.1 bottom side, solder mask

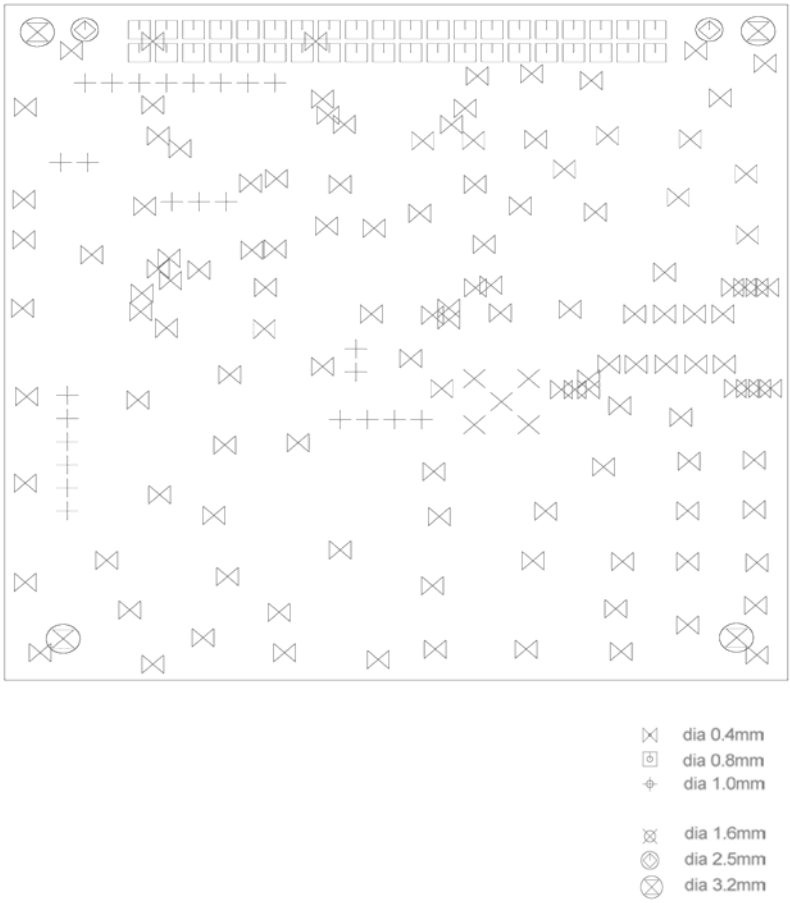

Figure 30 Infineon Evaluation Board V1.1 drill map and tool list

Pos.	Part	Value	Package	Device / Type	Tolerance	Manufacturer	Remark
1	IC1	TDA5150	PG-TSSOP-10	SMD		Infineon	
2	R1	n.p.	0603				
3	R4	n.p.	0603				
4	C1	see Table 6	0603	SMD	+/-1%		
5	C2	see Table 6	0603	SMD	+/-1%		matching network, ± 1% or ± 0.1 pF tolerance, whichever is greater
6	C3	see Table 6	0603	SMD	+/-1%		matching network, ± 1% or ± 0.1 pF tolerance, whichever is greater
7	C4	100pF	0603	SMD - C0G cap	+/- 5%		matching network
8	C5	100nF	0603	SMD - X7R cap	+/-10%		
9	C6	8.2pF	0603	SMD	+/-1%		
10	C7	100nF	0603	X7R	+/-10%		
11	C8	100nF	0603	X7R	+/-10%		
12	C9	n.p.	293B	Tantal 10V	+/-20%		
13	C10	see Table 6	0603		+/-2%		harmonic suppresion, ± 2% or ± 0.1 pF tolerance, whichever is greater
14	L1	see Table 6	0603	0603CS	+/-2%	Coilcraft	matching network, ± 2% or ± 0.1 pF tolerance, whichever is greater
15	L2	see Table 6	0603	0603CS	+/-2%	Coilcraft	matching network, ± 2% or ± 0.1 pF tolerance, whichever is greater
16	L3	n.p.	0603				harmonic suppresion,
17	Q1	see Table 6	3.1 x 4.9 mm	EXS00A-03515	10 ppm	NDK	
18	X1	SMA male connector		Straight PCB mounting			RF OUT
19	X2	SMA male connector		90° PCB mounting			Only footprint
20	X3	2 pins		test port			Ext Supply
21	JP1	3 pins		jumper			VBAT SEL
22	JP2	2 pins		jumper			1_VBat test port
23	JP3	2 pins		jumper			1_PA test port @ VBat
24	JP3	2 pins		jumper			1_PA test port @ VReg - ONLY FOOTPRINT
25	X6	6 pins		test port			GND test port
26	X7	8 pins		test port			Signals test port
27	X8	2x20 pins					Connection to SIB (PC Interface) Manufactured by 3M , Type **5140-B7A2JL**
28	PCB1	TDK5150_EB_101					Board material 1,6 mm FR4 ,35µm copper on both sides

Table 5 Bill of Materials, Infineon Evaluation Board V1.1

*Note: frequency dependent component values (PA matching network for instance) are listed in **Table 6***

Table 6 Frequency band dependent component values

315 MHz	C1	C2	C3	C4	L1	L2	Xtal	Note
315_5dBm	2p7	100p	15p	100p	72n	100n	13.000	
315_8dBm	2p7	100p	10p	100p	72n	100n	13.000	
315_10dBm	2p7	100p	5p6	100p	72n	100n	13.000	
434 MHz	C1	C2	C3	C4	L1	L2	Xtal	
434_5dBm	1p5	33p	12p	100p	51n	51n	13.000	
434_8dBm	1p5	33p	6p8	100p	51n	51n	13.000	
434_10dBm	1p5	33p	4p7	100p	51n	51n	13.000	
868 MHz	C1	C2	C3	C4	L1	L2	Xtal	
868_5dBm				100p			13.000	
868_8dBm				100p			13.000	
868_10dBm	2p2	68p	5p6	100p	10n	9n5	13.000	
915 MHz	C1	C2	C3	C4	L1	L2	Xtal	
915_5dBm				100p			13.000	
915_8dBm				100p			13.000	
915_10dBm	1p5	68p	4p7	100p	9n5	8n7	13.000	
Tolerance	± 0.1 pF	± 2%	± 0.1 pF	± 2%	± 2%	± 2%		

4 Electrical Characteristics

4.1 Absolute Maximum Ratings

Attention: Stresses above the maximum values listed below may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit.

Table 7 Absolute Maximum Ratings

	Parameter	Symbol	Values			Unit	Note/ Test Condition
			min.		max.		
A1	Supply voltage	V_{BAT}	-0.3	-	+4	V	
A2	Junction Temperature	T_j	-40		+125	°C	
			-40	-	+150		1) Max. 24 hrs. by Tmax. accumulated over lifetime 2)V_{BAT} =3,6V
A3	Storage Temperature	T_s	-50	-	+150	°C	Max 1000 hours by Tmax or Tmin
A4	Transient Temperature	T_{tran}		-	+175	°C	Max 180 sec, 10 x Tcycles over lifetime.
A5	ESD HBM integrity (all pins except pin 6, RF-PA output)	V_{HBM}	-4	-	+4	kV	Acc. to JEDEC EIA /JESD22-A114-B
A6	ESD HBM integrity (pin 6)	V_{HBMRF}	-4	-	+4	kV	Acc. to JEDEC EIA /JESD22-A114-B
A7	ESD SDM integrity	V_{SDM}	-500	-	+500	V	All pins except corner pins
			-750	-	+750	V	All corner pins
A8	Latch up	I_{LU}	100	-		mA	AEC-Q100 (transient current)

	Parameter	Symbol	Values			Unit	Note/ Test Condition
			min.		max.		
A9	Maximum Input Voltage @ digital input pins	V_{in}	-0.3	-	V_{BAT} + 0.3	V	
A10	Maximum Current into digital input and output pins	I_{IOmax}		-	4	mA	Note 1
A11	Maximum Input Voltage @ XTAL pin (pin 2)	$V_{In,XTAL}$	-0,3		V_{REG} + 0.3		Note 2

Note1: It is not allowed to apply higher voltages than specified by A9, even if current is limited to values below A10. The voltage limiting effect of the internal ESD structures must not be used as “level shifter” by interconnection(s) to digital logic with higher output voltage!

Note2: V_{REG} is the output voltage of the internal voltage regulator, accessible on pin 4, (VREG).

4.2 Operating Range

Table 8 Supply Voltage Operating Range and Temperature Operating Range

	Parameter	Symbol	Values			Unit	Note/ Test Condition
			min.	typ	max.		
B1	Supply Voltage	V_{BAT}	1.9	-	3.6	V	[-40..+85]°C
B2	Operating Temperature	T_{amb}	-40	-	+85	°C	

4.2.1 AC/DC Characteristics

Supply voltage V_{BAT} = 1.9V ... 3.6V; Ambient temperature T_{amb} =[-40...+85] °C, unless otherwise specified. Maximum 10 pF capacitive load at CLKOUT (pin 8).

Frequency of clock on CLKOUT (pin 8), $f_{CLKOUT} = f_{XTAL} / 16$.

Attention: Test ■ means that the parameter is not subject to production test. It was verified by design and/or characterization.

Table 9 AC/DC Characteristics

Pin #	Parameter	Symbol	Limit Values			Unit		Test Conditions Remarks
			min	typ	max			
C1	Transmit Frequency Bands	f_{TX}	300 425 863		320 450 928	MHz MHz MHz		
C2	Modulation Types		ASK (OOK), FSK(CPFSK), GFSK					
C3	Encoding Modes		Manchester, differential Manchester, Miller, Biphase-mark, Biphase-space, scrambled NRZ					
C4	Chip Rate		0.5		100	kchip/s	■	See **Chapter 2.4.4** for chip rate definition
C5	Carrier Frequency Step	f_{step}			7	Hz	■	f_{XTAL} / 2exp(21)
C6	Frequency Deviation (Programmable)	f_{dev}	1		64	kHz	■	See **Chapter 2.4.7** for frequency shift calculation
C7	Crystal Frequency Range	f_{XTAL}	12		14	MHz	■	Total max. cap. (including parasitics) between XTAL (pin2) and GND max. 4 pF
C8	Crystal Osc Margin	R_{START} [1)]	|-500|			Ohm		1)$f_{crystal}$ = 13,56 MHz T_{amb} = 25 °C
		L_{OSC}	3.85	5.5	7.15	µH		
C9	XTAL Startup Time	t_{XTAL}			1	ms		with crystal NDK NX5032SA on TDA5150 Evaluation Board

Pin #	Parameter	Symbol	Limit Values			Unit		Test Conditions Remarks
			min	typ	max			
C10	CLKOUT Output Frequency	f_{CLKOUT}			14	MHz		For divider ratio calculations see **Chapter 2.4.5.1**
C11	Voltage Regulator Output Voltage	V_{REG}		2.1 1) 2)		V		100 nF decoupling on VREG pin. No external DC load allowed 1)V_{BAT} =3V@27°C 2)$V_{BAT} \geq$ 2.2 V for effective regulator operation
C12	Supply Current Sleep Mode	I_{sleep}		0.4 1)	2.5 2)	µA		1)by T=27°C 2)by Tmax=85°C
C13	Supply Current Standby Mode	$I_{standby}$		0.5 1)	6 2)	µA		1)by T=27°C 2)by Tmax=85°C
C14	Low-Battery Detector Threshold	$V_{LBD\_2.1}$	2.0	-	2.2	V		monitored @V_{BAT}
		$V_{LBD\_2.4}$	2.3	-	2.5	V		
C15	Brownout Detector Voltage Threshold	V_{BOD}	1.7	-	1.8	V		in Active Mode monitored @V_{REG}
		V_{BOD}	0.7	-	1.7	V		in Standby Mode monitored @V_{REG} and @V_{BAT}
C16	Supply Current PLL is ON PA is OFF @315/434 MHz	$I_{pllenable}$		6,3	8	mA		V_{BAT} =3V
C17	Supply Current PLL is ON PA is OFF @868/915MHz	$I_{pllenable}$		6,6	8,5	mA		V_{BAT} =3V
C18	Supply Current Transmit Mode @315/434 MHz	I_{T5dbm}		9	12	mA	1)	1)@P_{out}=5/8/10 dBm measured with 50 Ohms load 2)V_{BAT} =3V
		I_{T8dbm}		11	14	mA	2)	
		I_{T10dbm}		13	16	mA		

Pin #	Parameter	Symbol	Limit Values			Unit		Test Conditions Remarks
			min	typ	max			
C19	Supply Current Transmit Mode @868/915 MHz	I_{T5dbm}		11	14	mA	1)	1)@P_{out}=5/8/10 dBm measured into 50 Ohms load 2) V_{BAT}=3V
		I_{T8dbm}		13	16	mA	2)	
		I_{T10dbm}		16	19	mA		
C20	Power Level Tolerance vs. nominal value	$P_{var5dbm}$	-1.5		+1.5	dB	1)	Referenced to V_{BAT}=3V @27°C (not including matching network comp. tolerance) 1)315 & 434 MHz band 2)868 & 915 MHz band
		$P_{var8dbm}$					1)	
		$P_{var10dbm}$					1)	
		$P_{var5dbm}$	-2		+2	dB	2)	
		$P_{var8dbm}$					2)	
		$P_{var10dbm}$					2)	
C21	Power Level Variation vs. temperature	$P_{var5dbm}$	-1.5		+1.5	dB	■	T_{amb} =[-40..+85]°C V_{BAT}= 3 Volt RF P_o measured on Evaluation Board
		$P_{var8dbm}$	-1.5		+1.5	dB	■	
		$P_{var10dbm}$	-1.5		+1.5	dB	■	
C22	Power Level Variation vs. battery voltage	$P_{var5dbm}$		5.5	7	dB		V_{BAT}=[1.9...3.6] V RF P_o measured on IFX Evaluation Boards
		$P_{var8dbm}$		5.5	7	dB		
		$P_{var10dbm}$		5.5	7	dB		
C23	Power Level Step Size	$P_{delta\ step}$	1	2	3	dB		maximum 10 steps
C24	PLL bandwidth		150[1)]		410[1)]	kHz	■	1) the PLL BW is programable. SFR **CPTRIM** (0x24.3:0) controls the chargepump current and SFR **PLLBW TRIM** (0x25.6:4)fis the selector for loop filter damping resistor value 150 kHz is the smallest and 410 kHz the largest **nominal** PLL BW. See **Table2** for **PLL recommended settings**

Pin #	Parameter	Symbol	Limit Values			Unit		Test Conditions Remarks
			min	typ	max			
C25	Band Switching Time	$t_{bandswitch}$			100	us		jump between band end frequencies [f_{min} .. f_{max}]
C26	Channel Switching Time	$t_{chswitch}$		20		us	■	1 MHz hop away from adj. channel
C27	SSB Phase Noise @ 315/434 MHz PLLBW = 150 kHz			-86	-80	dBc/Hz		@ 10 kHz offset, +27°C
				-86	-80	dBc/Hz		@ 100 kHz offset, +27°C
				-105	-100	dBc/Hz	■	@ 1 MHz offset, +27°C
				-135	120	dBc/Hz	■	@ 10 MHz offset, +27°C
C28	SSB Phase Noise @ 868/915MHz PLLBW = 150 kHz			-80	-75	dBc/Hz		@ 10 kHz offset, +27°C
				-80	-75	dBc/Hz		@ 100 kHz offset, +27°C
				-105	-100	dBc/Hz	■	@ 1 MHz offset, +27°C
				-135	-120	dBc/Hz	■	@ 10 MHz offset, +27°C

4.3 SPI Characteristics

Attention: Test ■ means that the parameter is not subject to production test. It was verified by design and/or characterization.

Table 10 SPI Timing Characteristics

	Parameter	Symbol	Values			Unit		Note/ Test Condition
			min	typ	max			
D1	Clock Frequency	f_c			2	MHz	■	
D2	Clock High Time	t_{CH}	150			ns	■	
D3	Clock Low Time	t_{CL}	150			ns	■	
D4	Active SetUp Time	t_{SSu}	20			ns	■	
D5	Not Active Hold Time	t_{EN}	20			ns	■	
D6	Active Hold Time	t_{SHo}	20			ns	■	
D7	Not Active SetUp Time	t_{NEN}	20			ns	■	
D8	Deselect Time	t_{DS}	150			ns	■	
D9	Input Data SetUp Time	t_{IDSu}	50			ns	■	
D10	Input Data Hold Time	t_{IDHo}	50			ns	■	
D11	Clock to Output Data Valid @ 20pF Load	t_{CODV}			150	ns	■	
D12	Output Data Rise Time @ 20pF Load	t_{ODri}			25	ns	■	
D13	Output Data Fall Time @ 20pF Load	t_{ODfa}			25	ns	■	

	Parameter	Symbol	Values			Unit		Note/ Test Condition
			min	typ	max			
D14	Input Data Tristate Setup Time	t_{IDZSu}	0			ns		
D15	Output Data Disable Time	t_{NODZ}			150	ns		

Table 11 SPI Electrical Characteristics

	Parameter	Symbol	Values			Unit		Note/ Test Condition
			min	typ	max			
E1	Input Low Voltage	V_{IL}	-0.2	-	0.4	V		Pins EN, SCK, SDIO
E2	Input High Voltage	V_{IH}	V_{BAT} - 0.4	-	V_{BAT} + 0.2	V		Pins EN, SCK, SDIO
E3	Output Low Voltage	V_{OH}			0.5	V		Pins SDIO, CLKOUT
E4	Output High Voltage	V_{OH}	V_{BAT} - 0.5			V		Pins SDIO, CLKOUT
E5	Parasitic capacitance	C_{pad}			5	pF	■	
E6	Internal Pull-down Resistor	R_{down}	175	250	360	kOhm		

5 Package Outline

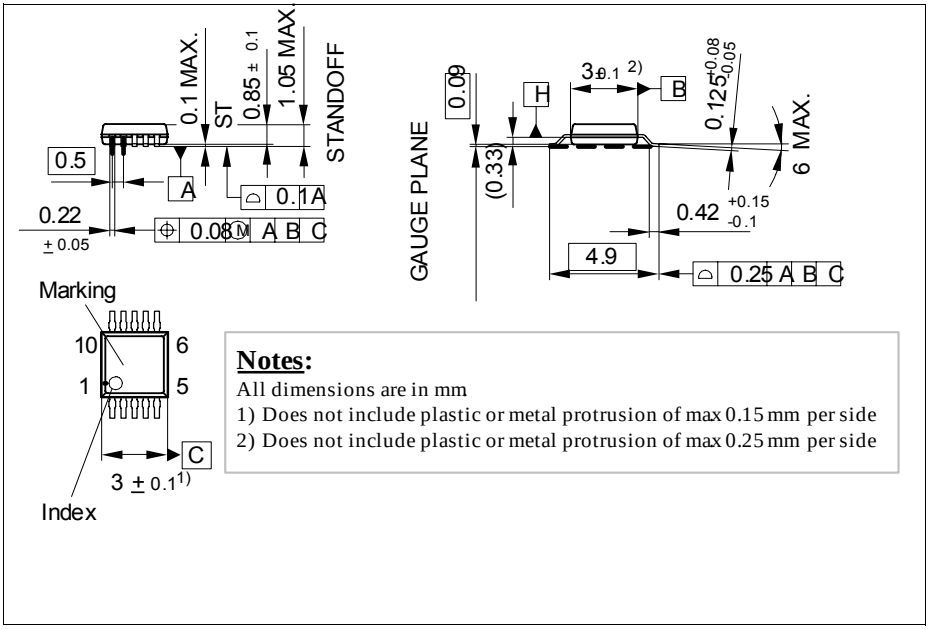

Figure 31 Green Package TSSOP-10 outline

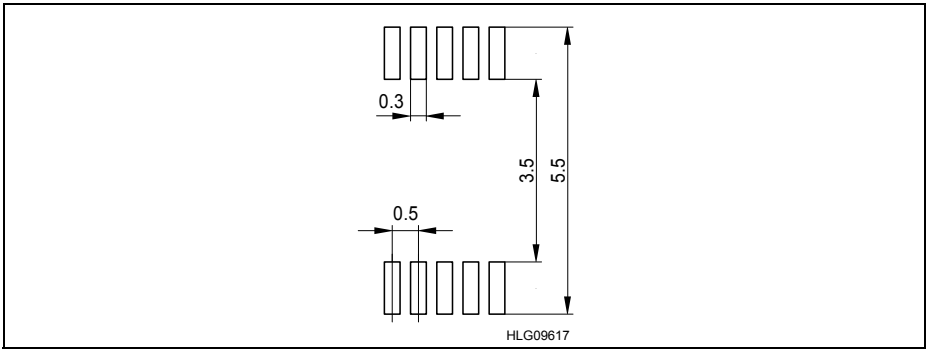

Figure 32 Footprint TSSOP-10 package

You can find all of our packages, types of packing and other information on the Infineon Internet Page “Products”:**http://www.infineon.com/products**

SMD = Surface Mounted Device

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