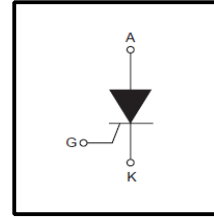


Sensitive Gate Silicon Controlled Rectifiers

Features

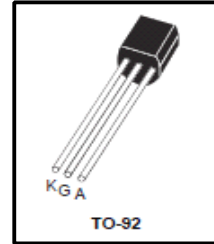
- Sensitive gate trigger current: $I_{GT}=200\mu\text{A}$ maximum
- Low on-state voltage: $V_{TM}=1.2(\text{typ.})@ I_{TM}$
- Low reverse and forward blocking current:
 $I_{DRM}/I_{PRM}=100\mu\text{A}@TC=125^\circ\text{C}$
- Low holding current: $I_H=5\text{mA}$ maximum



General Description

Sensitive triggering SCR is suitable for the application where gate current limited such as microcontrollers, logic integrated circuits, small motor control, gate driver for large SCR, sensing and detecting circuits.

General purpose switching and phase control applications



Absolute Maximum Ratings (T_j=25°C unless otherwise specified)

Symbol	Parameter		Value	Units	
V_{DRM}/V_{RRM}	Repetitive peak off-state voltage		Note(1)	400	V
$I_{T(RMS)}$	RMS on-state current (180° conduction angles)	T _I =85°C	0.8	A	
$I_{T(AV)}$	Average on-state current (80° conduction angles)	T _I =85°C	0.5	A	
I_{TSM}	Non repetitive surge peak on-state current	tp = 8.3 ms	9	A	
		tp = 10 ms	8		
I^2t	I ² t Value for fusing	tp = 8.3 ms	0.41	A ² s	
P_{GM}	Peak gate power		2	W	
di/dt	Critical rate of rise of on-state current $I_{TM} = 2\text{A}; I_G = 10\text{mA}; di_G/dt = 100\text{mA}/\mu\text{s}$	T _J =125°C	50	A/μs	
$P_{G(AV)}$	Average gate power dissipation		T _J =125°C	0.1	W
I_{FGM}	Peak gate current		T _J =125°C	1	A
V_{RGM}	Peak gate voltage		T _J =125°C	5	V
T _J	Junction temperature			-40~125	°C
T _{stg}	Storage temperature			-40~150	°C

Note1: Although not recommended, off-state voltages up to 800 V may be applied without damage, but the thyristor may switch to the on-state. The rate of rise of current should not exceed 15 A/μs.

Thermal Characteristics

Symbol	Parameter	Value			Units
		Min	Typ	Max	
R _{QJC}	Thermal resistance, Junction-to-Case	-	-	60	°C/W
R _{QJA}	Thermal resistance, Junction-to-Ambient	-	-	150	°C/W

Electrical Characteristics ($T_J = 25^\circ\text{C}$, $R_{GK} = 1\text{ k}\Omega$ unless otherwise specified)

Symbol	Characteristics	Min	Typ.	Max	Unit	
I_{DRM}/I_{RRM}	off-state leakage current ($V_{AK} = V_{DRM}/V_{RRM}$)	$T_c=25^\circ\text{C}$	-	-	1	μA
		$T_c=125^\circ\text{C}$			100	
V_{TM}	Forward "On" voltage ($I_{TM} = 1\text{ A}$ tp = 380 μs) (Note2.1)	-	1.2	1.7	V	
I_{GT}	Gate trigger current (continuous dc) (Note2.2) ($V_{AK} = 7\text{ Vdc}$, $R_L = 100\ \Omega$)	15	-	200	μA	
V_{GT}	Gate Trigger Voltage (Continuous dc) (Note2.2) ($V_{AK} = 7\text{ Vdc}$, $R_L = 100\ \Omega$)	-	-	0.8	V	
V_{GD}	Gate threshold Voltage (Note2.1)	0.2	-	-	V	
dv/dt	Voltage Rate of Rise Off-State Voltage ($V_D=0.67V_{DRM}$; exponential waveform)	$T_J=125^\circ\text{C}$	500	800	-	V/ μs
		Gate open circuit		25		
I_H	Holding Current ($V_D = 12\text{ V}$; $I_{GT} = 0.5\text{ mA}$)	-	2	5	mA	
I_L	latching current ($V_D = 12\text{ V}$; $I_{GT} = 0.5\text{ mA}$)	-	2	6	mA	
R_d	Dynamic resistance					
		$T_J=125^\circ\text{C}$	-	-	245	m Ω

Note 2.1 Pulse width \leq 1.0ms,duty cycles \leq 1%
 2.2 R_{GK} current is not included in measurement.

Fig 1. Gate Characteristics

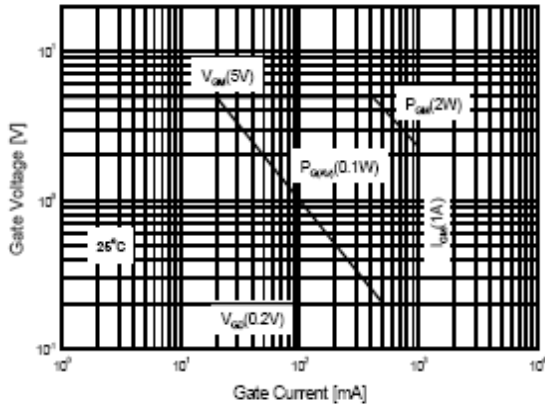


Fig 2. Maximum Case Temperature

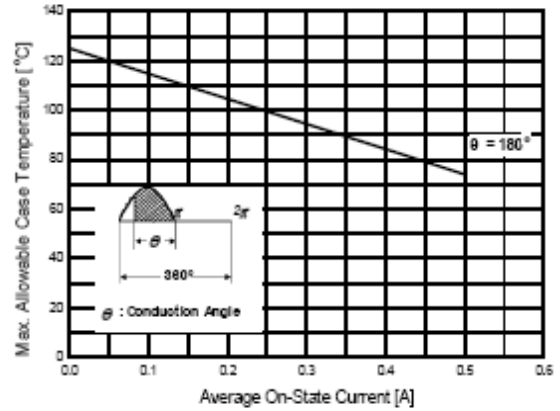


Fig 3. Typical Forward Voltage

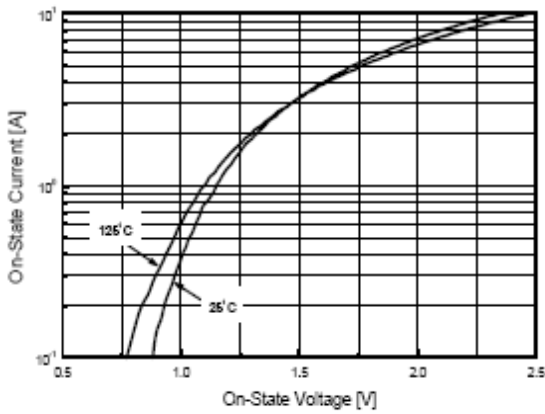


Fig 4. Thermal Response

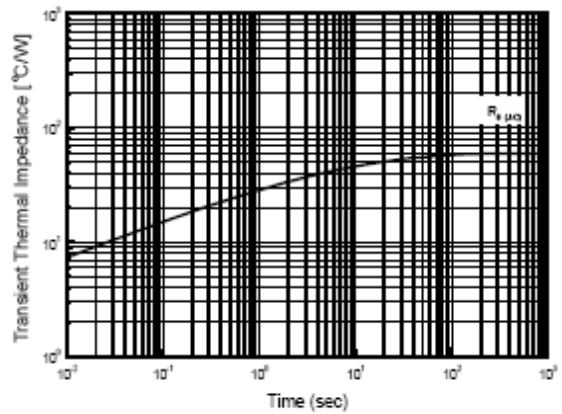


Fig 5. Typical Gate Trigger Voltage vs. Junction Temperature

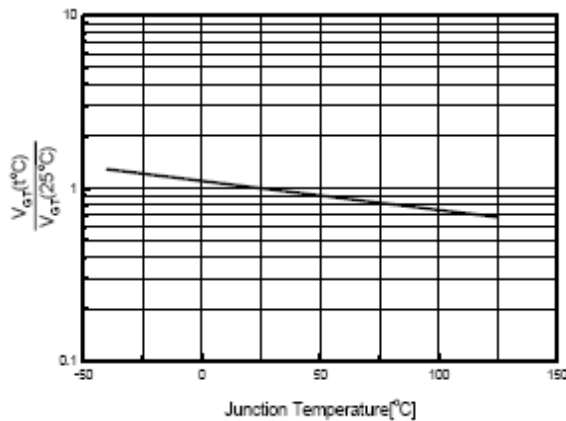


Fig 6. Typical Gate Trigger Current vs. Junction Temperature

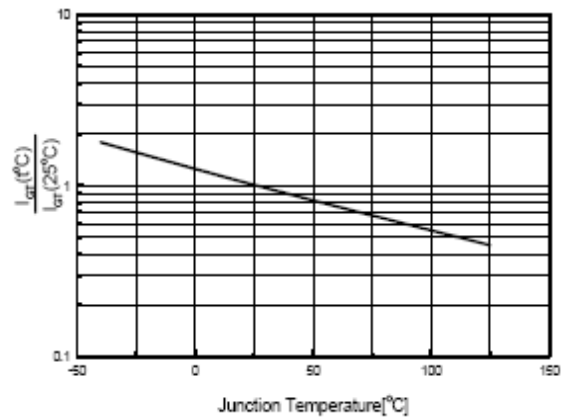


Fig 7. Typical Holding Current

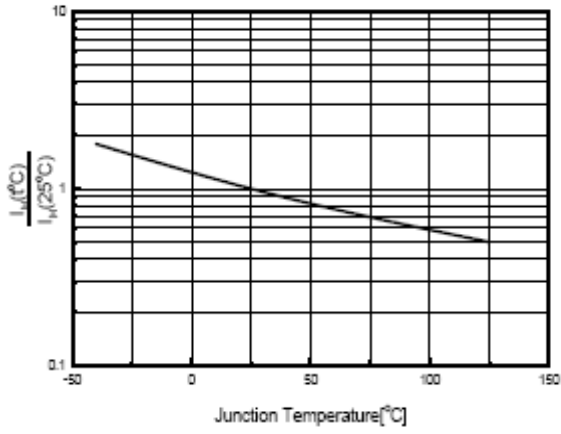
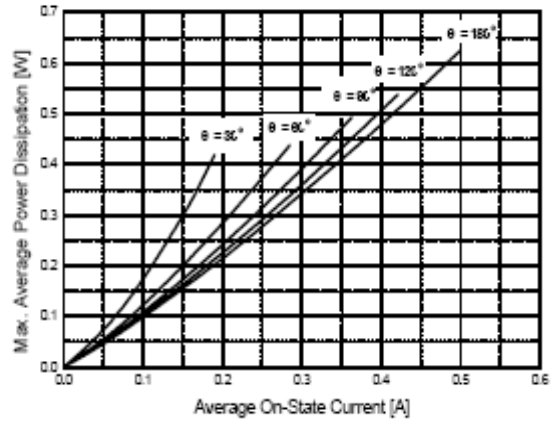


Fig 8. Power Dissipation



TO-92 Package Dimension

