AN-6073

FAN6751 — Highly Integrated Green-Mode PWM Controller

Introduction

This application note describes a detailed design strategy for a high-efficiency, compact flyback converter. Design considerations and mathematical equations are presented as well as guidelines for a printed circuit board layout. The highly integrated FAN6751 series of PWM controllers provides several features to enhance the performance for LCDM/TV, NB, and adapters.

The green-mode function includes off-time modulation and burst mode to reduce the PWM frequency at light-load and in no-load conditions. To avoid acoustic noise problems, the minimum PWM frequency is set above 18KHz. This green-mode function enables the power supply to meet international power conservation requirements. With the internal high-voltage startup circuitry, the power loss due to bleeding resistors is also eliminated. Built-in synchronized slope compensation achieves stable peak-current-mode control. The proprietary external line compensation ensures constant output power limit over a wide AC input voltage range, from $90V_{AC}$ to $264V_{AC}$.

FAN6751 provides many protection functions, as shown in Table 1. In addition to cycle-by-cycle current limiting, the internal open-loop protection circuit ensures safety should an open-loop or output short-circuit failure occur.

Features

- High-Voltage Startup
- Low Operating Current: 4mA
- Linearly Decreasing PWM Frequency to 18KHz
- Fixed PWM Frequency: 65KHz
- Peak-Current-Mode Control
- Cycle-by-Cycle Current Limiting
- Leading-Edge Blanking (LEB)
- Synchronized Slope Compensation
- Internal Open-loop Protection
- GATE Output Maximum Voltage Clamp: 18V
- V_{DD} Under-Voltage Lockout (UVLO)
- V_{DD} Over-Voltage Protection (OVP)
- Internal Recovery Circuit (OVP, OLP)
- Internal Sense Short-Circuit Protection
- External Constant Power Limit (Full AC Input Range)
- Internal OTP Sensor with Hysteresis
- Built-in 5ms Soft-Start Function
- Built-in VIN Pin Pull HIGH (> 4.7V) Recovery Function for Second-Side Output OVP
- Brownout Protection with Hysteresis

Applications

General-purpose, switch-mode power supplies and flyback power converters, including:

- Power Adapters
- Open-frame SMPS
- LCD Monitor/TV

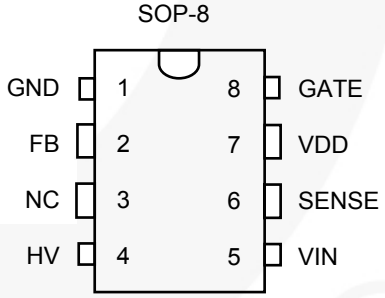

Figure 1. Pin Configuration (Top View)

Table 1. Protection Functions of FAN6751 Series

Part Number	OVP (V_{DD})	OLP (FB)	Pull-High Protection (V_{IN})	OTP (Internal)	SCP (SENSE)	PWM Frequency
FAN6751MRMY	Recovery	Recovery	Recovery	Recovery	Recovery	65KHz
FAN6751HLMY	Latch	Latch	Latch	Recovery	Recovery	100KHz

Typical Application

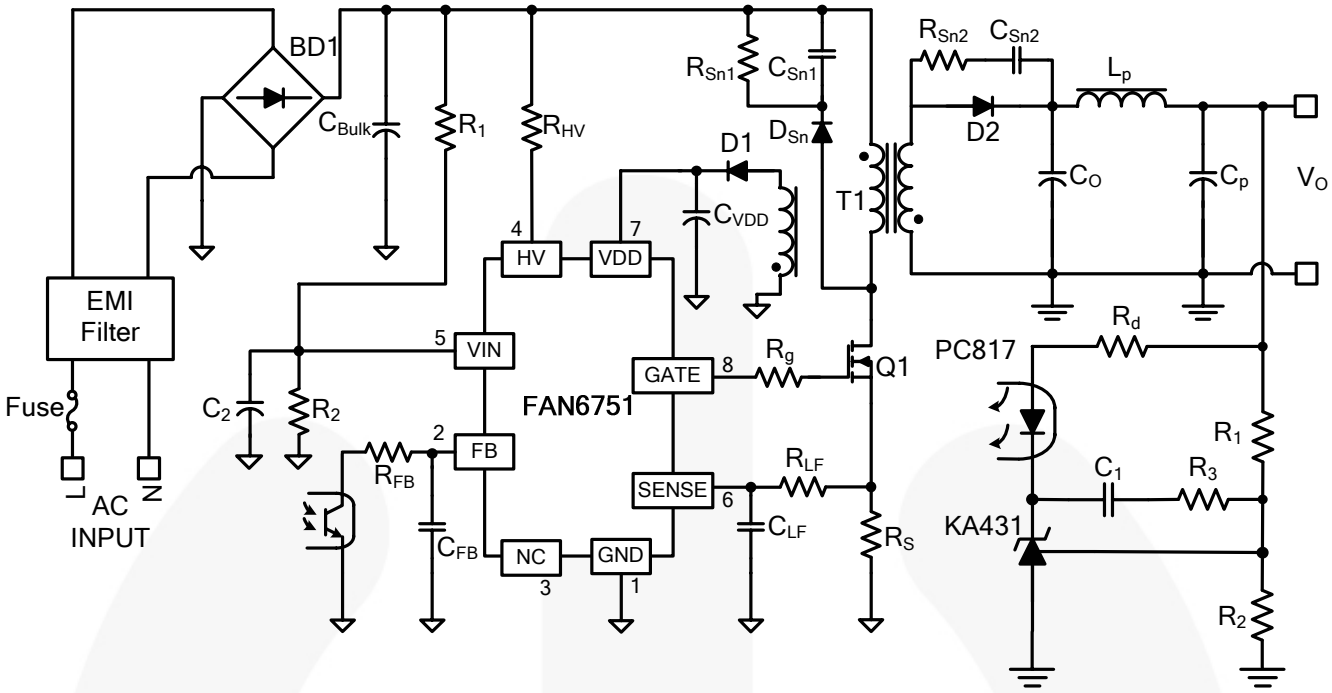

Figure 2. Typical Application

Block Diagram

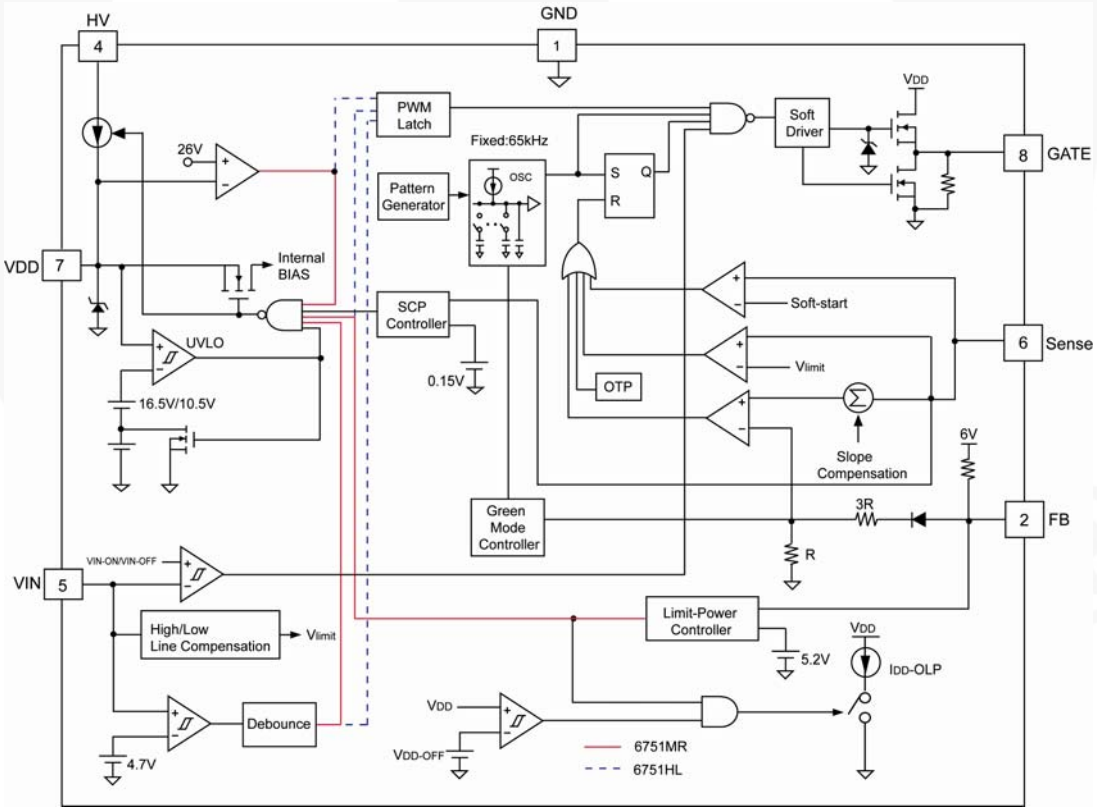

Figure 3. Functional Block Diagram

Internal Block Operation

Startup and Soft-Start Circuitry

When power is turned on, the internal high-voltage startup current (typically 2mA) charges the hold-up capacitor C_1 through startup resistor R_{HV}. R_{HV} can be directly connected by V_{BULK} to the HV pin. The built-in 5ms soft-start circuit starts when the VDD pin reaches the start threshold voltage V_{DD-ON}. Soft-start helps reduce the inrush current, the startup current spike, and output voltage overshoot during the startup period, as shown in Figure 4. When V_{DD} reaches V_{DD-ON}, the internal high-voltage startup current is switched off and the supply current is drawn from the auxiliary winding of the main transformer, as shown in Figure 5.

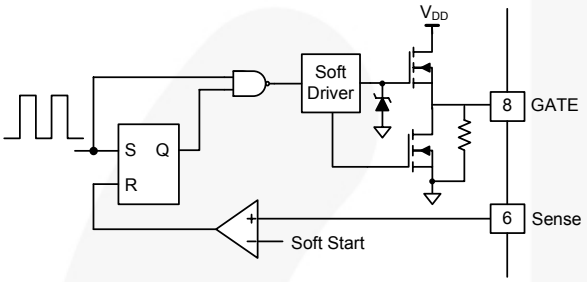

Figure 4. Soft-start Circuit

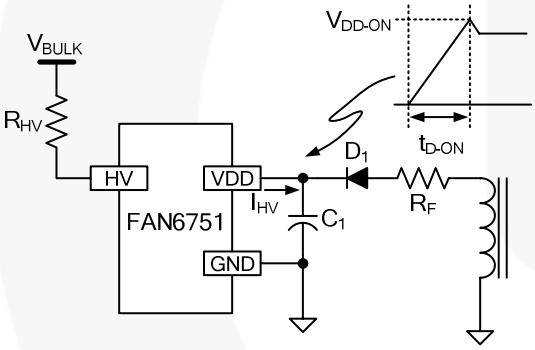

Figure 5. Startup Circuit for Power Transfer

If a shorter startup time is required, a two-step startup circuit, as shown Figure 6, is recommended. In this circuit, a smaller capacitor C_1 can be used to reduce startup time. The energy supporting the FAN6751 after startup is mainly from a larger capacitor C_2. If a shorter releasing latch mode time is required, a D_{HV} and R_{HV} can be directly connected by V_{AC} to the HV pin.

When the supply current is drawn from the transformer, it draws a leakage current of about 1μA from HV pin. The maximum power dissipation of the R_{HV} is:

$$P_{RHV} = I_{HV-LC}^{2} \times R_{HV} = I\mu A^2 \times 100K\Omega \cong 0.1\mu W \quad (1)$$

where

I_{HV-LC} is the supply current drawn from HV pin, and

R_{HV} is 100KΩ.

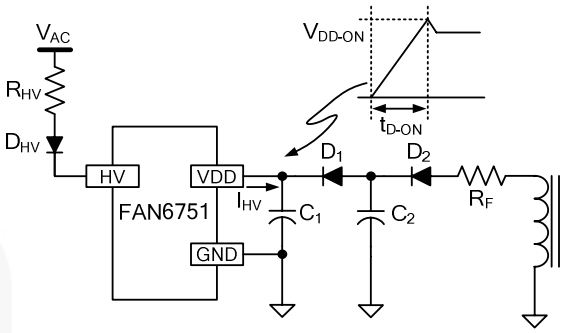

Figure 6. UVLO Specification

Under-Voltage Lockout (UVLO)

The FAN6751 has a voltage detector on the V_{DD} pin to ensure that the chip has enough power to drive the MOSFET. Figure 7 shows a hysteresis of the turn-on and turn-off threshold levels and an open-loop-release voltage.

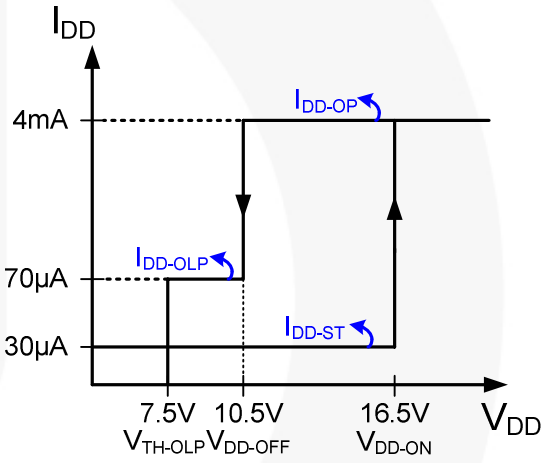

Figure 7. UVLO Specification

The turn-on and turn-off thresholds are internally fixed at 16.5V and 10.5V. During startup, the V_{DD}'s capacitor must be charged to 16.5V to enable the IC. The capacitor continues to supply the V_{DD} until the energy can be delivered from the auxiliary winding of the main transformer. The V_{DD} must not drop below 10.5V during the startup sequence.

To further limit the input power under a short-circuit or open-loop condition, a special two-step UVLO mechanism prolongs the discharge time of the V_{DD} capacitor. Figure 8 shows the traditional UVLO method along with the special two-step UVLO method. In the two-step UVLO mechanism, an internal sinking current, I_{DD-OLP}, pulls the V_{DD} voltage toward the V_{DD-OLP}. This sinking current is disabled after the V_{DD} drops below V_{DD-OLP}; after which, the V_{DD} voltage is again charged towards V_{DD-ON}. With the addition of the two-step UVLO mechanism, the average input power during a short-circuit or open-loop condition is greatly reduced. As a result, over-heating does not occur.

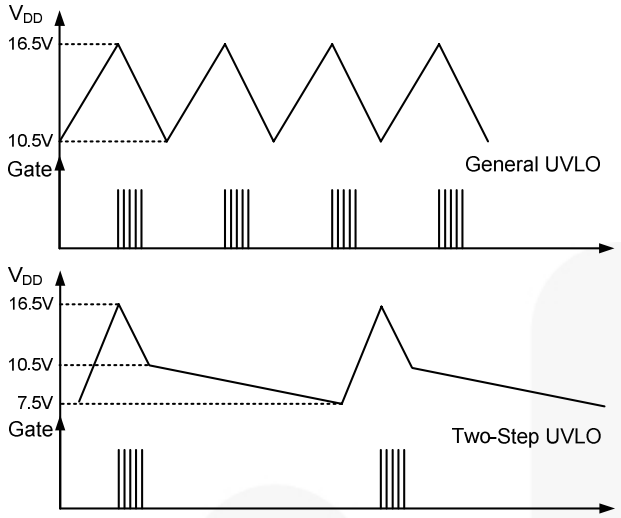

Figure 8. UVLO Effect

FB Input

The FAN6751 is designed for peak-current-mode control. A current-to-voltage conversion is done externally with a current-sense resistor R_S. Under normal operation, the FB level controls the peak inductor current:

$$V_{SENSE} = I_{pk} \times R_S = \frac{V_{FB} - 0.6}{4} \quad (2)$$

where V_{FB} is the voltage on FB pin and 4 is an internal divider ratio.

When V_{FB} is less than 0.6V, the FAN6751 terminates the output pulses.

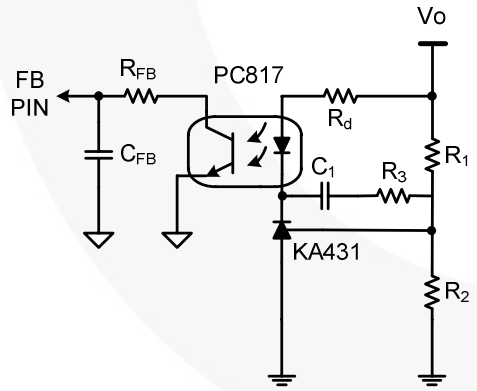

Figure 9. Feedback Circuit

Figure 9 is a typical feedback circuit consisting mainly of a shunt regulator and an opto-coupler. R_1 and R_2 form a voltage divider for the output voltage regulation. R_3 and C_1 are adjusted for control-loop compensation. A small-value RC filter (e.g. R_{FB}= 100Ω, C_{FB}= 1nF) placed on the FB pin to the GND can further increase the stability. The maximum sourcing current of the FB pin is 1.5mA. The phototransistor must be capable of sinking this current to pull FB level down at no load. The value of the biasing resistor R_b is determined as:

$$\frac{V_o - V_D - V_Z}{R_b} \bullet K \geq 1.5mA \quad (3)$$

where:

V_D is the drop voltage of photodiode, approximately 1.2V;
V_Z is the minimum operating voltage, 2.5V of the shunt regulator; and
K is the current transfer rate (CTR) of the opto-coupler.

For an output voltage V_O=5V with CTR=100%, the maximum value of R_b is 860Ω.

Green Mode Operation

Green mode includes off-time modulation and burst mode to reduce the PWM frequency at light-load and in no-load conditions. The feedback voltage of the FB pin is taken as a reference. When the feedback voltage is lower than V_{FB-N}, the PWM frequency decreases. Because most losses in a switching-mode power supply are proportional to the PWM frequency, the off-time modulation reduces the power consumption of the power supply at light-load and no-load conditions. Figure 10 is the PWM frequency is 65KHz at nominal load and decreases to 18KHz at light load.

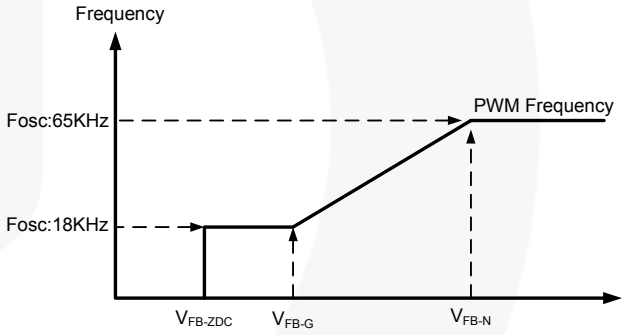

Figure 10. PWM Frequency vs. FB Voltage

The power supply enters "burst mode" in no-load conditions. As shown in Figure 11 and Figure 12, when V_{FB} drops below V_{FB-ZDC}, the PWM output is shuts off and the output voltage drops at a rate dependent on load current. This causes the feedback voltage to rise. Once V_{FB} exceeds V_{FB-ZDC}, the internal circuit starts to provide switching pulse. The feedback voltage then falls and the process repeats. Burst mode operation alternately enables and disables switching of the MOSFET, reducing the switching losses in standby mode.

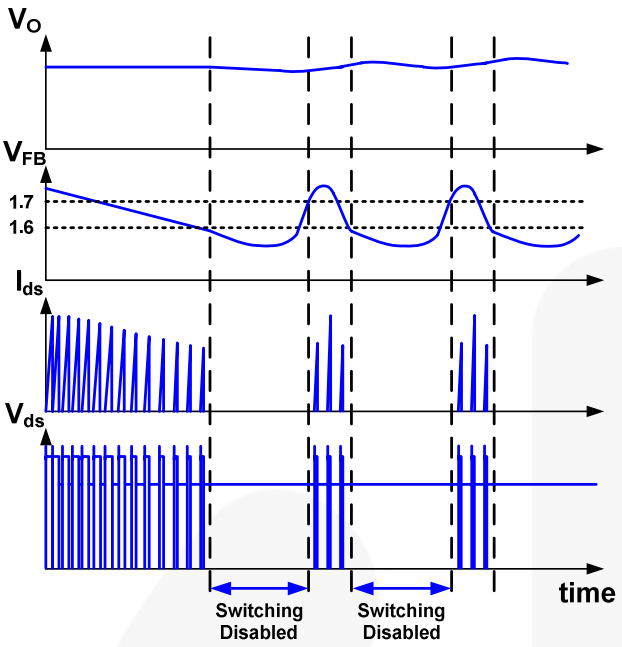

Figure 11. FAN6751HL Burst-mode Operation

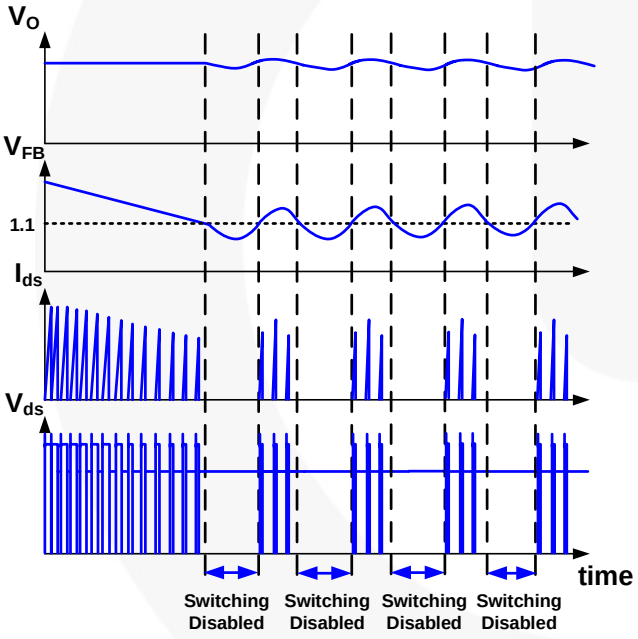

Figure 12. FAN6751MR Burst-Mode Operation

Built-in Slope Compensation

A flyback converter can be operated in either discontinuous current mode (DCM) or continuous current mode (CCM). There are many advantages when operating the converter in CCM. With the same output power, a converter in CCM exhibits a smaller peak inductor current than in DCM. Therefore, a small-sized transformer and a low-rated MOSFET can be applied. On the secondary side of the transformer, the RMS output current of DCM can be twice that of CCM. Larger wire gauge and output capacitors with larger ripple current ratings are required. DCM operation also results in a higher output voltage spike. A large LC filter is added. Therefore, a flyback converter in CCM achieves better performance with lower component cost.

Despite the above advantages of CCM operation, there is one concern—stability. In CCM operation, the output power is proportional to the average inductor current, while the peak current remains controlled. This causes sub-harmonic oscillation when the PWM duty cycle exceeds 50%. Adding slope compensation (reducing the current-loop gain) is an effective way to prevent oscillation. The FAN6751 introduces a synchronized positive-going ramp (V_{SLOPE}) in every switching cycle to stabilize the current loop. Therefore, the FAN6751 can be used to design a cost-effective, highly efficient, compact flyback power supply operating in CCM without additional external components.

The positive ramp added is:

$$V_{SLOPE} = V_{SL} \bullet D \quad (4)$$

where V_{SL} = 0.33V and D = duty cycle.

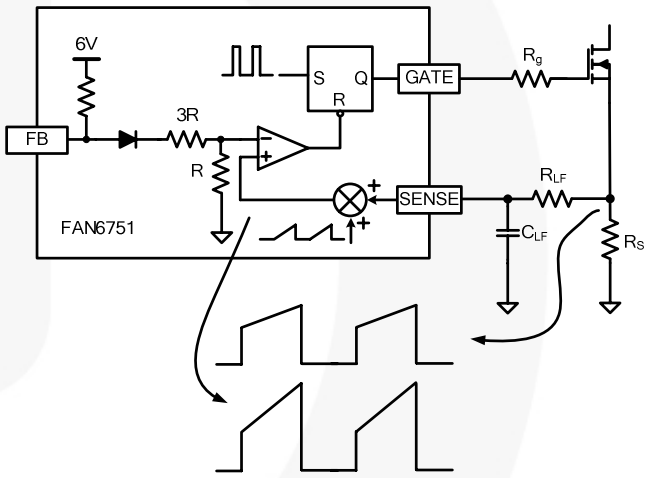

Figure 13. Synchronized Slope Compensation

Over-Power Compensation

The maximum output power of a flyback converter can generally be designed by the current-sense resistor R_S. When the load increases, the peak inductor current increases accordingly. As the current-sense signal of the SENSE pin exceeds the internal limit V_{SENSE}, 0.83V typically, as V_{IN}=1V, FAN6751 stops the PWM pulse immediately. The output power of a flyback power supply in DCM is calculated as follows:

$$P_{OUT} = \frac{1}{2} \bullet L_P \bullet I_{PK}^2 \bullet f_S \bullet \eta \quad (5)$$

where:
L_p is the transformer primary-side inductance;
I_{PK} is the peak inductor current;
f_S is the PWM frequency; and
η is the conversion efficiency.

If the conversion efficiency remains unchanged for a wide input voltage range, the maximum output power would be the same for a fixed I_{PK}, which is limited by the internal current limiting threshold voltage V_{TH} and R_S. However, due to the time delay from the comparator to output stage inside the FAN6751, the maximum output power with high-line input is always higher than with low line. A 30% error is common for the universal input voltage range if the converter is operated in DCM. In CCM operation, the deviation becomes even larger. For the purpose of constant output power limit, the peak current limit V_{TH} must be adjustable according to the VIN pin, which is proportional to input voltage. V_{IN}=1V and V_{SENSE}=0.83V at low line; V_{IN}=3V and V_{SENSE}=0.7 at high line.

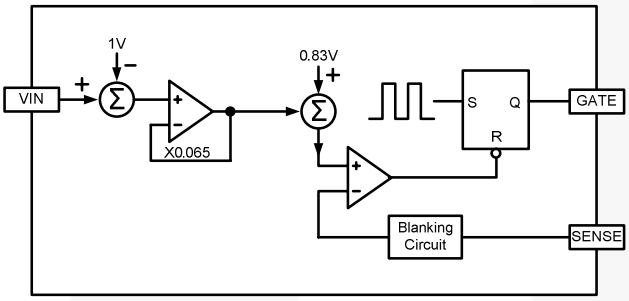

Figure 14. Universal Line Voltage Compensation for Constant Output Power Limit

Protection Functions

FAN6751 has protection functions in two categories: some enter Latch Mode and the others enter Recovery Mode. The Latch Mode can only be restart if V_{DD} falls below 5V, as shown Figure 15. The Recovery Mode lets V_{DD} decrease to UVLO mechanism until the fault condition removed, as shown Figure 16. Both modes prevent the SMPS from destructive states. Table 2 shows the relationship between protection functions and part numbers.

Table 2. Protection Functions

Protection Functions	FAN6751MR	FAN6751HL
V_{DD} Over-Voltage Protection (OVP)	Recovery	Latch
Overload Protection (OLP)	Recovery	Latch
Pull-High Protection Function by V_{IN} > 4.7V	Recovery	Latch
Internal Over Temperature Protection(OTP)	Recovery	Recovery
SENSE Pin Short-Circuit Protection	Recovery	Recovery
Brownout Protection	Recovery	Recovery

V_{DD} Over-Voltage Protection (OVP)

V_{DD} OVP has protection prevents damage due to over-voltage conditions. When the V_{DD} voltage exceed 26V due to abnormal conditions, PWM output is turned off until the V_{DD} voltage drops below UVLO then starts again (for MR) or Latched (for HL). OVP condition is usually caused by feedback open loops.

Overload Protection (OLP)

If the secondary output short circuits or the feedback loop is open, the FB pin voltage rises rapidly toward the open-loop voltage, $V_{FB-OPEN}$. If the FB voltage remains above V_{FB-OLP} and lasts for t_{D-OLP}, the FAN6751 stops emitting output pulses and enters Recovery Mode (for FAN6751MR) or latched-up mode (for FAN6751HL), as shown in Figure 17.

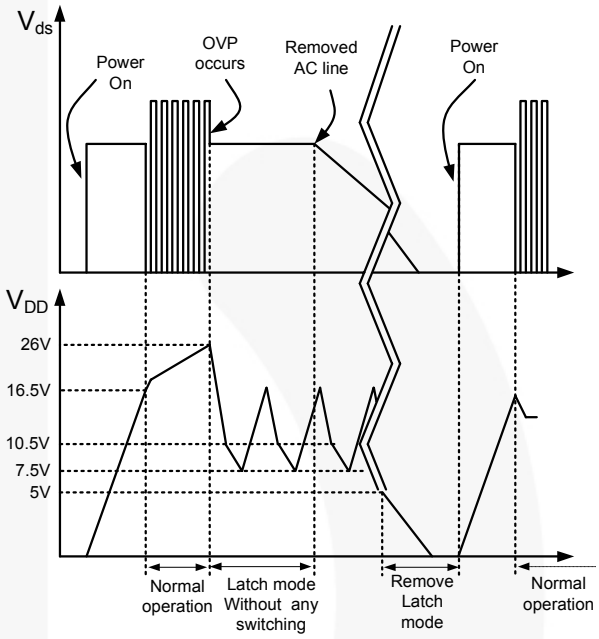

Figure 15.V_{DD} OVP Protection Waveforms for FAN6751HL, Latch Off

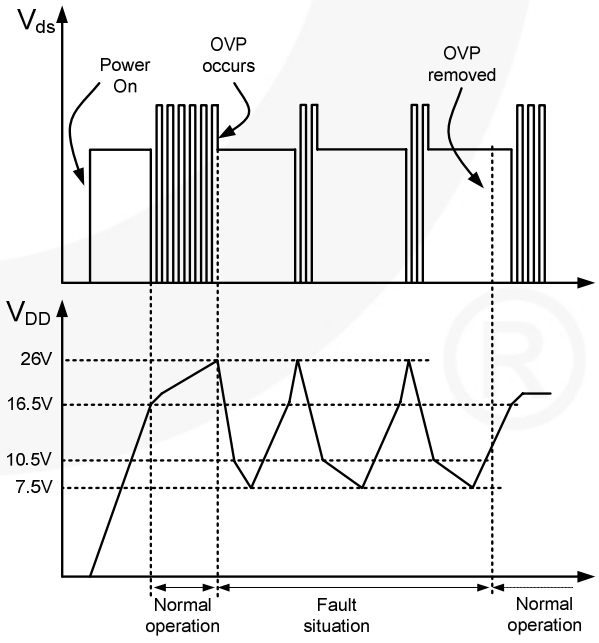

Figure 16. V_{DD} OVP Protection Waveforms for FAN6751MR, Recovery

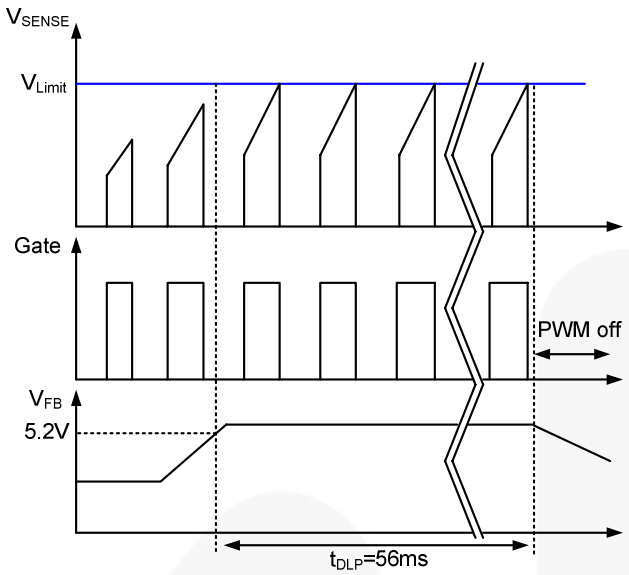

Figure 17. Overload Protection Waveforms

Pull-HIGH Protection Function in VIN Pin

The pull-high protection function is also included in the VIN pin. When V_{IN} is higher than 4.7V, FAN6751 latches up and stops regulating. Figure 18 shows the external latch circuit for secondary-side output OVP. If the output voltage (V_O) is higher than V_Z (Zener diode voltage), V_{DD} passes through the $R_{RESTRICT}$ to VIN pin (there are three Zener diodes to clamp this over-voltage at 6V) to achieve the latch mode.

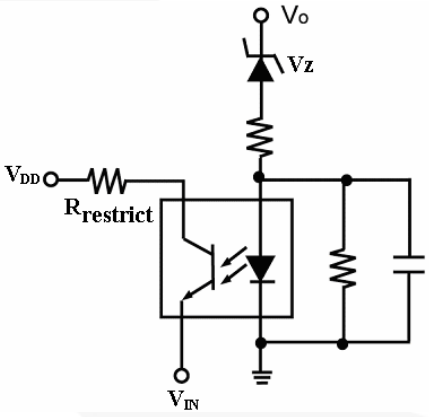

Figure 18. External Circuit for Second OVP

Internal Over-Temperature Protection (OTP)

The FAN6751 has a built-in temperature sensing circuit to shut down PWM output once the junction temperature exceeds 135°C. While PWM output is shut down, the V_{DD} voltage gradually drops to the UVLO voltage (around 7.5V). Then V_{DD} is charged up to the startup threshold voltage of 16.5V through the startup resistor until PWM output is restarted. This "hiccup" mode protection continues as long as the temperature remains above 130°C. The temperature hysteresis window for the OTP circuit is 25°C.

SENSE Pin Short-Circuit Protection

The FAN6751 provides a safety protection for power supply production. When the sense resistor is shorted by soldering during production, the pulse-by-pulse current limiting loses efficiency for the purpose of providing over-power protection of the unit. The unit may be damaged when the loading is larger than the original maximum load. To protect against a short circuit across the current-sense resistor, the controller immediately shuts down if a continuously low voltage (~0.15V/150µs) on the SENSE pin is detected.

Brownout Protection

Since the VIN pin is connected through a resistive divider to the rectified AC input line voltage, it can also be used for brownout protection. If the V_{IN} voltage is less than 0.7V, the PWM output is shut off. As the V_{IN} voltage reaches 0.92V, the PWM output is turned on again. The hysteresis window for ON/OFF is around 0.22V. The recommended values for R_{Bo1}, R_{Bo2}, and C_{Bo1} are 10M (5M+5M), 100K, and 2.2µF. Using these values in the test board, the power supply is turned off at 66V (maximum load) and recovered at 70V.

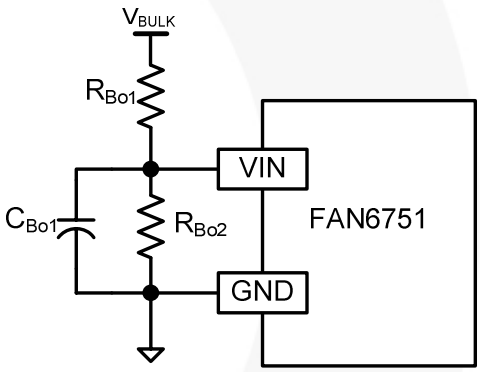

Figure 19. Circuit for Brownout

Leading-Edge Blanking (LEB)

A voltage signal proportional to the MOSFET current develops on the current-sense resistor R_S. Each time the MOSFET is turned on, a spike induced by the diode reverse recovery and by the output capacitances of the MOSFET and diode, appears on the sensed signal. Inside the FAN6751, a leading-edge blanking time of about 350ns helps avoid premature termination of MOSFET by the spike. Therefore, only a small-value RC filter (e.g. 100Ω + 470pF) is required between the SENSE pin and R_S. Still, a non-inductive resistor for the R_S is recommended.

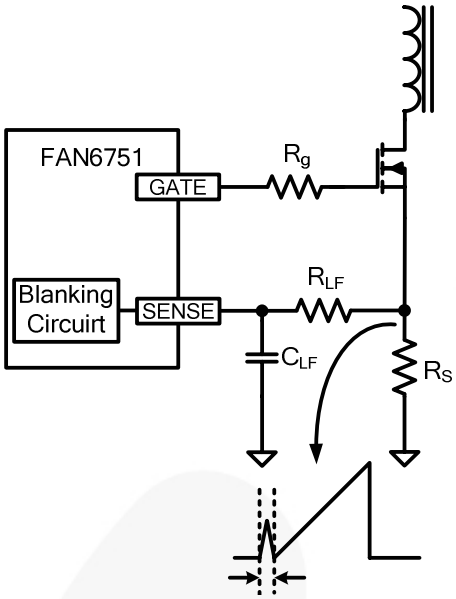

Figure 20. Turn-On Spike

Output Driver / Soft Driving

The FAN6751's output stage is a fast totem-pole gate driver capable of directly driving an external MOSFET. An internal Zener diode clamps the driver voltage under 18V to protect the MOSFET against over-voltage. By integrating special circuits to control the slew rate of switch-on rising time, the external resistor R_g may not be necessary to reduce switching noise, improving EMI performance.

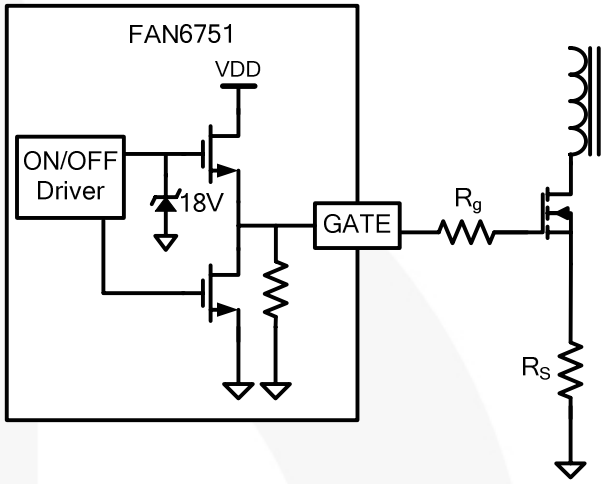

Figure 21. Gate Driver

Printed Circuit Board Layout

Current/voltage/switching frequency makes printed circuit board layout and design a very important issue. Good PCB layout minimizes excessive EMI and prevents the power supply from being disrupted during surge/ESD tests. The following are some general guidelines:

- To get better EMI performance and reduce line frequency ripples, the output of the bridge rectifier should be connected to capacitor C_{bulk} first, then to the switching circuits.
- The high-frequency current loop is found in **C_{bulk} – Transformer – MOSFET – R_S – C_{bulk}**. The area enclosed by this current loop should be as small as possible. Keep the traces (especially 4→1) short, direct, and wide. High-voltage drain traces related to the MOSFET and RCD snubber should be kept far way from control circuits to prevent unnecessary interference. If a heatsink is used for the MOSFET, it is recommended to ground the heatsink.
- As indicated by 3, the control circuit's ground should be connected first, then to other circuitry.
- As indicated by 2, the area enclosed by the **transformer auxiliary winding, D_1, and C_1**, should be kept small. Place C_1 close to the FAN6751 for good decoupling.

Two suggestions with different pros and cons for ground connections are recommended.

- GND3→2→4→1: Possible method for circumventing the sense signals common impedance interference.
- GND3→2→1→4: Potentially better for ESD testing where a ground is not available for the power supply. The charges for ESD discharge path go from the secondary through the transformer stray capacitance to the GND2 first. Then, the charges go from GND2 to GND1 and back to the mains. Control circuits should not be placed on the discharge path. Point discharge for common choke can decrease high-frequency impedance and help increase ESD immunity.
- Should a Y-cap between primary and secondary be required, the Y-cap should be connected to the **positive terminal of the C_{bulk} (V_{DC})**. If this Y-cap is connected to the primary GND, it should be connected to the **negative terminal of the C_{bulk} (GND1)** directly. Point discharge of the Y-cap also helps with ESD. However, according to safety requirements, the creepage between the two pointed ends should be at least 5mm.

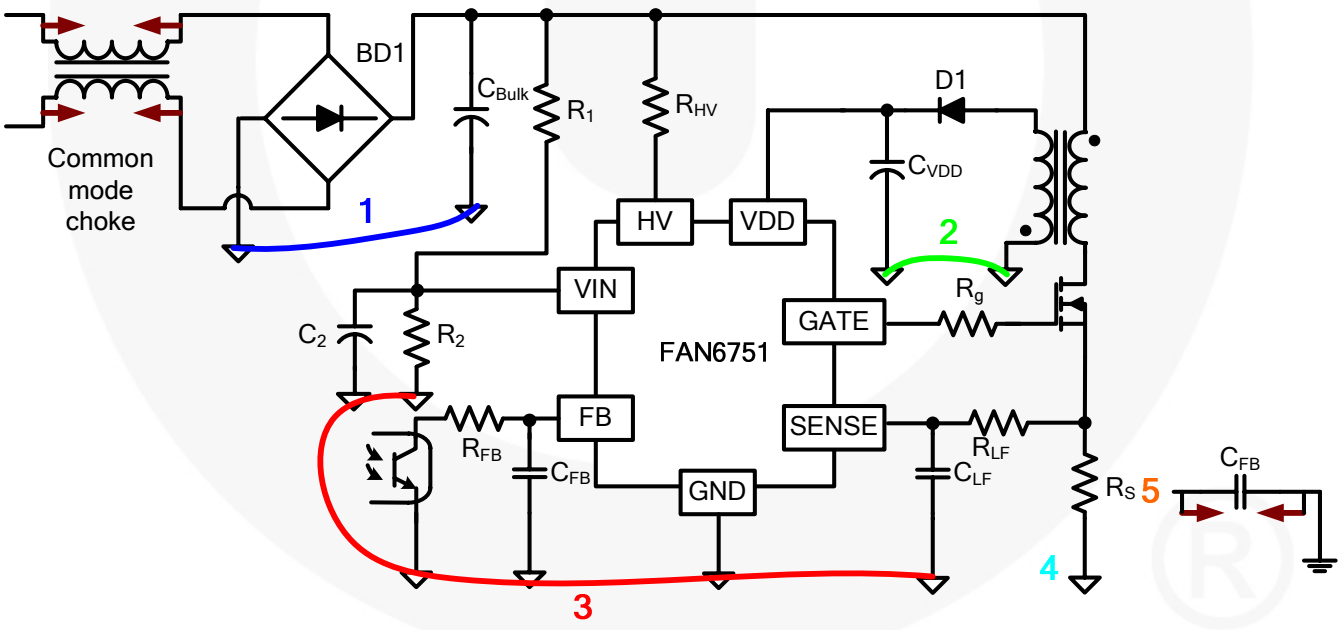

Figure 22. Layout Considerations

Typical Application Circuit

Application	Output Power	Input Voltage Range	Output Voltage/Maximum Current
LCD Monitor Power Supply	44W	Universal Input (90-264V_{AC})	12V/2A 5V/4A

Features

- High-Voltage Startup
- Built-in 5ms Soft-Start Function
- Built-in VIN Pin Pull-High (> 4.7V) Recovery Function for Second-Side Output OVP
- Brownout Protection with Hysteresis
- Low Standby Mode Power Consumption (Input Wattage <0.3W at No-Load Condition)

Key Design Notes

- Resistors R_{12} and R_{13} work as a startup resistor to provide necessary current for IC startup. After startup, there is no power loss on these resistors. The recommended values for R_{12} and R_{13} are 130KΩ(1/4W) and 51KΩ(1/4W).
- Because the VIN pin is connected through a resistive divider R_3 and R_{16} to the rectified AC input line voltage, it can also be used for brownout protection. If the V_{IN} voltage is less than 0.7V, the PWM output is shut off. As the V_{IN} voltage reaches 0.92V, the PWM output is turned on again. The hysteresis window for ON/OFF is 0.22V. The recommended values for R_3+R_{15}, R_{16}, and C_{16} are 10MΩ (5MΩ+5MΩ), 100KΩ, and 2.2μF. Using these values in the test board, the power supply is turned off at 66V (maximum load) and recovered at 70V.
- The secondary-side over-voltage protection (OVP) is achieved by pulling the VIN pin high. ZD_1, ZD_2, R_{29}, R_{30}, R_{31}, R_{32}, C_{15}, and U_3 form a secondary-side over-voltage protection (OVP) circuit. When each output reaches OVP, photocoupler U3 pulls the VIN pin high. The OVP voltages of the 12V-output and 5V-output are 15V and 6.8V, respectively.

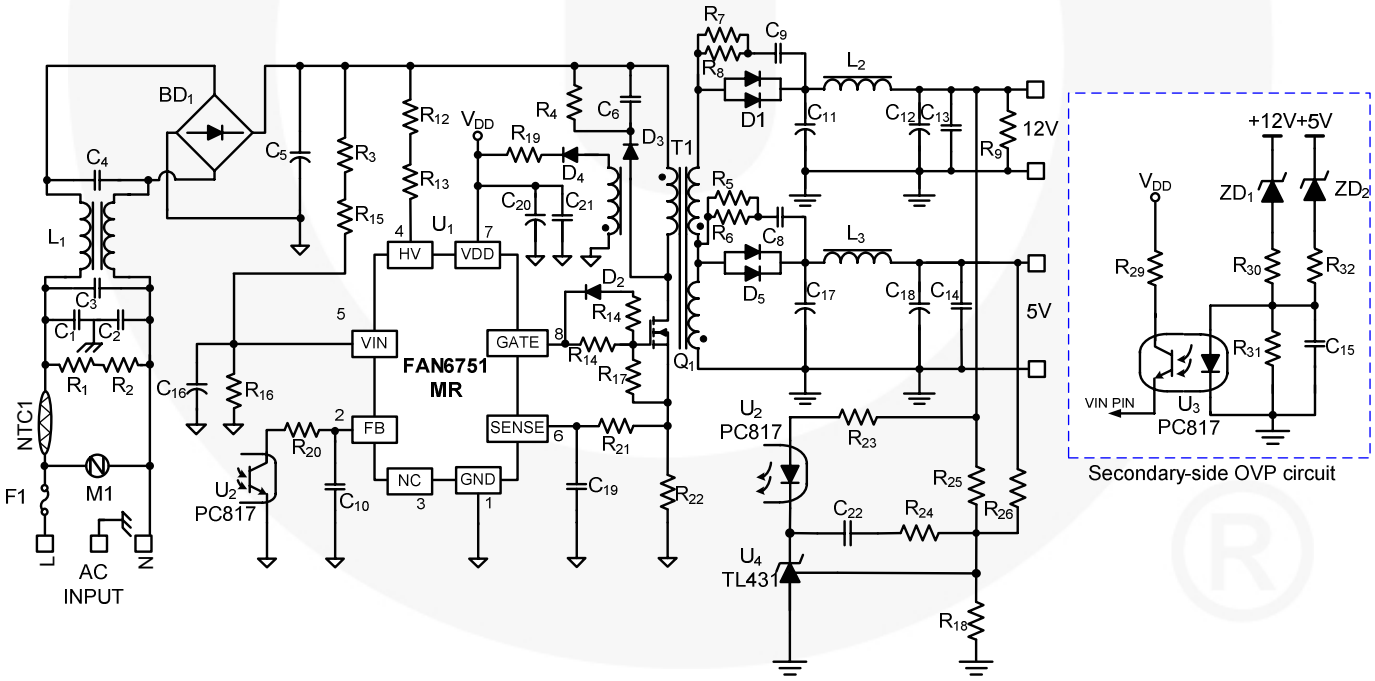

Figure 23. Schematic

Table 3. Experimental Results

Input Voltage	Input Wattage (No load)	Output Current Protection (5V)
90V/60Hz	0.198W	5.8A
264V/50Hz	0.277W	5.1A

Table 4. 44W LCD Monitor Evaluation Board Part List

PART#	VALUE	NOTE	PART#	VALUE	NOTE
Fuse			Capacitor		
F1	4A/250V	Glass	C1	2.2nF/250V	Y2, Ceramic
NTC			C2	2.2nF/250V	Y2, Ceramic
NTC1	5Ω		C3	0.33μF/250V	Box Capacitor
Resistor			C4	0.22μF/250V	Box Capacitor
R1, R2	1MΩ	1206+/-5%	C5	120μF/400V	Electrolytic
R3	10MΩ	1206 +/-5%	C6	10nF /1KV	Ceramic
R4	47KΩ	2W +/-5%	C7	2.2nF /250V	Ceramic
R5, R6, R7, R8	47Ω	1206+/-5%	C8	2.2nF	1206
R9	2KΩ	0805 +/-5%	C9	1nF	1206
R10	0Ω	0805 +/-5%	C10	1nF	1206
R11	NC		C11	1000μF/16V	Electrolytic
R12	130KΩ	2W +/-5%	C12	1000μF/16V	Electrolytic
R13	51KΩ	2W +/-5%	C13	0.1μF/50V	1206
R14	10Ω	0805+/-5%	C14	0.1μF/50V	1206
R15	0Ω	1206+/-5%	C15	0.1μF/50V	1206
R16	100KΩ	1206+/-5%	C16	4.7μF/50V	Electrolytic
R17	22KΩ	1/4W	C17	2200μF/10V	Electrolytic
R18	10KΩ	0805	C18	1000μF/10V	Electrolytic
R19	15Ω	5μH,1/2W	C19	470pF	0805
R20	100Ω	1/4W	C20	10μF/50V	Electrolytic
R21	100Ω	0805+/-5%	C21	0.1μF	0805
R22	0.5Ω	1W	Diode		
R23	750Ω	0805+/-5%	D1	STPS20H100CT	100V/20A
R24	4.7KΩ	0805+/-5%	D2	1N4148	
R25	120KΩ	0805+/-5%	D3	FR107	
R26	15KΩ	0805+/-5%	D4	FR103	
R29	10KΩ	1206+/-5%	D5	MBR2060CT	60V/20A
R30	1KΩ	0805+/-5%	ZD1	6.8V	
R31	1KΩ	0805+/-5%	ZD2	15V	
R32	1KΩ	0805+/-5%	BD1	KBP206G	
IC			MOSFET		
U1	FAN6751MR	Fairchild	Q1	FQP8N60C	Fairchild
U2	PC817	Fairchild	Filter		
U3	PC817	Fairchild	L1	9mH	
U4	TL431	Fairchild	L2	2.7μH	
TNR			L3	2.7μH	
M1	470V	7ψ			

Transformer Specification

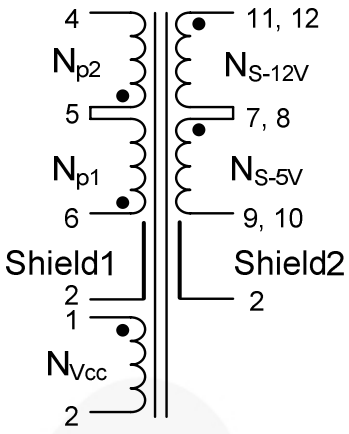

Figure 24. Transformer Schematic

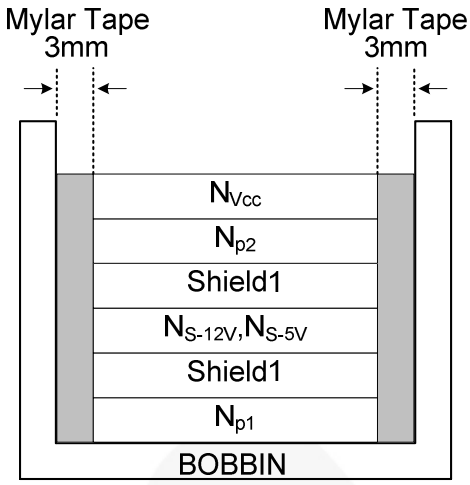

Figure 25. Winding Sequence

Winding Specification

No		Pin(s-f)		Wire	Turns		Winding Method
N_{p1}		6-5		0.4Φ	36Ts		Solenoid Winding
Insulation: Polyester Tape t = 0.03mm, 1 Layers							
Shield1		-2		Copper Tape	1.2Ts		Not Shorted
Insulation: Polyester Tape t = 0.03mm, 3 Layers							
N_{S-5V}	N_{S-12V}	7,8-9,10	7,8-11,12	0.6Φ*2	5 Ts	6 Ts	Solenoid Winding
Insulation: Polyester Tape t = 0.03mm, 3 Layers							
Shield1		-2		Copper Tape	1.2Ts		Not Shorted
Insulation: Polyester Tape t = 0.03mm, 1 Layers							
N_{p2}		5-4		0.4Φ	32Ts		Solenoid Winding
Insulation: Polyester Tape t = 0.03mm, 5 Layers							
N_{Vcc}		1-2		0.2Φ	14Ts		Solenoid Winding
Insulation: Polyester Tape t = 0.03mm, 3 Layers							

Electrical Specification

	Pin	Value	Remarks
Inductance	6-4	800μH	1KHz, 0.25V
Leakage	6-4	40μH	2nd Shorted

- Core: EER2828
- Bobbin: EER2828
- Ae: 82.1 [mm^2]

Related Datasheets

FAN6751 — Highly Integrated Green-Mode PWM Controller