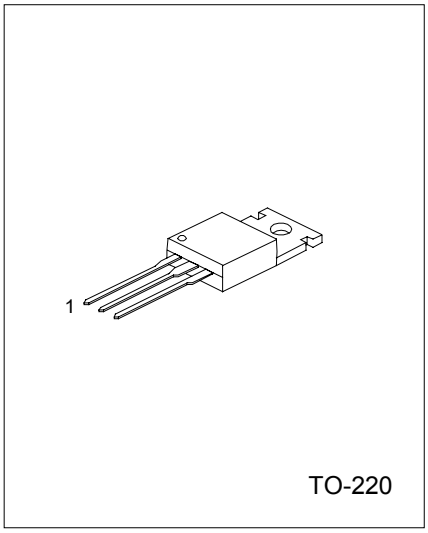
TRIACS

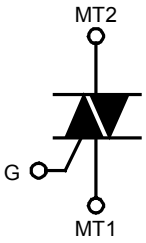
DESCRIPTION

Passivated, sensitive gate triacs in a plastic envelope, intended for use in general purpose bidirectional switching and phase control applications, where high sensitivity is required in all four quadrants.



1:MT1 2:MT2 3:GATE

SYMBOL



ABSOLUTE MAXIMUM RATINGS

PARAMETER		SYMBOL	RATINGS	UNIT
Repetitive peak off-state voltages	UT136E-5	V_{DRM}	500*	V
	UT136E-6		600*	
	UT136E-8		800	
RMS on-state current full sine wave; $T_{mb} \leqslant 107$ °C		$I_{T(RMS)}$	4	A
Non-repetitive peak on-state current (Full sine wave; T_j = 25 °C prior to surge)		I_{TSM}		A
t = 20ms			25	
t = 16.7 ms			27	
I^2t for fusing		I^2t		A^2s
t = 10 ms			3.1	
Repetitive rate of rise of on-state current after triggering I_{TM} = 6 A; I_G = 0.2A; dI_G/dt = 0.2A/μs		dI_T/dt		A/μs
	T2+ G+		50	
	T2+ G-		50	
	T2- G-		50	
	T2- G+		10	
Peak gate voltage		V_{GM}	5	V
Peak gate current		I_{GM}	2	A
Peak gate power		P_{GM}	5	W
Average gate power (over any 20 ms period)		$P_{G(AV)}$	0.5	W
Storage temperature		T_{stg}	-40 ~ 150	℃
Operating junction temperature		T_j	125	℃

*Although not recommended, off-state voltages up to 800V may be applied without damage, but the traic may switch to the on-state. The rate of rise of current should not exceed 3A/μs.

THERMAL RESISTANCES

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Thermal resistance Junction to mounting base Full cycle Half cycle	$R_{th\ j\text{-}mb}$			 3.0 3.7	K/W
Thermal resistance Junction to ambient (In free air)	$R_{th\ j\text{-}a}$		60		K/W

STATIC CHARACTERISTICS (T_j=25°C, unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Gate trigger current	I_{GT}	V_D = 12 V; I_T = 0.1 A				
		T2+ G+		2.5	10	mA
		T2+ G-		4.0	10	
		T2- G-		5.0	10	
		T2- G+		11	25	
Latching current	I_L	V_D = 12 V; I_{GT} = 0.1 A				
		T2+ G+		3.0	15	mA
		T2+ G-		10	20	
		T2- G-		2.5	15	
		T2- G+		4.0	20	
Holding current	I_H	V_D = 12 V; I_{GT} = 0.1 A		2.2	15	mA
On-state voltage	V_T	I_T = 5 A		1.4	1.7	V
Gate trigger voltage	V_{GT}	V_D = 12 V; I_T = 0.1 A		0.7	1.5	V
		V_D = 400V ; I_T = 0.1 A; T_j =125°C	0.25	0.4		V
Off-state leakage current	I_D	V_D = $V_{DRM(max)}$; T_j = 125 °C		0.1	0.5	mA

DYNAMIC CHARACTERISTICS(T_j=25°C, unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Critical rate of rise of Off-state voltage	dV_D/dt	V_{DM} = 67% $V_{DRM(max)}$; T_j =125°C; exponential waveform; gate open circuit		50		V/μs
Gate controlled turn-on time	t_{gt}	I_{TM} = 6 A; V_D= $V_{DRM(max)}$; I_G=0.1A; dI_G/dt=5A/μs		2		μs

TYPICAL CHARACTERISTICS

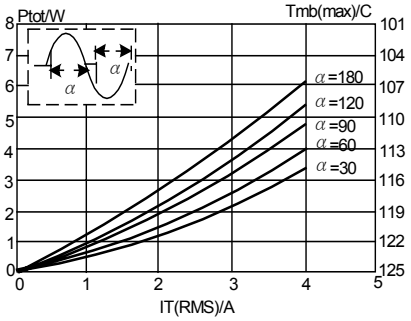


Fig.1. Maximum on-state dissipation, P_{tot}, versus rms on-state current, $I_{T(RMS)}$ where α =conduction angle.

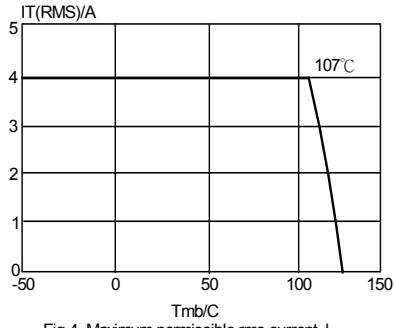


Fig.4. Maximum permissible rms current $I_{T(RMS)}$, versus mounting base temperature T_{mb}

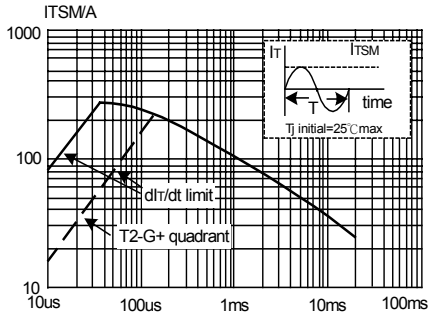


Fig.2.Maximum Permissible non-repetitive peak on-state Current I_{TSM}, versus pulse width t_p for sinusoidal currents, $t_p \leqq 20ms$

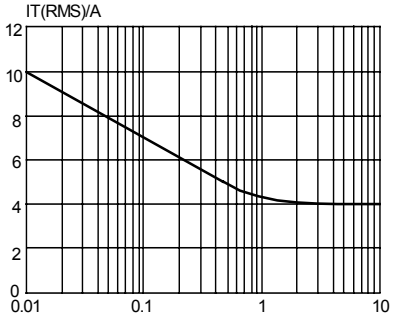


Fig. 5.Maximum permissible repetitive rms on-state current $I_{T(RMS)}$, versus surge duration, for sinusoidal currents, f=50HZ; $T_{mb} \leqq 107℃$

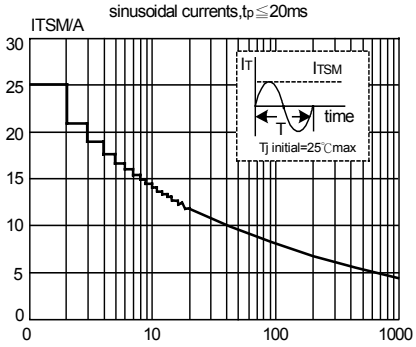


Fig3.Maximum Permissible non-repetitive peak on-state current I_{TSM}, versus number of cycles, for sinusoidal currents, f=50HZ.

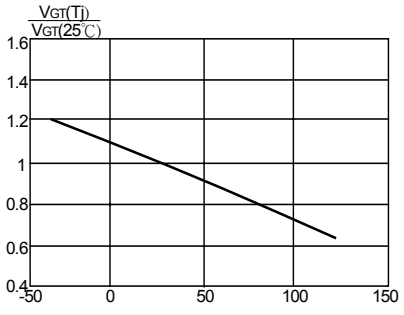


Fig.6. Normalised gate trigger voltage $V_{GT}(T_j)/V_{GT}(25℃)$, versus junction temperature T_j

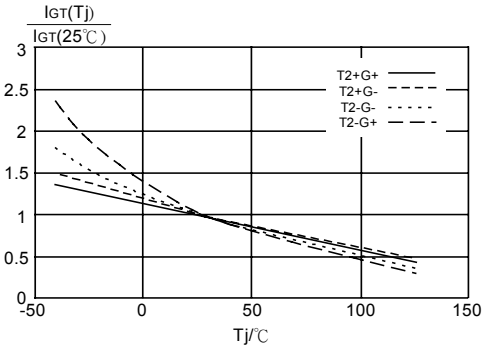


Fig. 7.Normalised gate trigger Current $I_{GT}(Tj)/I_{GT}(25℃)$,versus junction temperature Tj.

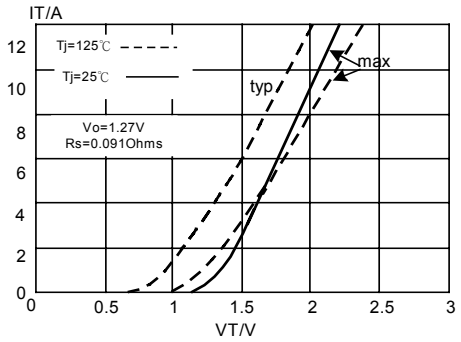


Fig.10.Typical and maximum on-state characteristic.

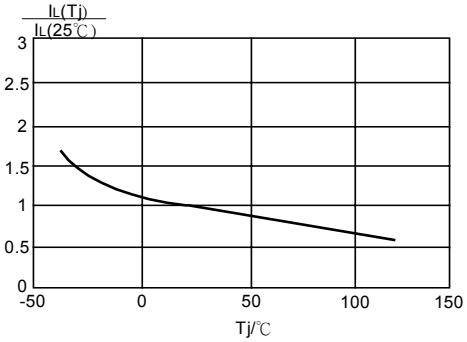


Fig.8.Normalised latching Current $I_L(Tj)/I_L(25℃)$, versus junction temperature Tj

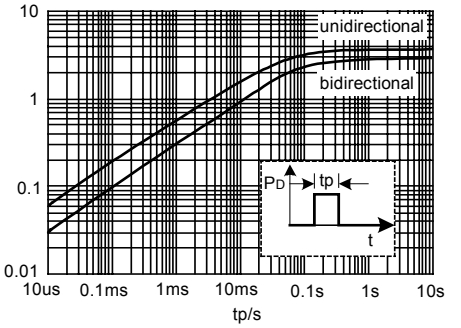


Fig.11.Transient thermal impedance Zthj-mb,versus pulse width tp.

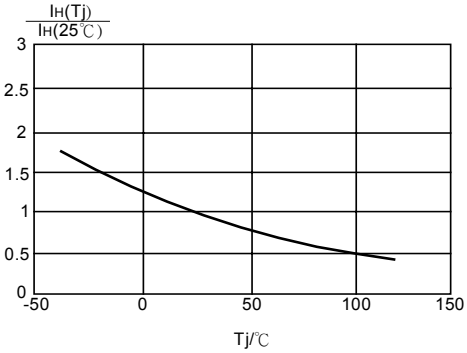


Fig. 9.Normalised holding current $I_H(Tj)/I_H(25℃)$, versus junction temperature Tj.

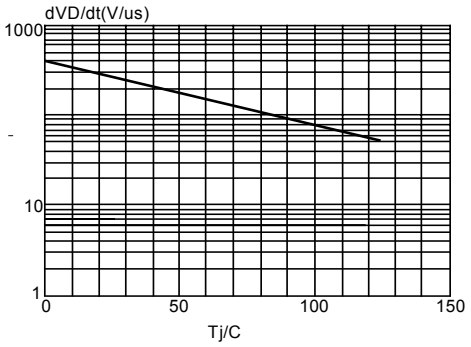


Fig.12.Typical,critical rate of rise of off-satate voltage,dV_D/dt versus junction temperature Tj