M5L8286P/M5L8287P

T-52-31

MITSUBISHI(MICMPTR/MIPRC)

OCTAL BUS TRANSCEIVER

DESCRIPTION

The M5L8286P and M5L8287P are semiconductor integrated circuits consisting of a set of eight 3-state output bus transceivers for use with a variety of microprocessor systems.

FEATURES

- 3-state, high-fanout outputs (I_{OL}=16mA, I_{OH}=−1mA for the A outputs and I_{OL} = 32mA, I_{OH} = −5mA for the B outputs)
- Low power dissipation

APPLICATION

Two-way bus transceivers for microcomputer systems

FUNCTION

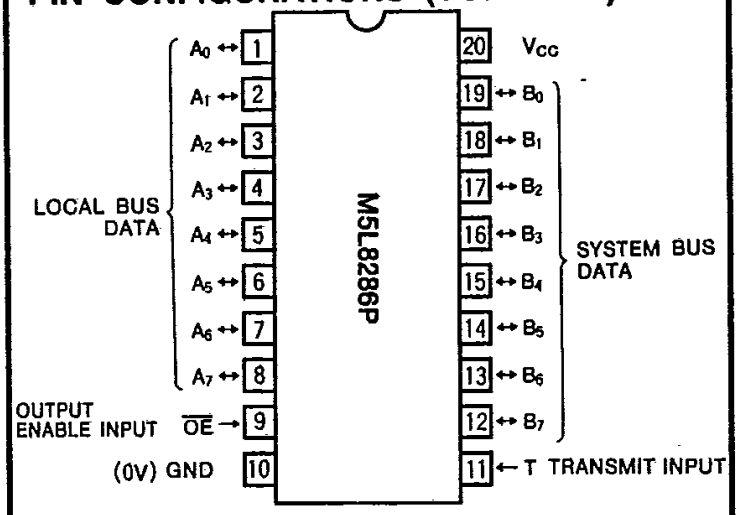
The M5L8286P and M5L8287P are two-way bus transceivers with non-inverted and inverted outputs respectively.

When the output enable input $\overline{OE}$ is high, the local bus data pins $A_0 \sim A_7$ and system data pins $B_0 \sim B_7$ are both placed in the high-impedance state.

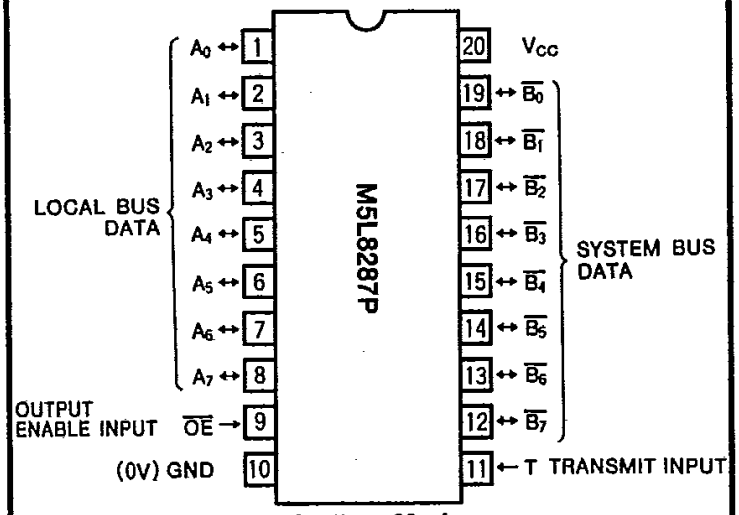
When the output enable input $\overline{OE}$ is low, the input and output states are controlled by the transmit input T.

When T is high, $A_0 \sim A_7$ are input pins and $B_0 \sim B_7$ are output pins. When T is low, $B_0 \sim B_7$ are input pins and $A_0 \sim A_7$ are output pins.

PIN CONFIGURATIONS (TOP VIEW)

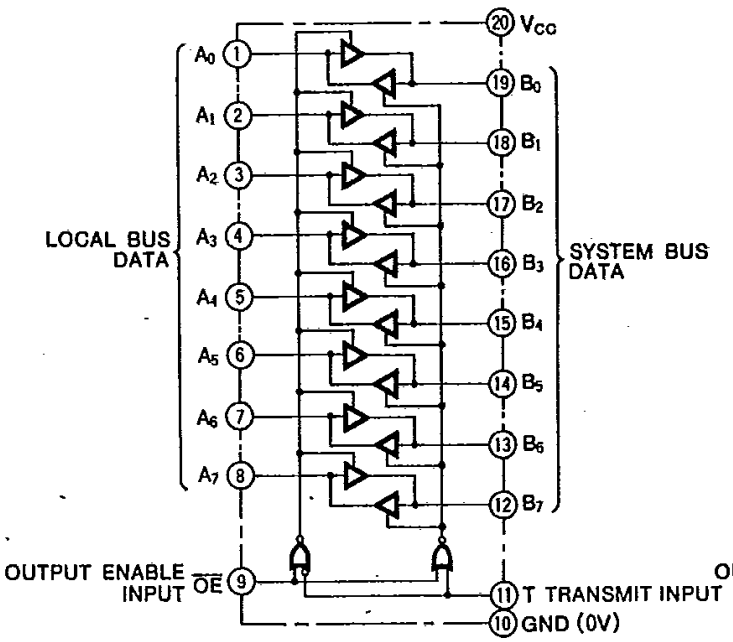


Outline 20P4

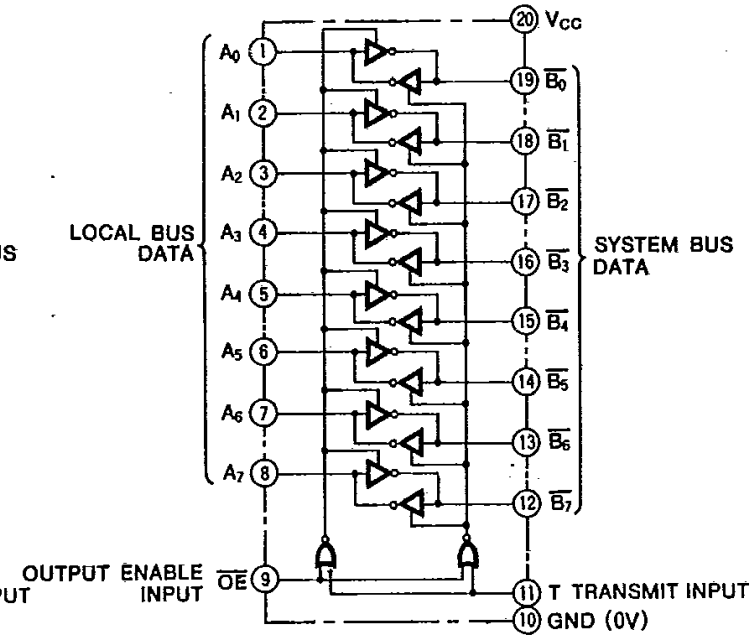


Outline 20P4

BLOCK DIAGRAM



M5L8286P



M5L8287P

FUNCTION TABLES (Note 1)

M5L8286P

$\overline{OE}$	T	A	B
L	L	O	I
L	H	I	O
H	X	Z	Z

M5L8287P

$\overline{OE}$	T	A	B
L	L	$\overline{O}$	I
L	H	I	$\overline{O}$
H	X	Z	Z

Note 1 : I : Input pin
O, $\overline{O}$: Output pin (non-inverted for the M5L8286P and inverted for the M5L8287P)
Z : Indicated the high-impedance state (A and B are separated)
X : Either high or low

ABSOLUTE MAXIMUM RATINGS (T_a=0~75℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5~+7	V
V_I	Input voltage		−0.5~+5.5	V
V_C	Output voltage		−0.5~V_{CC}	V
T_{opr}	Operating free-air temperature range		0~+75	℃
T_{stg}	Storage temperature range		−65~+150	℃

RECOMMENDED OPERATING CONDITIONS (T_a=0~75℃, unless otherwise noted)

Symbol	Parameter			Limits			Unit
				Min	Nom	Max	
V_{CC}	Supply voltage			4.5	5	5.5	V
I_{OH}	High-level output current	V_{OH}≧2.4V	A output	0		−1	mA
			B output	0		−5	
I_{OL}	Low-level output current	V_{OL}≦0.45V	A output	0		16	mA
			B output	0		32	

ELECTRICAL CHARACTERISTICS (T_a=0~75℃, unless otherwise noted)

Symbol	Parameter		Test conditions		Limits			Unit
					Min	Typ	Max	
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage	A input					0.8	V
		B input					0.9	
V_{IC}	Input clamp voltage		V_{CC}=4.5V, I_{IC}=−5mA				−1	V
V_{OH}	High-level output voltage	A output	V_{CC}=4.5V, I_{OH}=−1mA		2.4			V
		B output	V_{CC}=4.5V, I_{OH}=−5mA		2.4			V
V_{OL}	Low-level output voltage	A output	V_{CC}=4.5V, I_{OL}=16mA				0.45	V
		B output	V_{CC}=4.5V, I_{OL}=32mA				0.45	V
I_{OZH}	Off-state output current with high-level applied at the output	A output	V_{CC}=5.5V, V_I=2V	V_I=0.8V			50	μA
		B output	V_O=5.25V	V_I=0.9V				
I_{OZL}	Off-state output current with low-level applied the output	A output	V_{CC}=5.5V, V_I=2V	V_I=0.8V			−0.2	mA
		B output	V_O=0.45V	V_I=0.9V				
I_{IH}	High-level input current		V_{CC}=5.5V, V_I=5.25V				50	μA
I_{IL}	Low-level input current		V_{CC}=5.5V, V_I=0.45V				−0.2	mA
I_{CC}	Supply current	M5L8286P	V_{IC}=5.5V				110	mA
		M5L8287P					110	
C_{IN}	Input capacitance		F=1MHz, V_{BIAS}=2.5V, V_{CC}=5V, T_a=25℃				12	pF

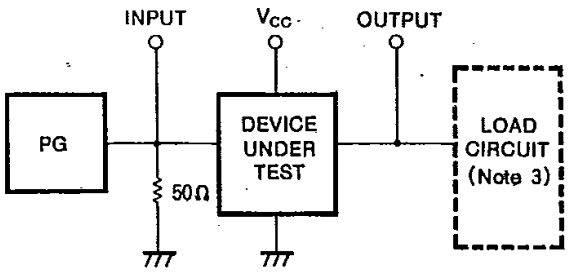
SWITCHING CHARACTERISTICS (V_{CC}=5V±10%, T_a=0~75℃, unless otherwise noted)

Symbol	Parameter	Alternate symbol	Test conditions	M5L8286P Limits			M5L8287P Limits			Unit
				Min	Typ	Max	Min	Typ	Max	
t_{PLH} t_{PHL}	Low-level to high-level and high-level and low-level transition time from input A, B to outputs B, A	TIVOV	(Note 2)	5		30	5		22	ns
t_{PZH} t_{PZL}	Output enable time from $\overline{OE}$ input to A or B output	TELOV		10		30	10		30	ns
t_{PHZ} t_{PLZ}	Output disable time from $\overline{OE}$ input to A or B output	TEHOZ		5		18	5		18	ns

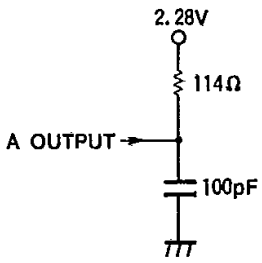
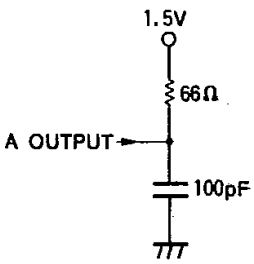
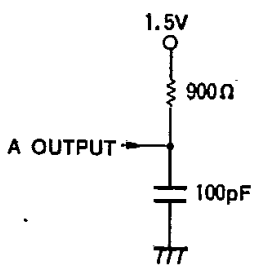
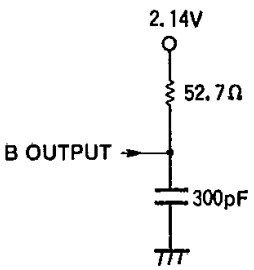
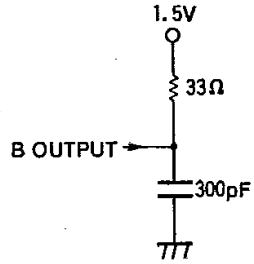
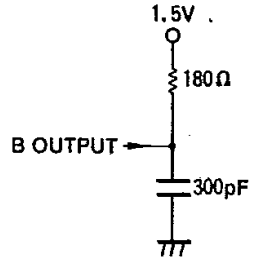
TIMING REQUIREMENTS (V_{CC}=5V±10%, T_a=0~75℃, unless otherwise noted)

Symbol	Parameter	Alternate Symbol	Test conditions	Limits			Unit
				Min	Typ	Max	
t_{su}	T setup time with respect to $\overline{OE}$	T_{TVFL}		10			ns
t_h	T hold time with respect to $\overline{OE}$	T_{EHTV}		5			ns

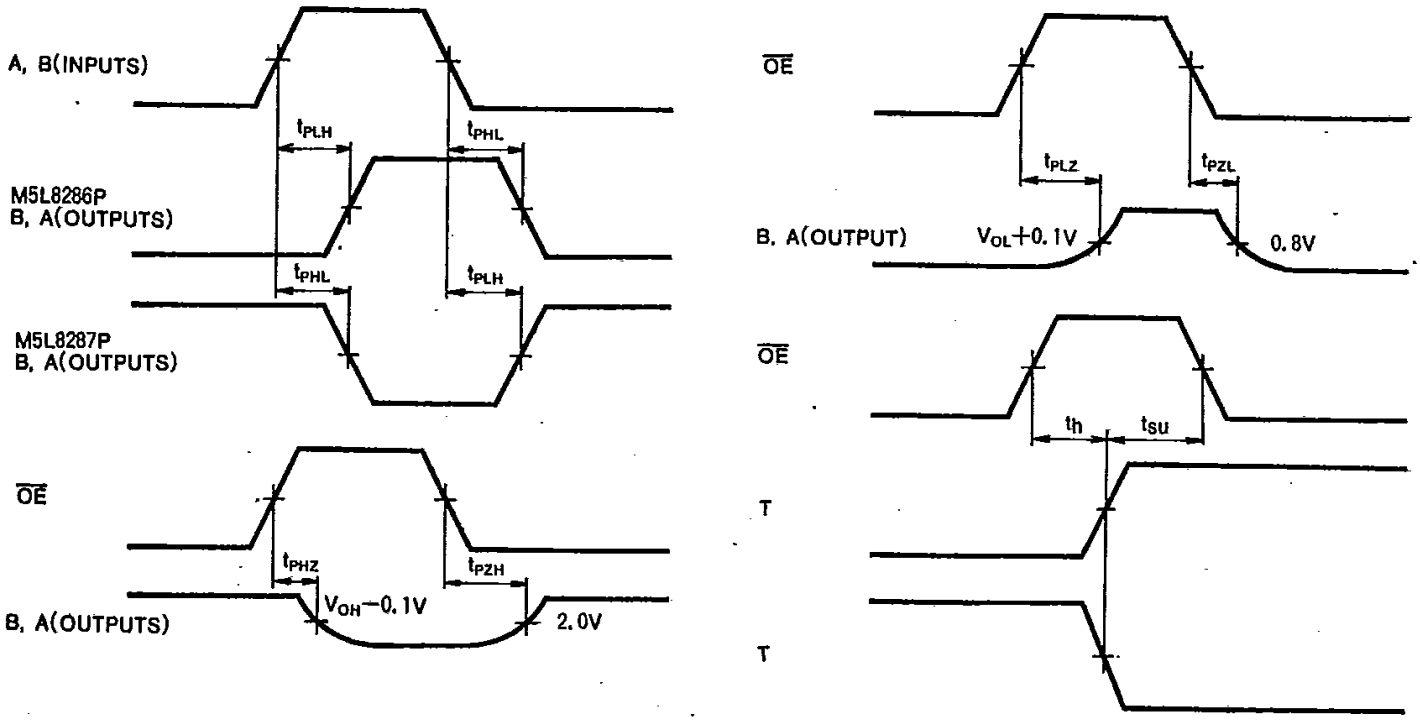
Note 2 : Test Circuit



Note 3

Test Item	t_{PLH}, t_{PHL}	t_{PLZ}, t_{PZL}	t_{PHZ}, t_{PZH}
A OUTPUT LOAD CIRCUIT			
B OUTPUT LOAD CIRCUIT			

TIMING DIAGRAM (Reference voltage=1.5V)



APPLICATION EXAMPLE