DATA SHEET

TE7753/TE7754

SUPER I/O EXPANDER

[Outline]

TE7753 and TE7754 are peripheral devices connected to a microprocessor, or general-purpose interface devices each having nine 8-bit parallel data input/output ports.
Two port I/O setting modes, soft mode and hard mode, can be selected. Switching the modes eases the connection to an 86-series or 68-series CPU.

[Characteristics]

1. Equipped with nine 8-bit parallel I/O ports
2. Allowing I/O setting in bit units (port 8 only)
3. Interface designed for connections with various types of CPUs
4. High drive current (IOL = 12 mA: Port 9 only)
5. Choice of two modes
   Soft mode : I/O setting is enabled for nine ports by software instructions from the CPU.
   Hard mode : I/O setting is enabled for six ports by hardware setting of pins IOS2 to IOS0.
6. Space merit (body size 14 mm x 14 mm)
7. State of ports after resetting
   Soft mode : All ports are in input state.
   Hard mode : TE7753: Output ports are in High state.
   TE7754: Output ports are in Low state.
8. CMOS, 5 V (single supply voltage)

[Contents]

[Notations]

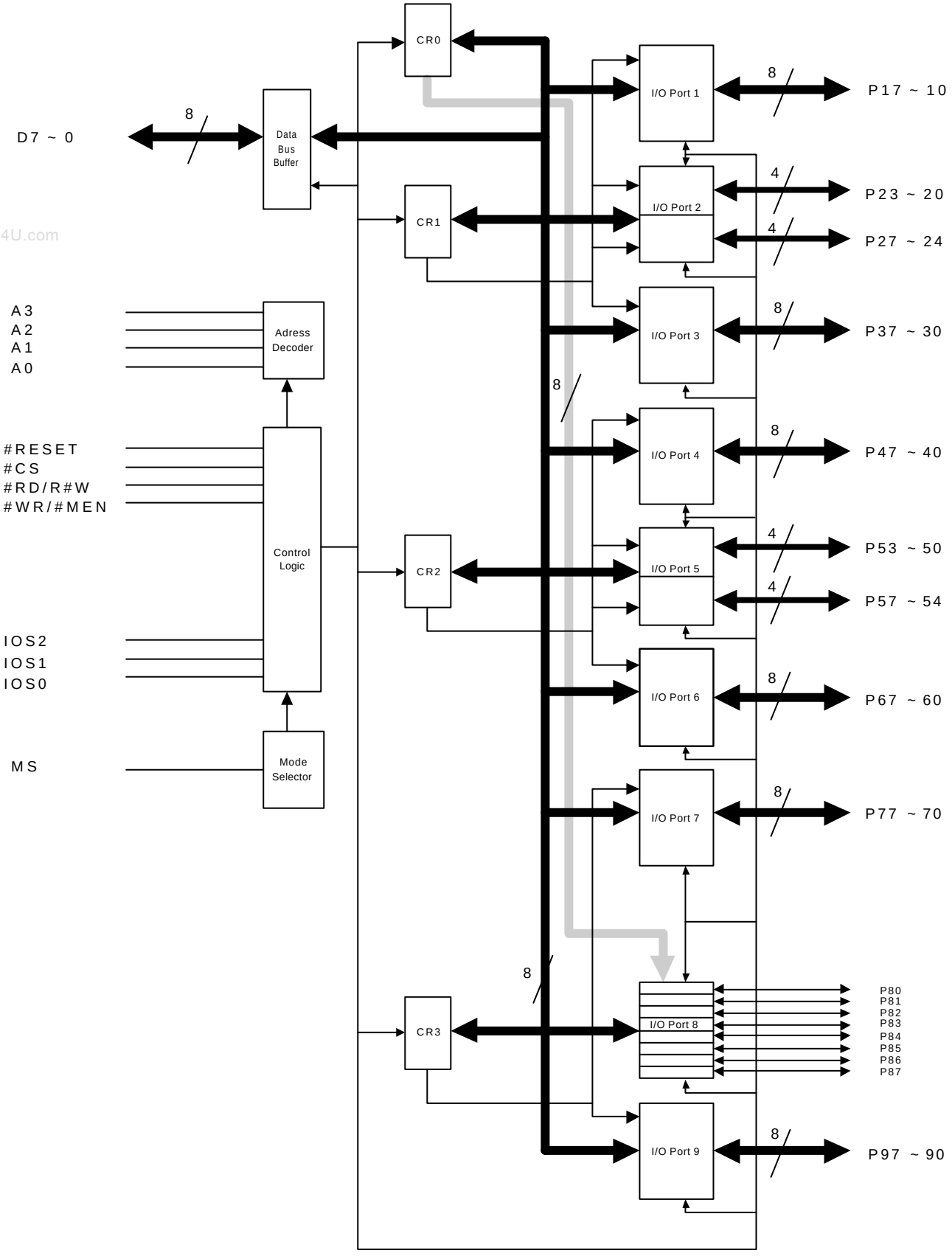
1. Voltage levels are indicated differently for input and output signals.

Voltage level	Input signal	Output signal
V_{DD}	1	H
V_{SS}	0	L

2. A signal with the enable level being negative logic is indicated with its name preceded by # as shown below:
   Examples: #CS, #RD

3. The value indicated in a register is the initial value after resetting.

[Block Diagram]



[Pin Assignments]

NO.	I/O	SYMBOL	NOTES	NO.	I/O	SYMBOL	NOTES
1	-	V_{DD}		51	-	V_{DD}	
2	B	P81		52	B	P47	
3	B	P82		53	B	D0	
4	B	P83		54	B	D1	
5	B	P84		55	B	D2	
6	B	P85		56	B	D3	
7	B	P86		57	B	D4	
8	B	P87		58	B	D5	
9	B	P90		59	B	D6	
10	B	P91		60	B	D7	
11	B	P92		61	I	#RESET	
12	B	P93		62	I	#CS	
13	B	P94		63	I	#RD	
14	B	P95		64	I	#WR	
15	B	P96		65	I	A0	
16	B	P97		66	I	A1	
17	B	P10		67	I	A2	
18	B	P11		68	I	A3	
19	B	P12		69	I	IOS0	
20	B	P13		70	I	IOS1	
21	B	P14		71	I	IOS2	
22	B	P15		72	I	MS	
23	B	P16		73	B	P50	
24	B	P17		74	B	P51	
25	-	V_{DD}		75	-	V_{DD}	
26	-	V_{SS}		76	-	V_{SS}	
27	B	P20		77	B	P52	
28	B	P21		78	B	P53	
29	B	P22		79	B	P54	
30	B	P23		80	B	P55	
31	B	P24		81	B	P56	
32	B	P25		82	B	P57	
33	B	P26		83	B	P60	
34	B	P27		84	B	P61	
35	B	P30		85	B	P62	
36	B	P31		86	B	P63	
37	B	P32		87	B	P64	
38	B	P33		88	B	P65	
39	B	P34		89	B	P66	
40	B	P35		90	B	P67	
41	B	P36		91	B	P70	
42	B	P37		92	B	P71	
43	B	P40		93	B	P72	
44	B	P41		94	B	P73	
45	B	P42		95	B	P74	
46	B	P43		96	B	P75	
47	B	P44		97	B	P76	
48	B	P45		98	B	P77	
49	B	P46		99	B	P80	
50	-	V_{SS}		100	-	V_{SS}	

I : Input

O : Output

B : Both input and output

[Description of Pins]

Pin name	No.	I/O	Pin function	Description
V_{DD}	1,25, 51,75	-	POWER SUPPLY	Connect all pints to the power supply.
V_{SS}	26,50, 76, 100	-	GROUND	Connect all pins to the ground.
D7-0	53-60	B	DATA BUS	8-bit bidirectional pins used for data communication with the CPU. The #CS, #RD, and #WR signals control the opening and closing the bus signal and data direction.
A3-0	65-68	I	ADDRESS INPUT	For communication with the CPU, this signal is used to select nine ports and four command registers.
#RESET	61	I	RESET	Initialization pulse input pin. Initialization is performed when a level-0 signal is input. CMOS Schmitt trigger input
#CS	62	I	CHIP SELECT	When a level-0 signal is input to this pin, the data bus is released so that data communication can be performed with the CPU.
#RD	63	I	READ/READ WRITE SELECT	When a level-0 signal is input while MS is 0, data is read from each port. When MS is 1, #RD is used in combination with the #WR signal. When a level-1 signal is input, data is read. When a level-0 signal is input, data is written.
#WR	64	I	WRITE/M ENABLE	When a level-0 signal is input while MS is 0, data is written to command register of each port. When MS is 1, this signal becomes an R#W signal enable signal.
MS	72	I	MODE SELECT	This signal is used to select the mode of interfacing with the connected CPU. For more information, refer to “CPU Interface.”
IOS2-0	69-71	I	INPUT OUTPUT SELECT	In soft mode, set all pins to input of 0. In hard mode, these three input pins can be used to select input/output combinations of each port. For more information, refer to 1, “Soft mode and hard mode,” of “Description of Operation.”

Pin name	No.	I/O	Pin function	Description
P17-10	17-24	B	PORT	Port 1 8-bit general-purpose input/output port In hard mode, this port is always an input port. I_{OL}=4mA
P27-20	27-34			Port 2 8-bit general-purpose input/output port In soft mode, input or output can be performed in units of 4 bits. I_{OL}=4mA
P37-30	35-42			Port 3 8-bit general-purpose input/output port I_{OL}=4mA
P47-40	43-49, 52			Port 4 8-bit general-purpose input/output port I_{OL}=4mA
P57-50	73,74 77-82			Port 5 8-bit general-purpose input/output port In soft mode, input or output can be performed in units of 4 bits. I_{OL}=4mA
P67-60	83-90			Port 6 8-bit general-purpose input/output port I_{OL}=4mA
P77-70	91-98			Port 7 8-bit general-purpose input/output port I_{OL}=4mA
P87-80	2-8,99			Port 8 8-bit general-purpose input/output port In either mode, input or output can be performed in units of 4 bits. I_{OL}=4mA
P97-90	9-16			Port 9 8-bit general-purpose input/output port In hard mode, this port is always an output port. I_{OL}=12mA

[CPU Interface]

The TE7753 and TE7754 each support the two CPU interface modes shown below. The MS pin is used to select the mode.

[Relationship between CPU and select signal]

Operation	MS="0"	MS="1"
Read	#RD	R#W
Write	#WR	#MEN

The data sheet given here uses the signal names (#RD and #WR) applicable when MS is 0. For MS being 1, read them for the corresponding signal names shown above.

[Description of Operation]

1. Soft mode and hard mode

The MS pin is used to select the mode of interfacing with the connected CPU.
When MS is 0, separate pins are used for read and write signals (mainly for the 86 series). When MS is 1, a single pin is used for both read and write signals and another pin is used for the enable signal (mainly for the 68 series).

The IOS2 to IOS0 pins are used to select the soft or hard mode.

A port after resetting is in input state in soft mode and "H" output state in hard mode ("H" output with the TE7753 and "L" output with the TE7754).

Mode selection	IOS2	IOS1	IOS0
Soft mode	0	0	0
Hard mode	Other than the above		

The TE7753 and TE7754 each can read port-output data through the CPU bus (D7-0). Read it by specifying the address (A3-0) while the port is in the output state.

[Soft mode]

The input and output of each port can be programmed by writing software commands to the command registers (CR) CR3-0 from the CPU.

By writing output data in advance to each port before writing to the CR, data is output immediately after the port is set for output by the CR.

IOS2→"0", IOS1→"0", IOS0→"0"

Port No	CR used	Nibble input/output	Bit input/output
1	CR1	NG	NG
2		OK	NG
3		NG	NG
4	CR2	NG	NG
5		OK	NG
6		NG	NG
7	CR3	NG	NG
8	CR0	OK	OK
9	CR3	NG	NG

[Description of Registers]

In soft mode, CR is used to set a port for input or output.
To set a port for output, write 0 to the register. To set it for input, write 1 to the register.
The values indicated in each register are the initial values after resetting.

	CR0			CR1			CR2			CR3	
D0→	1	→P80	D0→	1	→P20-23	D0→	1	→P50-53			
D1→	1	→P81	D1→	1	→P30-37	D1→	1	→P60-67	D1→	1	→P90-97
D2→	1	→P82									
D3→	1	→P83	D3→	1	→P24-27	D3→	1	→P54-57			
D4→	1	→P84	D4→	1	→P10-17	D4→	1	→P40-47	D4→	1	→P70-77
D5→	1	→P85									
D6→	1	→P86									
D7→	1	→P87									

When MS is 0

[Read mode]

MS	#CS	#RD	#WR	A3	A2	A1	A0	Operation	CPU operation
0	0	0	1	0	0	0	0	Port1→DataBus	Input
0	0	0	1	0	0	0	1	Port2→DataBus	
0	0	0	1	0	0	1	0	Port3→DataBus	
0	0	0	1	0	0	1	1	Port4→DataBus	
0	0	0	1	0	1	0	0	Port5→DataBus	
0	0	0	1	0	1	0	1	Port6→DataBus	
0	0	0	1	0	1	1	0	Port7→DataBus	
0	0	0	1	0	1	1	1	Port8→DataBus	
0	0	0	1	1	0	0	0	Port9→DataBus	

[Write mode]

MS	#CS	#RD	#WR	A3	A2	A1	A0	Operation	CPU operation
0	0	1	0	0	0	0	0	DataBus→Port1	Output
0	0	1	0	0	0	0	1	DataBus→Port2	
0	0	1	0	0	0	1	0	DataBus→Port3	
0	0	1	0	0	0	1	1	DataBus→Port4	
0	0	1	0	0	1	0	0	DataBus→Port5	
0	0	1	0	0	1	0	1	DataBus→Port6	
0	0	1	0	0	1	1	0	DataBus→Port7	
0	0	1	0	0	1	1	1	DataBus→Port8	
0	0	1	0	1	0	0	0	DataBus→Port9	
0	0	1	0	1	0	0	1	DataBus→CR0	
0	0	1	0	1	0	1	0	DataBus→CR1	
0	0	1	0	1	0	1	1	DataBus→CR2	
0	0	1	0	1	1	0	0	DataBus→CR3	

When MS is 1

[Read mode]

MS	#CS	#RD	#WR	A3	A2	A1	A0	Operation	CPU operation
1	0	1	0	0	0	0	0	Port1→DataBus	Input
1	0	1	0	0	0	0	1	Port2→DataBus	
1	0	1	0	0	0	1	0	Port3→DataBus	
1	0	1	0	0	0	1	1	Port4→DataBus	
1	0	1	0	0	1	0	0	Port5→DataBus	
1	0	1	0	0	1	0	1	Port6→DataBus	
1	0	1	0	0	1	1	0	Port7→DataBus	
1	0	1	0	0	1	1	1	Port8→DataBus	
1	0	1	0	1	0	0	0	Port9→DataBus	

[Write mode]

MS	#CS	#RD	#WR	A3	A2	A1	A0	Operation	CPU operation
1	0	0	0	0	0	0	0	DataBus→Port1	Output
1	0	0	0	0	0	0	1	DataBus→Port2	
1	0	0	0	0	0	1	0	DataBus→Port3	
1	0	0	0	0	0	1	1	DataBus→Port4	
1	0	0	0	0	1	0	0	DataBus→Port5	
1	0	0	0	0	1	0	1	DataBus→Port6	
1	0	0	0	0	1	1	0	DataBus→Port7	
1	0	0	0	0	1	1	1	DataBus→Port8	
1	0	0	0	1	0	0	0	DataBus→Port9	
1	0	0	0	1	0	0	1	DataBus→CR0	
1	0	0	0	1	0	1	0	DataBus→CR1	
1	0	0	0	1	0	1	1	DataBus→CR2	
1	0	0	0	1	1	0	0	DataBus→CR3	

[Hard mode]

Use IOS2 to IOS0 in advance to set ports 2 to 7 for input or output.
However, set only port 8 in the same way as in soft mode; write an 8-bit command to CR0 to set each bit for input or output.

IOS2, IOS1, IOS0 → Setting other than all 0

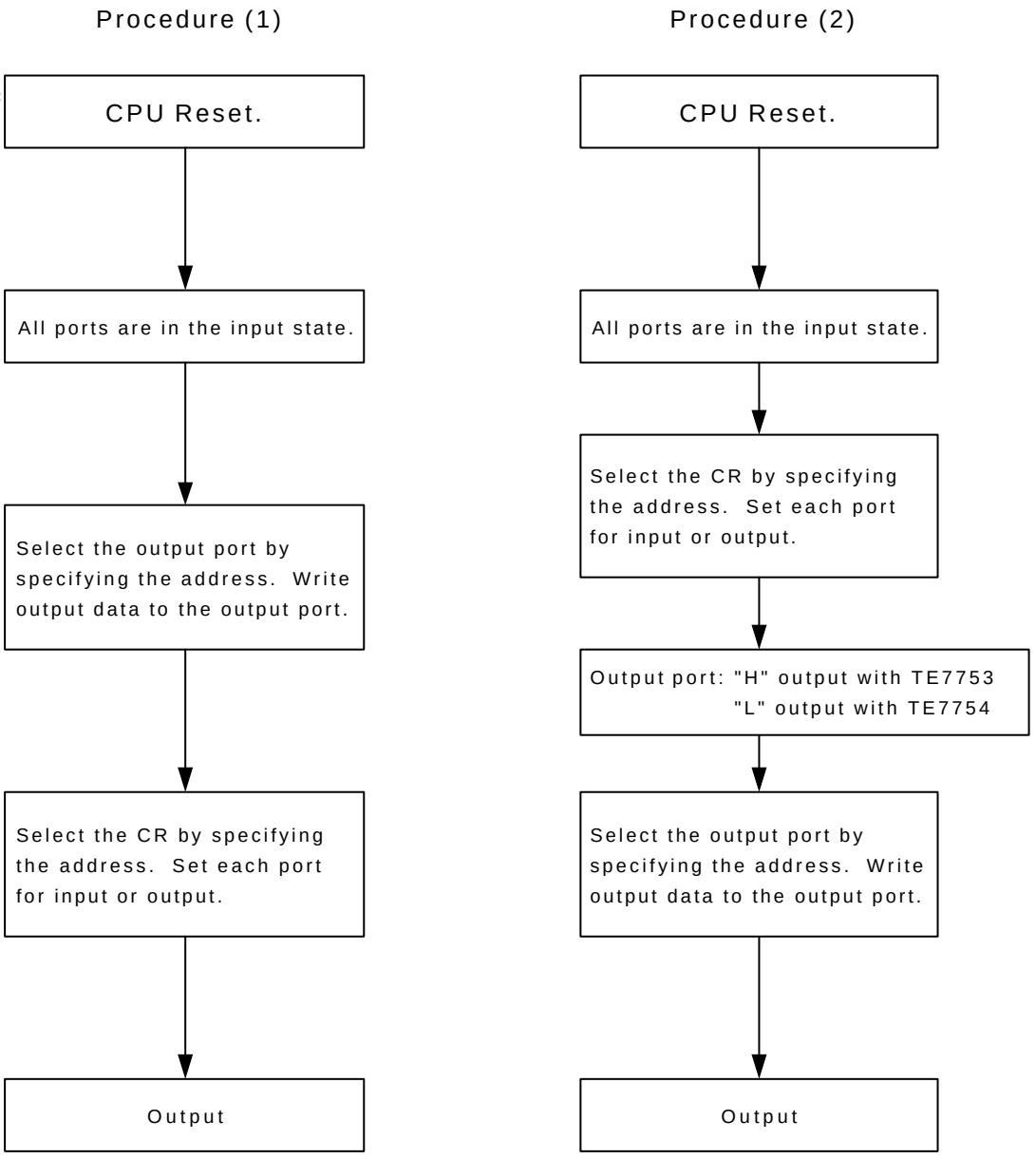
Port No	CR used	Nibble input/output	Bit input/output
1	Always input	NG	NG
2	IOS2	NG	NG
3		NG	NG
4	IOS1	NG	NG
5		NG	NG
6	IOS0	NG	NG
7		NG	NG
8	CR0	OK	OK
9	Always output	NG	NG

In hard mode, each port is set for input or output by IOS2, IOS1, and IOS0.

IOS0	IOS1	IOS2	PORT1	PORT2	PORT3	PORT4	PORT5	PORT6	PORT7	PORT9
0	0	1	I	O	O	O	O	O	O	O
0	1	0	I	I	O	O	O	O	O	O
0	1	1	I	I	I	O	O	O	O	O
1	0	0	I	I	I	I	O	O	O	O
1	0	1	I	I	I	I	I	O	O	O
1	1	0	I	I	I	I	I	I	O	O
1	1	1	I	I	I	I	I	I	I	O
0	0	0	Soft mode							

2. Setting Each Port for Input or Output Using CR

The following two procedures are available for setting each port for input or output using CR:



[Absolute Maximum Ratings]

The maximum ratings are the threshold values that must not be exceeded even momentarily. In other words, as long as the device is used within the range defined by the maximum ratings, no permanent damage is given to the device. However, this does not guarantee normal theoretical operation.

Item	Symbol	Rating	Unit
Supply voltage	V_{DD}	-0.5 ~ +6.0	V
Input voltage	V_I	-0.5 ~ V_{DD}+0.5	V
Output voltage	V_O	-0.5 ~ V_{DD}+0.5	V
Operating ambient temperature	T_{OP}	-40 ~ +85	°C
Storage ambient temperature	T_{ST}	-65 ~ +150	°C

[Recommended Operation Conditions]

The recommended operation conditions indicate the values with which normal logic operation of the device is guaranteed. In other words, it is guaranteed that the electrical characteristics (DC and AC characteristics) are satisfied as long as the device is used within the scope of the recommended operation conditions.

Item	Symbol	Min.	Max.	Pin
Supply voltage	V_{DD}	4.50	5.50	V
Operating ambient temperature	T_A	0	70	°C

[AC Characteristics]

Item	Symbol	Condition	Specifications		Unit
			Min.	Max.	
Supply current	I_{DDS}	Stopped state (*1)	-	0.1	mA
Level-1 input voltage	V_{IH}	TTL level standard	2.3	V_{DD}	V
Level-0 input voltage	V_{IL}	TTL level standard	V_{SS}	0.7	V
Level-H output voltage	V_{OH}	I_{OH}=-2mA	V_{DD}–0.4	V_{DD}	V
		I_{OH}=-4mA	V_{DD}–0.4	V_{DD}	
Level-L output voltage	V_{OL}	I_{OL}=4mA	V_{SS}	0.4	V
		I_{OL}=12mA	V_{SS}	0.4	

*1 Voltage applied to input pin: Fixed to 0 V, V_{DD}.

<CMOS Schmitt trigger input characteristics>

Item	Symbol	Min.	Max.	Unit
Level-1 threshold voltage	V_{T+}	2.8	3.8	V
Level-0 threshold voltage	V_{T-}	1.1	1.8	
Hysteresis width	V_{T+}-V_{T-}	1.3	2.0	

[Input/Output Pin Capacity]

Item	Symbol	Specifications	Unit
Input pin	C_{IN}	Up to 20	PF
Output pin	C_{OUT}	Up to 20	
Input/output pin	$C_{I/O}$	Up to 20	

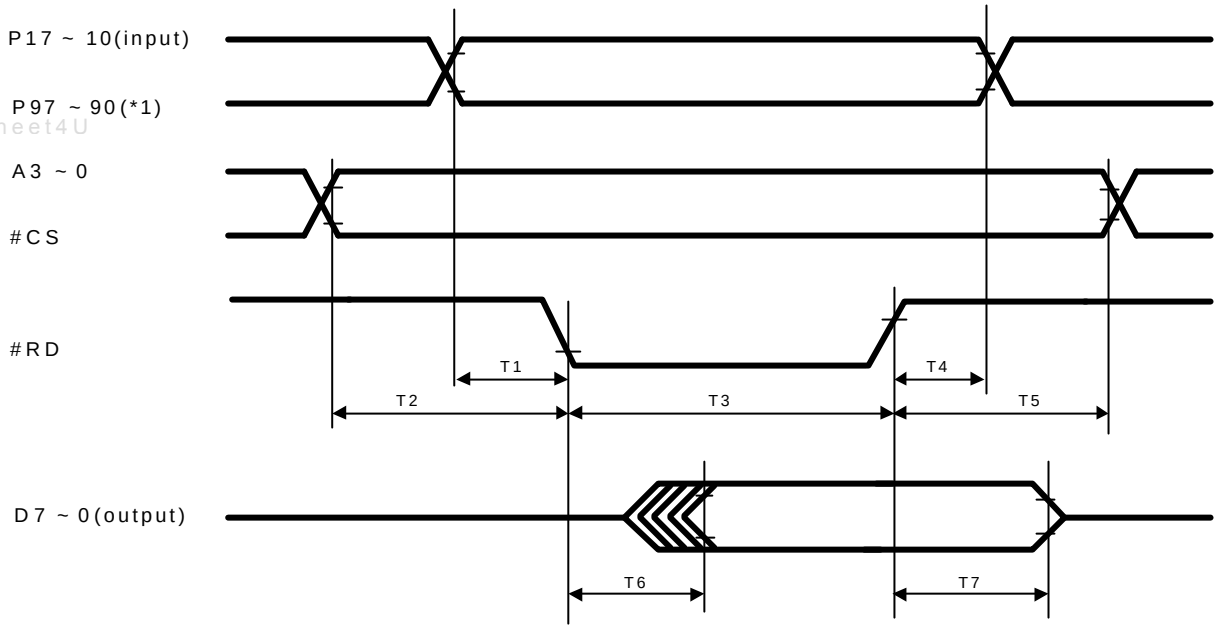
[AC Characteristics]

Load characteristics are specified as 85 pF for an input/output pin and an output pin.

1. Writing to or reading from a port

[When MS is 0]

<Port → D7 to D0>

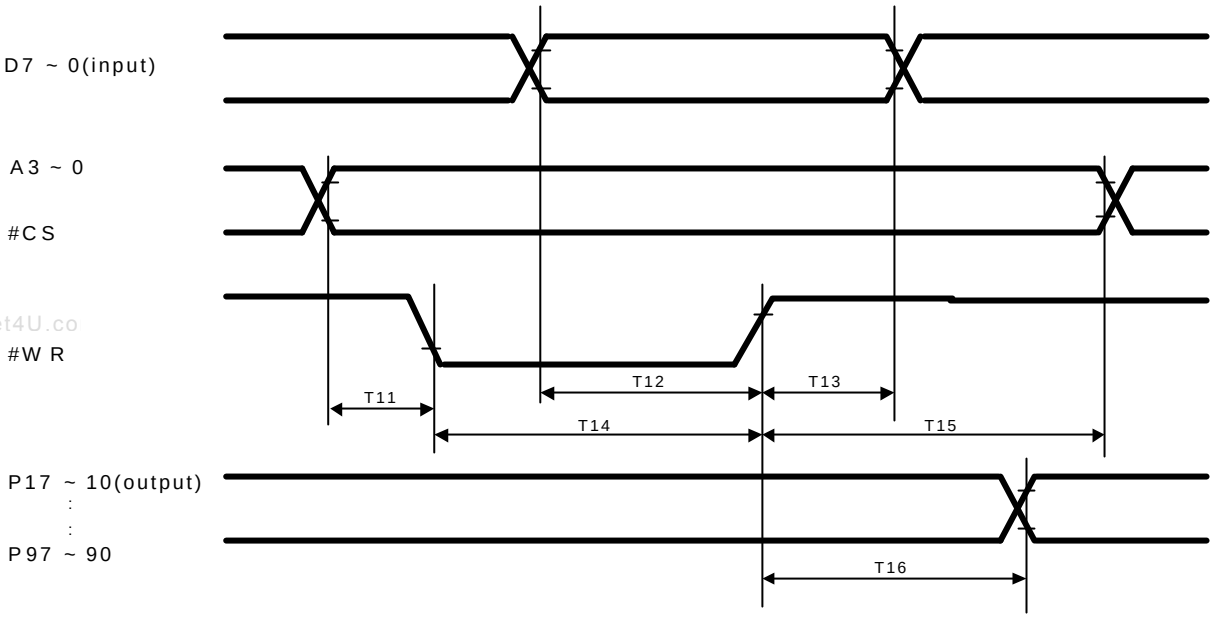


Timing No.	Reference signal	Applicable signal	Type	Min.	Max.	Unit
T1	#RD↓	P17 ~ 10 : : P97 ~ 90	S	0	-	ns
T2	#RD↓	A3 ~ 0 #CS	S	0	-	
T3	#RD↓	#RD↑	W	55	-	
T4	#RD↑	P17 ~ 10 : : P97 ~ 90	H	0	-	
T5	#RD↑	A3 ~ 0 #CS	H	0	-	
T6	#RD↓	D7 ~ 0	D	-	40	
T7	#RD↑	D7 ~ 0	H	5	20	

Type specification : S: Setup H: Hold D: Delay W: Width

*1 “P17 ~ 10” in the applicable signal column includes all of ports 1 to 9.
:
:
P97 ~ 90

<D7 ~ D0 → port>

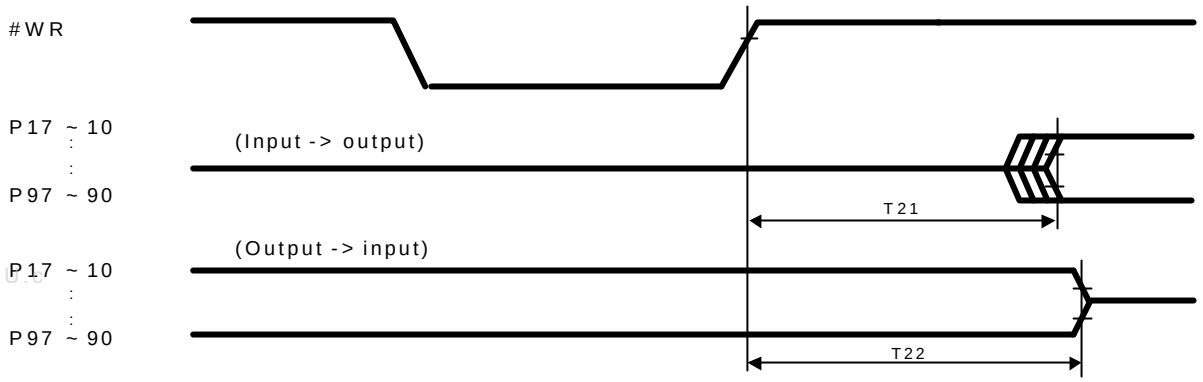


Timing No.	Reference signal	Applicable signal	Type	Min.	Max.	Unit
T11	#WR↓	A3 ~ 0 #CS	S	3	-	ns
T12	#WR↑	D7 ~ 0	S	6	-	
T13	#WR↑	D7 ~ 0	H	0	-	
T14	#WR↓	#WR↑	W	25	-	
T15	#WR↑	A3 ~ 0 #CS	H	0	-	
T16	#WR↑	P17 ~ 10 : : P97 ~ 90	D	-	30	

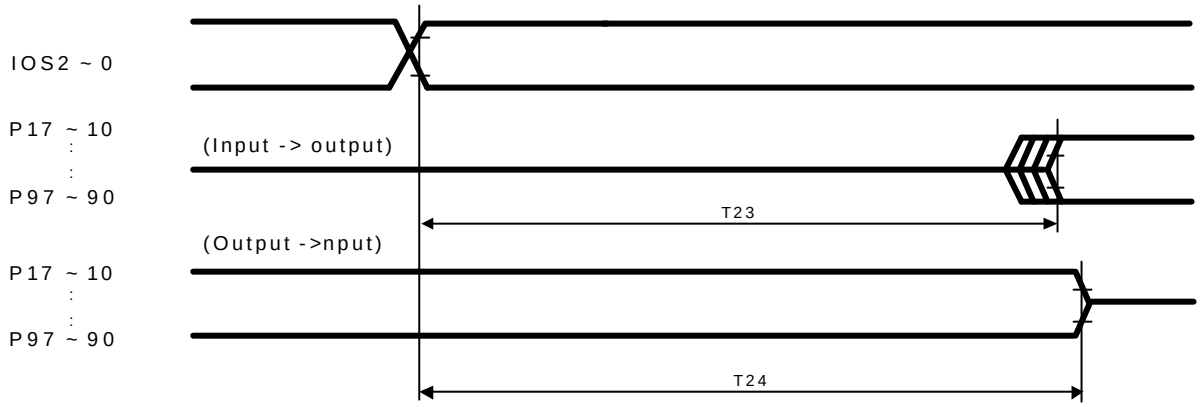
Type specification : S: Setup H: Hold D: Delay W: Width

<Switching between port input and output>

Soft mode



Hard mode

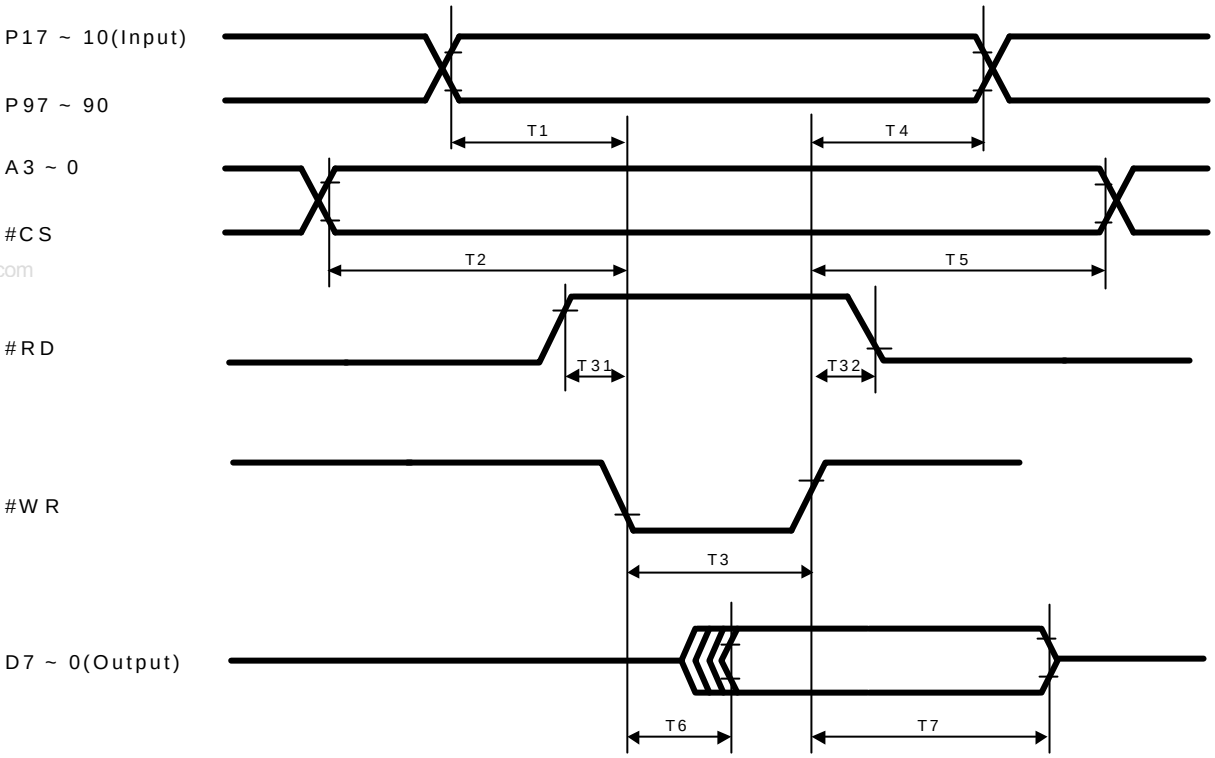


Timing No.	Reference signal	Applicable signal	Type	Min.	Max.	Unit
T21	#WR↑	P17 ~ 10 : : P97 ~ 90	D	-	30	ns
T22	#WR↑	P17 ~ 10 : : P97 ~ 90	D	-	25	
T23	IOS2 ~ 0	P17 ~ 10 : : P97 ~ 90	D	-	15	
T24	IOS2 ~ 0	P17 ~ 10 : : P97 ~ 90	D	-	10	

Type specification : S: Setup H: Hold D: Delay W: Width

[When MS is 1]

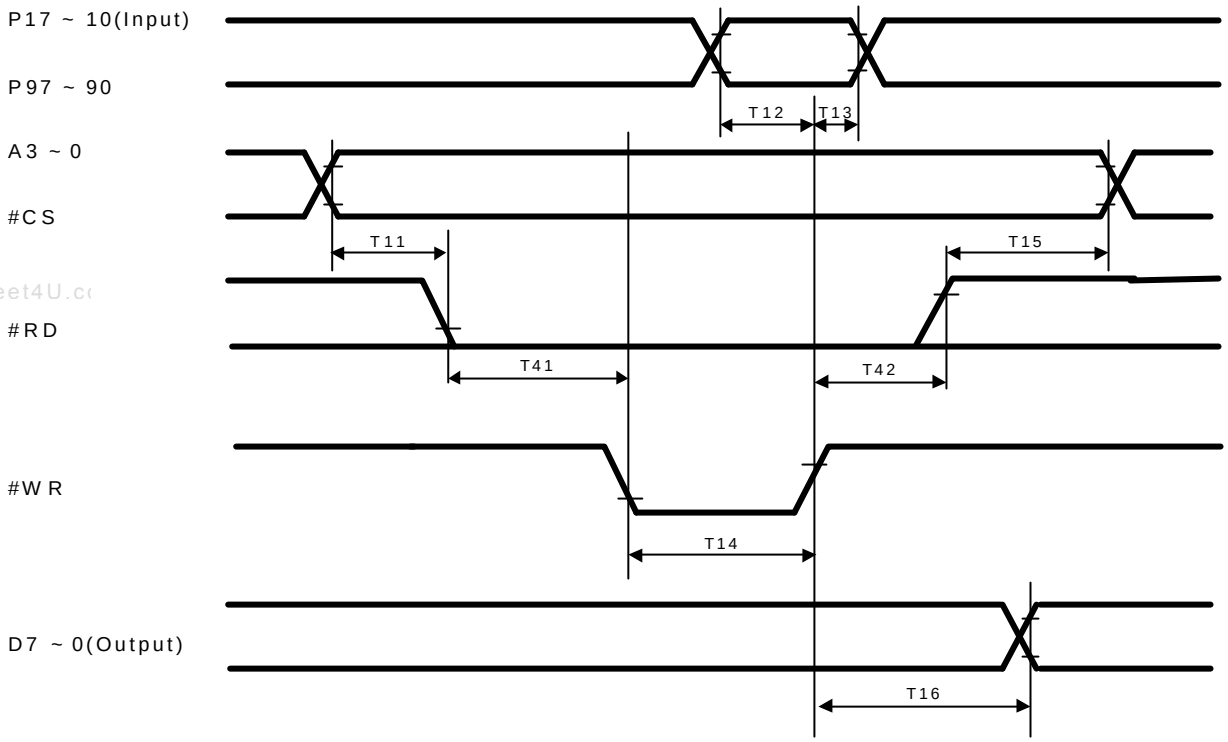
<Port -> D7 ~ 0>



Timing No.	Reference signal	Applicable signal	Type	Min.	Max.	Unit
T31	#WR↓	#RD↑	S	5	-	ns
T32	#WR↑	#RD↓	H	5	-	

Type specification : S: Setup H: Hold D: Delay W: Width

< D7 ~ 0 ->port>

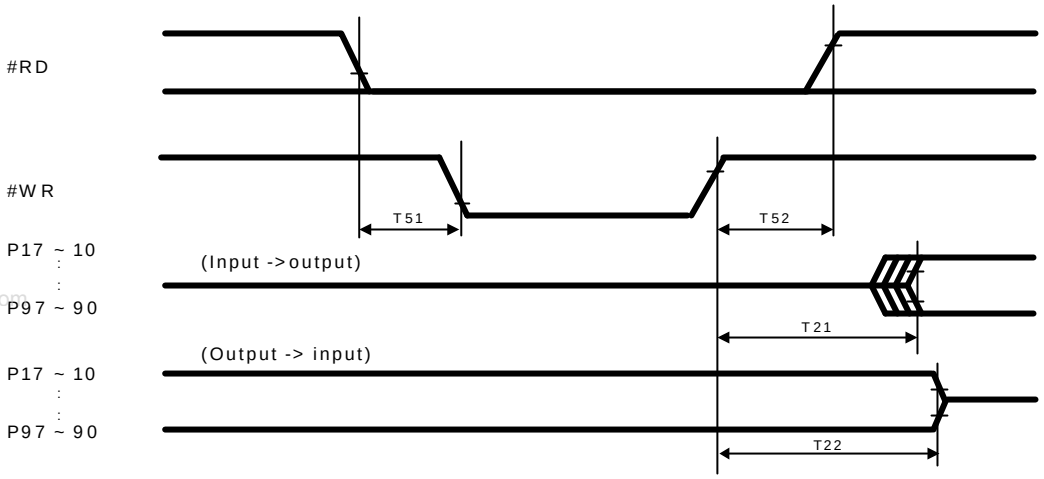


Timing No.	Reference signal	Applicable signal	Type	Min.	Max.	Unit
T41	#WR↓	#RD↓	S	5	-	ns
T42	#WR↑	#RD↑	H	5	-	

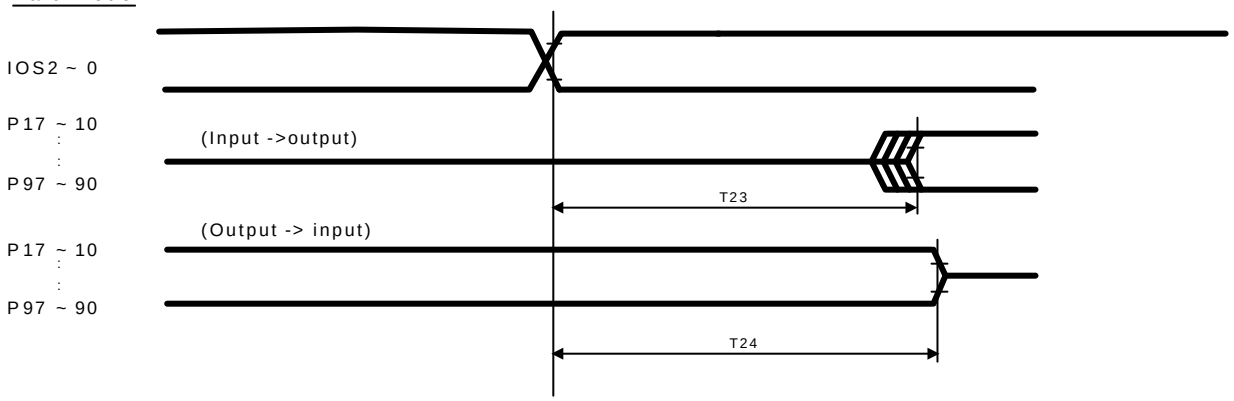
Type specification : S: Setup H: Hold D: Delay W: Width

<Switching between port input and output>

Soft mode



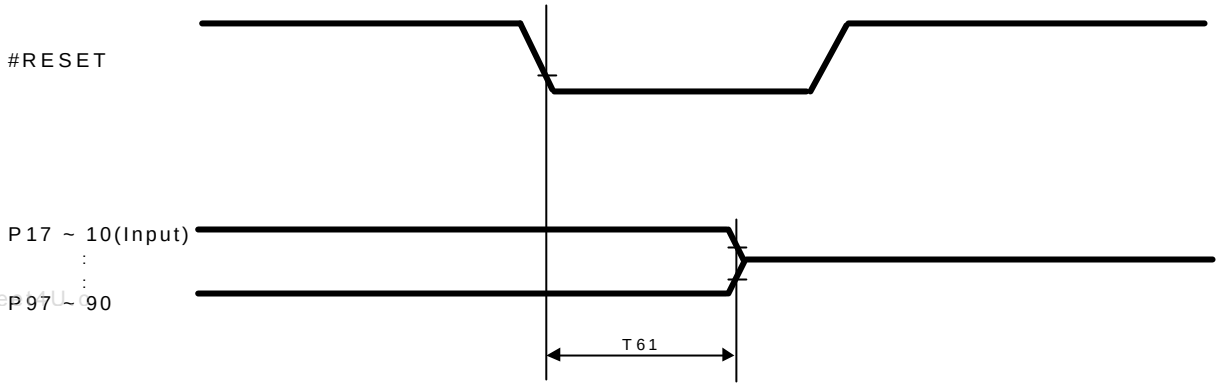
Hard mode



Timing No.	Reference signal	Applicable signal	Type	Min.	Max.	Unit
T51	#WR↓	#RD↓	S	5	-	ns
T52	#WR↑	#RD↑	H	5	-	

Type specification : S: Setup H: Hold D: Delay W: Width

2. Reset Timing

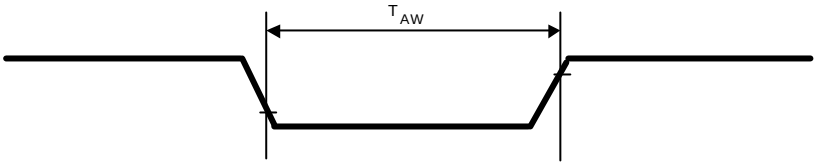


Timing No.	Reference signal	Applicable signal	Type	Min.	Max.	Unit
T61	#RESET↓	P17 ~ 10 : : P97 ~ 90	D	-	25	ns

Type specification : S: Setup H: Hold D: Delay W: Width

[Reset Input Conditions]

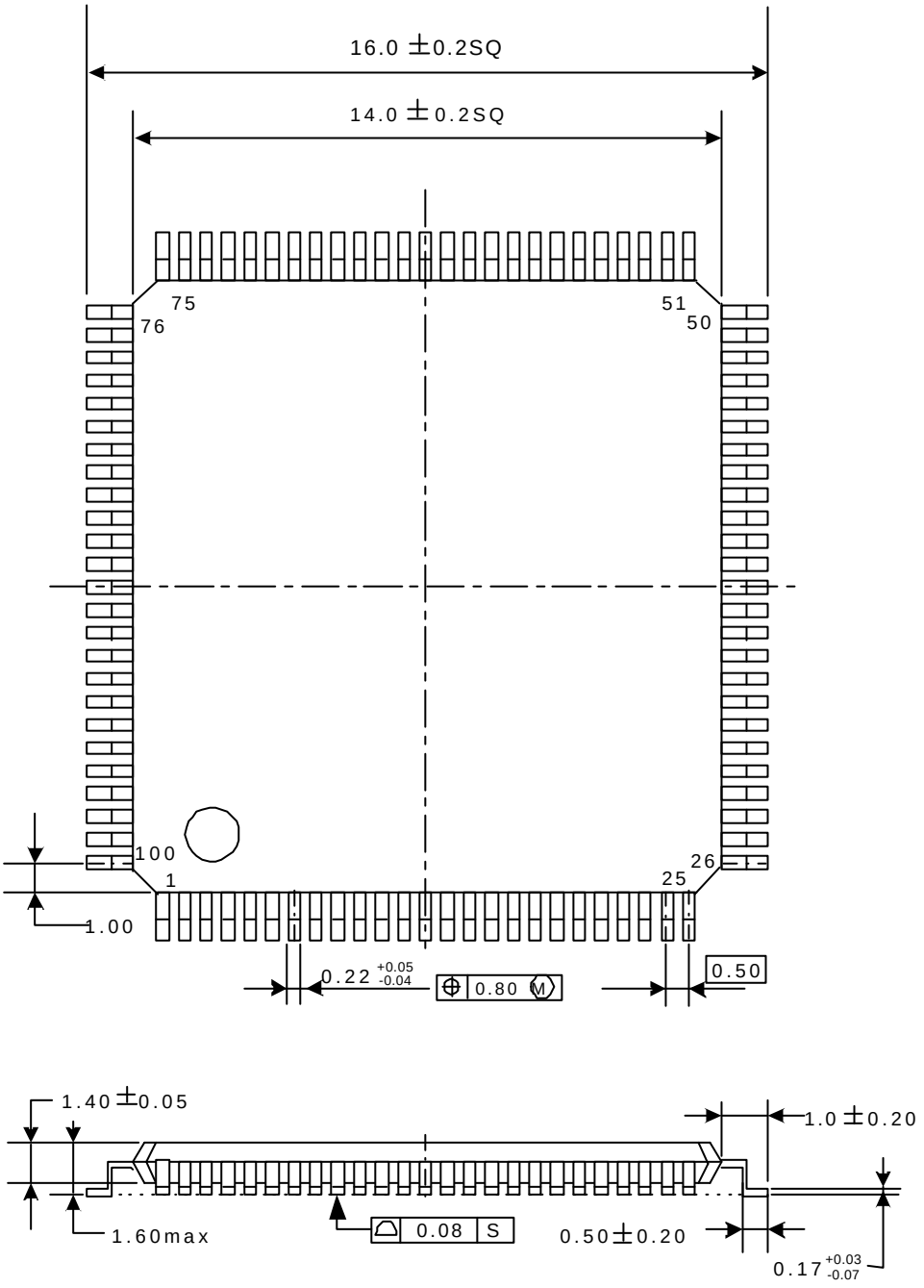
The TE7753/TE7754 reset input conditions are as follows:



Characteristics	Symbol	Min.	Max.	Unit
Reset width	T_{AW}	20	-	ns

[Outside Dimensions]

100-pin plastic QFP (unit: mm)



memo

memo

NOTES

1) Tokyo Electron Device Limited does not assume any responsibility for any circuitry described other than the circuitry embodied in its product, nor represents that circuitry described herein is free from patent or copyright infringement or other rights of third parties which may result from its use.

2) Tokyo Electron Device Limited reserves the right to make changes without further notice to any products herein. TEL shall not be liable for any claim or action by third parties alleging an infringement of the intellectual property rights, such as the patent, utility models right, mask works right and copyright, where alleged liability of Users arises by reason of using “this device” in combination with other products, or of any derivative products integrating “this device”.

TOKYO ELECTRON DEVICE LIMITED

ASIA and EUROPE

TOKYO ELECTRON DEVICE LIMITED
TOP Marketing Group
1, Higashi-Kata-Chou, Tsuzuki-ku,
Yokohama-City, Kanagawa 224-0045
JAPAN
TEL:+81-45-474-7035 FAX:+81-45-474-5624
E-mail:top-e@teldevice.co.jp

U.S. and CANADA

TOKYO ELECTRON AMERICA INC.
2953 Bunker Hill Lane, Suite 201
Santa Clara, CA 95054
U.S.A.
TEL: +1-408-919-4772
E-mail: top@scl.telusa.com

Your Local Contact