

## 512K (64K x 8-bit) UV and OTP EPROM

### DESCRIPTION

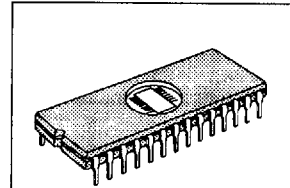
The Hitachi HN27512 is a 512-Kilobit Ultraviolet Erasable and One-Time Programmable Electrically Programmable Read Only Memory organized as 65,536 x 8-bits.

The HN27512 features low power dissipation and high speed programming.

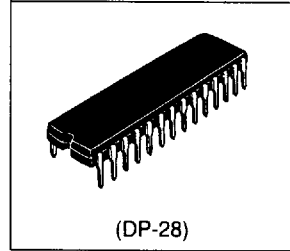
Hitachi's HN27512 is offered in JEDEC-Standard Byte-Wide EPROM pinouts in a 28-pin Ceramic and Plastic DIP packages.

### FEATURES

- Fast Access Times:  
250 ns/300 ns (max)
- Single Power Supply:  
 $V_{CC} = 5 V \pm 10\%$
- Low Power Dissipation:  
Active Mode: 45 mA (typ)  
Standby Mode: 40 mA (max)
- High Speed Programming
- Programming Power Supply:  
 $V_{PP} = 12.5 V \pm 0.3 V$
- Pin Arrangement:  
JEDEC Standard Byte-Wide EPROM
- Package:  
28-pin Ceramic DIP  
28-pin Plastic DIP



(DG-28)



(DP-28)

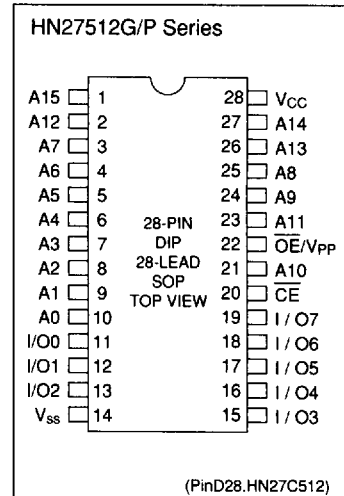
### ORDERING INFORMATION

Type No.	Access Time	Package
HN27512G-25	250 ns	28-pin Ceramic DIP
HN27512G-30	300 ns	(DG-28)
HN27512P-25	250 ns	28-pin Plastic DIP
HN27512P-30	300 ns	(DP-28)

### PIN DESCRIPTION

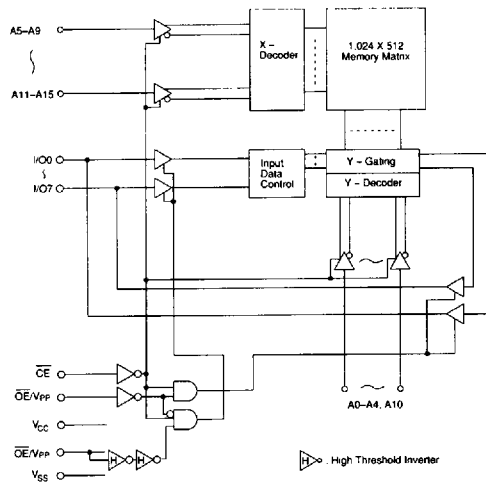
Pin Name	Function
$A_0 - A_{15}$	Address
$I/O_0 - I/O_7$	Input/Output
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$V_{CC}$	Power Supply
$V_{PP}$	Programming Supply
$V_{SS}$	Ground

### PIN ARRANGEMENT



# HN27512 Series

## ■ BLOCK DIAGRAM



(BD.HN27512)

## ■ MODE SELECTION

Mode	$V_{CC}$	$\overline{CE}$	$\overline{OE/V_{PP}}$	$A_9$	I/O
Read	$V_{CC}$	$V_{IL}$	$V_{IL}$	X <sup>1</sup>	$D_{OUT}$
Output Disable	$V_{CC}$	$V_{IL}$	$V_{IH}$	X	High-Z
Standby	$V_{CC}$	$V_{IH}$	X	X	High-Z
Program	$V_{CC}$	$V_{IL}$	$V_{PP}$	X	$D_{IN}$
Program Verify	$V_{CC}$	$V_{IL}$	$V_{IL}$	X	$D_{OUT}$
Program Inhibit	$V_{CC}$	$V_{IH}$	$V_{PP}$	X	High-Z
Identifier	$V_{CC}$	$V_{IL}$	$V_{IL}$	$V_H$ <sup>2</sup>	ID

- Notes: 1. X = Don't Care.  
2.  $11.5\text{ V} \leq V_H \leq 12.5\text{ V}$

## ■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Supply Voltage <sup>1</sup>	$V_{CC}$	-0.6 to +7.0	V
Programming Voltage <sup>1</sup>	$V_{PP}$	-0.6 to +13.5	V
All Input and Output Voltage <sup>1</sup>	$V_{IN}, V_{OUT}$	-0.6 to +7.0	V
$A_9$ Input Voltage	$V_{ID}$	-0.6 to +13.5	V
Operating Temperature Range	$T_{OPR}$	0 to +70	°C
Storage Temperature Range	$T_{STG}$	-65 to +125 <sup>2</sup> -55 to +125 <sup>3</sup>	°C
Storage Temperature Under Bias	$T_{BIAS}$	-10 to +80	°C

- Notes: 1. Relative to  $V_{SS}$ .  
2. HN27512G.  
3. HN27512P.

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■ CAPACITANCE ( $T_a = 25^\circ\text{C}$ ,  $f = 1\text{MHz}$ )

Item	Symbol	Typ.	Max.	Unit	Test Condition
Input Capacitance	$C_{IN}$	4	6	pF	$V_{IN} = 0\text{V}$ , all pins except $\overline{OE}/V_{PP}$
Output Capacitance	$C_{OUT}$	8	12	pF	$V_{OUT} = 0\text{V}$

■ DC ELECTRICAL CHARACTERISTICS FOR READ OPERATION

( $V_{CC} = 5\text{V} \pm 10\%$ ,  $T_a = 0$  to  $70^\circ\text{C}$ )

Item	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Input Leakage Current	$I_{LI}$	-	-	10	$\mu\text{A}$	$V_{IN} = 0\text{V}$ to $V_{CC}$
Output Leakage Current	$I_{LO}$	-	-	10	$\mu\text{A}$	$V_{OUT} = 0\text{V}$ to $V_{CC}$
Operating $V_{CC}$ Current	$I_{CC}$	-	45	100	mA	$\overline{CE} = \overline{OE} = V_{IL}$
Standby $V_{CC}$ Current	$I_{SB}$	-	-	40	mA	$\overline{CE} = V_{IH}$
Input Voltage	$V_{IH}$	2.2	-	$V_{CC} + 1^2$	V	
	$V_{IL}$	-0.1 <sup>1</sup>	-	0.8	V	
Output Voltage	$V_{OH}$	2.4	-	-	V	$I_{OH} = 1.0\text{mA}$
	$V_{OL}$	-	-	0.45	V	$I_{OL} = 2.1\text{mA}$

- Notes: 1.  $V_{IL}$  min = -0.6 V for pulse width  $\leq 20\text{ns}$ .  
 2.  $V_{IH}$  max =  $V_{CC} + 1.5\text{V}$  for pulse width  $\leq 20\text{ns}$ .  
 If  $V_{IH}$  is over the specified maximum value, Read operation can not be guaranteed.

■ AC ELECTRICAL CHARACTERISTICS FOR READ OPERATION

( $V_{CC} = 5\text{V} \pm 10\%$ ,  $T_a = 0$  to  $70^\circ\text{C}$ )

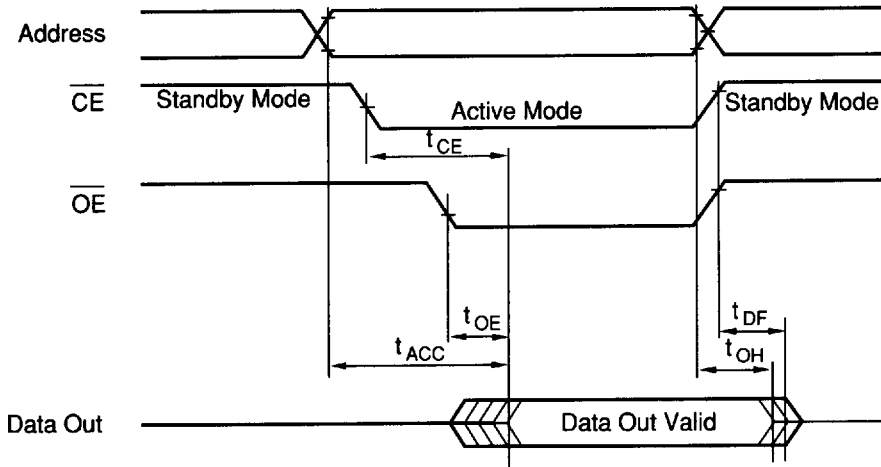
Test Conditions

- Input pulse levels: 0.45 V / 2.4 V
- Input rise and fall times:  $\leq 20\text{ns}$
- Output load: 1 TTL Gate + 100 pF (Including scope and jig)
- Reference levels for measuring timing: 0.8 V / 2.0 V

Item	Symbol	-25		-30		Unit	Test Condition
		Min.	Max.	Min.	Max.		
Address Access Time	$t_{ACC}$	-	250	-	300	ns	$\overline{CE} = \overline{OE} = V_{IL}$
Chip Enable Access Time	$t_{CE}$	-	250	-	300	ns	$\overline{OE} = V_{IL}$
Output Enable Access Time	$t_{OE}$	-	100	-	120	ns	$\overline{CE} = V_{IL}$
Output Disable to High-Z <sup>1</sup>	$t_{DF}$	0	60	0	105	ns	$\overline{CE} = V_{IL}$
Output Hold to Address Change	$t_{OH}$	0	-	0	-	ns	$\overline{CE} = \overline{OE} = V_{IL}$

- Note: 1.  $t_{DF}$  is defined as the time at which the output becomes an open circuit and data is no longer driven.

■ READ TIMING WAVEFORM



(TD.R.HN27512)

■ DC ELECTRICAL CHARACTERISTICS FOR PROGRAMMING OPERATIONS

( $V_{CC} = 6.0\text{ V} \pm 0.25\text{ V}$ ,  $V_{PP} = 12.5\text{ V} \pm 0.3\text{ V}$ ,  $T_a = 25\text{ }^\circ\text{C} \pm 5\text{ }^\circ\text{C}$ )

Item	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Input Leakage Current	$I_{LI}$	-	-	10	$\mu\text{A}$	$V_{IN} = 5.25\text{ V}$
Operating $V_{CC}$ Current	$I_{CC}$	-	-	100	mA	
Operating $V_{PP}$ Current	$I_{PP}$	-	35	50	mA	$\overline{CE} = V_{IL}$
Input Voltage <sup>1</sup>	$V_{IH}$	2.0	-	$V_{CC} + .5$ <sup>2</sup>	V	
	$V_{IL}$	-0.1 <sup>1</sup>	-	0.8	V	
Output Voltage	$V_{OH}$	2.4	-	-	V	$I_{OH} = -400\text{ }\mu\text{A}$
	$V_{OL}$	-	-	0.45	V	$I_{OH} = 2.1\text{ mA}$

- Notes: 1.  $V_{IL}$  min = -0.6 V for pulse width  $\leq 20\text{ ns}$ .  
 2. If  $V_{IH}$  is over the specified maximum value, programming operation can not be guaranteed.

■ **AC ELECTRICAL CHARACTERISTICS FOR PROGRAMMING OPERATIONS**

( $V_{CC} = 6\text{ V} \pm 0.25\text{ V}$ ,  $V_{PP} = 12.5\text{ V} \pm 0.5\text{ V}$ ,  $T_a = 25^\circ\text{C} \pm 5^\circ\text{C}$ )

**Test Conditions**

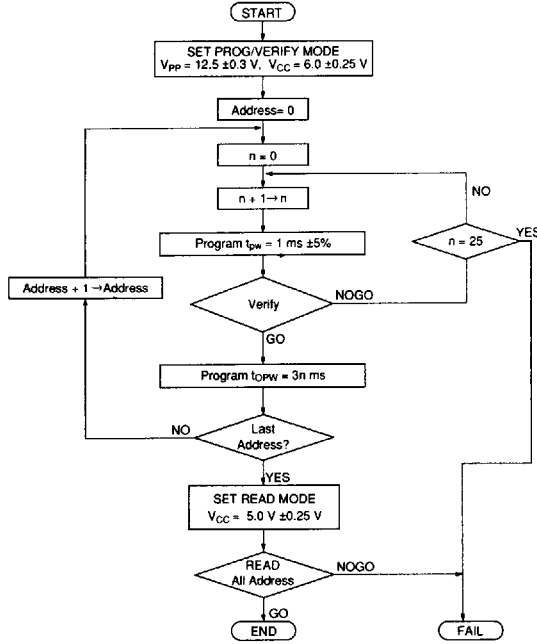
- Input pulse levels: 0.45 V / 2.4 V
- Input rise and fall times:  $\leq 20\text{ ns}$
- Reference levels for measuring timing: 0.8 V / 2.0V

Item	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Address Setup Time	$t_{AS}$	2	-	-	$\mu\text{s}$	
Address Hold Time	$t_{AH}$	0	-	-	$\mu\text{s}$	
Data Setup Time	$t_{DS}$	2	-	-	$\mu\text{s}$	
$V_{PP}$ Setup Time	$t_{VPS}$	2	-	-	$\mu\text{s}$	
$V_{CC}$ Setup Time	$t_{VCS}$	2	-	-	$\mu\text{s}$	
Output Enable Hold Time	$t_{OEHL}$	2	-	-	$\mu\text{s}$	
Output Disable Time	$t_{DF}$	0	-	130	ns	
$\overline{CE}$ Initial Programming Pulse Width	$t_{PW}$	0.95	1.0	1.05	ms	
$\overline{CE}$ Overprogramming Pulse Width	$t_{OPW}$	2.85	-	78.75	ms	
Data Hold Time	$t_{DH}$	2	-	-	$\mu\text{s}$	
$V_{PP}$ Recovery Time	$t_{VR}$	2	-	-	$\mu\text{s}$	
Data Valid from Chip Enable	$t_{DV}$	-	-	1	$\mu\text{s}$	

Note: 1.  $t_{DF}$  is defined as the time at which the output becomes an open circuit and data is no longer driven.

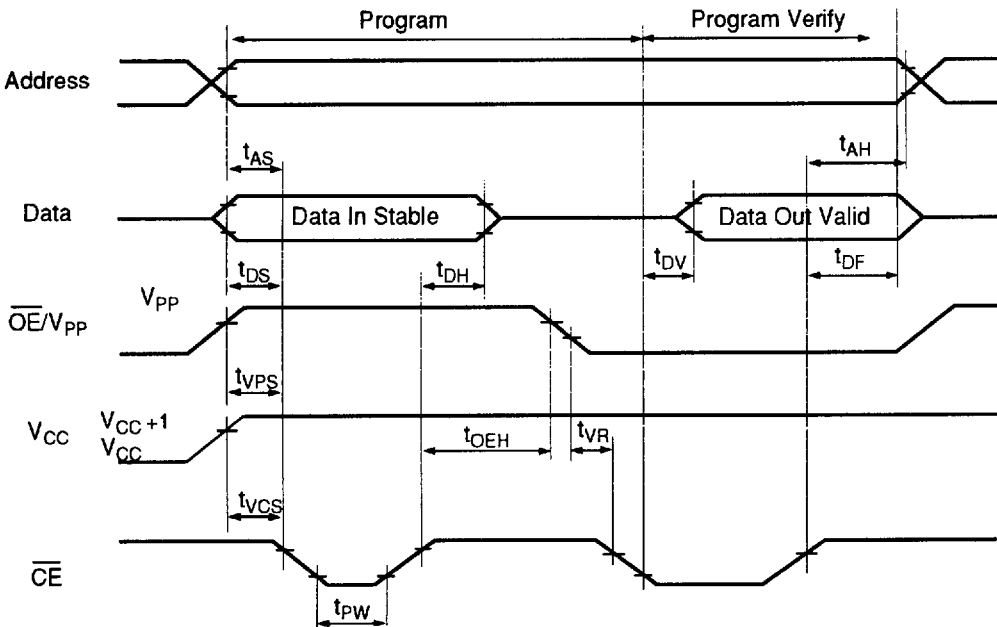
**■ HIGH PERFORMANCE PROGRAMMING FLOWCHART**

The Hitachi HN27512 can be programmed with the High Performance Programming algorithm shown in the following flowchart. This algorithm provides a fast programming time without voltage stress to the device or deterioration in reliability of programmed data.



(FC.P.HN27512)

**■ HIGH PERFORMANCE PROGRAMMING TIMING WAVEFORM**



(TD.PP.HN27512)

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■ ERASING THE HN27512

The Hitachi HN27512 Ceramic DIP package allows the device to be erased by exposure to ultraviolet light of 2537Å. All of the data is changed to "1" after this erasure procedure. The minimum integrated dose (UV intensity x exposure time) for erasure is 15 W-sec/cm<sup>2</sup>.

■ DEVICE IDENTIFIER MODE DESCRIPTION

The Device Identifier Mode allows binary codes to be read from the outputs that identify the manufacturer and the type of device. Using this mode with programming equipment, the device will automatically match its own erase and programming algorithm.

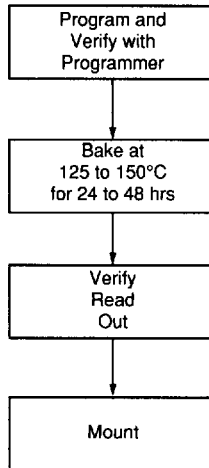
■ HN27512 SERIES IDENTIFIER CODE

Identifier	A <sub>0</sub>	I/O <sub>7</sub>	I/O <sub>6</sub>	I/O <sub>5</sub>	I/O <sub>4</sub>	I/O <sub>3</sub>	I/O <sub>2</sub>	I/O <sub>1</sub>	I/O <sub>0</sub>	Hex Data
Manufacturer Code	V <sub>IL</sub>	0	0	0	0	0	1	1	1	07
Device Code	V <sub>IH</sub>	1	0	0	1	0	1	0	0	94

- Notes: 1. A<sub>9</sub> = 12.0 V ± 0.5V  
 3. A<sub>1</sub>-A<sub>8</sub>, A<sub>10</sub>-A<sub>15</sub>,  $\overline{CE}$ ,  $\overline{OE}/V_{PP} = V_{IL}$

■ HN27512P RECOMMENDED SCREENING CONDITIONS

Before mounting the HN27512P package, please make the following screening (baking without bias) shown below:



(RSC.EPROM)