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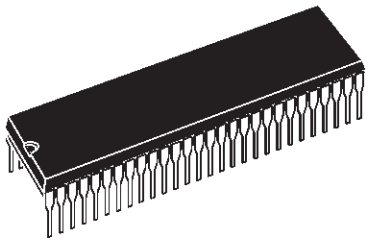
ST92195B

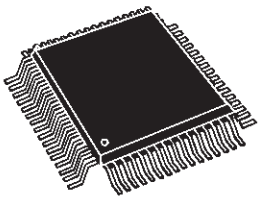
32-64K ROM HCMOS MCU WITH ON-SCREEN-DISPLAY AND TELETEXT DATA SLICER

DATA BRIEFING

- Register File based 8/16 bit Core Architecture with RUN, WFI, SLOW and HALT modes
- 0°C to +70°C operating temperature range
- Up to 24 MHz. operation @ 5V±10%
- Min. instruction cycle time: 165ns at 24 MHz.
- 32, 48, 56 or 64 Kbytes ROM
- 256 bytes RAM of Register file (accumulators or index registers)
- 256 bytes of on-chip static RAM
- 2, 6 or 8 Kbytes of TDSRAM (Teletext and Display Storage RAM)
- 28 fully programmable I/O pins
- Serial Peripheral Interface
- Flexible Clock controller for OSD, Data Slicer and Core clocks running from a single low frequency external crystal.
- Enhanced display controller with 26 rows of 40/80 characters
  - Serial and Parallel attributes
  - 10x10 dot matrix, 512 ROM characters, definable by user
  - 4/3 and 16/9 supported in 50/60Hz and 100/120 Hz mode
  - Rounding, fringe, double width, double height, scrolling, cursor, full background color, half-intensity color, translucency and half-tone modes
- Teletext unit, including Data Slicer, Acquisition Unit and up to 8 Kbytes RAM for data storage
- VPS and Wide Screen Signalling slicer (on some devices)
- Integrated Sync Extractor and Sync Controller
- 14-bit Voltage Synthesis for tuning reference voltage
- Up to 6 external interrupts plus one Non-Maskable Interrupt
- 8 x 8-bit programmable PWM outputs with 5V open-drain or push-pull capability
- 16-bit watchdog timer with 8-bit prescaler
- One 16-bit standard timer with 8-bit prescaler
- 4-channel A/D converter; 5-bit guaranteed



PSDIP56



TQFP64

See end of document for ordering information

- Rich instruction set and 14 addressing modes
- Versatile development tools, including Assembler, Linker, C-compiler, Archiver, Source Level Debugger and hardware emulators with Real-Time Operating System available from third parties
- Pin-compatible EPROM and OTP devices available

Device Summary

Device	Program Memory	TDS RAM	VPS/ WSS	Package
ST92195B1	32K ROM	2K	Yes	PSDIP56/ TQFP64
ST92195B2	32K ROM	6K	No	
ST92195B3	32K ROM	6K	Yes	
ST92195B4	48K ROM	6K	Yes	
ST92195B5	48K ROM	8K	Yes	
ST92195B6	56K ROM	8K	Yes	
ST92195B7	64K ROM	8K	Yes	
ST92T195B7	64K OTP	8K	Yes	
ST92E195B7	64K EPROM	8K	Yes	CSDIP56 /CQFP64

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1 GENERAL DESCRIPTION

1.1 INTRODUCTION

The ST92195B microcontroller is developed and manufactured by STMicroelectronics using a proprietary n-well HCMOS process. Its performance derives from the use of a flexible 256-register programming model for ultra-fast context switching and real-time event response. The intelligent on-chip peripherals offload the ST9 core from I/O and data management processing tasks allowing critical application tasks to get the maximum use of core resources. The ST92195B MCU supports low power consumption and low voltage operation for power-efficient and low-cost embedded systems.

1.1.1 ST9+ Core

The advanced Core consists of the Central Processing Unit (CPU), the Register File and the Interrupt controller.

The general-purpose registers can be used as accumulators, index registers, or address pointers. Adjacent register pairs make up 16-bit registers for addressing or 16-bit processing. Although the ST9 has an 8-bit ALU, the chip handles 16-bit operations, including arithmetic, loads/stores, and memory/register and memory/memory exchanges.

Two basic addressable spaces are available: the Memory space and the Register File, which includes the control and status registers of the on-chip peripherals.

1.1.2 Power Saving Modes

To optimize performance versus power consumption, a range of operating modes can be dynamically selected.

Run Mode. This is the full speed execution mode with CPU and peripherals running at the maximum clock speed delivered by the Phase Locked Loop (PLL) of the Clock Control Unit (CCU).

Wait For Interrupt Mode. The Wait For Interrupt (WFI) instruction suspends program execution until an interrupt request is acknowledged. During WFI, the CPU clock is halted while the peripheral and interrupt controller keep running at a frequency programmable via the CCU. In this mode, the power consumption of the device can be reduced by more than 95% (Low power WFI).

Halt Mode. When executing the HALT instruction, and if the Watchdog is not enabled, the CPU and its peripherals stop operating and the status of the machine remains frozen (the clock is also stopped). A reset is necessary to exit from Halt mode.

1.1.3 I/O Ports

Up to 28 I/O lines are dedicated to digital Input/ Output. These lines are grouped into up to five I/O Ports and can be configured on a bit basis under software control to provide timing, status signals, timer and output, analog inputs, external interrupts and serial or parallel I/O.

1.1.4 TV Peripherals

A set of on-chip peripherals form a complete system for TV set and VCR applications:

– Voltage Synthesis

– VPS/WSS Slicer

– Teletext Slicer

– Teletext Display RAM

– OSD

1.1.5 On Screen Display

The human interface is provided by the On Screen Display module, this can produce up to 26 lines of up to 80 characters from a ROM defined 512 character set. The character resolution is 10x10 dot. Four character sizes are supported. Serial attributes allow the user to select foreground and background colors, character size and fringe background. Parallel attributes can be used to select additional foreground and background colors and underline on a character by character basis.

1.1.6 Teletext and Display Storage RAM

The internal Teletext and Display storage RAM can be used to store Teletext pages as well as Display parameters.

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INTRODUCTION (Cont'd)

1.1.7 Teletext, VPS and WSS Data Slicers

The three on-board data slicers using a single external crystal are used to extract the Teletext, VPS and WSS information from the video signal. Hardware Hamming decoding is provided.

1.1.8 Voltage Synthesis Tuning Control

14-bit Voltage Synthesis using the PWM (Pulse Width Modulation)/BRM (Bit Rate Modulation) technique can be used to generate tuning voltages for TV set applications. The tuning voltage is output on one of two separate output pins.

1.1.9 PWM Output

Control of TV settings can be made with up to eight 8-bit PWM outputs, with a maximum frequency of 23,437Hz at 8-bit resolution (INTCLK = 12 MHz). Low resolutions with higher frequency operation can be programmed.

1.1.10 Serial Peripheral Interface (SPI)

The SPI bus is used to communicate with external devices via the SPI, or I C bus communication standards. The SPI uses a single data line for data input and output. A second line is used for a synchronous clock signal.

1.1.11 Standard Timer (STIM)

The ST92195B has one Standard Timer (STIM0) that includes a programmable 16-bit down counter and an associated 8-bit prescaler with Single and Continuous counting modes.

1.1.12 Analog/Digital Converter (ADC)

In addition there is a 4-channel Analog to Digital Converter with integral sample and hold, fast 5.75µs conversion time and 6-bit guaranteed resolution.

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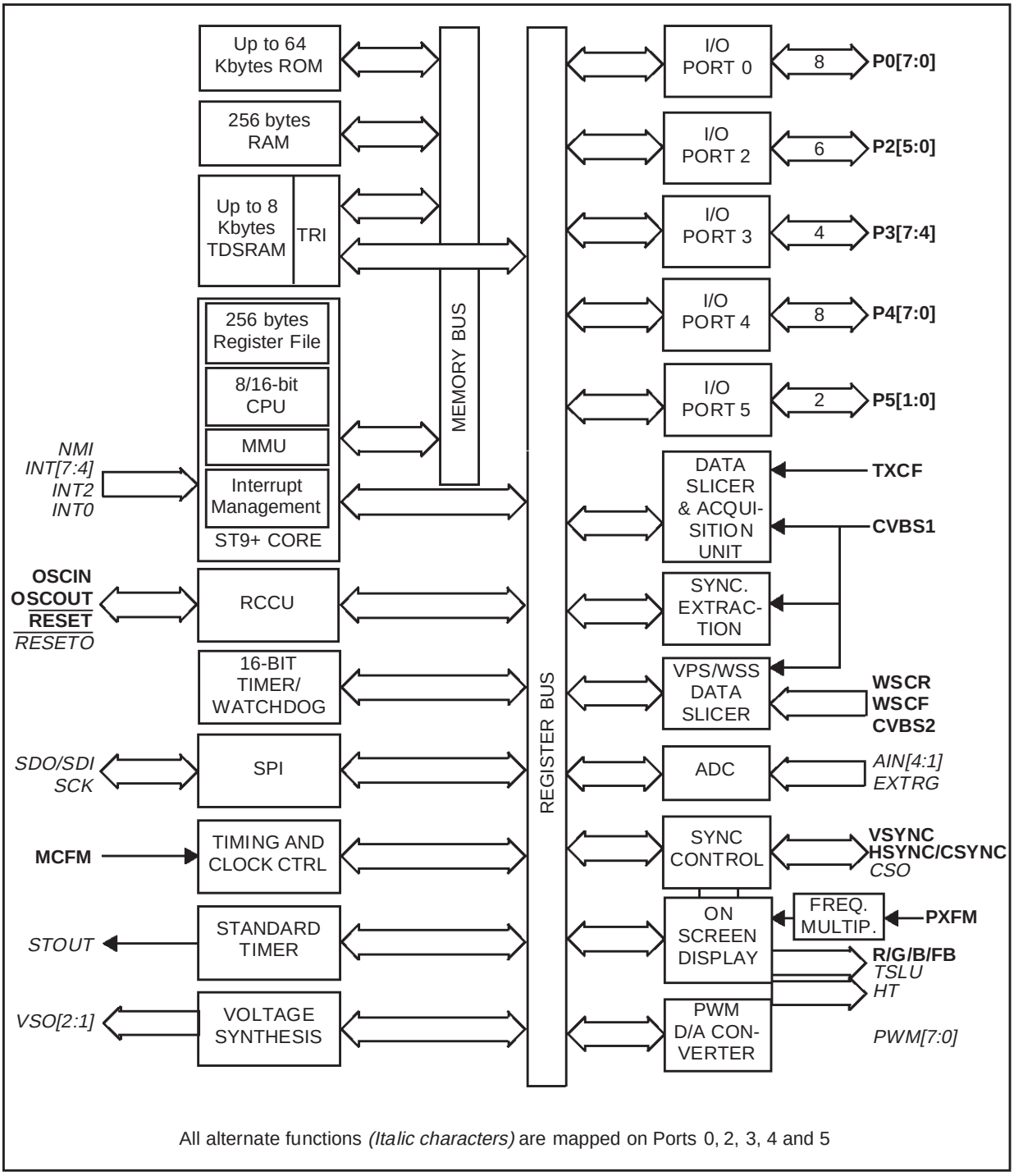
INTRODUCTION (Cont'd)

Figure 1. ST92195B Block Diagram



All alternate functions *(Italic characters)* are mapped on Ports 0, 2, 3, 4 and 5

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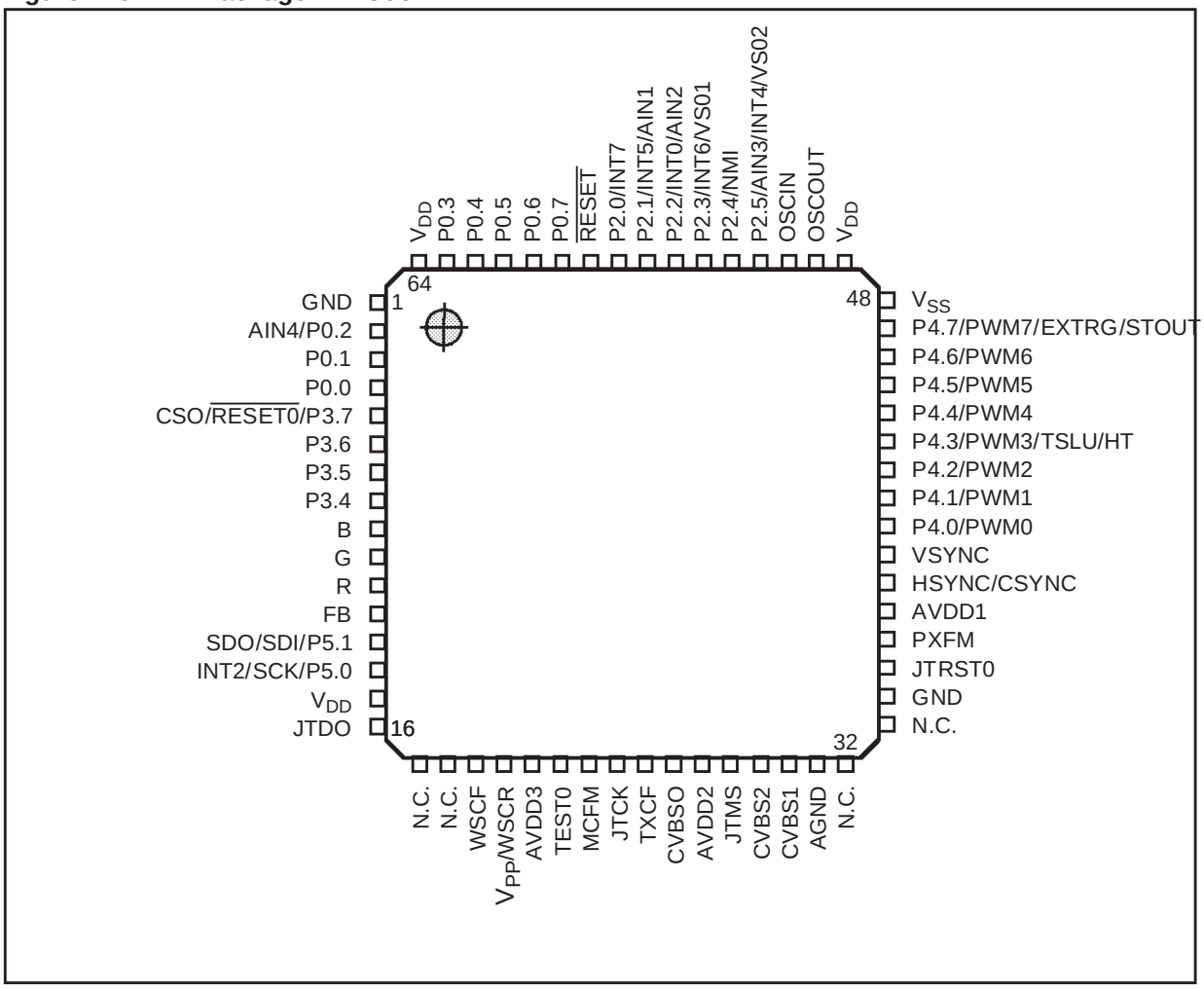
1.2 PIN DESCRIPTION

Figure 2. 64-Pin Package Pin-Out



N.C. = Not connected

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PIN DESCRIPTION (Cont'd)

$\overline{\text{RESET}}$ *Reset* (input, active low). The ST9+ is initialised by the Reset signal. With the deactivation of RESET, program execution begins from the Program memory location pointed to by the vector contained in program memory locations 00h and 01h.

R/G/B *Red/Green/Blue*. Video color analog DAC outputs.

FB *Fast Blanking*. Video analog DAC output.

V_{DD} Main power supply voltage (5V±10%, digital)

WSCF, WSCR Analog pins for the VPS/WSS slicer . These pins must be tied to ground or not connected.

V_{PP}: On EPROM/OTP devices, the WSCR pin is replaced by V_{PP} which is the programming voltage pin. V_{PP} should be tied to GND in user mode.

MCFM Analog pin for the display pixel frequency multiplier.

OSCIN, OSCOUT *Oscillator* (input and output). These pins connect a parallel-resonant crystal (24MHz maximum), or an external source to the on-chip clock oscillator and buffer. OSCIN is the input of the oscillator inverter and internal clock generator; OSCOUT is the output of the oscillator inverter.

VSYNC *Vertical Sync*. Vertical video synchronisation input to OSD. Positive or negative polarity.

HSYNC/CSYNC *Horizontal/Composite sync*. Horizontal or composite video synchronisation input to OSD. Positive or negative polarity.

PXFM Analog pin for the Display Pixel Frequency Multiplier

AVDD3 *Analog V_{DD} of PLL*. This pin must be tied to V_{DD} externally.

GND Digital circuit ground.

AGND Analog circuit ground (must be tied externally to digital GND).

CVBS1 Composite video input signal for the Teletext slicer and sync extraction.

CVBS2 Composite video input signal for the VPS/WSS slicer. Pin AC coupled.

AVDD1, AVDD2 Analog power supplies (must be tied externally to AVDD3).

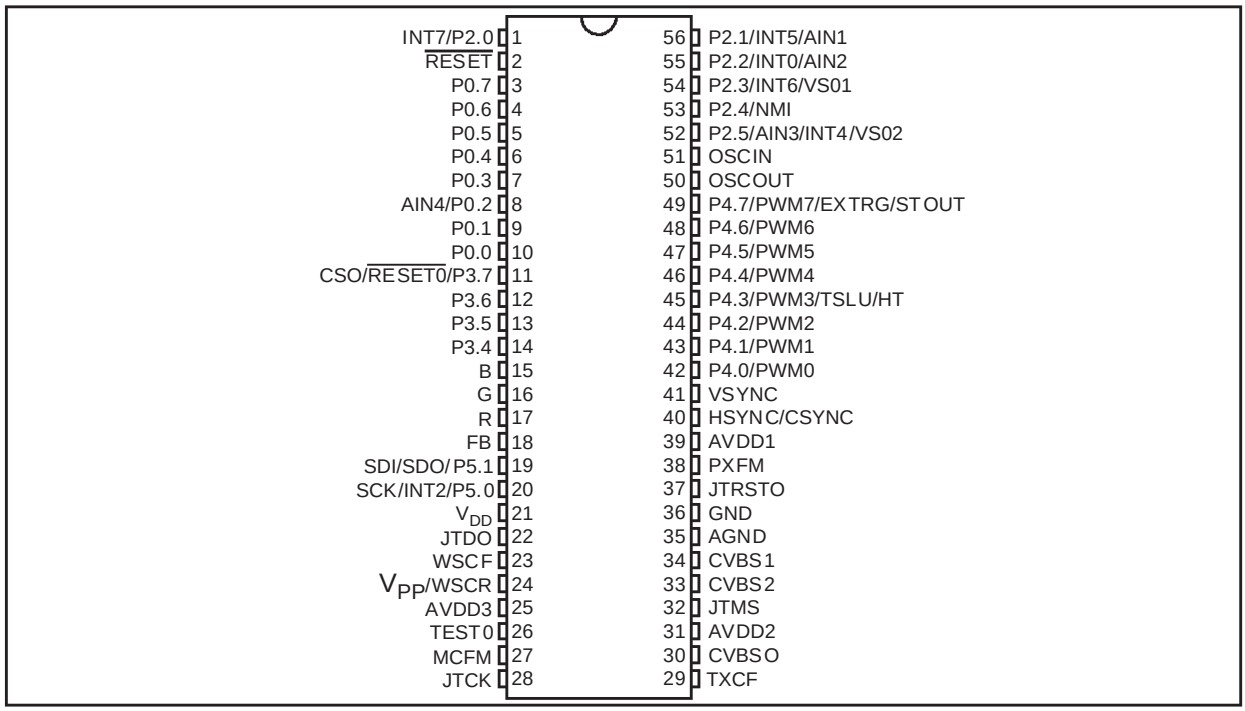
TXCF Analog pin for the Teletext slicer line PLL.

CVBSO, JTDO, JTCK Test pins: leave floating.

TEST0 Test pins: must be tied to AVDD2.

JTRST0 Test pin: must be tied to GND.

Figure 3. 56-Pin Package Pin-Out



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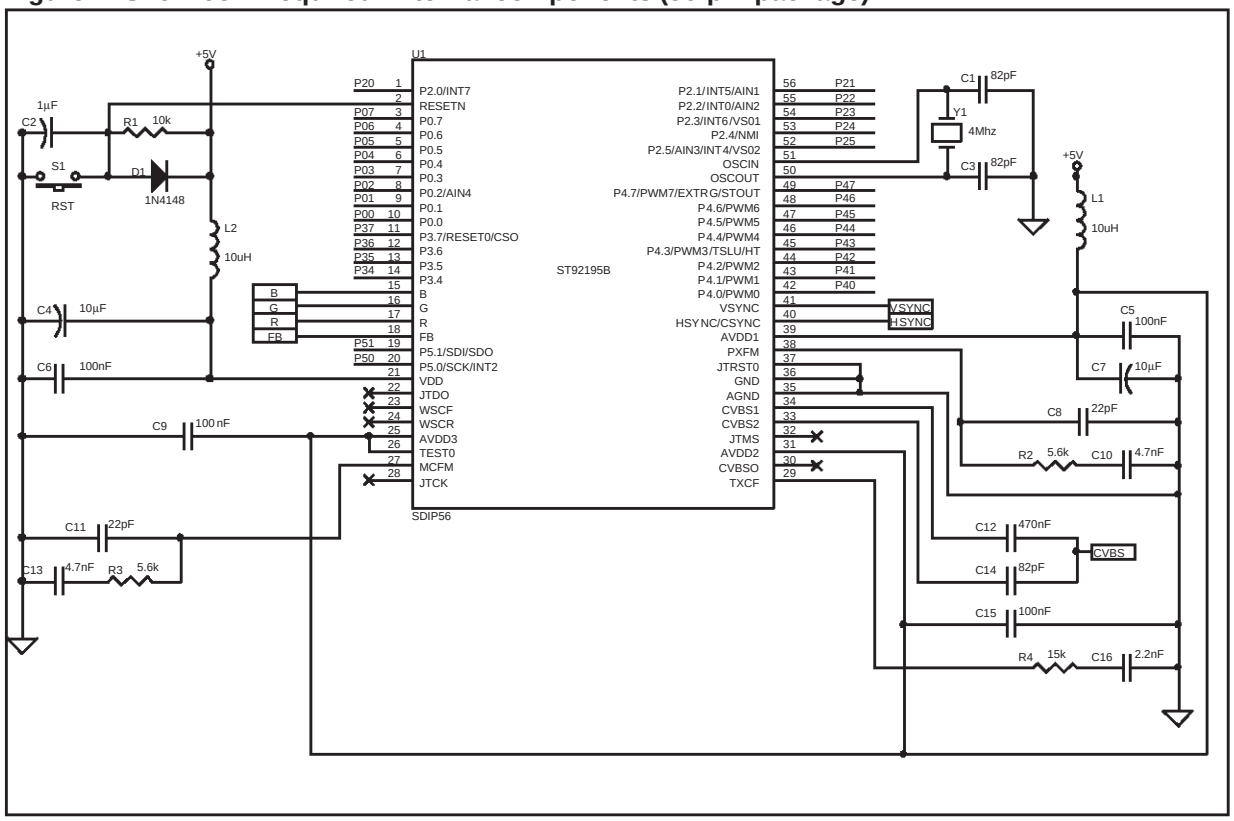
PIN DESCRIPTION (Cont'd)

Figure 4. ST92195B Required External components (56-pin package)



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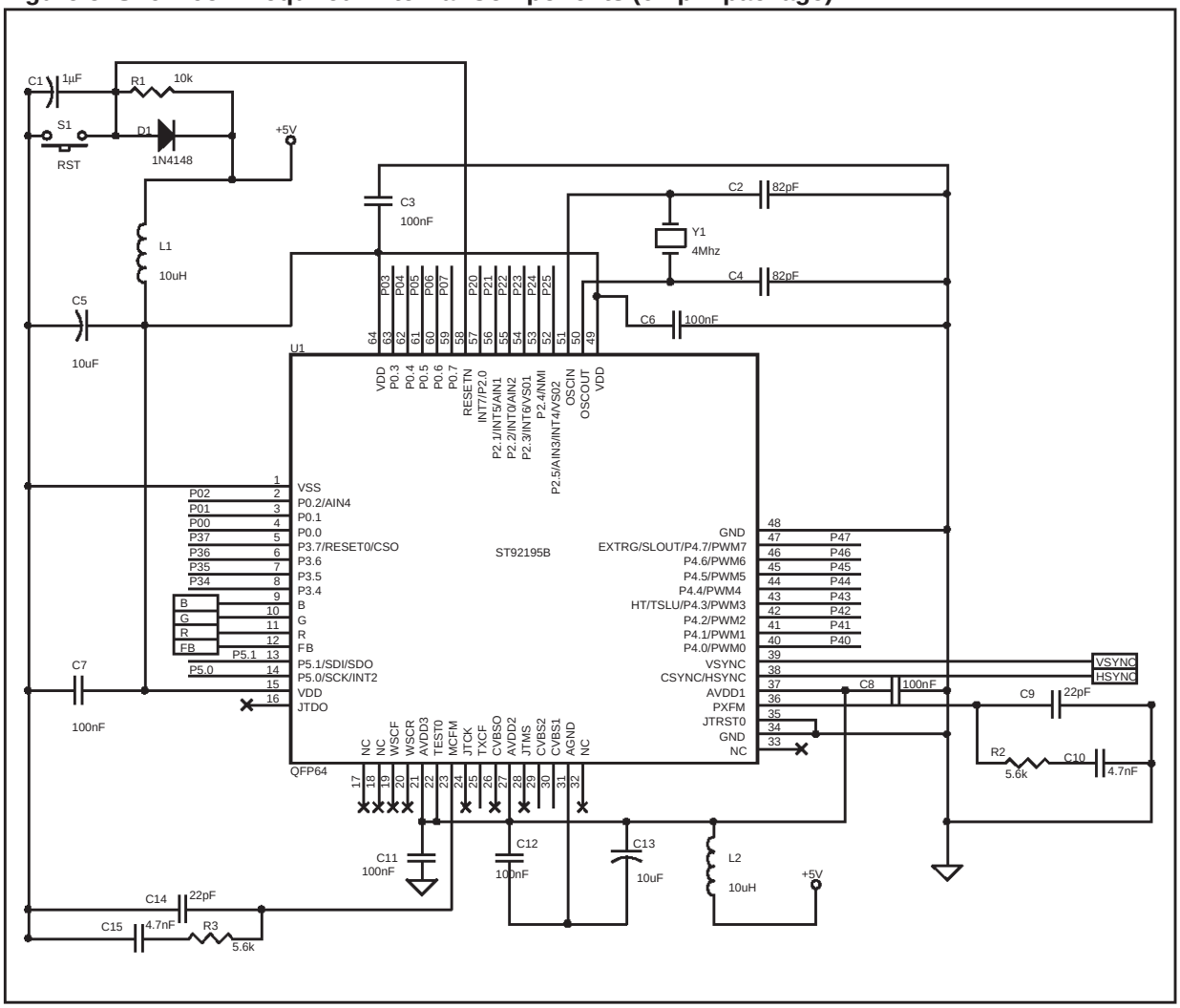
PIN DESCRIPTION (Cont'd)

Figure 5. ST92195B Required External Components (64-pin package)



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PIN DESCRIPTION (Cont'd)

P0[7:0], P2[5:0], P3[7:4], P4[7:0], P5[1:0]
I/O Port Lines (Input/Output, TTL or CMOS compatible).

28 lines grouped into I/O ports, bit programmable as general purpose I/O or as Alternate functions (see I/O section).

Important: Note that open-drain outputs are for logic levels only and are not true open drain.

1.2.1 I/O Port Alternate Functions.

Each pin of the I/O ports of the ST92195B may assume software programmable Alternate Functions (see Table 1).

Table 1. ST92195B I/O Port Alternate Function Summary

Port Name	General Purpose I/O	Pin No.		Alternate Functions		
		TQFP64	SDIP56			
P0.0	All ports useable for general purpose I/O (input, output or bidirectional)	4	10		I/O	
P0.1		3	9		I/O	
P0.2		2	8	AIN4	I	A/D Analog Data Input 4
P0.3		63	7		I/O	
P0.4		62	6		I/O	
P0.5		61	5		I/O	
P0.6		60	4		I/O	
P0.7		59	3		I/O	
P2.0		57	1	INT7	I	External Interrupt 7
P2.1		56	56	AIN1	I	A/D Analog Data Input 1
				INT5	I	External Interrupt 5
P2.2		55	55	INT0	I	External Interrupt 0
				AIN2	I	A/D Analog Data Input 2
P2.3		54	54	INT6	I	External Interrupt 6
				VSO1	O	Voltage Synthesis Output 1
P2.4		53	53	NMI	I	Non Maskable Interrupt Input
P2.5		52	52	AIN3	I	A/D Analog Data Input 3
				INT4	I	External Interrupt 4
				VSO2	O	Voltage Synthesis Output 2
P3.4		8	14		I/O	
P3.5		7	13		I/O	
P3.6		6	12		I/O	
P3.7		5	11	$\overline{\text{RESET0}}$	O	Internal Reset Output
				CSO	O	Composite Sync output
P4.0		40	42	PWM0	O	PWM Output 0
P4.1		41	43	PWM1	O	PWM Output 1
P4.2		42	44	PWM2	O	PWM Output 2
P4.3		43	45	PWM3	O	PWM Output 3
				TSLU	O	Translucency Digital Output
				HT	O	Half-tone Output
P4.4		44	46	PWM4	O	PWM Output 4

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Port Name	General Purpose I/O	Pin No.		Alternate Functions		
		TQFP64	SDIP56			
P4.5	All ports useable for general purpose I/O (input, output or bidirectional)	45	47	PWM5	O	PWM Output 5
P4.6		46	48	PWM6	O	PWM Output 6
P4.7		47	49	EXTRG	I	A/D Converter External Trigger Input
				PWM7	O	PWM Output 7
				STOUT	O	Standard Timer Output
P5.0		14	20	INT2	I	External Interrupt 2
				SCK	O	SPI Serial Clock
P5.1		13	19	SDO	O	SPI Serial Data Out
				SDI	I	SPI Serial Data In

1.2.2 I/O Port Styles

Pins	Weak Pull-Up	Port Style	Reset Values
P0[7:0]	no	Standard I/O	BID / OD / TTL
P2[5,4,3,2]	no	Standard I/O	BID / OD / TTL
P2[1,0]	no	Schmitt trigger	BID / OD / TTL
P3.7	yes	Standard I/O	AF / PP / TTL
P3[6,5,4]	no	Standard I/O	BID / OD / TTL
P4[7:0]	no	Standard I/O	BID / OD / TTL
P5[1:0]	no	Standard I/O	BID / OD / TTL

Legend:

AF= Alternate Function, BID = Bidirectional, OD = Open Drain
PP = Push-Pull, TTL = TTL Standard Input Levels

How to Read this Table

To configure the I/O ports, use the information in this table and the Port Bit Configuration Table in the I/O Ports Chapter of the datasheet.

Port Style= the hardware characteristics fixed for each port line.

Inputs:

– If port style = Standard I/O, either TTL or CMOS input level can be selected by software.

– If port style = Schmitt trigger, selecting CMOS or TTL input by software has no effect, the input will always be Schmitt Trigger.

Weak Pull-Up = This column indicates if a weak pull-up is present or not.

– If WPU = yes, then the WPU can be enabled/disable by software

– If WPU = no, then enabling the WPU by software has no effect

Alternate Functions (AF) = More than one AF cannot be assigned to an external pin at the same time:

An alternate function can be selected as follows.

AF Inputs:

– AF is selected implicitly by enabling the corresponding peripheral. Exception to this are ADC analog inputs which must be explicitly selected as AF by software.

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PIN DESCRIPTION (Cont'd)

AF Outputs or Bidirectional Lines:

– In the case of Outputs or I/Os, AF is selected explicitly by software.

Example 1: ADC trigger digital input

AF: EXTRG, Port: P4.7, Port Style: Standard I/O.

Write the port configuration bits (for TTL level):

P4C2.7=1

P4C1.7=0

P4C0.7=1

Enable the ADC trigger by software as described in the ADC chapter.

Example 2: PWM 0 output

AF: PWM0, Port: P4.0

Write the port configuration bits (for output push-pull):

P4C2.0=0

P4C1.0=1

P4C0.0=1

Example 3: ADC analog input

AF: AIN1, Port : P2.1, Port style: does not apply to analog inputs

Write the port configuration bits:

P2C2.1=1

P2C1.1=1

P2C0.1=1

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1.3 MEMORY MAP

Internal ROM
The ROM memory is mapped in a single continuous area starting at address 0000h in MMU segment 00h.

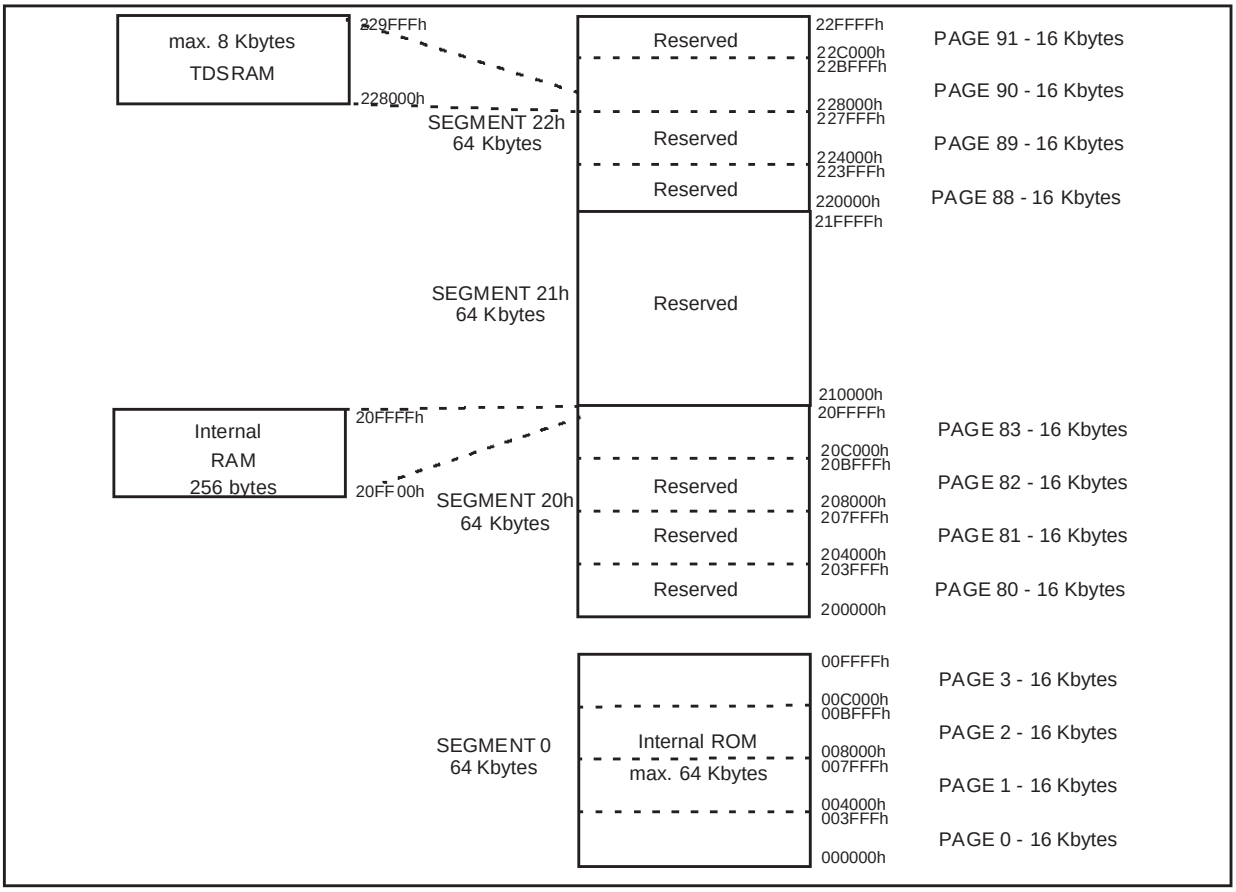
Device	Size	Start Address	End Address
ST92195B1/B2/B3	32K	0000h	7FFFh
ST92195B4/B5	48K	0000h	BFFFh
ST92195B6	56K	0000h	DFFFh
ST92195B7	64K	0000h	FFFFh

Internal RAM, 256 bytes
The internal RAM is mapped in MMU segment 20h; from address FF00h to FFFFh.

Internal TDSRAM
The Internal TDSRAM is mapped starting at address 8000h in MMU segment 22h. It is a fully static memory.

Device	Size	Start Address	End Address
ST92195B1	2K	8000h	87FFh
ST92195B2/B3/B4	6K	8000h	97FFh
ST92195B5/B6/B7	8K	8000h	9FFFh

Figure 6. ST92195B Memory Map



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2 ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	V_{SS} - 0.3 to V_{SS} + 7.0	V
V_{SSA}	Analog Ground	V_{SS} - 0.3 to V_{SS} + 0.3	V
V_{DDA}	Analog Supply Voltage	V_{DD} -0.3 to V_{DD} +0.3	V
V_I	Input Voltage	V_{SS} - 0.3 to V_{DD} +0.3	V
V_{AI}	Analog Input Voltage (A/D Converter)	V_{SS} - 0.3 to V_{DD} +0.3 V_{SSA} - 0.3 to V_{DDA} +0.3	V
V_O	Output Voltage	V_{SS} - 0.3 to V_{DD} + 0.3	V
T_{STG}	Storage Temperature	- 55 to + 150	°C
I_{INJ}	Pin Injected Current Maximum Accumulated Pin Injected Current In Device	- 5 to + 5 - 50 to +5 0	mA mA

Note: Stress above those listed as “Absolute maximum ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value		Unit
		Min.	Max.	
T_A	Operating Temperature	0	70	°C
V_{DD}	Supply Voltage	4.5	5.5	V
V_{DDA}	Analog Supply Voltage (PLL)	4.5	5.5	V
f_{OSCE}	External Oscillator Frequency	3.3	8.7	MHz
f_{OSCI}	Internal Clock Frequency (INTCLK)		24	MHz

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DC ELECTRICAL CHARACTERISTICS

(V_{DD}= 5V +/-10%; T_A= 0 to 70°C; unless otherwise specified)

Symbol	Parameter	Test Conditions	Value		Unit
			Min.	Max.	
V_{IHCK}	Clock In high level	External clock	0.7 V_{DD}		V
V_{ILCK}	Clock in low level	External clock		0.3 V_{DD}	V
V_{IH}	Input high level	TTL	2.0		V
V_{IL}	Input low level	TTL		0.8	V
V_{IH}	Input high level	CMOS	0.8 V_{DD}		V
V_{IL}	Input low level	CMOS		0.2 V_{DD}	V
V_{IHRS}	Reset in high level		0.7 V_{DD}		V
V_{ILRS}	Reset in low level			0.3 V_{DD}	V
V_{HYRS}	Reset in hysteresis		0.3		V
V_{IHY}	P2.(1:0) input hysteresis		0.9		V
V_{IHVH}	HSYNC/VSYNC input high level		0.7 V_{DD}		V
V_{ILVH}	HSYNC/VSYNC input low level			0.3 V_{DD}	V
V_{HYHV}	HSYNC/VSYNC input hysteresis		0.5		V
V_{OH}	Output high level	Push-pull Ild=-0.8mA	V_{DD}-0.8		V
V_{OL}	Output low level	Push-pull Id=+1.6mA		0.4	V
I_{WPU}	Weak pull-up current	bidir. state V_{OL}= 3V V_{OL}= 7V	50	 350	µA
I_{LKIO}	I/O pin input leakage current	$0<V_{IN}<V_{DD}$	-10	+10	µA
I_{LKRS}	Reset pin input	$0<V_{IN}<V_{DD}$	-10	+10	µA
I_{LKAD}	A/D pin input leakage current	alternate funct. op. drain	-10	+10	µA
I_{LKOS}	OSCIN pin input leakage current	$0<V_{IN}<V_{DD}$	-10	+10	µA

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AC ELECTRICAL CHARACTERISTICS

PIN CAPACITANCE

(V_{DD}= 5V +/-10%; T_A= 0 to 70°C; unless otherwise specified))

Symbol	Parameter	Conditions	Value		Unit
			min	max	
C_{IO}	Pin Capacitance Digital Input/Output			10	pF

CURRENT CONSUMPTION

(V_{DD}= 5V +/-10%; T_A= 0 to 70°C; unless otherwise specified)

Symbol	Parameter	Conditions	Value			Unit
			min	typ.	max	
I_{DD1}	Run Mode Current	notes 1,2; all On		70	100	mA
I_{DDA1}	Run Mode Analog Current (pin V_{DDA})	Timing Controller On		35	50	mA
I_{DD2}	HALT Mode Current	notes 1,4		10	100	µA
I_{DDA2}	HALT Mode Analog Current (pin V_{DDA})	notes 1,4		40	100	µA

Notes:

1. Port 0 is configured in push-pull output mode (output is high). Ports 2, 3, 4 and 5 are configured in bi-directional weak pull-up mode resistor. The external CLOCK pin (OSCIN) is driven by a square wave external clock at 8 MHz. The internal clock prescaler is in divide-by-1 mode.
2. The CPU is fed by a 24 MHz frequency issued by the Main Clock Controller. VSYNC is tied to V_{SS}, HSYNC is driven by a 15625Hz clock. All peripherals working including Display.
3. The CPU is fed by a 24 MHz frequency issued by the Main Clock Controller. VSYNC is tied to V_{SS}, HSYNC is driven by a 15625Hz clock. The TDSRAM interface and the Slicers are working; the Display controller is not working.
4. VSYNC and HSYNC tied to V_{SS}. External CLOCK pin (OSCIN) is hold low. All peripherals are disabled.

EXTERNAL INTERRUPT TIMING TABLE (rising or falling edge mode)

(V_{DD}= 5V +/-10%; T_A= 0 to 70°C; unless otherwise specified))

Symbol	Parameter	Conditions	Value		Unit
		INTCLK=24 MHz.	min	max	
T_{wLR}	low level pulse width	TpC+12	95		ns
T_{wHR}	high level pulse width	TpC+12	95		ns

TpC is the INTCLK clock period.

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AC ELECTRICAL CHARACTERISTICS (Cont'd)

SPI TIMING TABLE

(V_{DD}= 5V +/-10%; T_A= 0 to 70°C; Cload= 50pF)

Symbol	Parameter	Condition	Value		Unit
			min	max	
T_{sDI}	Input Data Set-up Time		tbd		ns
T_{hDI}	Input Data Hold Time (1)	OSCIN/2 as internal Clock	1INTCLK	+100ns	ns
T_{dOV}	SCK to Output Data Valid			tbd	ns
T_{hDO}	Output Data Hold Time		tbd		ns
T_{wSKL}	SCK Low Pulse Width		tbd		ns
T_{wSKH}	SCK High Pulse Width		tbd		ns

(1) TpC is the OSCIN clock period; TpMC is the "Main Clock Frequency" period.

SKEW CORRECTOR TIMING TABLE

(V_{DD}= 5V +/-10%, T_A= 0 to 70°C, unless otherwise specified)

Symbol	Parameter	Conditions	max Value	Unit
T_{jskw}	Jitter on RGB output	36 MHz Skew corrector clock frequency	5*	ns

(*) The OSD jitter is measured from leading edge to leading edge of a single character row on consecutive TV lines. The value is an envelope of 100 fields

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AC ELECTRICAL CHARACTERISTICS (Cont'd)

OSD DAC CHARACTERISTICS (ROM DEVICES ONLY)
(V_{DD}= 5V +/-10%, T_A= 0 to 70°C, unless otherwise specified).

Symbol	Parameter	Conditions	Value			Unit
			min	typical	max	
	Output impedance: FB,R,G,B		300	500	700	Ohm
	Output voltage: FB,R,G,B	Cload= 20pF RL = 100K				
	code= 111			1.000	1.250	V
	code= 011			0.450	0.500	V
	code= 000			0.025	0.080	V
	FB= 1		2.4	2.7	3.4	V
	FB= 0		0	0.025	0.080	V
	Global voltage accuracy				+/-5	%

OSD DAC CHARACTERISTICS (EPROM AND OTP DEVICES ONLY)
(V_{DD}= 5V +/-10%, T_A= 0 to 70°C, unless otherwise specified).

Symbol	Parameter	Conditions	Value			Unit
			min	typical	max	
	Output impedance: FB,R,G,B		300	500	700	Ohm
	Output voltage: FB,R,G,B	Cload= 20pF RL = 100K				
	code= 111			1.100	1.400	V
	code= 011			0.600	0.800	V
	code= 000			0.200	0.350	V
	FB= 1		V_{DD}-0.8			V
	FB= 0				0.400	V
	Global voltage accuracy				+/-5	%

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AC ELECTRICAL CHARACTERISTICS (Cont'd)

A/D CONVERTER, EXTERNAL TRIGGER TIMING TABLE

(V_{DD}= 5V +/-10%; T_A= 0 to 70°C; unless otherwise specified

Symbol	Parameter	OSCIN divide by 2;min/max	OSCIN divide by 1; min/max	Value		Unit
				min	max	
T_{low}	Pulse Width			1.5 INTCLK		ns
T_{high}	Pulse Distance					ns
T_{ext}	Period/fast Mode			78+1 INTCLK		µs
T_{str}	Start Conversion Delay			0.5	1.5	INTCLK
Core Clock issued by Timing Controller						
T_{low}	Pulse Width					ns
T_{high}	Pulse Distance					ns
T_{ext}	Period/fast Mode					µs
T_{str}	Start Conversion Delay					ns

A/D CONVERTER. ANALOG PARAMETERS TABLE

(V_{DD}= 5V +/-10%; T_A= 0 to 70°C; unless otherwise specified))

Parameter	Value			Unit	Note
	typ (*)	min	max	(**)	
Analog Input Range		V_{SS}	V_{DD}	V	
Conversion Time Fast/Slow		78/138		INTCLK	(1,2)
Sample Time Fast/Slow		51.5/87.5		INTCLK	(1)
Power-up Time		60		µs	
Resolution	8			bits	
Differential Non Linearity	1.5		2.5	LSBs	(4)
Integral Non Linearity	2		3	LSBs	(4)
Absolute Accuracy	2		3	LSBs	(4)
Input Resistance			1.5	Kohm	(3)
Hold Capacitance			1.92	pF	

Notes: (*) The values are expected at 25 Celsius degrees with V_{DD}= 5V
(**) 'LSBs' , as used here, as a value of V_{DD}/256
(1) @ 24 MHz external clock
(2) including Sample time
(3) it must be considered as the on-chip series resistance before the sampling capacitor
(4) DNL ERROR= max {[V(i) -V(i-1)] / LSB-1} INL ERROR= max {[V(i) -V(0)] / LSB-i}
ABSOLUTE ACCURACY= overall max conversion error

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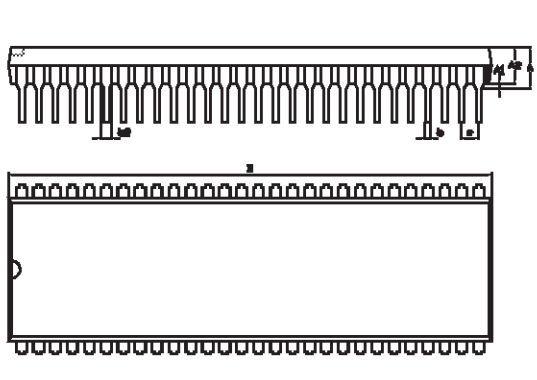
3 GENERAL INFORMATION

3.1 PACKAGE MECHANICAL DATA

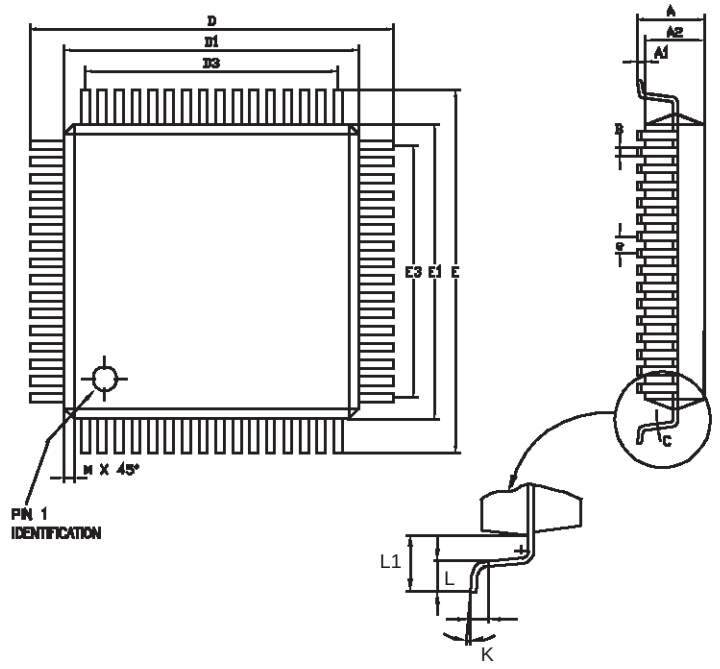
Figure 7. 56-Pin Shrink Plastic Dual In Line Package, 600-mil Width



PDIP56S

Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A			6.35			0.250
A1	0.38			0.015		
A2	3.18		4.95	0.125		0.195
b		0.41			0.016	
b2		0.89			0.035	
C	0.20		0.38	0.008		0.015
D	50.29		53.21	1.980		2.095
E		15.01			0.591	
E1	12.32		14.73	0.485		0.580
e		1.78			0.070	
eA		15.24			0.600	
eB			17.78			0.700
L	2.92		5.08	0.115		0.200
	Number of Pins					
N	56					

Figure 8. 64-Pin Thin Quad Flat Package



Dim	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A			1.60			0.063
A1	0.05		0.15	0.002		0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
B	0.30	0.37	0.45	0.012	0.015	0.018
C	0.09		0.20	0.004		0.008
D		16.00			0.630	
D1		14.00			0.551	
D3		12.00			0.472	
E		16.00			0.630	
E1		14.00			0.551	
E3		12.00			0.472	
e		0.80			0.031	
K	0°	3.5°	7°			
L	0.45	0.60	0.75	0.018	0.024	0.030
L1		1.00			0.039	
	Number of Pins					
N	64		ND	16	NE	16

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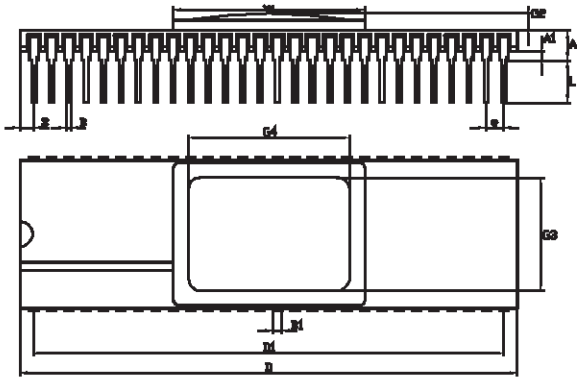
PACKAGE MECHANICAL DATA (Cont'd)

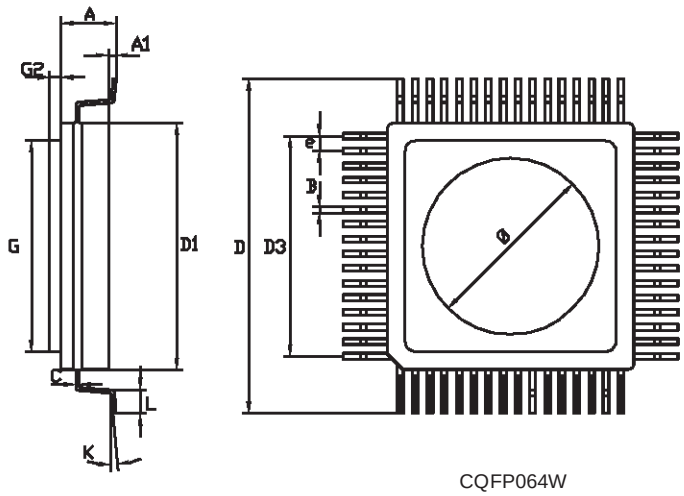
Figure 9. 56-Pin Shrink Ceramic Dual In Line Package, 600-mil Width



CDIP56SW

Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A			4.17			0.164
A1	0.76			0.030		
B	0.38	0.46	0.56	0.015	0.018	0.022
B1	0.76	0.89	1.02	0.030	0.035	0.040
C	0.23	0.25	0.38	0.009	0.010	0.015
D	50.04	50.80	51.56	1.970	2.000	2.030
D1		48.01			1.890	
E1	14.48	14.99	15.49	0.570	0.590	0.610
e		1.78			0.070	
G	14.12	14.38	14.63	0.556	0.566	0.576
G1	18.69	18.95	19.20	0.736	0.746	0.756
G2		1.14			0.045	
G3	11.05	11.30	11.56	0.435	0.445	0.455
G4	15.11	15.37	15.62	0.595	0.605	0.615
L	2.92		5.08	0.115		0.200
S		1.40			0.055	
	Number of Pins					
N	56					

Figure 10. 64-Pin Ceramic Quad Flat Package



CQFP064W

Dim	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A			3.27			0.129
A1		0.50			0.020	
B	0.30	0.35	0.45	0.012	0.014	0.018
C	0.13	0.15	0.23	0.005	0.006	0.009
D	16.65	17.20	17.75	0.656	0.677	0.699
D1	13.57	13.97	14.37	0.534	0.550	0.566
D3		12.00			0.472	
e		0.80			0.031	
G		12.70			0.500	
G2		0.96			0.038	
L	0.35	0.80		0.014	0.031	
θ		8.31			0.327	
	Number of Pins					
N	64					

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3.2 ORDERING INFORMATION

Each device is available for production in a user programmable version (OTP) as well as in factory coded version (ROM). OTP devices are shipped to customer with a default blank content FFh, while ROM factory coded parts contain the code sent by customer. The common EPROM versions for debugging and prototyping features the maximum memory size and peripherals of the family. Care must be taken to only use resources available on the target device.

3.2.1 Transfer Of Customer Code

Customer code is made up of the ROM contents and the list of the selected options (if any). The ROM contents are to be sent on diskette, or by electronic means, with the hexadecimal file generated by the development tool. All unused bytes must be set to FFh.

Figure 11. ROM Factory Coded Device Types

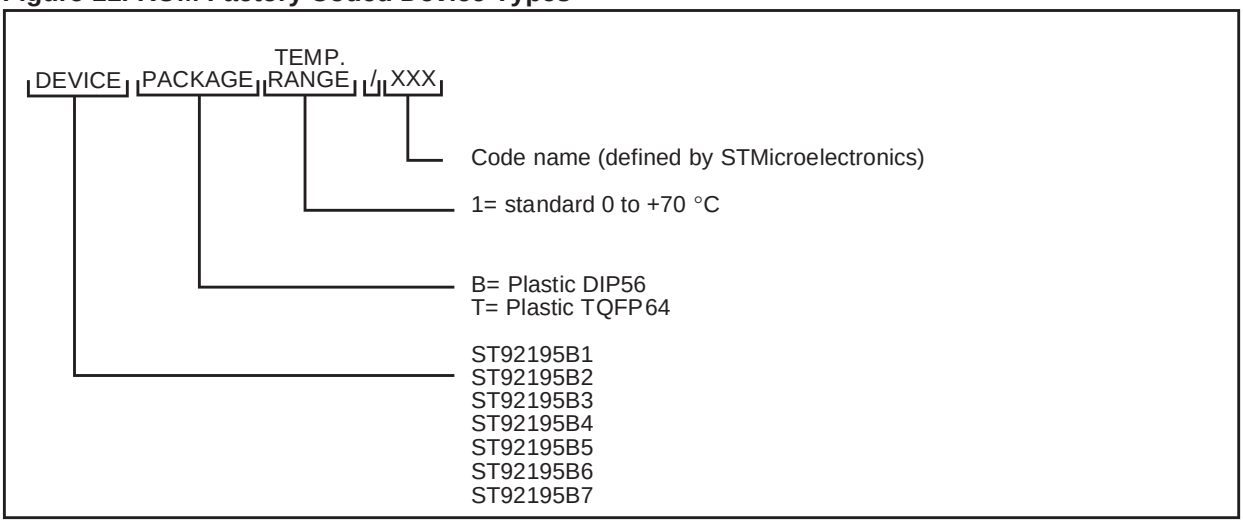


Figure 12. OTP User Programmable Device Types

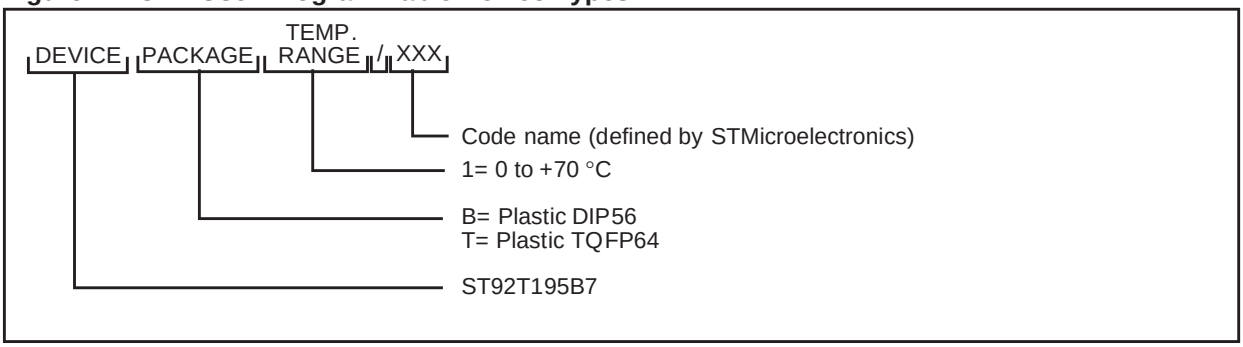
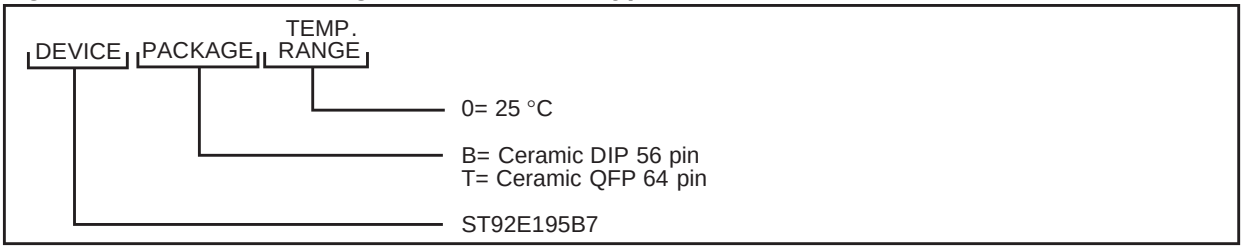


Figure 13. EPROM User Programmable Device Types



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