GBL GigaBit Logic

16G061A
ADVANCE
T-52-07

Dual High Speed Pin Driver
1.5 GHz Operating Frequency

FEATURES

- DC to 1.5 GHz operation
- 600 ps propagation delay (ECL/GaAs)
- 150 ps output rise and fall times (ECL/GaAs)
- 200 ps output rise and fall times for up to 5Vp-p
- Adjustable output edge rate from 150 ps to 2000 ps
- Programmable output voltages up to 5.5 Vp-p over -2.5V to +5.5V range
- 100 mA output current drive capability

- High impedance, three state output control
- High speed ECL/GaAs compatible differential inputs
- On chip VBBS (-1.2V) reference voltage
- Available in C-leaded or leadless chip carriers or in die form. Packages contain internal decoupling capacitors for optimum high frequency performance
- Packaged parts available in 50Ω series terminated or unterminated (Rs=8Ω) configurations

APPLICATIONS

- ATE pin driver
- Switch Driver
- CRT preamplifier
- Laser driver
- Level comparator
- General purpose driver
- Differential Line Receiver
- Precision Pulse Generator

FUNCTIONAL DESCRIPTION

The 16G061A is a dual pin driver designed for use in very high speed GaAs/ECL as well as TTL/CMOS logic test systems. The A and B drivers of the 16G061A are electrically independent and have separate power supplies. Under control of the differential inputs, the output is switched between the levels provided on the VH (V High) and VL (V Low) inputs. The differential inputs can be driven with ECL or GaAs levels. The 16G061A has an on-chip threshold voltage generator (VBBS). When VBBS is connected to the D- inputs, the D+ inputs of the 16G061A can be driven single-ended. The VHigh output level is adjustable from -1.1V to +5.5V and the VLow output level can be adjusted from -2.5V to +1.5V. The output amplitude extends to 5.5Vp-p. Controls are provided (TSA, TSB) to force the outputs into a high impedance, three state condition. External unity gain amplifiers such as the LM324 or higher current operational amplifiers such as the LM759 can be used to buffer the VHigh (VH) and VLow (VL) inputs when driven from DACs.

The 16G061A features a continuously variable Edge Rate Control (ERCA and ERCB) to vary the output rise and fall times. Rise and fall times are typically 150 ps for a 1V peak to peak output (GaAs/ECL) and 200 ps for a 5V peak to peak output when Edge Rate Control (ERC) is biased at VSS. This translates to a slew rate of 6.5V/ns for a 1V output and 25V/ns for a 5V output. Rise and fall times can be increased to 2ns for a 5V peak to peak output by connecting ERC to VEE. This translates to a slew rate of 2.5V/ns for a 5V output. Between -5.1V and -4.8V the Edge Rate Control varies the edge rate at approximately 2 ps/mV for an ECL output swing and 3.5 ps/mV for a TTL output swing. System timing requirements are achieved through a specified 500ps driver propagation delay for ECL/GaAs levels, 600 ps delay for fast edge rate TTL/CMOS levels and 1.5 ns delay for slow edge rate TTL/CMOS levels.

The 16G061A is fabricated using GigaBit's high volume GaAs MESFET processing technology.

BLOCK DIAGRAM
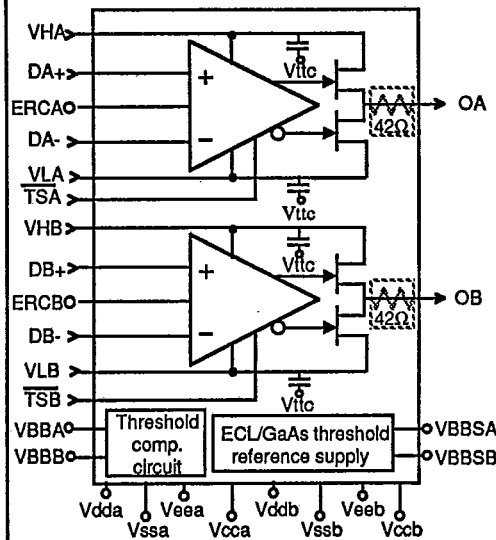
16G061A ORDERING INFORMATION

Package Type	Speed (Min. 25°C)	
	1.5 GHz	
	Unterminated	50Ω Terminated*
C-leaded CC	16G061A-UCE	16G061A-TCE
Leadless CC	16G061A-ULE	16G061A-TLE
Die	16G061A-XE	

*Option T: 42Ω series resistor in the package; Rs=42+8=50Ω

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	ABSOLUTE MAXIMUM RATINGS		
	(Beyond which useful life may be impaired) (Notes 1, 4)		
SYMBOL	**PARAMETER**	**ABSOLUTE MAXIMUM RATINGS**	**NOTES**
TSTOR	Storage Temperature	-65 °C to +150 °C	
TJ	Junction Temperature	-55 °C to +150 °C	
TC	Case Temperature Under Bias	-55 °C to +125 °C	2
VDD	Output Driver Gnd Supply	VSS to +1.0 V	
VSS	Supply Voltage	-4.0 V to +0.5 V	
VEE	Supply Voltage	-7.0 V to VSS +0.5 V	
VCC	Supply Voltage	+0.5 V to +10.0 V	
VIN	Voltage Applied to Any Input; Continuous VSS = -3.4 V, VEE = -5.2 V	-4.0 V to +0.5 V	
I IN	Current Into Any Input; Continuous	-0.5 mA to 1.0 mA	3
VOUT	Voltage Applied to Any Output	VL to VL+7.0 V	5
IOUT	Current From Any Output; Continuous	-150 mA	
PD	Power Dissipation Per Output POUT = (VDDO-VOUT) x IOUT	100 mW	
VBB	Threshold Reference Input Voltage	-4.0V to +0.5V	
IBB	Input current (from interfacing family)	-0.5 mA to +1.0 mA	
VTTC	VH/VL Internal Decoupling Cap. Return	-6.0 V to VL	
VTT	Load Termination Supply	-6.0 V to VDD + 6.0 V	
VH-VL	Output Voltage Amplitude	7V	

Notes:
1. All voltages specified with VDD defined as Gnd. Positive current is defined as current into the device.
2. TC is measured at case top.
3. Subject to IOUT and power dissipation limitations.
4. Power supply sequencing is not necessary, but since the VEE supply is used to bias off the normally-on depletion mode transistors, sustained (>5 secs.) application of VSS in the absence of VEE may result in excessive power dissipation and damage to the device.
5. Voltage applied through a 42Ω series resistor.

	RECOMMENDED OPERATING CONDITIONS (Note 3)					
SYMBOL	**PARAMETER**	**MIN**	**TYP**	**MAX**	**UNITS**	**NOTES**
TC	Case Operating Temperature	25		60	°C	1
VDD	Supply Voltage		Gnd		V	
VCC	Supply Voltage	+3	VH + 2	7.5	V	
VSS	Supply Voltage	-3.5	-3.4	-3.3	V	
VEE	Supply Voltage	-5.5	-5.2	-5.1	V	
VH	High level set voltage	-1.1		5.5	V	
VL	Low level set voltage	-2.5		1.5	V	
VH - VL	Output voltage amplitude	0		5.5	V	2

Notes:
1. Tcase measured at case top.   **User attention to device thermal management is recommended.**
   See GigaBit Application Note 3, "Thermal Management of PicoLogic and NanoRam GaAs Digital IC Families" for a complete discussion of all aspects of device thermal management. Heatsinks are available from GigaBit.
2. For series terminations. For shunt termination: $Voh = VH \times (\frac{Rt}{Rt+Ron})$; $Vol = VL \times (\frac{Rt}{Rt+Ron})$;
   Rt: termination resistance.
3. Max. safe voltage applied to any output through a 42Ω series resistor is limited to VL to VL + 7.0V.

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DC CHARACTERISTICS (DC to 500 MHz - Note 1)

Tc = 25°C to 60°C, Vss = -3.5V to -3.3V, Vee = -5.5V to -5.1V, Vcc = 3.0V (ECL) or 7.0V (TTL), Vdd = Gnd

Symbol	Parameter	Min	Typ	Max	Units	Test Conditions	Notes
Vih	Input voltage high	-1.0		Vdd	V		
Vil	Input voltage low	Vss		-1.6	V		
Vcm	Common mode Vin	-1.9	VBB	-0.5	V		
Iin	Input current	-500		500	µA	Vin = -0.5V to -1.9V	
Vbbs	Threshold Ref. voltage (ECL/GaAs)	-1.05	-1.2	-1.4	V		3
Voh	Output voltage high	VH -.02	VH	VH	V	No DC load, VH-VL≤5.5V	
Vol	Output voltage low	VL	VL	VL +.02	V	No DC load, VH-VL≤5.5V	
Ioh	Output drive current		±100		mA		2
Ron	Driver FET on rest.	6.5	8	9.5	Ω	At Voh, Vol	
Voffset	Input Offset Voltage		50		mV		
ICC	Supply Current		120		mA		
IEE	Supply Current		140		mA		
ISS	Supply Current		65		mA		
PdE	Power Dissipation		1.2		W	VCC = 2.0V (ECL)	4
PdT	Power Dissipation		1.8		W	VCC = 7.0V (TTL)	4
Izl	Three state output leakage		±40		µA	@40°C	5

Notes:
1. Test conditions unless otherwise indicated: -D input = -1.30V.
2. Test Conditions: VH - Vout ≥ 1V; VL - Vout ≤ -1.0V.
3. Source impedance = 40Ω nominally. ΔVBBS/ΔTemp. = +0.6mV/°C; ΔVBBS/ΔVSS = +0.2mV/mV.
4. Measured at nominal supply voltages, 50% output duty cycle and both drivers powered.
5. Voh=2.7V, Vol=0.4V

AC CHARACTERISTICS (Note 1, 2)

Tc = 25°C to 60°C, Vss = -3.5V to -3.3V, Vee = -5.5V to -5.1V, Vcc = 2.0V (ECL) or 7.0V (TTL), Vdd = Gnd

Symbol	Parameter	ECL/GaAs Output Levels			TTL Output Levels			Units	Test Cond.	Notes
		Min	Typ	Max	Min	Typ	Max			
F	Operating frequency	1000	1500		300	500		MHz	ERC = VSS	
td	Propagation delay		600			700		ps	ERC = VEE	
tds	Prop. delay, slow edge rates		1500			1500		ps	ERC = VSS	
td3	3-state delay		750			850		ps	ERC = VEE	
td3s	3-state delay, slow edge rates		1500			1500		ps	ERC = VSS	
Δtdm	Prop. Delay match; H-L, L-H		50	100		50	100	ps	ERC = VEE	
Δtdms	ΔProp. Delay match, slow mode		300			300		ps	ERC = VSS	
Δtd/Δdc	Δ Prop. delay with duty cycle		±100			±100		ps	or VEE	
Δtd/ΔT	Prop. delay temp. coeff.		±1.0			±1.0		ps/°C		
T	Output slew rate		7			25		V/ns	ERC = VSS	3
Tr,f	Output rise and fall times		150			200		ps	ERC = VEE	
Ts	Slow Output slew rate		0.7			2.5		V/ns	ERC = VEE	3
Tsr,sf	Slow Output rise and fall times		1500			2000		ps		
Tset	Settling time to 0.05 (Voh - Vol)		0.2	1.0		0.2	1.0	ns		
W	Output crosstalk		.05(Voh-Vol)			.05(Voh-Vol)		V	@ 100MHz	

Notes:
1. VBB = -1.3V, Vih = -1.0V, Vil = -1.6V.
2. ECL Vp-p output = 1.0V; TTL Vp-p output = 5.0V.
3. Output rise and fall times are measured at 10% and 90% points.

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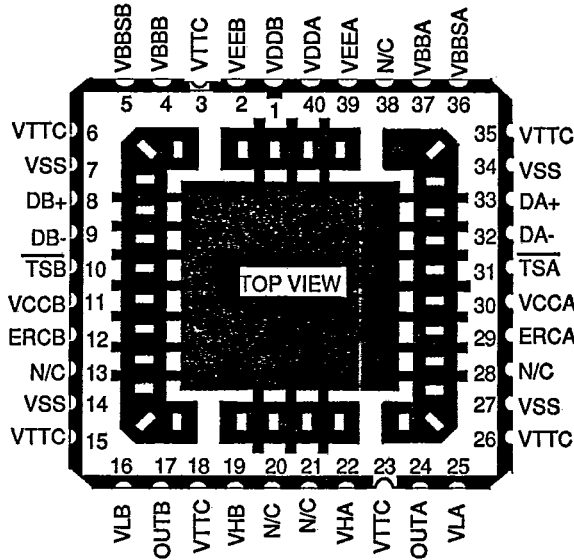
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PIN DESCRIPTIONS

DA+, DA-	Differential data inputs A.
DB+, DB-	Differential data inputs B.
OA, OB	Output A, Output B.
VLA, VLB	Output Low level set voltages.
VHA, VHB	Output High level set voltages.
TSA, TSB	Three-State output controls. Output, OA or OB, is forced into a high impendance condition when TSA or TSB respectively is low.
ERCA, ERCB	Edge Rate Controls. Output Edge rates are continuously slowed when ERC is moved from VSS to VEE. Fast edge rates are obtained when ERC is tied to VSS. Slow edge rates are obtained when ERC is tied to VEE.
VDDA, VDDB	Ground Pins (0V).
VSS	- 3.4V power supplies.
VEEA, VEEB	- 5.2V power supplies.
VCCA, VCCB	Positive power supplies. Nominally VH + 2V.

VTTC	AC return pin for the package-internal decoupling capacitors tied to VH (VHigh) and VL (VLow) pins. For proper decoupling, VTTC should be tied to a voltage no more positive than VLow. When driving TTL/CMOS levels, VTTC = DUT ground is appropriate. When driving ECL/GaAs levels, VTTC should be connected to the DUT output termination voltage (DUT VTT). Connecting VTTC to the termination voltage associated with the16G061A input signal may couple noise to the output.
VBBA, VBBB	Reference input to the 10G061A's input threshold compensation circuit. Connect to the VBB supplied from ECL when driving from ECL. Otherwise connect to corresponding VBBS pin.
VBBSA, VBBSB	Picologic Threshold reference output voltage. Connect to VBB when driving from PicoLogic Δ VBBS/Δ Temp = 0.6mV/°C, Δ VBBS/ΔVSS = 0.2 mV/mV.

Pin Function Drawing
Package Types "L" and "C"

24 PIN HYBRID PACKAGE
Type H

Tolerances: ±0.005
All dimension in inches

R. 0.015 Max.
0.040 Typ.   Section A-A   0.010
                    See Detail B

0.040 DIA.
0.160   0.050
Detail B
0.020 ± 0.002
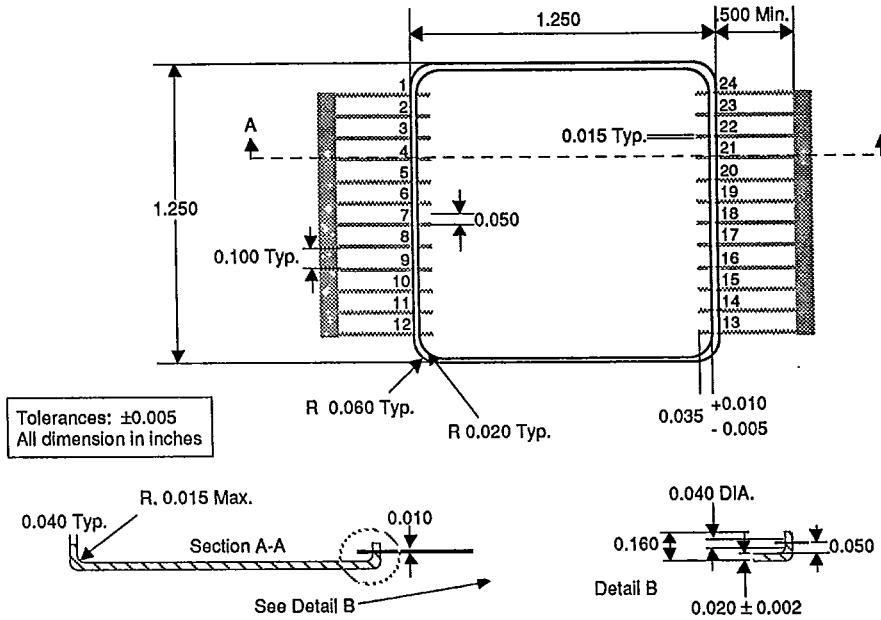
18 PIN LEADLESS CHIP CARRIER
TYPE L1
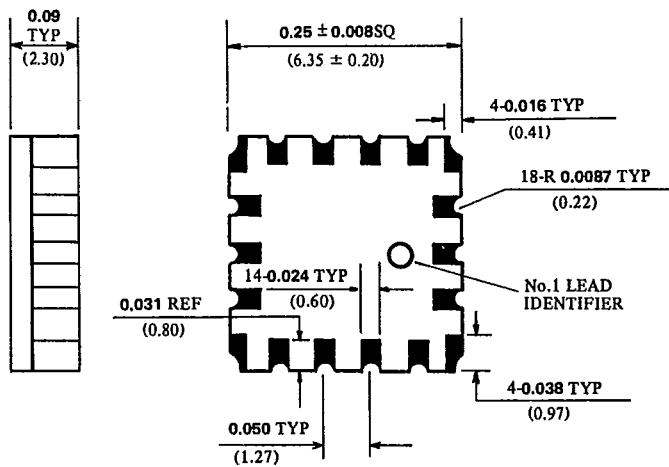
All dimensions shown in **inches** and (millimeters)

11-4

GBL GigaBit Logic · **36 PIN PACKAGES**

36 PIN LEADLESS CHIP CARRIER
TYPE L36
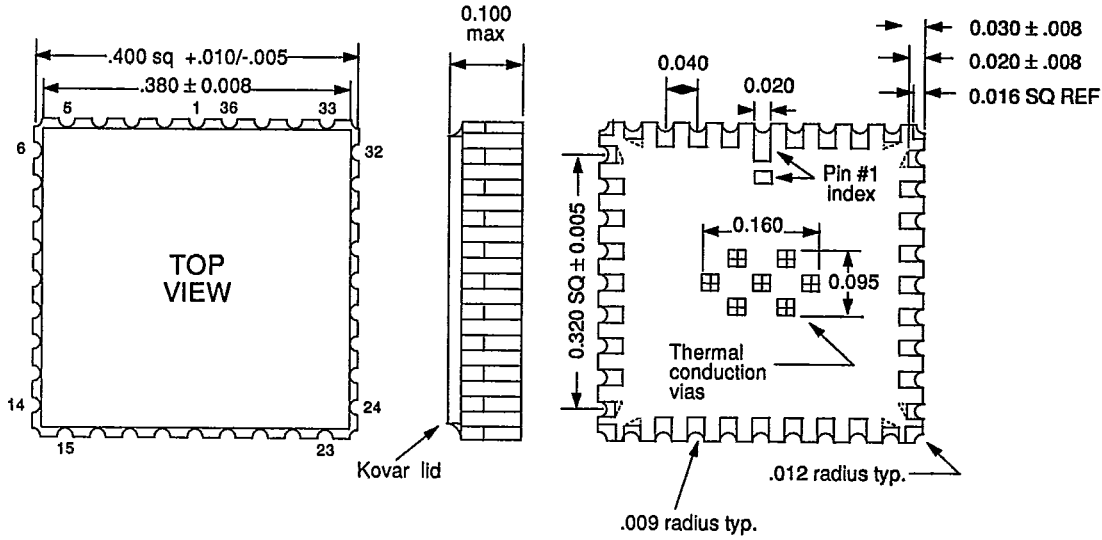
NOTES:
1) The package bottom thermal vias, top lid surface and 4 metallized corner castellations (when present) are all at Vss potential.
2) All dimensions in inches.
3) Pin #1 identifier may be an elongated pad or small, square gray marker.

36 I/O LEAD FLATPACK
TYPE F

GBL GigaBit Logic   **40 PIN PACKAGES**

40 PIN LEADLESS CHIP CARRIER
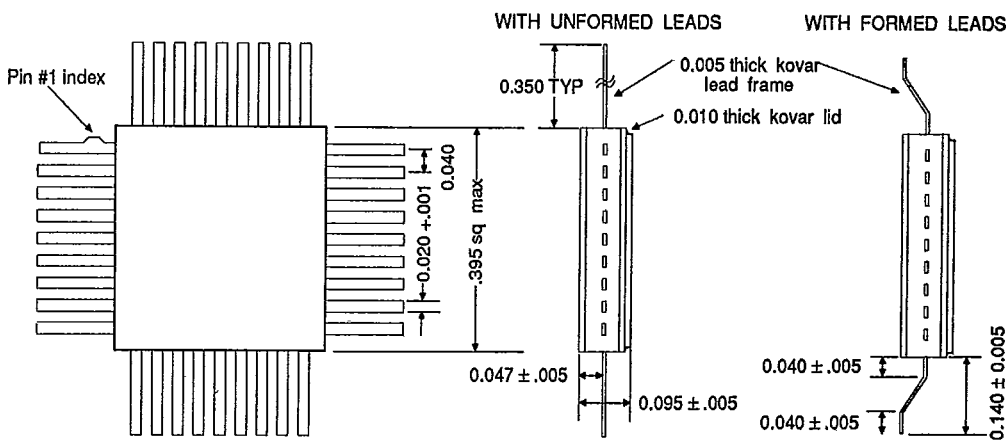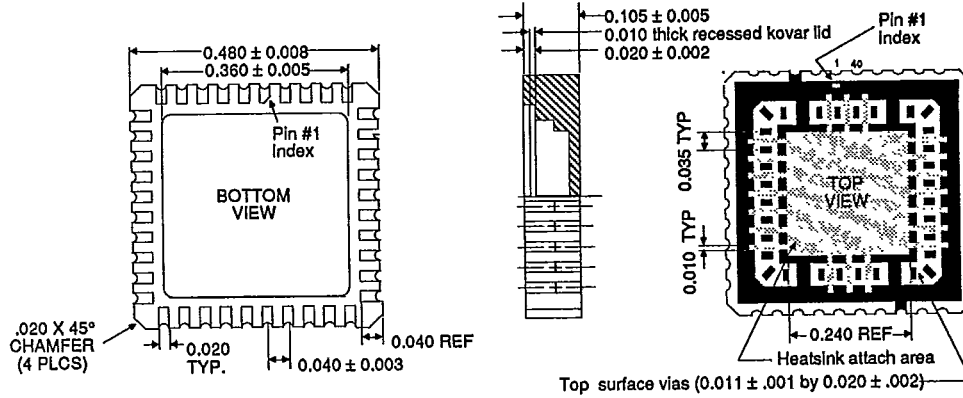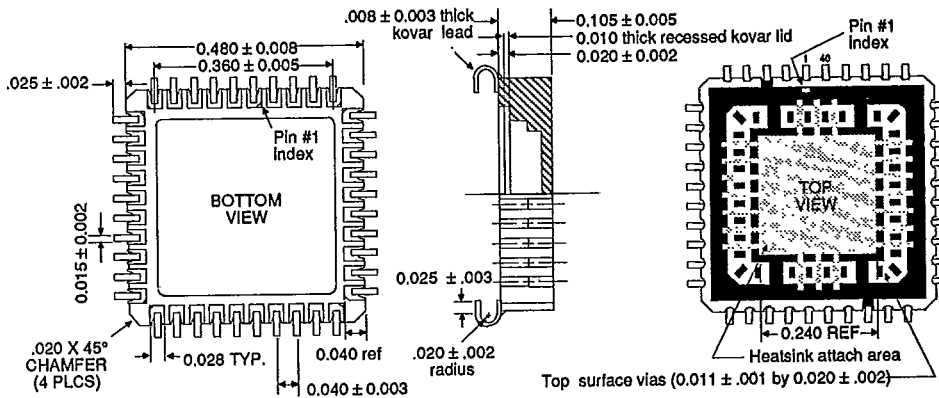### TYPE L

0.105 ± 0.005
0.010 thick recessed kovar lid
0.020 ± 0.002

Pin #1 Index

0.480 ± 0.008
0.360 ± 0.005

Pin #1 Index

BOTTOM VIEW

0.035 TYP

0.010 TYP

TOP VIEW

.020 X 45° CHAMFER (4 PLCS)

0.020 TYP.

0.040 ± 0.003

0.040 REF

0.240 REF

Heatsink attach area

Top surface vias (0.011 ± .001 by 0.020 ± .002)

40 PIN LEADED CHIP CARRIER
TYPE C

.008 ± 0.003 thick kovar lead

0.105 ± 0.005
0.010 thick recessed kovar lid
0.020 ± 0.002

Pin #1 Index

0.480 ± 0.008
0.360 ± 0.005

.025 ± .002

Pin #1 Index

BOTTOM VIEW

0.015 ± 0.002

TOP VIEW

0.025 ± .003

.020 X 45° CHAMFER (4 PLCS)

0.028 TYP.

0.040 ref

.020 ± .002 radius

0.040 ± 0.003

0.240 REF

Heatsink attach area

Top surface vias (0.011 ± .001 by 0.020 ± .002)

NOTES:
(1) Footprint is JEDEC standard outline.
(2) Top surface vias (for terminating resistors and decoupling capacitors) are not available on pins 3,4,17, 18, 23,24,37 and 38.
(3) Top surface metal (not including vias) and pins 3 and 23 are fixed at VTT potential.
(4) Recommended top surface chip resistors are 0.040 long by 0.020 wide by 0.010 thick typ, 100 mw min. nominal power rating (Mini-Systems MSR-21 or equivalent.)
(5) Recommended top surface chip capacitors are 0.040 long by 0.030 wide by 0.020 thick typ, 25V VDCW, 1000 pf, min. (Johanson R09 case or equivalent).
(6) Recommended heatsinks are GBL P/Ns 90GHS-40-A and 90GHS-40-B.
(7) Thermally conductive, electrically non-conductive epoxy is recommended for heatsink attachment (Ablestick 789-4 or 561K, or Thermalloy Thermalbond™ or equivalent.)
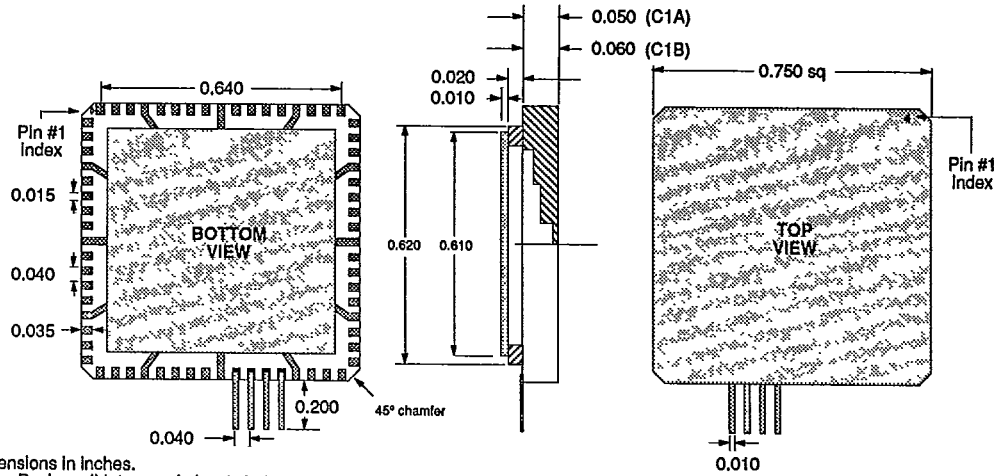(8) L40 and C40 packages are dimensionally identical except for contact finger width.

TOP SURFACE LEGEND:

Metalized Ceramic...... ■

Screened Dielectric..... ▨

Bare Ceramic............. ☐

Top Surface Terminating/Decoupling Detail

SCREENED DIELECTRIC TO ACT AS SOLDER DAM AND PROVIDE ISOLATION FROM GROUND PLANE

INPUT SIGNAL OR POWER SUPPLY VIA

50Ω TERMINATING RESISTOR OR DECOUPLING CAP

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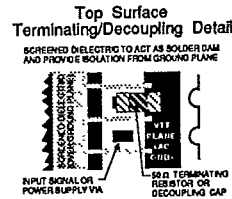
68 PIN LEADED CHIP CARRIER
TYPE C1

(1) All dimensions in inches.
(2) a. C1A: Package lid, top, and pins 4, 9, 14, 21, 26, 31, 38, 43, 48, 55, 60, 65 are at common potential (system ground).
b. C1B: Package lid and pins 4, 9, 14, 21, 26, 31, 38, 43, 48, 55, 60, 65 are at common potential (system ground).

132 PIN LEADED CHIP CARRIER
TYPE C3

□ Power Pins (8)
■ Ground Pins (28)
▨ Signal pins (96)

All dimensions in inches

11