LITEON

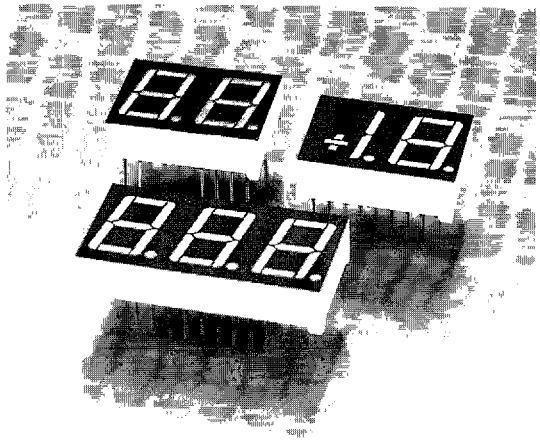
LTM- 8522 8529 8530 SERIES

T-41-37

0.56 INCH 7-SEGMENT NUMERIC DISPLAY WITH MOS I.C. DRIVER

FEATURES

- 0.56 INCH (14.22mm) DIGIT HEIGHT.
- WIDE SUPPLY VOLTAGE OPERATION.
- SERIAL DATA INPUT.
- CONSTANT CURRENT DRIVERS.
- CONTINUOUS BRIGHTNESS CONTROL.
- SOLID STATE RELIABILITY-LONG OPERATION LIFE.
- WIDE VIEWING ANGLE.
- CHOICE OF SIX BRIGHT COLORS-RED/BRIGHT RED / GREEN / YELLOW / ORANGE / HIGH EFFICIENCY RED.



DESCRIPTION

The LTM-8522/8529/8530 series are 0.56 inch (14.22mm) height numeric display modules, and a built-in M5450 MOS integrated circuits. The integrated circuit contains series data input, 35 bit shift register, 34 LED driver output and brightness control.

The red devices utilized LED chips which are made from GaAsP on a GaAs substrate. The bright red and green devices utilized LED chips which are made from GaP on a transparent GaP substrate. The orange and high efficiency red devices utilized LED chips which are made from GaAsP on a transparent GaP substarate. The MOS integrated circuits produced with N-channel silicon gate technology.

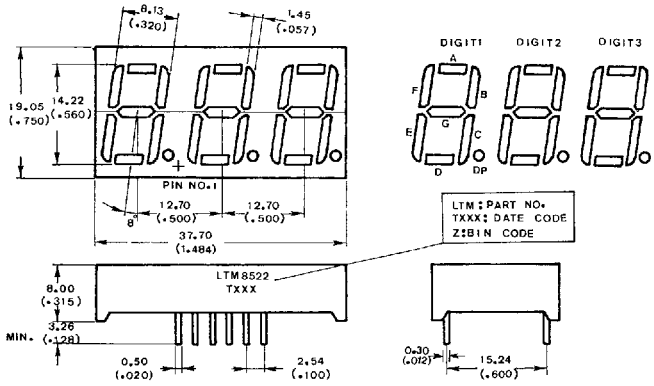
Red and bright red displays have black face and red segment color. Green and yellow displays have gray face and white segment color. Orange displays have orange face and orange segment color. High efficiency red displays have red face and red segment color.

DEVICES

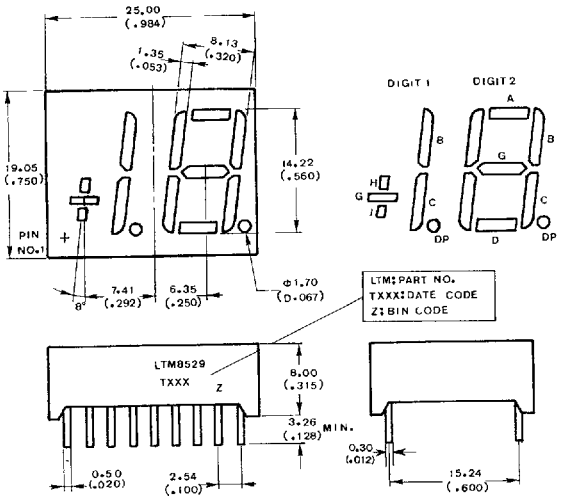
PART NO. LTM–						DESCRIPTION	PACKAGE DIMEN-SION
RED	BRIGHT RED	GREEN	YELLOW	ORANGE	HI.-EFF. RED		
8522R	8522P	8522G	8522Y	8522E	8522HR	3 Digit, Rt Hand Decimal	A
8529R	8529P	8529G	8529Y	8529E	8529HR	1½ Digit, Rt. Hand Decimal	B
8530R	8530P	8530G	8530Y	8530E	8530HR	2 Digit, Rt. Hand Decimal	C

PACKAGE DIMENSIONS

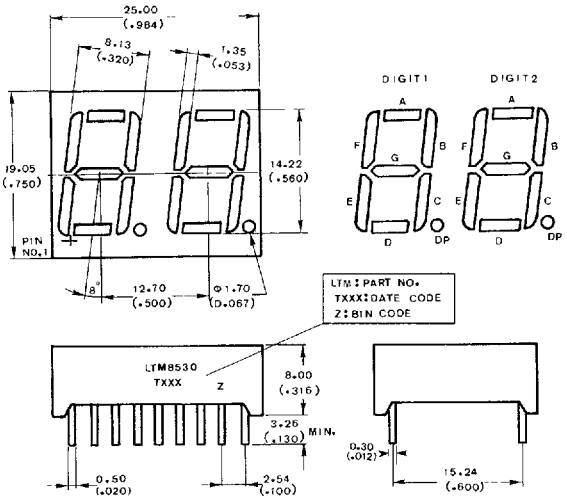
A. LTM-8522



B. LTM-8529



C. LTM-8530



NOTE: All dimensions are in $\frac{\text{millimeters}}{(\text{inches})}$ tolerance are:

1. Lead length (from seating plane) minimum value $\frac{+1.00}{-0.00}$ mm $\left(\frac{+0.040''}{-0.000''}\right)$
2. $\frac{\pm 0.25\text{mm}}{(0.010'')}$ unless otherwise noted.

PIN CONNECTION

PIN NO.	CONNECTION		
	LTM-8522	LTM-8529	LTM-8530
1	V_{SS}	V_{SS}	V_{SS}
2	VLED	VLED	VLED
3	VLED	NO PIN	NO PIN
4	Bit 25 Output	NO PIN	NO PIN
5	Bit 25 Output	NO PIN	NO PIN
6	Bit 27 Output	Bit 15 Output	Bit 17 Output
7	Bit 28 Output	Bit 16 Output	Bit 18 Output
8	Bit 29 Output	Bit 17 Output	Bit 19 Output
9	Bit 30 Output	Bit 18 Output	Bit 20 Output
10	Bit 31 Output	Bit 19 Output	Bit 21 Output
11	Bit 32 Output	Bit 20 Output	Bit 22 Output
12	Bit 33 Output	Bit 21 Output	Bit 23 Output
13	Bit 34 Output	Bit 22 Output	Bit 24 Output
14	Data Enable	Data Enable	Data Enable
15	Data Input	Data Input	Data Input
16	Clock Input	Clock Input	Clock Input
17	VDD	VDD	VDD
18	BRT. Control	BRT. Control	BRT. Control

ABSOLUTE MAXIMUM RATING AT $T_A = 25°C$

PARAMETER	SYMBOL	MIN.	MAX.	UNITS
Supply Voltage *1	V_{DD}	−0.3	15	V
Input Voltage	VI	−0.3	15	V
Off State Output Voltage	Vo (off)		15	V
LED Supply Voltage	V_{LED}	2.8	3.5	V
Power Dissipation of IC *2	PD (IC)		350	mW
Supply Current	I_{DD}		7	mA
Operating Temperature Range	Top	−20	+60	°C
Storage Temperature Range	Tstg	−20	+60	°C
Solder Temperature 1/16 inch Below Seating Plane for 3 Seconds at 260°C				

NOTES: 1. All voltages are with respect to V_{SS} (GND)

2. Power dissipation of IC is given by $P_D = (V_{LED} - V_F) \bullet (I_F) \bullet (\text{No. of Segment} + (7mA) \cdot V_{DD})$
*VF is LED forward voltage.

RECOMMENDED OPERATING CONDITION AT $T_A = 25°C$

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITION
Supply Voltage	V_{DD}	4.75		13.2	V	
Input Voltage						
Logical "0" Level		−0.3		0.8	V	± 10μA Input Bias
Logical "1" Level	V_I	2.2		V_{DD}	V	$4.75V < V_{DD} < 5.25V$
Logical "1" Level		V_{DD} -2		V_{DD}	V	$V_{DD} > 5.25V$
Brightness Input Current	I_B	0		0.75	mA	
Brightness Input Voltage	V_B	3		4.3	V	Input Current = 750μA
Off State Voltage	Vo (off)			13.2	V	
Output Sink Current						
Segment Off				10	μA	$I_B = 0$ μA
Segment On			3		mA	$I_B = 100$ μA
			6		mA	$I_B = 200$ μA
Input Clock Frequency	F_{CLOCK}	0		0.5	MHZ	
Output Matching	Io			±20	%	

ELECTRICAL/OPTICAL CHARACTERISTICS AT $T_A = 25°C$
LTM-8522R/8529R/8530R

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITION
Average Luminous Intensity	Iv	200	500		μcd	$I_B = 0.4$mA
Peak Emission Wavelength	λp		655		nm	$I_B = 0.4$ mA
Spectral Line Half-Width	Δλ		24		nm	$I_B = 0.4$ mA
Luminous Intensity Matching Ratio	Iv-m			2:1		$I_B = 0.4$ mA

LTM-8522P/8529P/8530P

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITION
Average Luminous Intensity	Iv	300	700		μcd	$I_B = 0.4$mA
Peak Emission Wavelength	λp		700		nm	$I_B = 0.4$ mA
Spectral Line Half-Width	Δλ		90		nm	$I_B = 0.4$ mA
Luminous Intensity Matching Ratio	Iv-m			2:1		$I_B = 0.4$ mA

LTM-8522G/8529G/8530G

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITION
Average Luminous Intensity	Iv	800	2000		μcd	I_B = 0.4 mA
Peak Emission Wavelength	λp		565		nm	I_B = 0.4 mA
Spectral Line Half-Width	Δλ		30		nm	I_B = 0.4 mA
Luminous Intensity Matching Ratio	Iv-m			2:1		I_B = 0.4 mA

LTM-8522Y/8529Y/8530Y

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITION
Average Luminous Intensity	Iv	700	1700		μcd	I_B = 0.4 mA
Peak Emission Wavelength	λp		585		nm	I_B = 0.4 mA
Spectral Line Half-Width	Δλ		35		nm	I_B = 0.4 mA
Luminous Intensity Matching Ratio	Iv-m			2:1		I_B = 0.4 mA

LTM-8522E/8529E/8530E

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITION
Average Luminous Intensity	Iv	800	2000		μcd	I_B = 0.4 mA
Peak Emission Wavelength	λp		630		nm	I_B = 0.4 mA
Spectral Line Half-Width	Δλ		40		nm	I_B = 0.4 mA
Luminous Intensity Matching Ratio	Iv-m			2:1		I_B = 0.4 mA

LTM-8522HR/8529HR/8530HR

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITION
Average Luminous Intensity	Iv	800	2000		μcd	I_B = 0.4 mA
Peak Emission Wavelength	λp		635		nm	I_B = 0.4 mA
Spectral Line Half-Width	Δλ		40		nm	I_B = 0.4 mA
Luminous Intensity Matching Ratio	Iv-m			2:1		I_B = 0.4 mA

FUNCTION DESCRIPTION

Series data transfer from the data source to the display driver is accomplished with 2 signals serial data and clock. Using a format of a leading "1" following by the 35 data bits allows data transfer without an additional load signal. The 35 data bits are latched after the 36th bit is complet, thus providing nonmultiplexed, direct drive to the display. Outputs change only if the serial data bits differ from the previous time.

Brightness of display is determined by control the output current of LED display. A InF capacitor shouled be connected to brightness control, Pin 18 to prevent possible oscillations. The output current is typically 25 times greater than the current into Pin 18 which is set by an external variable resistor. There is an internal limiting resistor of 400Ω nominal value. Figure 2 shows the input data format. A start bit of logical "1" preceed the 35 bits of data. At the 36th clock, a LOAD signal is generated synchronously with the high state of the clock, which loads the 35 bits of the shift registers into the latches. At the low state of the clock a RESET signal is generaled which clears all the shift registers for the next set of data. The shift registers are static master-slave configuration. There is no clear for master portion of the first register, thus allowing contionous operation.

There must be a complete set of 36 clocks or the shift registers won't clear. When power is first applied to the chip an internal power ON reset signal is generated which reset all registers and all latches. The START bit and first clock return the chip on its normal operation. Bit 1 is the first following the start bit and it will appear on the segment A of the digit 1. A logical "1" at the input will turn on the appropriate LED. Figure 3 shows the timing relationship between data, clock, and DATA ENABLE. A max. clock frequency of 0.5 MHz is assumed.

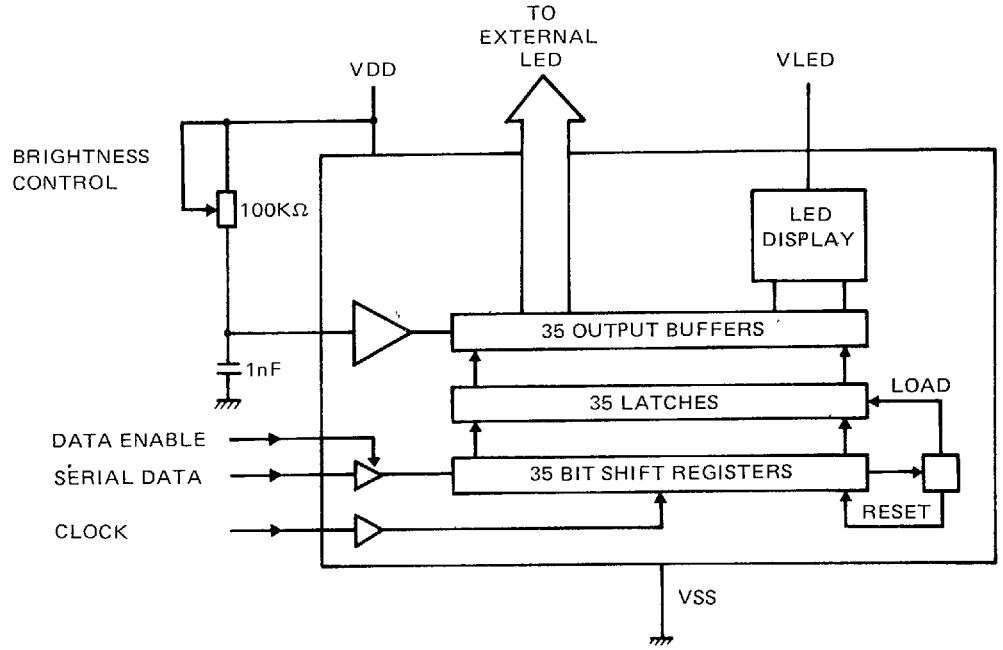


FIGURE 1. Internal Block Diagram

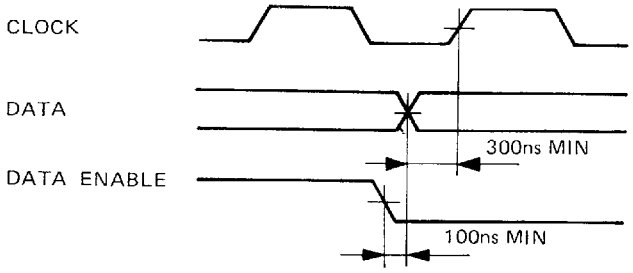


FIGURE 2. Input Data Format

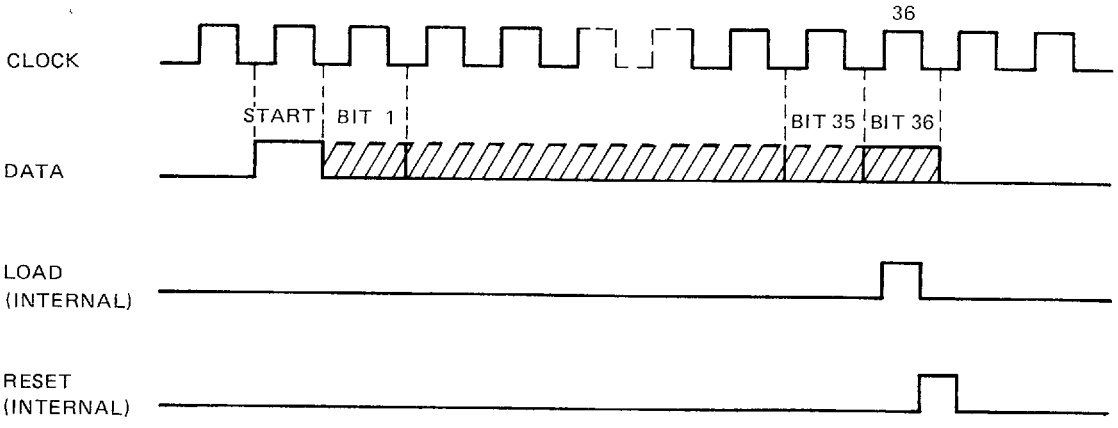


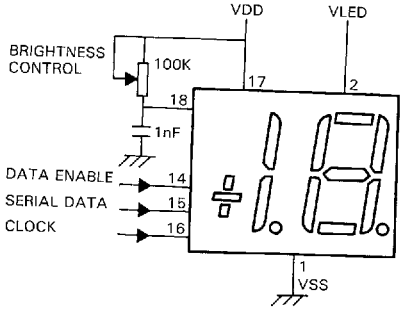
FIGURE 3. Timing Relationship.

TABLE I SERIAL DAT INPUT SEQUENCE

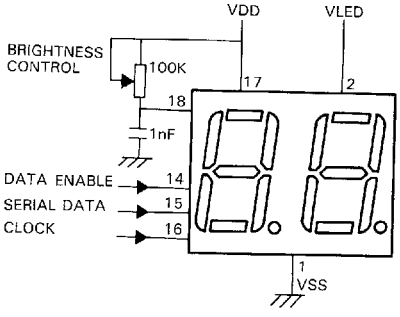
BIT	LTM-8522		LTM-8529		LTM-8530	
	DIGIT	SEGMENT	DIGIT	SEGMENT	DIGIT	SEGMENT
1	1	A	1	B	1	A
2	1	B	1	C	1	B
3	1	C	1	G	1	C
4	1	D	1	H	1	D
5	1	E	1	J	1	E
6	1	F	1	D.P.	1	F
7	1	G	2	A	1	G
8	1	D.P.	2	B	1	D.P.
9	2	A	2	C	2	A
10	2	B	2	D	2	B
11	2	C	2	E	2	C
12	2	D	2	F	2	D
13	2	E	2	G	2	E
14	2	F	2	D.P.	2	F
15	2	G		PIN 6	2	G
16	2	D.P.		PIN 7	2	D.P.
17	3	A		PIN 8		PIN 6
18	3	B		PIN 9		PIN 7
19	3	C		PIN 10		PIN 8
20	3	D		PIN 11		PIN 9
21	3	E		PIN 12		PIN 10
22	3	F		PIN 13		PIN 11
23	3	G		NO CONNECTION		PIN 12
24	3	D.P.		NO CONNECTION		PIN 13
25		PIN 4		NO CONNECTION		NO CONNECTION
26		PIN 5		NO CONNECTION		NO CONNECTION
27		PIN 6		NO CONNECTION		NO CONNECTION
28		PIN 7		NO CONNECTION		NO CONNECTION
29		PIN 8		NO CONNECTION		NO CONNECTION
30		PIN 9		NO CONNECTION		NO CONNECTION
31		PIN 10		NO CONNECTION		NO CONNECTION
32		PIN 11		NO CONNECTION		NO CONNECTION
33		PIN 12		NO CONNECTION		NO CONNECTION
34		PIN 13		NO CONNECTION		NO CONNECTION

TYPICAL APPLICATION

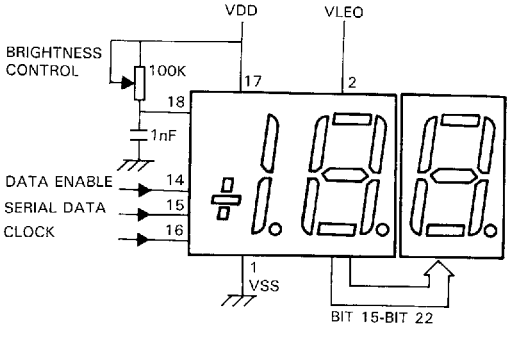
A. 1½ DIGIT DISPLAY



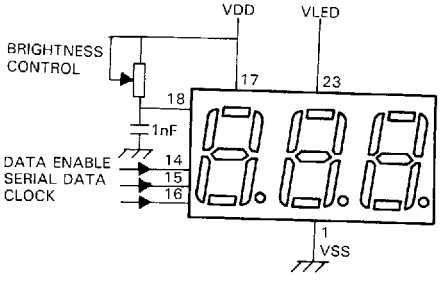
B. 2 DIGIT DISPLAY



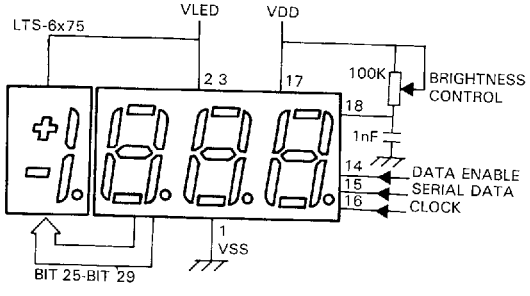
C. 2½ DIGIT DISPLAY



D. 3 DIGIT DISPLAY



E. 3½ DIGIT DISPLAY



F. 4 DIGIT DISPLAY