ST16-19RFRDCS

CHIP SET INTERFACE SPECIFICATION

FSD_CHIPSET_B/0104VP2

The present document contains CONFIDENTIAL INFORMATION.
Please refer to last page for obligations

DIFFERENCES BETWEEN:

FSD_CHIPSET_B/0006VP1 AND FSD_CHIPSET_B/0104VP2

DESCRIPTION OF THE MODIFICATION	PARAGRAPH ON VP2
Definition modification of the signal Tx-start	Chapter 1.2.2 "Interface signals definition", page 2
Modification of the figure 4	Chapter 1.7 "FPGA pin-out & Chip Set Block Diagram", page 8

Note: other modifications which are only editorial are not described in this table.

TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

CHIP SET INTERFACE SPECIFICATION

PRELIMINARY DATA

1 FPGA & MCU INTERFACE

1.1 DESCRIPTION

The goal of this document is to provide a Hardware / Software interface specifications of the FPGA component (Xilinx SPARTANXL XCS40XL-4PQ208C) used in the STMicroelectronics Contactless System.

The FPGA manages the communication between the MCU and the Analog Front End. This component formats the frames in accordance with ISO 14443 type B standard.

1.2 PHYSICAL INTERFACE BETWEEN FPGA AND MCU

This corresponds to a classical memory interface between bidirectional Data bus, Selection signal, Read/ Write signal and a signal used to select either FIFOs or Control/Status registers access

1.2.1 Interface signals description

In order to simplify interface specification, the FPGA logic has been designed with the same accesses for FIFOs and Control Registers. This is the reason why the read access chronogram show only one access type (figure 1)

However, for write access chronogram, two access types are shown (figures 2 & 3).

MCU accesses are done in burst mode for the FIFOs, it is not useful to generate addresses. So, there is no address bus for the MCU Interface. To address the different control registers, the two MSB bits from the data bus must be used.

These control registers have to be setted during the first transmission each time the code is down loaded in FPGA (start up of the reader) or when any parameter has to be modified. For later transmissions, the control registers don’t need to be re initialised.

The control Register Description is available in table 2.

1.2.2 Interface signals definition

The signals used for the interface between FPGA & MCU, in transmission and reception, are:

Mic_Data(7:0): Data bidirectional bus.

Mic_strb_b: FPGA strobe signal (Activ low) used to sample the data.
This signal is sent by the MCU to the FPGA

Mic_RW: Writing/Reading signal ('1'=reading, '0'=writing).
This signal is sent by the MCU to the FPGA

Mic_Ctrl_Data: Registers/FIFOs access signal ('1' = Register access, '0' = FIFOs access).
This signal is sent by the MCU to the FPGA

Tx_start: Transmission command, used to start data transmission from FIFO to output pin.
This signal is sent by the MCU to the FPGA

Tx_fifo_empty: Signal used to indicate transmission fifo empty.
This signal is sent by the FPGA to the MCU

Rx_fifo_empty: Signal used to indicate reception fifo empty.
This signal is sent by the FPGA to the MCU

Rx_irq_eof: IRQ reception end.
This signal is sent by the FPGA to the MCU

1.3 FIFOS ACCESS

1.3.1 Transmission FIFO (cf figure 1)

At the end of a transmission (or during power-on), the FPGA sets the transmission FIFO pointers to zero. This way, Tx_Fifo_Empty is validated, and so the software has to check that transmission FIFO is empty before sending a new frame.

1.3.2 Reception FIFO (cf figures 2 & 3)

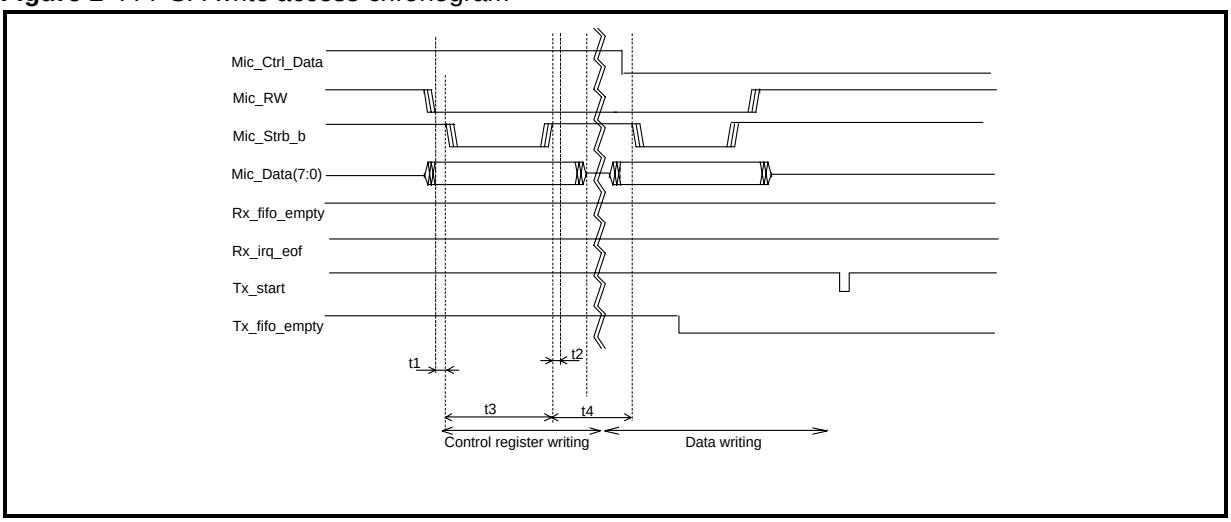
The reading pointer of reception FIFO is reset after each new frame received. It is impossible to get more than one frame in the FIFO. Thus, after each interruption, data stored in the FIFO has to be read until validation of Rx_Fifo_Empty signal.

WARNINGS: - Reception FIFO reading is done in "lookahead" mode. Bytes are read by the FPGA in internal mode before being read by the MCU. Thus, the Rx_Fifo_Empty signal is valid just before reading the last byte in the FIFO. FIFO reception has to be read once more when Rx_Fifo_Empty is valid to get the last byte of the received frame.

1.3.3 Write access chronogram

FPGA write access chronogram, for transmission FIFO or control register:

Figure 1 : FPGA write access chronogram

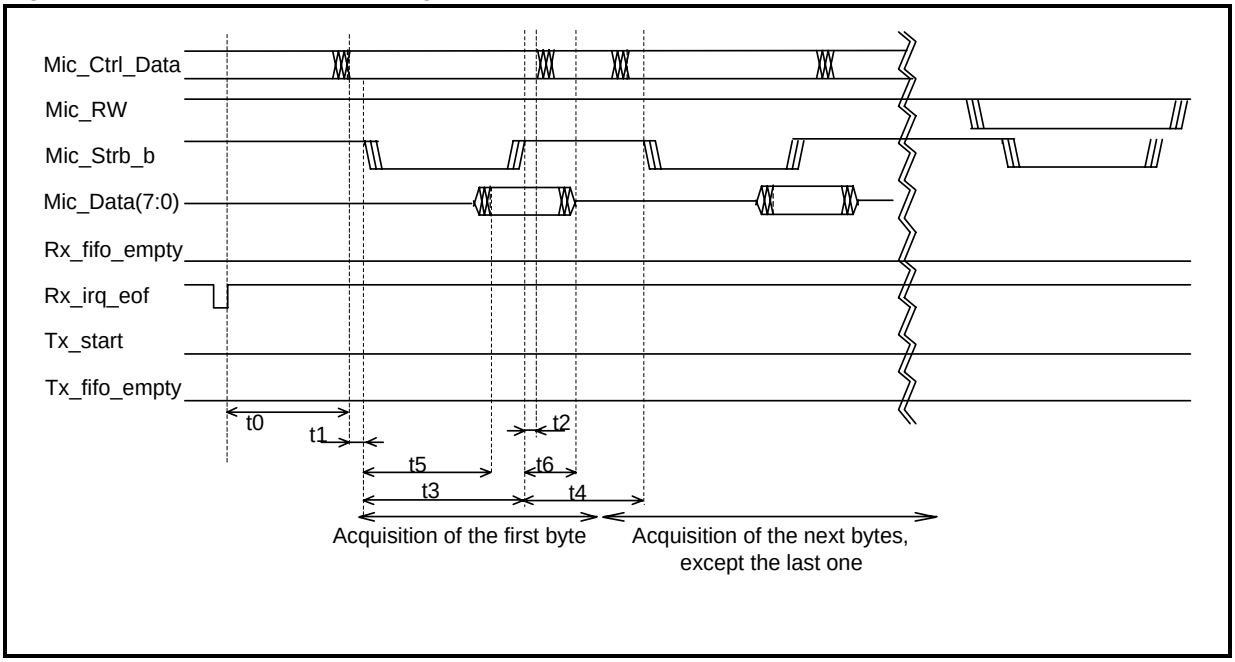


In figure1, two types of access are shown. The first one is a Control register access (Mic_Ctrl_Data = '1') and the second one is a FIFO access (Mic_Ctrl_Data = '0').

1.3.4 Read access chronogram

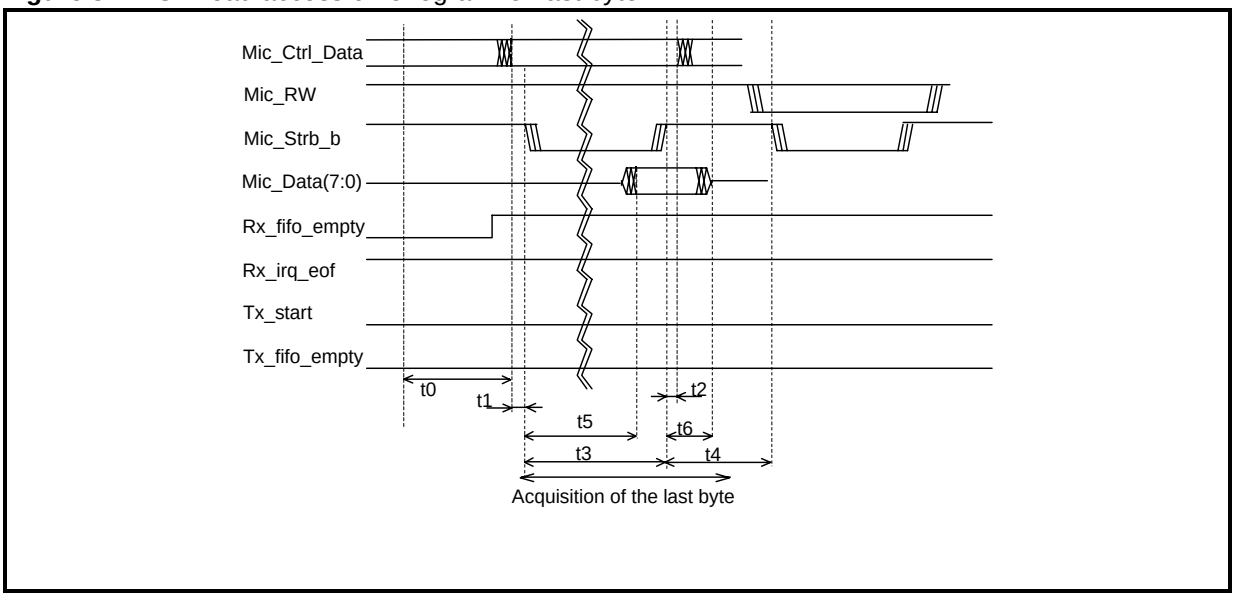
FPGA read access chronogram, for reception FIFO or status register:

Figure 2 FPGA read acces chronogram



In the figure 2, prior to sending data the FPGA takes the Rx_IRQ_EOF line low to indicate to the MCU that the data can be recuperated.

Figure 3 FPGA read access chronogram for last byte



Before sending the last byte the FPGA takes the Rx_fifo_empty line high to indicate to the MCU that this is the last data.

1.3.5 MCU interface timings

The following board provides interface timings (cf previous chronogram)

Table 1 : Interface timing

Timing	Parameter	Min. (ns)	Max. (ns)
t0	Rx_irq_eof to Mic_Strb_b Transition	0	
t1	Mic_Ctrl_Data, Mic_RW (and Mic_Data in writing) Setup Time before Mic_Strb_b Low Transition	0	
t2	Mic_Ctrl_Data, Mic_RW (and Mic_Data in writing) Hold Time before Mic_Strb_b High Transition	0	
t3	Mic_Strb_b Width Low (Activ)	240	
t4	Mic_Strb_b Width High (Inactiv)	80	
t5	Mic_Strb_b Activ to Valid Data in Reading		240
t6	Mic_Strb_b Inactiv to Tri-States Data in Reading		20

1.4 CONTROL REGISTERS

1.4.1 Reception control bits

Rx_Valid_Ext: Valid_Frame signal is provided by the Analog Front End or detected by the FPGA ('1'= External Valid, '0'= Digital Detection).

Rx_Speed_Auto: Reception Speed Detection ('1'= automatic, '0'= by Rx_Speed_Low Bit).

Rx_Speed_Config: Reception Rate ("00"=106K, "01"=212K, "10"=424K, "11"=424K).

1.4.2 Transmission Control bits

Tx_Speed_Config: Transmission Rate ("00"=106K, "01"=212K, "10"=424K, "11"=424K).

Tx_Egt_Config: Number of ETU bits between data characters.

Tx_CRC_Disable: Allows to insert or not the two CRC bytes at the end of the frame ('0'= CRC automatic, '1'= CRC disable).

Tx_SOF_0_11: Number of '0's inside the Start Of Frame ('0'=10, '1'=11).

Tx_SOF_1_3: Number of '1's inside the Start Of Frame ('0'=2, '1'=3).

Tx_EOF_0_11: Number of '0's inside the End Of Frame ('0'=10, '1'=11).

1.4.3 Others Control bits

Two bits control the functional mode and polarity of the interruption used to indicate the end of a received frame.

Cfg_Irq_Pulse: IRQ Functionality ('0'=Toggle, '1'=Pulse).

Cfg_Irq_High: Interrupt Pulse Polarity ('0'=Low, '1'=High).

In order to be able to test the Card Reader functionality at power-on, it's possible to connect the transmission on the reception inside the FPGA (Loop Mode).

Cfg_Loopback: Connection of the transmission on the reception. ('1'= Connection, '0'= Normal Running)

1.5 STATUS REGISTER

There is only one status register (for reception). This register can be read at the end of each reception. Its contents is modified by the end of frame interruption. It provides the status of the last received frame.

In order to access this register, after the last byte received in reception, take the Mic_Ctrl_Data line high and then read the data.

Rx_Speed_Value: Reception Rate ("00"=106K, "01"=212K, "10"=424K, "11"=424K). Comment: If the configuration bit Rx_Speed_Config is setting the speed, these bits are the same as configuration bits.

Rx_CRC_OK: CRC Status of the frame (’1’= Wrong, ’0’= OK).

Rx_EGT_TooLong: Bit used to indicate EGT overrun during reception.

Rx_Bad_StopBit: Bit used to indicate if a stop bit wasn’t at ’1’ during frame reception.This is may be due to bad synchronization.

If there is any mistake during the reception, this one will be stopped. In this case, the status register must be read to know the failure.

1.6 REGISTERS MAPPING

1.6.1 Control Registers

The control bits mapping is given by the following table:

Table 2 : Control register description

"Address	"Description
"00"	**Functionality Mode Setting** bit 0: **Cfg_Irq_Pulse** **'0'** = Toggle Mode '1' = Pulse Mode bit 1: **Cfg_Irq_High** **'0'** = Pulse Activ Low '1' = Pulse Activ High bit 2: **Cfg_Loopback** **'0'** = Usual Functionality '1' = Loop back bit 3: ST Reserved => set to '0' bit 4: ST Reserved => set to '0 bit 5: ST Reserved => set to '0' bit [7:6]: **Register Address Bits => set to "00"**
"01"	**Reception Control** bit 0: **Rx_Valid_Ext** '0' = Digital Detection '1' = External Valid bit 1: **Rx_Speed_Auto** '0' = By Rx_Speed_Config Bits '1' = Automatic bit [3:2]: **Rx_Speed_Config** "00" = 106K "01" = 212K "10" & "11" = 424K bit 4: ST Reserved => set to '0' bit 5: ST Reserved => set to '0' bit [7:6]: **Register Address Bits => set to "01"**
"10"	**Register 1 Transmission Control** bit [1:0]: **Tx_Speed_Config** **"**00" = 106K "01" = 212K "10" & "11" = 424K bit[4:2]: **Tx_Egt_Config** Number of d'EGT bits bit 5: ST Reserved => set to '0' bit [7:6]: **Register Address Bits => set to "10"**
"11"	**Register 2 Transmission Control** bit 0: **Tx_CRC_Disable** '0' = CRC automatic '1' = CRC disable bit 1: **Tx_SOF_0_11** '0' = SOF of 10 bits at '0' '1' = SOF of 11 bits at '0' bit 2: **Tx_SOF_1_3** '0' = SOF of 2 bits at '1' '1' = SOF of 3 bits at '1' bit 3: **Tx_EOF_0_11** '0' = EOF of 10 bits at '0' '1' = EOF of 11 bits at '0' bit 4: ST Reserved => set to '0' bit 5: ST Reserved => set to '0' bit [7:6]: **Register Address Bits => set to "11"**

Example:

Register " Reception Control ": MSB LSB

01000011

bit [7:6] "01": identification of the Register " Reception Control "

bit [5:4] "00": set to '0'

bit [3:2] "00": speed 106K

bit 1 '1' : automatic speed detection

bit 0 '1' : external valid

1.6.2 Status register

The mapping of the different state bits is given by the following table:

Table 3 : Reception status register description

"Address	"Description
’0	**Reception Control** bit [1:0]: **Rx_Speed_Value** "00" = 106K "01" = 212K "10" & "11"= 424K bit 2: **Rx_CRC_OK** ’0’ = CRC OK ’1’ = CRC Wrong bit 3: **Rx_EGT_TooLong** ‘0’ = EGT OK '1' = EGT too long bit 4: **Rx_Bad_StopBit** ‘0’ = Stop Bit Value OK '1' = Stop Bit wrong => frame wrong? bit 5: ST Reserved => read at '0' bit 6: ST Reserved => read at '0' bit 7: ST Reserved => read at '0'

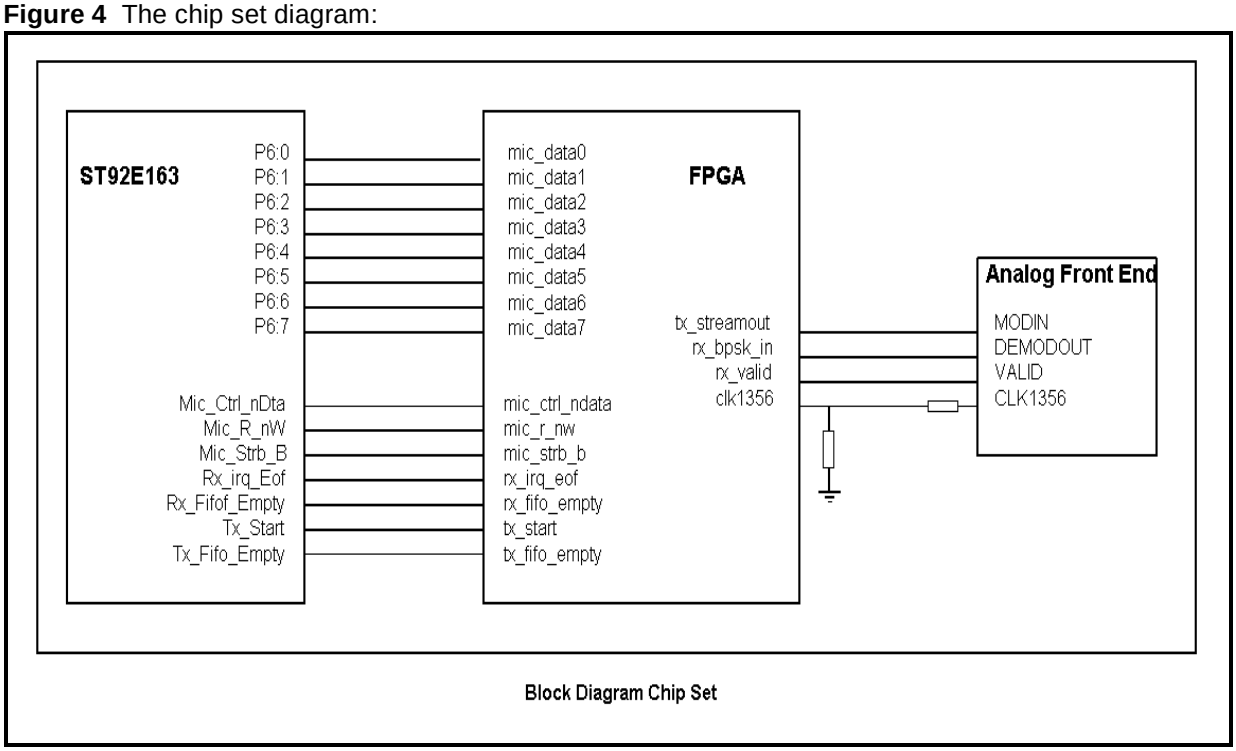
1.7 FPGA PIN-OUT & CHIP SET BLOCK DIAGRAM

The FPGA pin-out is given by the list below:

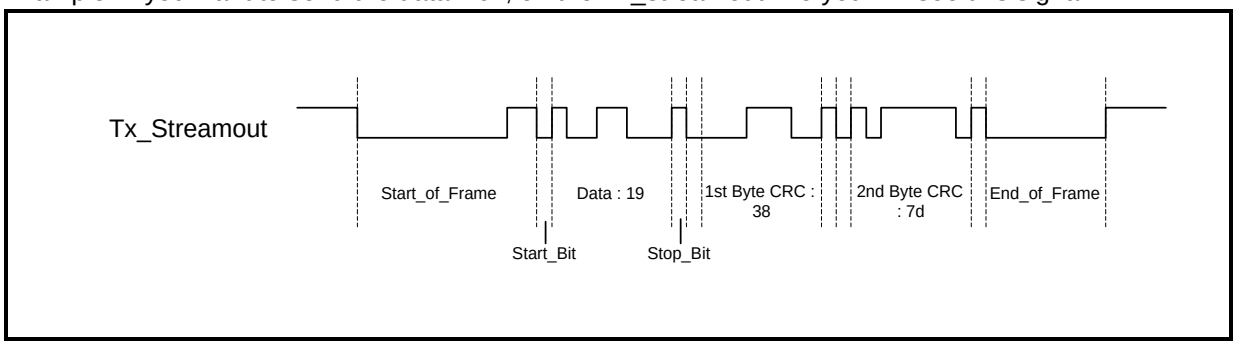
Table 4 : FPGA pin out

Signal	Site
clk1356	P2
mic_ctrl_ndata	P176
mic_data<0>	P184
mic_data<1>	P185
mic_data<2>	P186
mic_data<3>	P187
mic_data<4>	P188
mic_data<5>	P189
mic_data<6>	P190
mic_data<7>	P191
mic_r_nw	P181
mic_strb_b	P179
reset	P102
rx_bpsk_in	P48
rx_fifo_empty	P89
rx_irq_eof	P180
rx_valid	P198
tx_fifo_empty	P29
tx_start	P30
tx_streamout	P37

Figure 4 The chip set diagram:

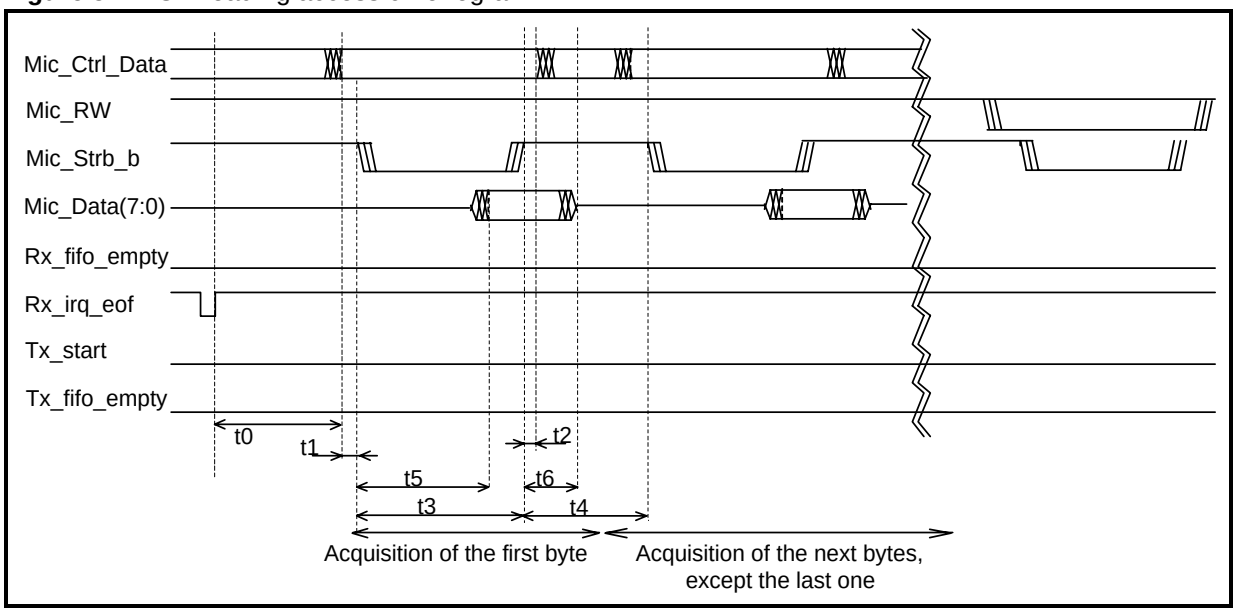


Example: If you want to send the data ’19 ’, on the Tx_streamout line you will see this signal:

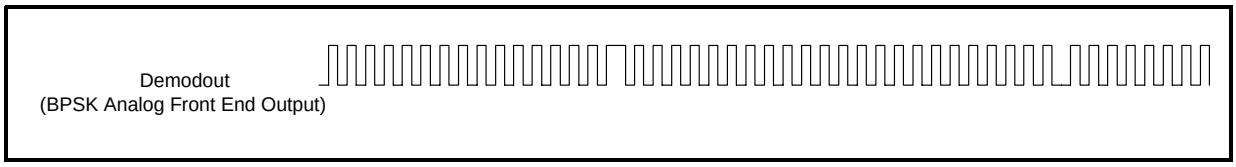


Example: Inputs and ouputs of the FPGA

Figure 5 FPGA reading access chronogram



Example: you will find hereafter an example of the Analog front End Output. This is a BPSK signal:



2 ANALOG FRONT END SPECIFICATION

2.1 DESCRIPTION

The Analog Front End is a combined RF generator and signal interface. It manages the communication between a reader so called proximity coupling device (PCDs) and a proximity contactless smartcard (PICCs). The AFE is connected to the FPGA component and the MCU used in the STMicroelectronics Contactless System (reader chip set).

The Analog Front End is full ISO 14443 type B compliant.

The Analog Front End operates at 13.56 MHz. As the contactless smart card carries no battery, the card is telepowered by a magnetic field, produced by the AFE, through the antenna. It also includes data modulation and demodulation circuits.

The AFE is a Dil 32 with only 12 pins package. In this version, only eight pins are used, the not connected pin will be used for the extension type A (Figure 6).

The device requires an external inductor, an external capacitance and resistance in order to resonate at 13.56 MHz.

$$FC = \frac{1}{2\pi\sqrt{L*C}}$$

Figure 7 shows a typical configuration of the external circuit for the AFE.

Figure 6 Pin Configuration:

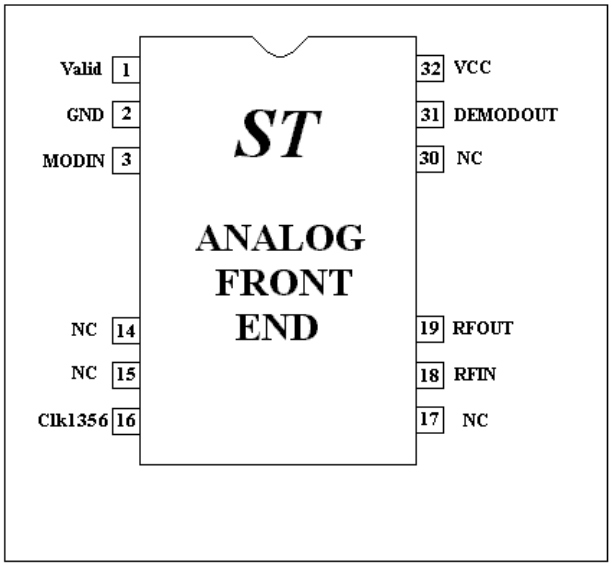
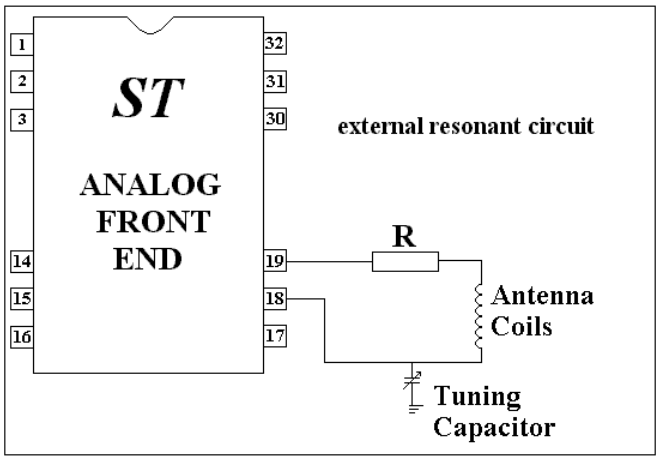


Figure 7 Configuration of external resonant circuit:



2.2 FEATURES

The AFE is full ISO 14443 type B compliant:

– Frequency of the RF operating field is: Fo= 13,56 MHz +/- 7 kHz
– Data rate from card to reader and reader to card: 106 k bits
– Data modulation from reader to card:- ASK of 10%, between 6 and 14%; NRZ

Data demodulation from Card to reader: BPSK NRZ load modulation, sub carrier F0/16 =847 kHz

Package: DIL 32

2.3 AC/DC ELECTRICAL CHARACTERISTICS

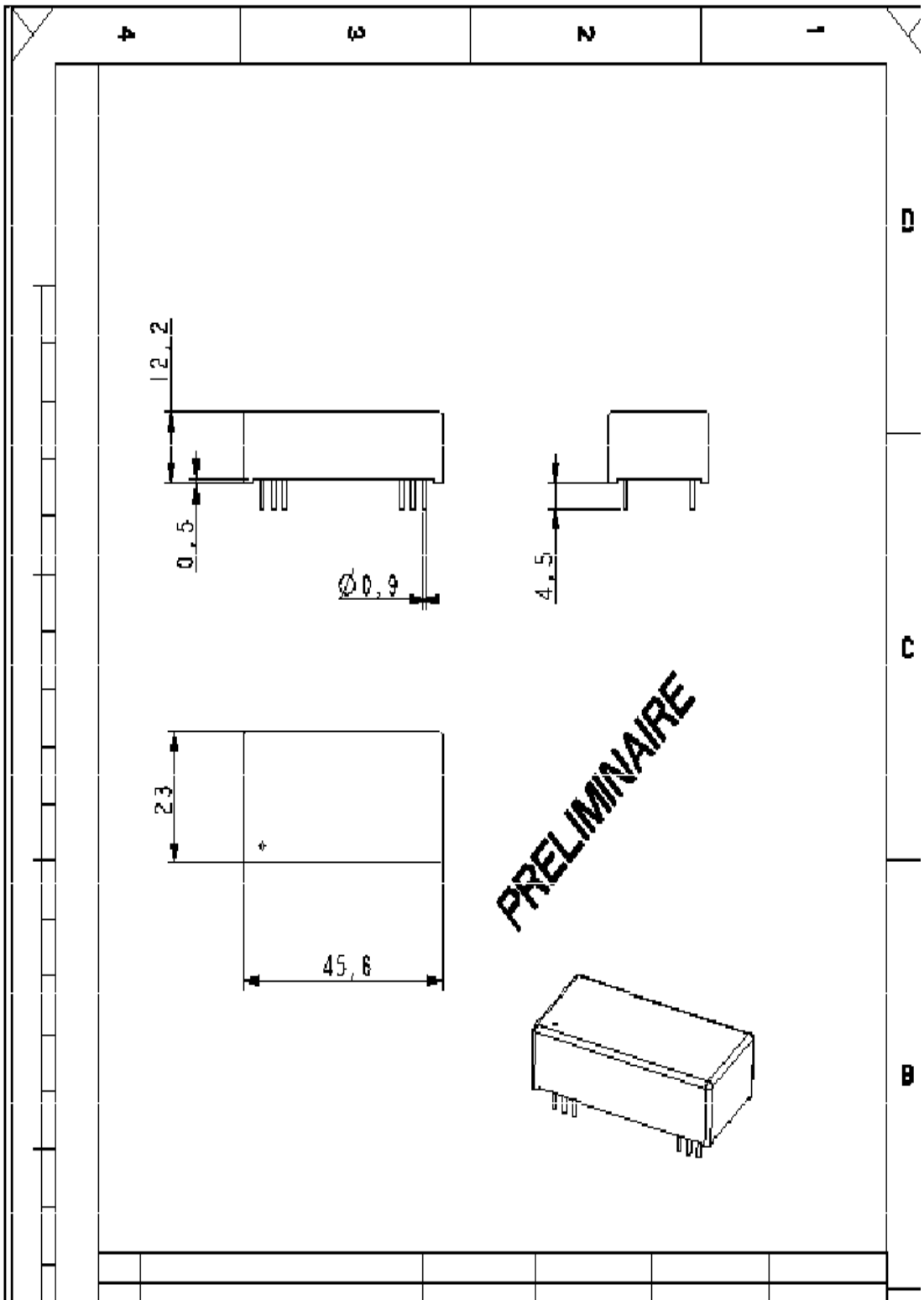
Vcc = +12 V, Ta = 25 °C, magnetic field = 7,5 A/m; unless otherwise stated.

Symbol	Parameter	Limits	Units
Vcc	Power supply voltage	12	V
	Current consumption	140	mA
F osc	Oscillator frequency	13.56	MHz
	Frequency stability	+/-100	Ppm
S	Demodulator Sensibility	10	mV

2.4 ABSOLUTE MAXIMUM RATINGS

Symbol	parameter	rating	units
Vcc	Maximum operating voltage	18	V
Tstg	Storage temperature range	- 20 to + 60	°C
Ta	Operating ambient temperature range	- 5 to + 50	°C

Figure 8 Preliminary Packaging Datasheet:



3 GLOSSARY

AFE	Analog Front End
ASK	Amplitude Shift Keying
BPSK	Binary Phase Shift Keying
CRC	Cyclic Redundancy Check error detection code
DIL	Dual-In-Line
EGT	Extra Guard Time
ETU	Elementary Time Unit. Duration of one bit of data transmission
FIFO	First In First Out
FPGA	Field Programmable Gate Array
IRQ	Interrupt Request
ISO Standard	ISO/IEC 14443-3
LSB	Least Significant Bit
MSB	Most Significant Bit
MCU	Micro Controller Unit
NRZ	Non-Return to Zero
PCD	Proximity Coupling Device
PICC	Proximity Integrated Circuit Cards