Low-voltage Highly Selective IR Receiver IC

T2527

Features

- No External Components Except PIN Diode
- Supply-voltage Range: 2.7 V to 3.6 V
- Available for Carrier Frequencies in the Range of 30 kHz to 56 kHz; Adjusted by Zener-diode Fusing
- Enhanced Bandpass Filter Accuracy of ±1.25%
- ESD: 4 kV HBM, 400 V MM
- Automatic Sensitivity Adaptation (AGC)
- Automatic Strong Signal Adaptation (ATC)
- Enhanced Immunity against Ambient Light Disturbances
- TTL and CMOS Compatible
- Suitable Minimum Burst Length ≥ 6 or 10 pulses

Applications

- Audio/Video Applications
- Home Appliances
- Remote Control Equipment

Description

The fully integrated IR receiver IC T2527 is designed to be used in all kinds of unidirectional infrared data transmission systems. It is especially optimized for carrier-frequency modulated transmission applications. Several built-in features enable best transmission quality.

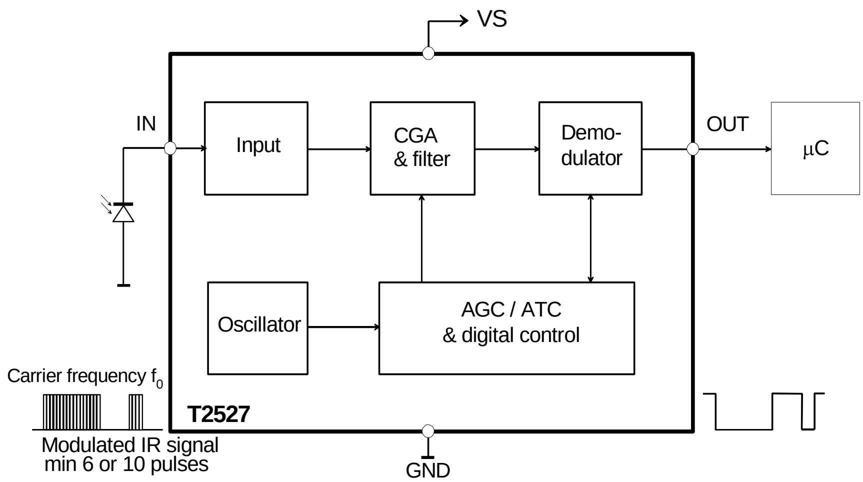
The input stage has two functions: first to provide the bias voltage for the PIN diode and secondly to transform the photo current signal into a voltage for further internal processing. This is carried out by a special circuit that is optimized for low-noise applications due to the fact that the incoming current signal is as small as 700 pA. This voltage signal is amplified by a so-called Controlled Gain Amplifier (CGA) followed by a bandpass filter. The filter frequency and therefore the operating carrier frequency are defined by a narrow-tuned bandpass filter. The enhanced bandpass filter tunes the input signal very accurately with a tolerance of ±1.25%.

The input burst signal is demodulated and converted into a digital envelope output pulse. An integrated dynamic feedback circuit block (which varies the gain as a function of the present environmental conditions such as ambient light, modulated lamps etc.) makes sure that the signal information is evaluated and that unwanted pulses are suppressed at the output pin.

The operating supply voltage range for the T2527 is 2.7 V to 3.6 V.

Rev. 4600B–IRDC–12/02

Figure 1. Block Diagram



Pad Layout

Figure 2. Pad Layout 1 (DDW Only)

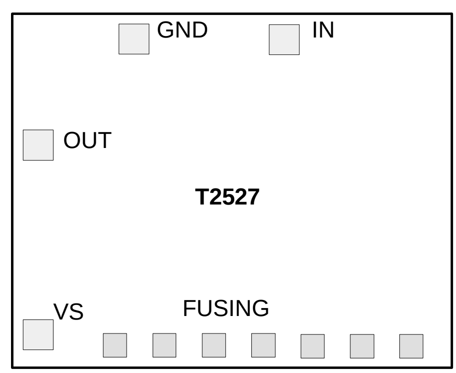
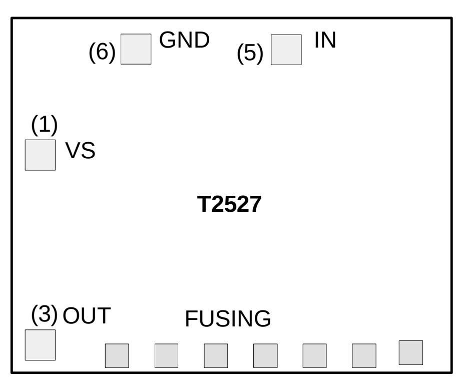
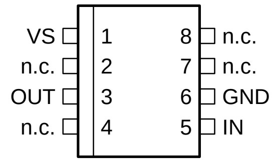


Figure 3. Pad Layout 2 (DDW, SO8 or TSSOP8)



Pin Configuration

Figure 4. Pinning SO8 and TSSOP8



Pin Description

Pin	Symbol	Function
1	VS	Supply voltage
2	n.c.	Not connected
3	OUT	Data output
4	n.c.	Not connected
5	IN	Input PIN diode
6	GND	Ground
7	n.c.	Not connected
8	n.c.	Not connected

Absolute Maximum Ratings

Parameters	Symbol	Value	Unit
Supply voltage	V_S	-0.3 to +4.0	V
Supply current	I_S	2.0	mA
Input voltage	V_{IN}	-0.3 to V_S	V
Input DC current at V_S = 3 V	I_{IN}	0.4	mA
Output voltage	V_O	-0.3 to V_S	V
Output current	I_O	10	mA
Operating temperature	T_{amb}	-25 to +85	°C
Storage temperature	T_{stg}	-40 to +125	°C
Power dissipation at T_{amb} = 25°C	P_{tot}	20	mW

Thermal Resistance

Parameters	Symbol	Value	Unit
Junction ambient SO8	R_{thJA}	130	K/W
Junction ambient TSSOP8	R_{thJA}	TBD	K/W

Electrical Characteristics

T_{amb} = -20°C to +70°C, V_S = 2.7 V to 3.6 V unless otherwise specified.

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
1	**Supply**								
1.1	Supply-voltage range		1	V_S	2.7	3.0	3.6	V	C
1.2	Supply current	I_{IN} = 0	1	I_S	0.7	0.9	1.2	mA	B
2	**Output**								
2.1	Internal pull-up resistor [1]	T_{amb} = 25°C; see Figure 12	1, 3	R_{PU}		30/40		kΩ	A
2.2	Output voltage low	R_2 = 2.4 kΩ; see Figure 12	3, 6	V_{OL}			250	mV	B
2.3	Output voltage high		3, 1	V_{OH}	V_S-0.25		Vs	V	B
2.4	Output current clamping	R_2 = 0; see Figure 12	3, 6	I_{OCL}		8		mA	B
3	**Input**								
3.1	Input DC current	V_{IN} = 0; see Figure 12	5	I_{IN_DCMAX}	-150			µA	C
3.2	Input DC current; see Figure 6	V_{IN} = 0; V_S = 3 V, T_{amb} = 25°C	5	I_{IN_DCMAX}		-350		µA	B
3.3	Min. detection threshold current; see Figure 5	Test signal: see Figure 11 V_S = 3 V, T_{amb} = 25°C, I_{IN_DC} = 1 µA; square pp, burst N = 16, f = f_0; t_{PER} = 10 ms, Figure 10; BER = 50 [2]	3	I_{Eemin}		-700		pA	B
3.4	Min. detection threshold current with AC current disturbance IIN_AC100 = 3 µA at 100 Hz		3	I_{Eemin}		-1500		pA	C
3.5	Max. detection threshold current with V_{IN} > 0V	Test signal: see Figure 11 V_S = 3 V, T_{amb} = 25°C, I_{IN_DC} = 1 µA; square pp, burst N = 16, f = f_0; t_{PER} = 10 ms, figure 10; BER = 5%[2]	3	I_{Eemax}	-200			µA	D
4	**Controlled Amplifier and Filter**								
4.1	Maximum value of variable gain (CGA)			G_{VARMAX}		51		dB	D
4.2	Minimum value of variable gain (CGA)			G_{VARMIN}		-5		dB	D

*) Type means: A =100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

Notes:
1. Depending on version, see “Ordering Information”.
2. BER = bit error rate; e.g., BER = 5% means that with P = 20 at the input Pin 19 to Pin 21 pulses can appear at the Pin OUT.
3. After transformation of input current into voltage.

Electrical Characteristics (Continued)

T_{amb} = -20°C to +70°C, V_S = 2.7 V to 3.6 V unless otherwise specified.

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
4.3	Total internal amplification (3)			G_{MAX}		71		dB	D
4.4	Center frequency fusing accuracy of bandpass	V_S = 3 V, T_{amb} = 25°C		f_{03V_FUSE}	-1.25	f_0	+1.25	%	A
4.5	Overall accuracy center frequency of bandpass	See Figure 7		f_{03V}	-3.5	f_0	+2.0	%	C
4.6	BPF bandwidth	-3 dB; f_0 = 38 kHz; see Figure 9		B		3.8		kHz	C

*) Type means: A =100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

Notes: 1. Depending on version, see “Ordering Information”.
2. BER = bit error rate; e.g., BER = 5% means that with P = 20 at the input Pin 19 to Pin 21 pulses can appear at the Pin OUT.
3. After transformation of input current into voltage.

ESD

All pins: 2000 V HBM; 200 V MM, MIL-STD-883C, Method 3015.7

Typical Electrical Curves at T_{amb} = 25°C

Figure 5. I_{Eemin} versus I_{IN_DC} , V_S = 3 V

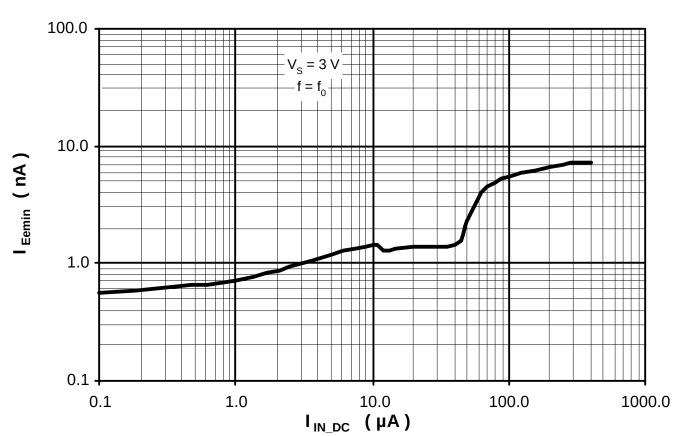


Figure 6. V_{IN} versus I_{IN_DC}, V_S = 3 V

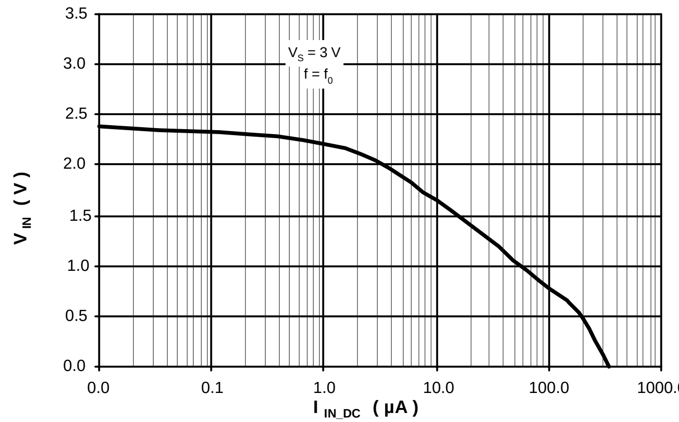


Figure 7. Overall Tolerance of Bandpass Inclusive Fusing

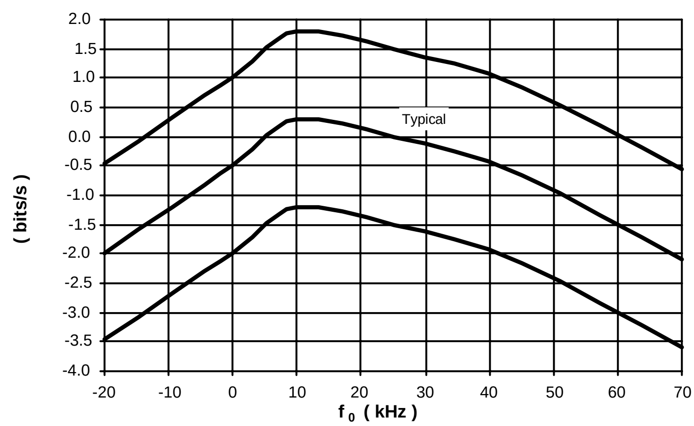


Figure 8. Data Transmission Rate, V_S = 3 V

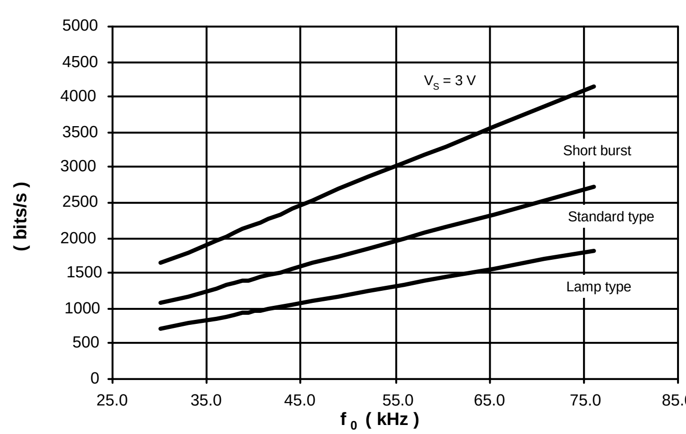
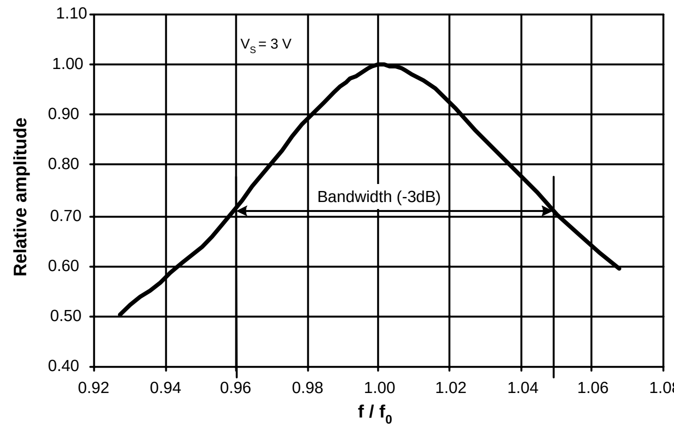


Figure 9. Typical Bandpass Curve



f_1 = 0.96 (at -3 dB)

$f_2 = f/f_0$

f_3 = 1.047 (at -3 dB)

B = bandwidth (-3 dB)

$Q = f_2 / B$

Example: $Q = 1/(1.047 - 0.960) = 11.5$

Figure 10. Illustration of Used Terms

Example: f = 30 kHz, burst with 16 pulses, 16 periods

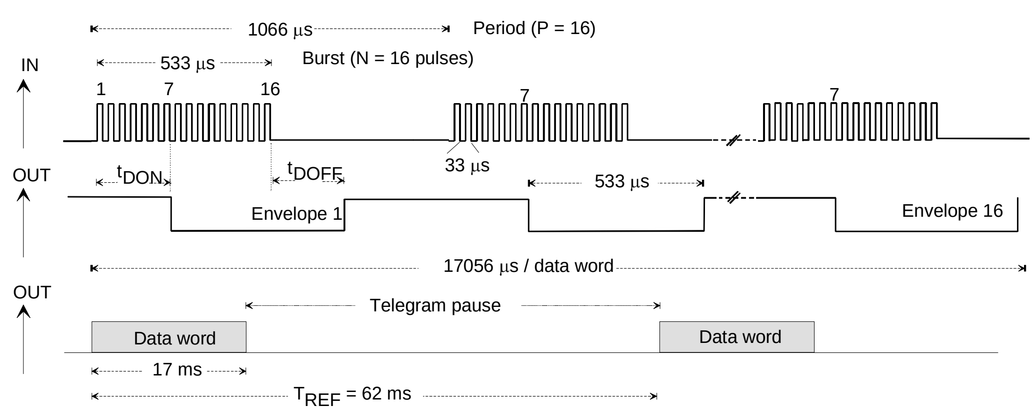


Figure 11. Test Circuit

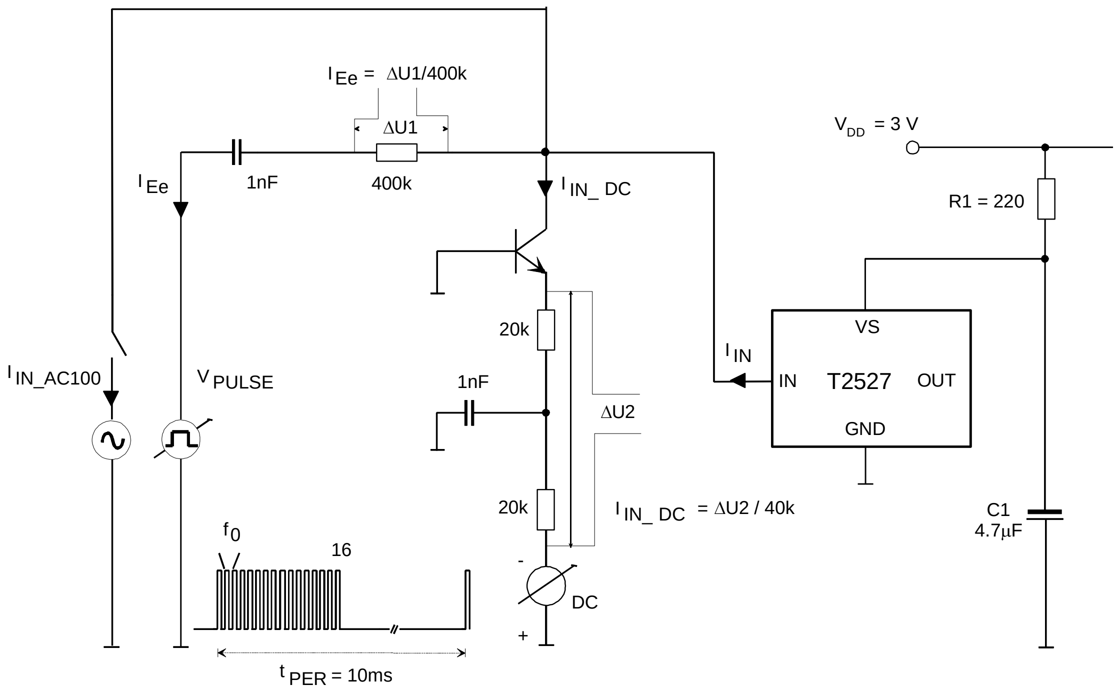
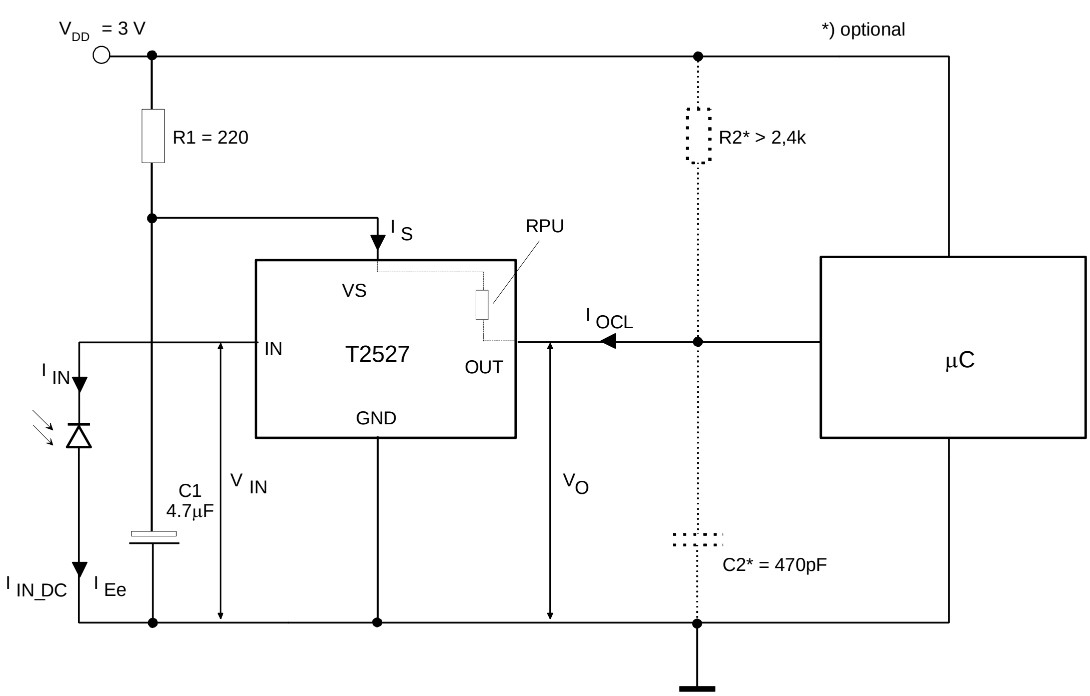
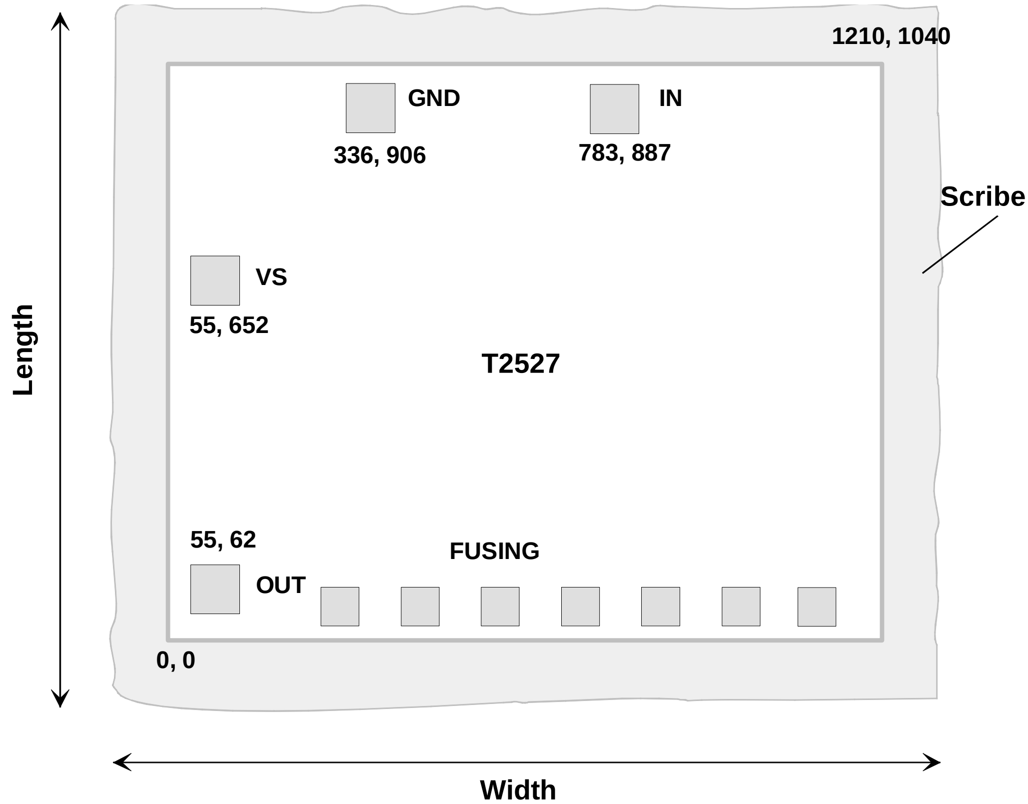


Figure 12. Application Circuit



Chip Dimensions

Figure 13. Chip Size in µm [1]



Note: 1. Pad coordinates are given for lower left corner of the pad in µm from the origin 0,0

Dimensions	Length incl. scribe	1.16 mm
	Width incl. scribe	1.37 mm
	Thickness	290 µ ± 5%
	Pads	90 µ x 90 µ
	Fusing pads	70 µ x 70 µ
Pad metallurgy	AlSiTi	
Finish	Si_3N_4 thickness 1.05 µm	

Ordering Information

Delivery: unsawn wafers (DDW) in box, SO8 (150 mil) and TSSOP8 (3 mm body).

Extended Type Number	PL[(2)]	R_{PU}[(3)]	D[(4)]	Type
T2527N0xx[(1)]-yyy[(5)]	2	30	2000	**Standard type:** ≥10 pulses, enhanced sensibility, high data rate
T2527N1xx[(1)]-DDW	1	30	2000	
T2527N2xx[(1)]-yyy[(5)]	2	40	1333	**Lamp type:** ≥10 pulses, enhanced suppression of disturbances, secure data transmission
T2527N3xx[(1)]-DDW	1	40	1333	
T2527N6xx[(1)]-yyy[(5)]	2	30	3060	**Short burst type:** ≥6 pulses, enhanced data rate
T2527N7xx[(1)]-DDW	1	30	3060	

Note:
1. xx means the used carrier frequency value f_0 30, 33, 36, 38, 40, 44 or 56 kHz (76 kHz type on request).
2. Two pad layout versions (see Figure 2 and Figure 3) available for different assembly demand.
3. Integrated pull-up resistor at PIN OUT (see electrical characteristics).
4. Typical data transmission rate up to bit/s with f_0 = 56 kHz, V_S = 3 V (see Figure 8).
5. yyy means kind of packaging: DDW -> unsawn wafers in box.

   ....DDW -> unsawn wafers in box

   ....6AQ -> (only on request, TSSOP8 taped and reeled)

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