

Radiation Hardened 3.3V Quad Differential Line Driver

The Intersil HS-26CLV31RH is a radiation hardened 3.3V quad differential line driver designed for digital data transmission over balanced lines, in low voltage, RS-422 protocol applications. CMOS processing assures low power consumption, high speed, and reliable operation in the most severe radiation environments.

The HS-26CLV31RH accepts CMOS level inputs and converts them to differential outputs. Enable pins allow several devices to be connected to the same data source and addressed independently. The device has unique outputs that become high impedance when the driver is disabled or powered-down, maintaining signal integrity in multi-driver applications.

Specifications for Rad Hard QML devices are controlled by the Defense Supply Center in Columbus (DSCC). The SMD numbers listed here must be used when ordering.

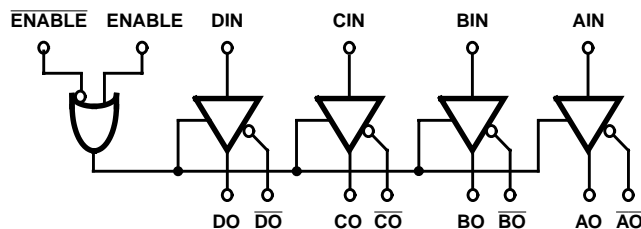
Detailed Electrical Specifications for these devices are contained in SMD 5962-96663. A "hot-link" is provided on our homepage for downloading.

www.intersil.com/spacedefense/space.htm

Ordering Information

ORDERING NUMBER	INTERNAL MKT. NUMBER	TEMP. RANGE (°C)
5962F9666302QEC	HS1-26CLV31RH-8	-55 to 125
5962F9666302QXC	HS9-26CLV31RH-8	-55 to 125
5962F9666302V9A	HS0-26CLV31RH-Q	25
5962F9666302VEC	HS1-26CLV31RH-Q	-55 to 125
5962F9666302VXC	HS9-26CLV31RH-Q	-55 to 125
HS1-26CLV31RH/PROTO	HS1-26CLV31RH/PROTO	-55 to 125
HS9-26CLV31RH/PROTO	HS9-26CLV31RH/PROTO	-55 to 125

Logic Diagram

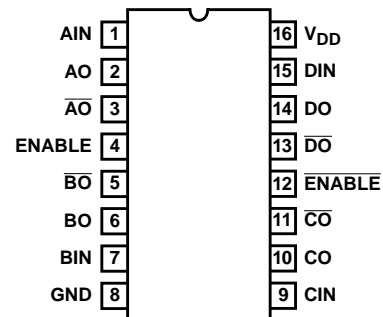


Features

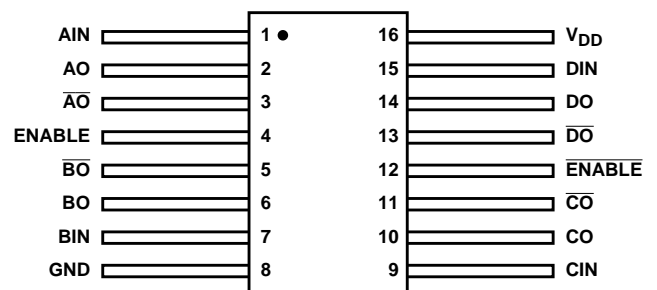
- Electrically Screened to SMD # 5962-96663
- QML Qualified per MIL-PRF-38535 Requirements
- 1.2 Micron Radiation Hardened CMOS
 - Total Dose 300 krad(Si)(Max)
 - Single Event Upset LET 100MeV/mg/cm²
 - Single Event Latch-up Immune
- Extremely Low Stand-by Current 100µA (Max)
- Operating Supply Range 3.0V to 3.6V
- CMOS Level Inputs $V_{IH} > (.7)(V_{DD})$; $V_{IL} < (.3)(V_{DD})$
- Differential Outputs $V_{OH} > 1.8V$; $V_{OL} < 0.5V$
- High Impedance Outputs when Disabled or Powered Down
- Low Output Impedance 10Ω or Less
- Full -55°C to 125°C Military Temperature Range

Pinouts

**HS1-26CLV31RH (SBDIP)
CDIP2-T16
TOP VIEW**



**HS9-26CLV31RH (FLATPACK)
CDFP4-F16
TOP VIEW**



Die Characteristics

DIE DIMENSIONS:

96.5 mils x 195 mils x 21 mils
(2450 x 4950)

INTERFACE MATERIALS:

Glassivation:

Type: PSG (Phosphorus Silicon Glass)
Thickness: $8\text{k}\text{\AA} \pm 1\text{k}\text{\AA}$

Metallization:

Bottom: Mo/TiW
Thickness: $5800\text{\AA} \pm 1\text{k}\text{\AA}$
Top: AlSiCu (Top)
Thickness: $10\text{k}\text{\AA} \pm 1\text{k}\text{\AA}$

Substrate:

AVLSI1RA

Backside Finish:

Silicon

ASSEMBLY RELATED INFORMATION:

Substrate Potential (Powered Up):

V_{DD}

ADDITIONAL INFORMATION:

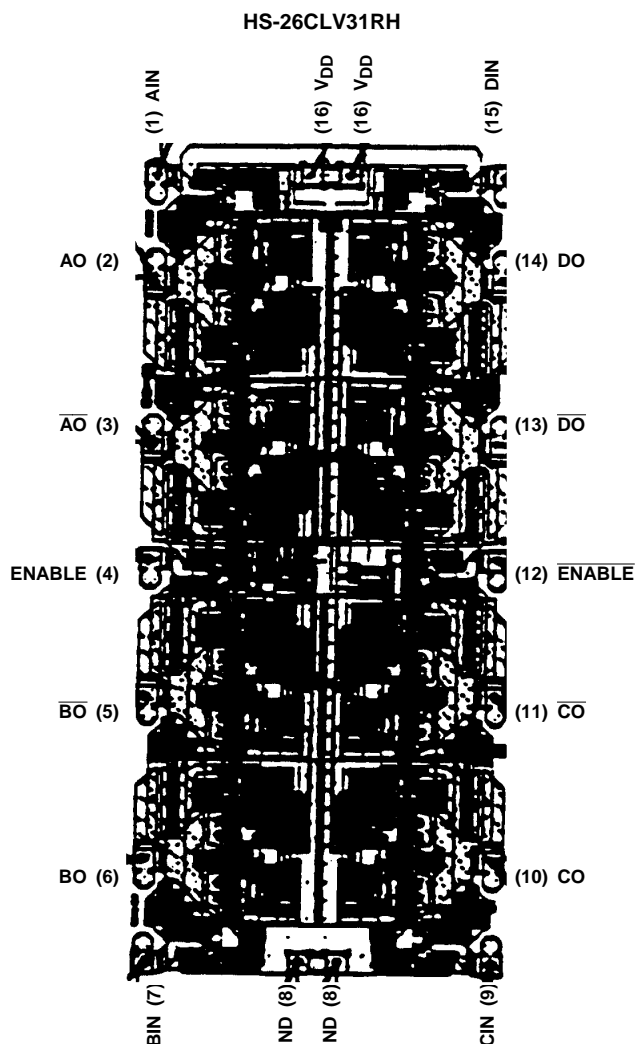
Worst Case Current Density:

$<2.0 \times 10^5 \text{A/cm}^2$

Bond Pad Size:

$110\mu\text{m} \times 100\mu\text{m}$

Metallization Mask Layout



All Intersil semiconductor products are manufactured, assembled and tested under **ISO9000** quality systems certification.

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