

Grounding for Low- and High-Frequency Circuits

Know Your Ground and Signal Paths for Effective Designs

Current Flow Seeks Path of Least Impedance — Not Just Resistance

by Paul Brokaw and Jeff Barrow

Noise reduction is a significant design issue in most electronic systems. Along with dissipation constraints, ambient temperature changes, size limitations, and speed & accuracy requirements, noise is an omnipresent factor that must be dealt with for a successful final design. We are not concerned here with techniques for reducing *external noise* (which arrives with the signal); since its presence is generally beyond the direct control of the design engineer; it must be dealt with in the operational design of the system by means such as filtering, analog signal processing, and digital algorithms.

In contrast, preventing *internal noise* (noise generated or coupled within the circuit or system) from corrupting the signal is a direct responsibility of the design engineer. Noise sources, if not fully considered *early in the design cycle*, can adversely affect final performance and prevent the high-resolution potential of a system from being realized; at the very least, costly redesign and rework may be required. Some of the design factors that relate noise to system behavior have been treated in earlier articles in these pages^{1,2,3,4,5}. Here, we consider the major role that schematic, topology, and final layout of the system “ground” play in minimizing the coupling of internally generated noise.

To deal adequately with noise, we need several perspectives: the actual internal pin connections of a component, versus the conceptual ones; the proposed schematic for ground-referenced signals; and the effects of layout on noise generation and pickup. These subjects divide into two overlapping domains, depending on bandwidth of the noise phenomena; ground-noise sources, problems, and solutions differ at low and high frequencies. Fortunately, good grounding practices in one band are generally compatible with those in the other.

¹“Noise and Operational Amplifier Circuits,” by D. H. Sheingold and L. R. Smith, *Analog Dialogue* 3-1 (1969).

²“Understanding Interference-Type Noise,” by Alan Rich, *Analog Dialogue* 16-3 (1982).

³“Shielding and Guarding,” by Alan Rich, *Analog Dialogue* 17-1 (1983).

⁴“Ground Rules for High-Speed Circuits,” by Don Brockman and Arnold Williams, *Analog Dialogue* 17-3 (1983).

⁵“Amplifier Noise Basics Revisited,” by Al Ryan and Tim Scranton, *Analog Dialogue* 18-1 (1984).

BASIC OP-AMP INTERCONNECTIONS

Many discussions of op amps present the ideal op amp as a three-terminal device with a pair of differential inputs and a single output (Figure 1). But the output voltage has to be measured with respect to some reference point, and output current from the amplifier must find a closed circuit back to the amplifier. The

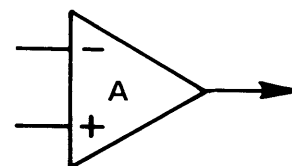


Figure 1. Conventional “three terminal” op amp.

infinite common-mode rejection of the ideal differential op amp disengages the input and output reference potentials, and the high input impedance eliminates the possibility of using an input terminal as an output current return; so there must be a fourth terminal, which some call “ground.”

Of course, most IC op amps don’t have a “ground” connection; the fourth terminal is generally considered to be the common connection of a dual power supply (which may also be serving other amplifiers and system elements). While it indeed serves this function at low frequencies, it will continue to do so only as long as the supply connections actually present the amplifier with a low (ideally zero) impedance at all frequencies within the amplifier bandwidth. When this requirement is not met, the impedance at the supply terminals affects the signal path and a wide variety of problems will arise, including noise, poor transient response, and oscillation.

An op amp must accept a fully differential signal and convert this to a single-ended output, with respect to the fourth terminal. Figure 2 shows the actual signal flow used by several basic and popular op amp families. Most of the voltage difference between the amplifier output and the negative rail appears across the compensating capacitor of the integrator (which controls the open-loop frequency response); if the negative supply voltage changes abruptly, the output of the integrator amplifier will immediately follow its “+” input. With the op amp in a typical closed-loop configuration, the input error signal tends to restore the output, with recovery limited by the integrator bandwidth.

This type of amplifier may have excellent low-frequency power-supply rejection, but negative supply rejection is limited at higher frequencies. Since the amplifier's gain is what causes the output to be restored, the negative supply rejection approaches zero for signals above the closed-loop bandwidth. The result: high-speed, high-level circuits can interact with the low-level circuits through the common impedance of the negative supply line.

Decoupling often is the recommended solution, but there are many wrong and some better ways. A decoupling capacitor near the

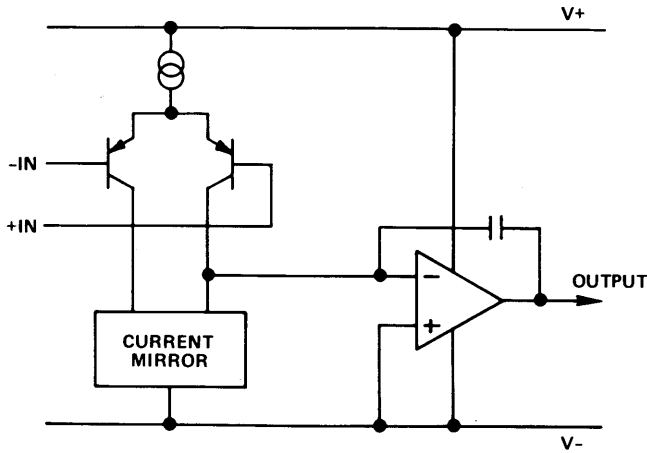


Figure 2. Simplified "real" op amp.

power supply may be separated from the op amp by many centimeters of wire, which looks like a high-Q inductor. Placing the decoupling capacitor near the op amp may still not solve the problem since, for decoupling, the other end of the capacitor must be connected to that mystical somewhere called "ground."

Figure 3* shows how a decoupling capacitor is connected to minimize disturbances between the negative rail and ground buses. The load current's high-frequency component is confined to a path that doesn't include any part of the ground path. As an example of a more complex case, in Figure 4, the op amp is driving a load that goes to virtual ground (input of the second amplifier) and actual load current does not return to ground. Instead, it must be supplied by the second amplifier via its positive supply. Decoupling the negative supply of the first amplifier to the positive supply of the second one closes the high-speed signal current loop without affecting ground or signal paths.

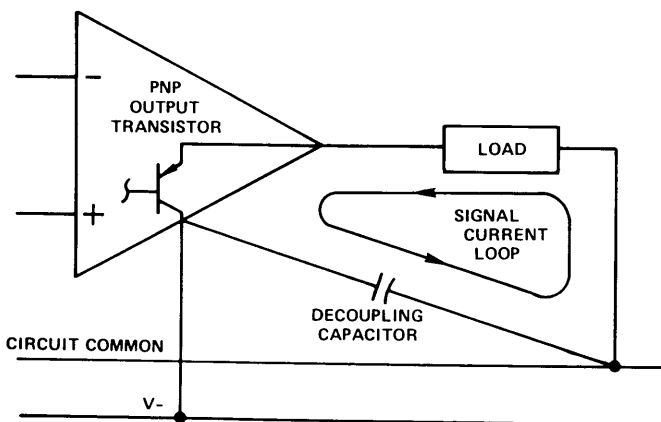


Figure 3. Decoupling of negative supply for a grounded load.

*Many of these illustrations can be found in the free Application Note, "An I. C. Amplifier User's Guide to Decoupling, Grounding, and Making Things Go Right for a Change," by Paul Brokaw.

Allowing ground currents to share a path with a low-level signal can cause problems. Figure 5 shows how careless grounding can degrade the performance of an amplifier driving a load resistor. The load current is supplied by the power supply and controlled by the amplifier. If points A and B are power supply "ground" connections, connecting the supply at A causes the load current to share a segment of wire with the input signal connections.

For example, fifteen centimeters of number 22 wire present about 8 mΩ of resistance to the load current. For a 2-kΩ load, a 10-volt

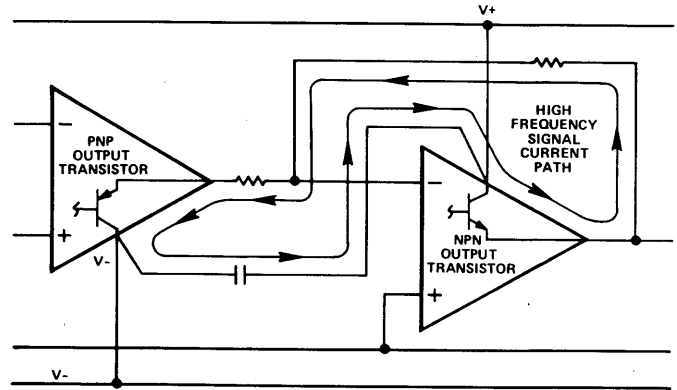


Figure 4. Decoupling of negative supply for "virtual ground" load.

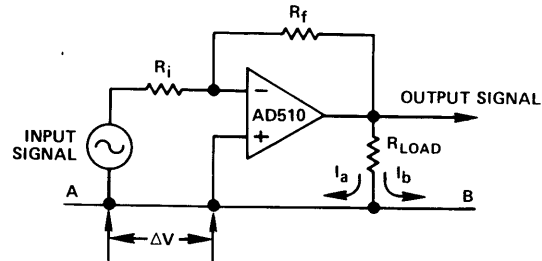


Figure 5. Proper choice of power connections will minimize this problem.

output swing results in about 40 μV between the points marked ΔV. This signal is in series with the non-inverting input and can result in significant errors: for an amplifier with a gain of 8 million, this positive feedback of 1/250,000 introduces a gain error factor 32× worse than that associated with the amplifier's open-loop gain alone. In addition, the positive feedback can cause circuit latchup or oscillation for large closed-loop gains (typically >250 V/mV). But the common feedback impedance can be eliminated by connecting the power supply to point B.

In a real system, the situation is more complicated. The input signal source, shown as floating in Figure 5, may also produce a current which must be returned to the power supply. With the supply's return at B, any current flowing in additional loads other than R_i may interfere with this amplifier's operation. Where amplifiers are cascaded, the scheme in Figure 6 shows how they can still drive auxiliary loads without common-impedance feedback coupling. Output currents flow through auxiliary loads and back to the power supply through the power common. Bypasses are connected as shown in Figure 4 so that currents in the input and feedback resistors are supplied from the power supply via the amplifiers. Only amplifier input current flows in signal common; its effect is usually small enough to ignore.

Understanding where the actual load and signal currents go is essential. The key to optimizing the circuit is to bypass these

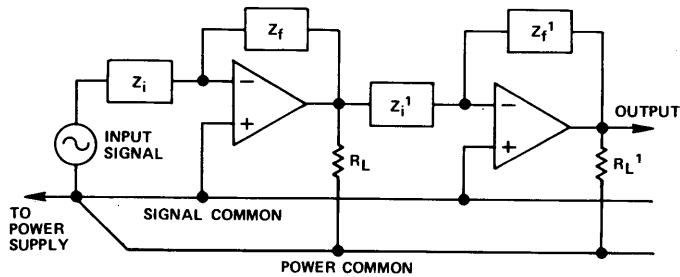


Figure 6. Minimizing common impedance coupling currents around ground and other signal paths. The voltage—more accurately called the potential difference—between two points defines such a current flow.

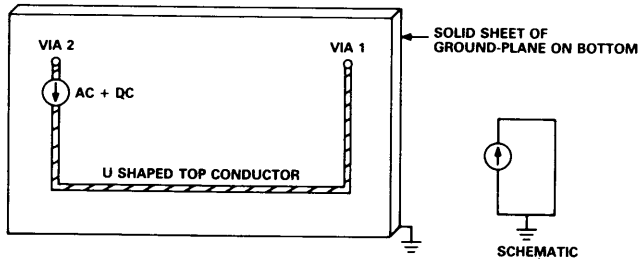


Figure 7. Schematic and layout of current source with U-shaped trace on pc board and return through ground plane.

GROUNDING FOR HIGH-FREQUENCY OPERATION

The “ground-plane” layer is often advocated as the best return for power and signal current, while providing a reference node for converters, references, and other subcircuits. However, even extensive use of a ground plane does not ensure a high quality ground reference for ac circuits.

The simple circuit shown in Figure 7, built on a two-layer printed circuit board, has an ac and dc current source on the top layer connected to via 1 at one end and to a single U-shaped copper trace connected to via 2. Both vias go through the circuit board and connect to the ground plane. Ideally, impedance is zero and the voltage appearing across the current source should be zero.

The simple schematic hardly begins to show the actual subtleties. But an understanding of how the current flows in the ground plane from via 1 to via 2 makes the realities apparent and shows how ground noise in high-frequency layouts can be avoided.

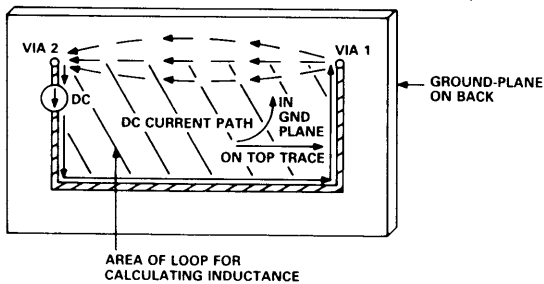


Figure 8. DC current path for Figure 7.

The dc current flows in the manner of Figure 8, as one might surmise, taking the path of least resistance from via 1 to via 2. Some current spreading occurs, but little current flows at substantial distance from this path. In contrast, the ac current does not take the path of least resistance; it takes the path of least *impedance*, which in turn depends on *inductance*.

Inductance is proportional to the area of the loop made by the current flow; the relationship can be illustrated by the right-hand rule and magnetic fields shown in Figure 9. Inside the loop, current along all parts of the loop produces magnetic field lines that add constructively. Away from the loop, however, field lines from different parts add destructively; thus the field is confined principally within the loop. A larger loop has greater inductance; this means that, for a given current level, it has more stored magnetic energy (Li^2), *greater impedance*—since $X_L = j\omega L$, and hence will develop more voltage at a given frequency.

Which path will the current choose in the ground plane? Naturally the lowest-impedance path. Considering the loop formed by the U-shaped surface lead and the ground plane, and neglecting resistance, high-frequency ac current will follow the path with the least inductance, hence the least area.

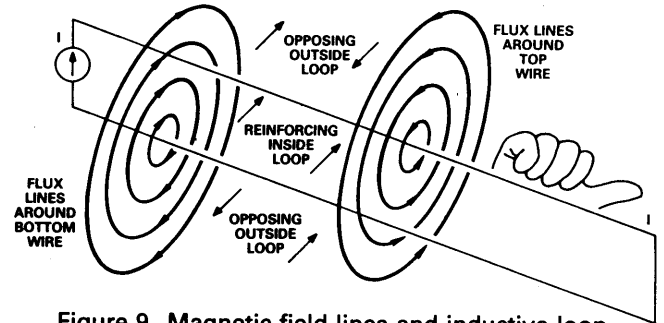


Figure 9. Magnetic field lines and inductive loop.

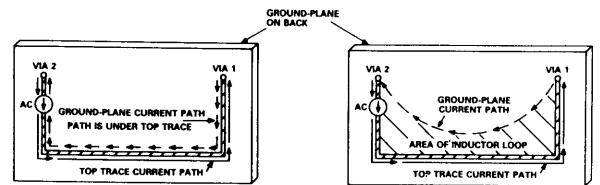


Figure 10. AC current path without (left) and with (right) resistance in ground plane.

In the simple example shown, the loop with the least area is quite evidently formed by the U-shaped top trace and the portion of the ground plane *directly underneath it*. So, while Figure 8 shows the dc current path, Figure 10 (left) shows that the path that most of the ac current takes in the ground plane, where it finds minimum area, directly under the U-shaped top conductor. In practice, the resistance in the ground plane causes the current flow at low- and mid-frequencies to be somewhere between straight back and directly under the top conductor (right). However, the return path is nearly under the top trace even at frequencies as low as 1 or 2 MHz.

Avoiding Layout Problems Once the return current paths in the ground-plane are understood, common layout trouble spots can be identified and corrected. For example, in Figure 11, path A is identified as critical, to be kept short, away from digital lines, and free of vias. Path B is of lesser importance, but needs to cross A. Typically, the ground plane is cut under A, and B is then routed through two vias and under A.

The unfortunate result is that inductance is introduced into the ground returns of both signals, because the interrupted ground plane makes both return loops larger. Since path A conducts a high-frequency signal, an induced voltage drop will appear across the opening of the ground plane. For typical ECL or TTL signals, this drop can be greater than several hundred millivolts, enough

to seriously compromise the performance of a 12-bit, 10-MHz converter or an 8-bit, 20-MHz unit. A simple fix is to install a wire directly across the cut in the ground plane to keep the loop area small.

Power distribution is another area of concern. Power supply lines must be kept at lowest possible characteristic impedance ($\sqrt{L/C}$). To keep this ratio small, inductance is reduced and capacitance increased by maintaining ground planes under the supply lines; capacitance can be further increased by selectively placing bypass capacitors at critical locations, as discussed earlier. If only capacitance is dealt with by, for example, placing 0.1- μ F capacitors on supply pins to lower their impedance, a supply line with 30-nH inductance will have damped oscillations at about 3 MHz after every transient.

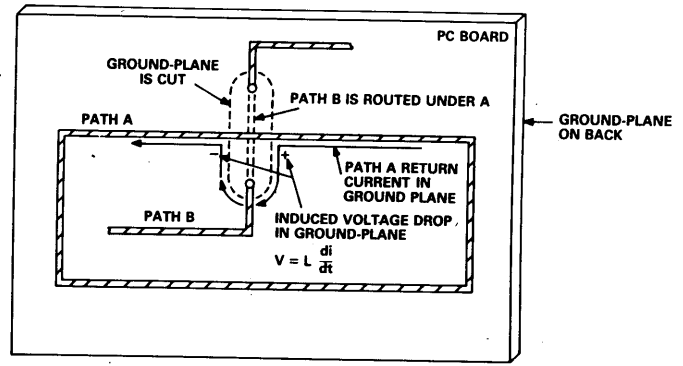


Figure 11. Typical PC layout problem, with paths crossing.