4-Lane 4-Port PCI Express® Switch

89HPES4T4
Data Sheet
Advance Information*

Device Overview

The 89HPES4T4 is a member of IDT's PRECISE™ family of PCI Express switching solutions. The PES4T4 is a 4-lane, 4-port peripheral chip that performs PCI Express Base switching. It provides connectivity and switching functions between a PCI Express upstream port and up to four downstream ports and supports switching between downstream ports.

Features

- High Performance PCI Express Switch
  - *Four 2.5 Gbps PCI Express lanes*
  - *Four switch ports*
  - *x1 Upstream port*
  - *Three x1 Downstream ports*
  - *Low latency cut-through switch architecture*
  - *Support for Max payload sizes up to 256 bytes*
  - *One virtual channel*
  - *Eight traffic classes*
  - *PCI Express Base Specification Revision 1.1 compliant*
- Flexible Architecture with Numerous Configuration Options
  - *Automatic lane reversal on all ports*
  - *Automatic polarity inversion on all lanes*
  - *Ability to load device configuration from serial EEPROM*
- Legacy Support
  - *PCI compatible INTx emulation*
  - *Bus locking*
- Highly Integrated Solution
  - *Requires no external components*
  - *Incorporates on-chip internal memory for packet buffering and queueing*
  - *Integrates four 2.5 Gbps embedded SerDes with 8B/10B encoder/decoder (no separate transceivers needed)*
- Reliability, Availability, and Serviceability (RAS) Features
  - *Internal end-to-end parity protection on all TLPs ensures data integrity even in systems that do not implement end-to-end CRC (ECRC)*
  - *Supports ECRC and Advanced Error Reporting*
  - *Supports PCI Express Native Hot-Plug, Hot-Swap capable I/O*
  - *Compatible with Hot-Plug I/O expanders used on PC mother-boards*
- Power Management
  - *Utilizes advanced low-power design techniques to achieve low typical power consumption*
  - *Supports PCI Power Management Interface specification (PCI-PM 1.2)*
  - *Unused SerDes are disabled.*
  - *Supports Advanced Configuration and Power Interface Specification, Revision 2.0 (ACPI) supporting active link state*
- Testability and Debug Features
  - *Built in Pseudo-Random Bit Stream (PRBS) generator*
  - *Numerous SerDes test modes*
  - *Ability to bypass link training and force any link into any mode*
  - *Provides statistics and performance counters*

Advance Information

Block Diagram

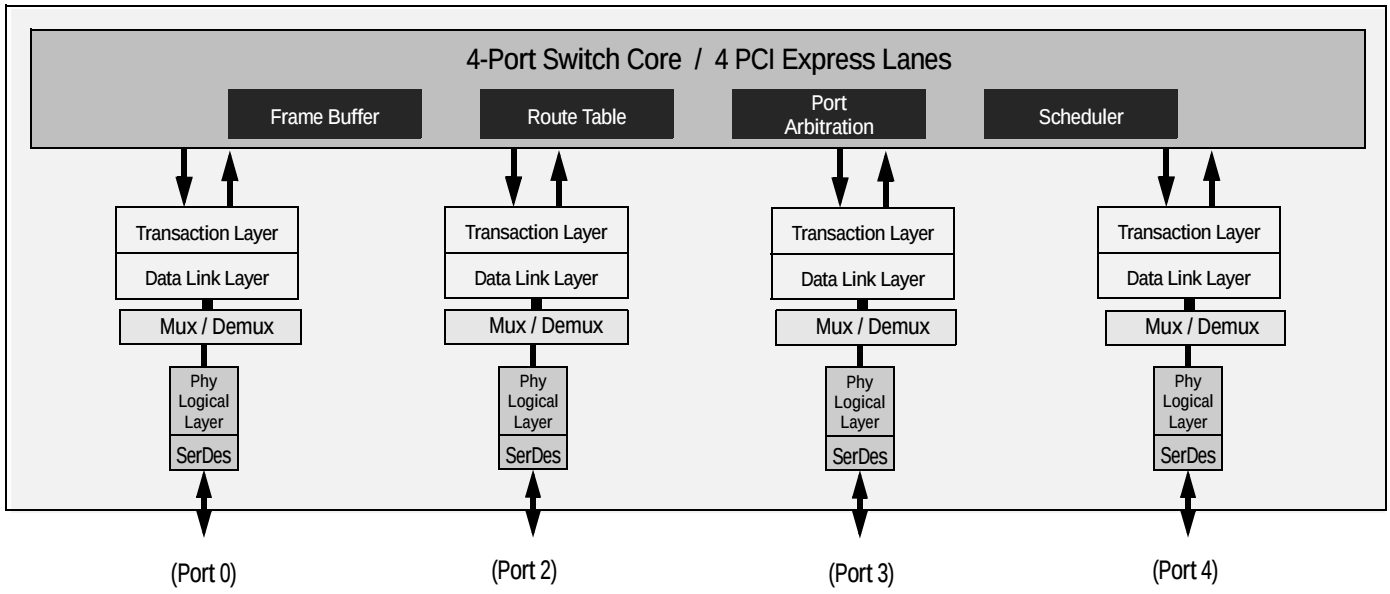


Figure 1 Internal Block Diagram

*Notice: The information in this document is subject to change without notice

- 5 General Purpose Input/Output Pins
  - *Each pin may be individually configured as an input or output*
  - *Each pin may be individually configured as an interrupt input*
  - *Each pin has a selectable alternate function*
- Packaged in a 13mm x 13mm 144-ball BGA with 1mm ball spacing

Product Description

Utilizing standard PCI Express interconnect, the PES4T4 provides the most efficient fan-out solution for applications requiring x1 connectivity, low latency, and simple board layout with a minimum number of board layers. Each lane provides 2.5 Gbps of bandwidth in both directions and is fully compliant with PCI Express Base specification 1.1.

The PES4T4 is based on a flexible and efficient layered architecture. The PCI Express layer consists of SerDes, Physical, Data Link and Transaction layers in compliance with PCI Express Base specification Revision 1.1. The PES4T4 can operate either as a store and forward or cut-through switch and is designed to switch memory and I/O transactions. It supports eight Traffic Classes (TCs) and one Virtual Channel (VC) with sophisticated resource management to allow efficient switching for applications requiring additional narrow port connectivity and also some high-end connectivity.

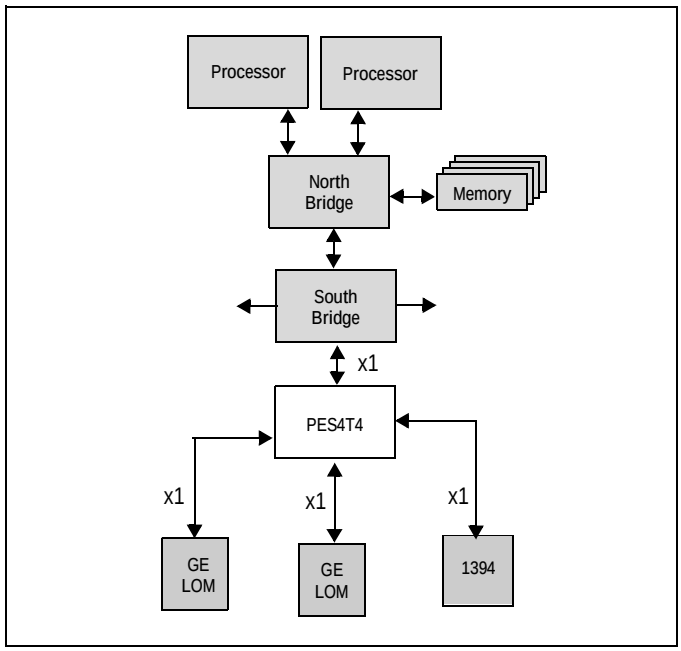


Figure 2 I/O Expansion Application

SMBus Interface

The PES4T4 contains an SMBus master interface. This master interface allows the default configuration register values of the PES4T4 to be overridden following a reset with values programmed in an external serial EEPROM. The master interface is also used by an external Hot-Plug I/O expander. Two pins make up the SMBus master interface. These pins consist of an SMBus clock pin and an SMBus data pin.

Hot-Plug Interface

The PES4T4 supports PCI Express Hot-Plug on each downstream port. To reduce the number of pins required on the device, the PES4T4 utilizes an external I/O expander, such as that used on PC motherboards, connected to the SMBus master interface. Following reset and configuration, whenever the state of a Hot-Plug output needs to be modified, the PES4T4 generates an SMBus transaction to the I/O expander with the new value of all of the outputs. Whenever a Hot-Plug input changes, the I/O expander generates an interrupt which is received on the IOEXPINTN input pin (alternate function of GPIO) of the PES4T4. In response to an I/O expander interrupt, the PES4T4 generates an SMBus transaction to read the state of all of the Hot-Plug inputs from the I/O expander.

General Purpose Input/Output

The PES4T4 provides 5 General Purpose Input/Output (GPIO) pins that may be used by the system designer as bit I/O ports. Each GPIO pin may be configured independently as an input or output through software control, and each GPIO pin is shared with another on-chip function. These alternate functions may be enabled via software or serial configuration EEPROM.

Pin Description

The following tables lists the functions of the pins provided on the PES4T4. Some of the functions listed may be multiplexed onto the same pin. The active polarity of a signal is defined using a suffix. Signals ending with an “N” are defined as being active, or asserted, when at a logic zero (low) level. All other signals (including clocks, buses, and select lines) will be interpreted as being active, or asserted, when at a logic one (high) level.

Signal	Type	Name/Description
PE0RP[0] PE0RN[0]	I	PCI Express Port 0 Serial Data Receive. Differential PCI Express receive pair for port 0.
PE0TP[0] PE0TN[0]	O	PCI Express Port 0 Serial Data Transmit. Differential PCI Express transmit pair for port 0.
PE2RP[0] PE2RN[0]	I	PCI Express Port 2 Serial Data Receive. Differential PCI Express receive pair for port 2.
PE2TP[0] PE2TN[0]	O	PCI Express Port 2 Serial Data Transmit. Differential PCI Express transmit pair for port 2.
PE3RP[0] PE3RN[0]	I	PCI Express Port 3 Serial Data Receive. Differential PCI Express receive pair for port 3.
PE3TP[0] PE3TN[0]	O	PCI Express Port 3 Serial Data Transmit. Differential PCI Express transmit pair for port 3.
PE4RP[0] PE4RN[0]	I	PCI Express Port 4 Serial Data Receive. Differential PCI Express receive pair for port 4.
PE4TP[0] PE4TN[0]	O	PCI Express Port 4 Serial Data Transmit. Differential PCI Express transmit pair for port 4.
PEREFCLKP PEREFCLKN	I	PCI Express Reference Clock. Differential reference clock pair input. This clock is used as the reference clock by on-chip PLLs to generate the clocks required for the system logic and on-chip SerDes.

Table 1 PCI Express Interface Pins

Signal	Type	Name/Description
MSMBCLK	I/O	Master SMBus Clock. This bidirectional signal is used to synchronize transfers on the master SMBus.
MSMBDAT	I/O	Master SMBus Data. This bidirectional signal is used for data on the master SMBus.

Table 2 SMBus Interface Pins

Signal	Type	Name/Description
GPIO[0]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. Alternate function pin name: P2RSTN Alternate function pin type: Output Alternate function: Reset output for downstream port 2
GPIO[1]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. Alternate function pin name: P4RSTN Alternate function pin type: Output Alternate function: Reset output for downstream port 4
GPIO[2]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. Alternate function pin name: IOEXPINTN0 Alternate function pin type: Input Alternate function: I/O Expander interrupt 0 input
GPIO[7]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. Alternate function pin name: GPEN Alternate function pin type: Output Alternate function: General Purpose Event (GPE) output
GPIO[9]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. Alternate function pin name: P3RSTN Alternate function pin type: Output Alternate function: Reset output for downstream port 3

Table 3 General Purpose I/O Pins

Signal	Type	Name/Description
APWRDISN	I	Auxiliary Power Disable Input. When this pin is active, it disables the device from using auxiliary power supply.
CCLKDS	I	Common Clock Downstream. The assertion of this pin indicates that all downstream ports are using the same clock source as that provided to downstream devices.This bit is used as the initial value of the Slot Clock Configuration bit in all of the Link Status Registers for downstream ports. The value may be override by modifying the SCLK bit in the downstream port's PCIELSTS register.
CCLKUS	I	Common Clock Upstream. The assertion of this pin indicates that the upstream port is using the same clock source as the upstream device. This bit is used as the initial value of the Slot Clock Configuration bit in the Link Status Register for the upstream port. The value may be overridden by modifying the SCLK bit in the PA_PCIELSTS register.
PERSTN	I	Fundamental Reset. Assertion of this signal resets all logic inside the PES4T4 and initiates a PCI Express fundamental reset.

Table 4 System Pins (Part 1 of 2)

Signal	Type	Name/Description
RSTHALT	I	**Reset Halt.** When this signal is asserted during a PCI Express fundamental reset, the PES4T4 executes the reset procedure and remains in a reset state with the Master SMBus active. This allows software to read and write registers internal to the device before normal device operation begins. The device exits the reset state when the RSTHALT bit is cleared in the PA_SWCTL register by the SMBus master.
SWMODE[2:0]	I	**Switch Mode.** These configuration pins determine the PES4T4 switch operating mode. 0x0 - Normal switch mode 0x1 - Normal switch mode with Serial EEPROM initialization 0x2 - through 0xF Reserved
WAKEN	I/O	**Wake Input/Output.** The WAKEN signal is an input or output. The WAKEN signal input/output selection can be made through WAKEDIR bit setting in the WAKEUPCNTL register.

Table 4 System Pins (Part 2 of 2)

Signal	Type	Name/Description
JTAG_TCK	I	**JTAG Clock.** This is an input test clock used to clock the shifting of data into or out of the boundary scan logic or JTAG Controller. JTAG_TCK is independent of the system clock with a nominal 50% duty cycle.
JTAG_TDI	I	**JTAG Data Input.** This is the serial data input to the boundary scan logic or JTAG Controller.
JTAG_TDO	O	**JTAG Data Output.** This is the serial data shifted out from the boundary scan logic or JTAG Controller. When no data is being shifted out, this signal is tri-stated.
JTAG_TMS	I	**JTAG Mode.** The value on this signal controls the test mode select of the boundary scan logic or JTAG Controller.
JTAG_TRST_N	I	**JTAG Reset.** This active low signal asynchronously resets the boundary scan logic and JTAG TAP Controller. An external pull-up on the board is recommended to meet the JTAG specification in cases where the tester can access this signal. However, for systems running in functional mode, one of the following should occur: 1) actively drive this signal low with control logic 2) statically drive this signal low with an external pull-down on the board

Table 5 Test Pins

Signal	Type	Name/Description
V_{DD}CORE	I	**Core VDD.** Power supply for core logic.
V_{DD}I/O	I	**I/O VDD.** LVTTL I/O buffer power supply.
V_{DD}PE	I	**PCI Express Digital Power.** PCI Express digital power used by the digital power of the SerDes.
V_{DD}APE	I	**PCI Express Analog Power.** PCI Express analog power used by the PLL and bias generator.
V_{TT}PE	I	**PCI Express Termination Power.**
V_{SS}	I	**Ground.**

Table 6 Power and Ground Pins

Pin Characteristics

Note: Some input pads of the PES4T4 do not contain internal pull-ups or pull-downs. Unused inputs should be tied off to appropriate levels. This is especially critical for unused control signal inputs which, if left floating, could adversely affect operation. Also, any input pin left floating can cause a slight increase in power consumption.

Function	Pin Name	Type	Buffer	I/O Type	Internal Resistor	Notes
PCI Express Interface	PE0RN[0]	I	CML	Serial Link		
	PE0RP[0]	I				
	PE0TN[0]	O				
	PE0TP[0]	O				
	PE2RN[0]	I				
	PE2RP[0]	I				
	PE2TN[0]	O				
	PE2TP[0]	O				
	PE3RN[0]	I				
	PE3RP[0]	I				
	PE3TN[0]	O				
	PE3TP[0]	O				
	PE4RN[0]	I				
	PE4RP[0]	I				
	PE4TN[0]	O				
	PE4TP[0]	O				
	PEREFCLKN	I	LVPECL/ CML	Diff. Clock Input		Refer toTable 8
	PEREFCLKP	I				
SMBus	MSMBCLK	I/O	LVTTL	STI[1]		
	MSMBDAT	I/O		STI		
General Purpose I/O	GPIO[9,7,2:0]	I/O	LVTTL	High Drive	pull-up	
System Pins	APWRDISN	I	LVTTL	Input	pull-down	
	CCLKDS	I			pull-up	
	CCLKUS	I			pull-up	
	PERSTN	I				
	RSTHALT	I			pull-down	
	SWMODE[2:0]	I			pull-down	
	WAKEN	I/O			open-drain	
EJTAG / JTAG	JTAG_TCK	I	LVTTL	STI	pull-up	
	JTAG_TDI	I		STI	pull-up	
	JTAG_TDO	O				
	JTAG_TMS	I		STI	pull-up	
	JTAG_TRST_N	I		STI	pull-up	

Table 7 Pin Characteristics

1. Schmitt Trigger Input (STI).

Advance Information

Logic Diagram — PES4T4

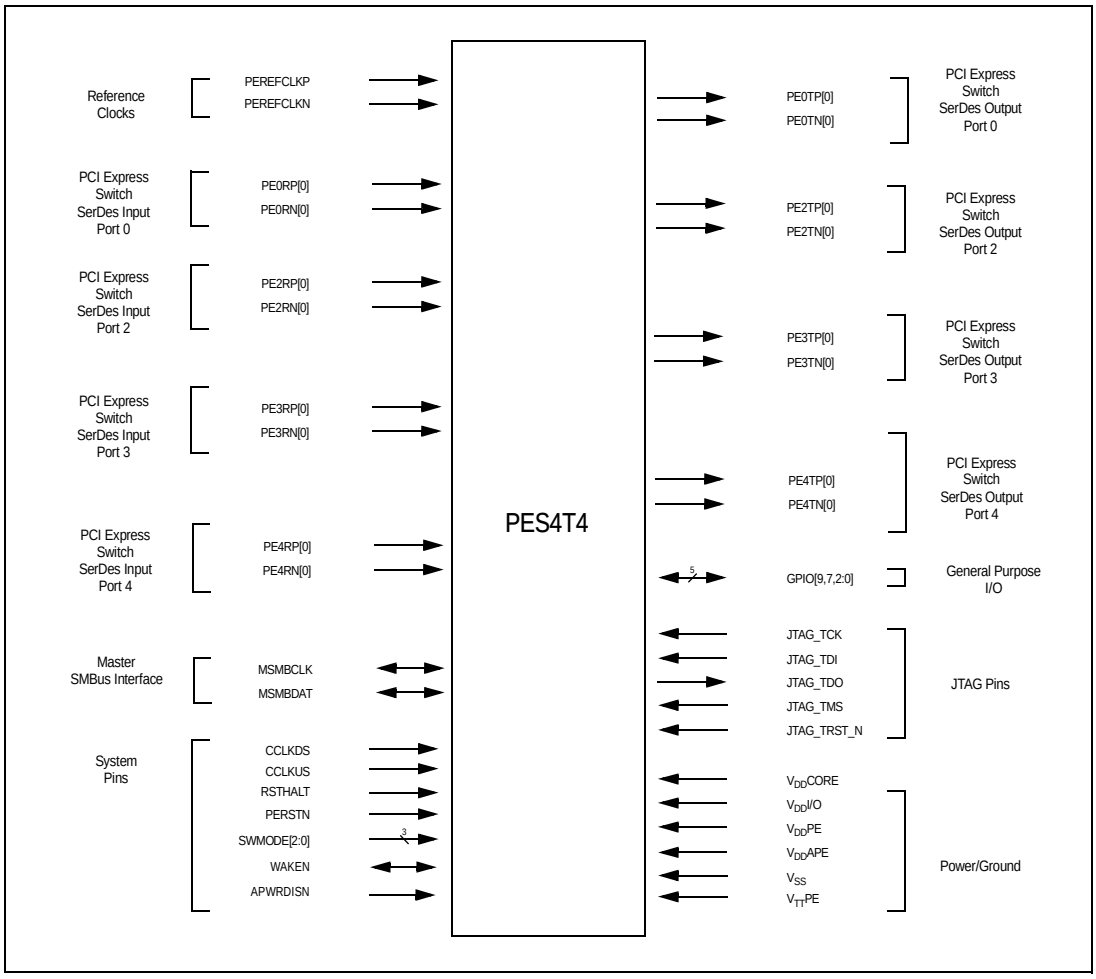


Figure 3 PES4T4 Logic Diagram

System Clock Parameters

Values based on systems running at recommended supply voltages and operating temperatures, as shown in Tables 12 and 13.

Parameter	Description	Min	Typical	Max	Unit
PEREFCLK					
$Refclk_{FREQ}$	Input reference clock frequency range	100		125[1]	MHz
$Refclk_{DC}$[2]	Duty cycle of input clock	40	50	60	%
T_R, T_F	Rise/Fall time of input clocks			0.2*RCUI	RCUI[3]
V_{SW}	Differential input voltage swing[4]	0.6		1.6	V
T_{jitter}	Input clock jitter (cycle-to-cycle)			125	ps

Table 8 Input Clock Requirements

1. The input clock frequency is 100 MHz.
2. ClkIn must be AC coupled. Use 0.01 — 0.1 µF ceramic capacitors.
3. RCUI (Reference Clock Unit Interval) refers to the reference clock period.
4. AC coupling required.

AC Timing Characteristics

Parameter	Description	Min	Typical	Max	Units
PCIe Transmit					
$T_{TX-RISE}$, $T_{TX-FALL}$	Rise / Fall time of TxP, TxN outputs	80		110[1]	ps
UI	Unit Interval	399.88	400	400.12	ps
$T_{TX-MAX-JITTER}$	Transmitter Total Jitter (peak-to-peak)			0.25[2]	UI
T_{TX-EYE}	Minimum Tx Eye Width (1 - $T_{TX-MAX-JITTER}$)	0.75			UI
$T_{TX-EYE-MEDIAN-to-MAX-JITTER}$	Maximum time between the jitter median and maximum deviation from the median			0.15	UI
$L_{TLAT-10}$	Transmitter data latency (for n=10)	9		11	bits
$L_{TLAT-20}$	Transmitter data latency (for n=20)	9		11	bits
$T_{TX-SKEW}$	Transmitter data skew between any 2 lanes		500	1300	ps
$T_{TX-IDLE-SET-TO-IDLE}$	Maximum time to transition to a valid electrical idle after sending an Electrical Idle ordered set		4	6	ns
T_{EIExit}	Time to exit Electrical Idle (L0s) state into L0		12	16	ns
T_{BTEn}	Time from asserting Beacon TxEn to beacon being transmitted on the lane		30	80	ns
$T_{RxDetectEn}$	Pulse width of RxDetectEn input	9.8	10	10.2	ns
$T_{RxDetect}$	RxDetectEn falling edge to RxDetect delay		1	2	ns
PCIe Receive					
$L_{RLAT-10}$	Recover data latency for n=10	28		29	bits
$L_{RLAT-20}$	Recover data latency for n=20	49		60	bits

Table 9 PCIe AC Timing Characteristics (Part 1 of 2)

Parameter	Description	Min	Typical	Max	Units
$T_{RX-SKEW}$	Receiver data skew between any 2 lanes			20	ns
T_{BDDly}	Beacon-Activity on channel to detection of Beacon[3]			200	µs
$T_{RX-IDLE\_ENTER}$	Delay from detection of Electrical Idle condition on the channel to assertion of TxIdleDetect output		10	20	ns
$T_{RX-IDLE\_EXIT}$	Delay from detection of L0s to L0 transition to de-assertion of TxIdleDetect output		5	10	ns
$T_{RX-MAX-JITTER}$	Receiver total jitter tolerance			0.65	UI
T_{RX-EYE}	Minimum Receiver Eye Width	0.35			UI
$T_{RX-EYE-MEDIAN-to-MAX\ JITTER}$	Maximum time between jitter median and max deviation from median			0.325	UI

Table 9 PCIe AC Timing Characteristics (Part 2 of 2)

1. As measured between 20% and 80% points. Will depend on package characteristics.
2. Measured using PCI Express Compliance Pattern.
3. This is a function of beacon frequency.

Signal	Symbol	Reference Edge	Min	Max	Unit	Timing Diagram Reference
GPIO						
GPIO[9,7,2:0][1]	Tpw_13b[2]	None	50	—	ns	See Figure 4.

Table 10 GPIO AC Timing Characteristics

1. GPIO signals must meet the setup and hold times if they are synchronous or the minimum pulse width if they are asynchronous.
2. The values for this symbol were determined by calculation, not by testing.

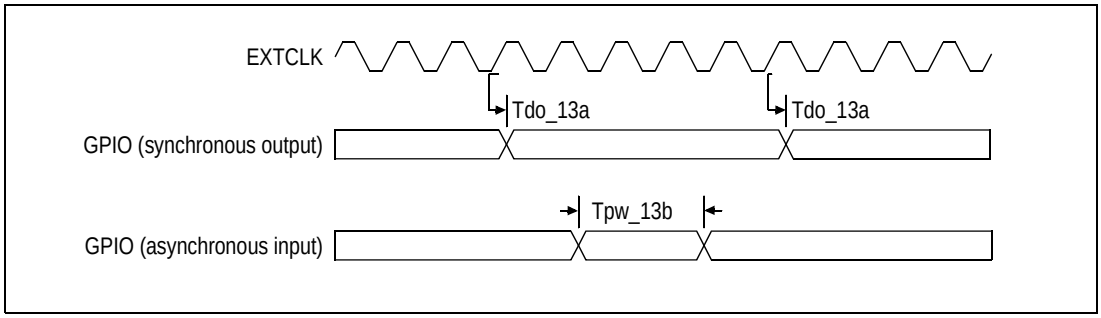


Figure 4 GPIO AC Timing Waveform

Signal	Symbol	Reference Edge	Min	Max	Unit	Timing Diagram Reference
JTAG						
JTAG_TCK	Tper_16a	none	25.0	50.0	ns	See Figure 5.
	Thigh_16a, Tlow_16a		10.0	25.0	ns	
JTAG_TMS[1], JTAG_TDI	Tsu_16b	JTAG_TCK rising	2.4	—	ns	
	Thld_16b		1.0	—	ns	
JTAG_TDO	Tdo_16c	JTAG_TCK falling	—	11.3	ns	
	Tdz_16c[2]		—	11.3	ns	
JTAG_TRST_N	Tpw_16d[2]	none	25.0	—	ns	

Table 11 JTAG AC Timing Characteristics

1. The JTAG specification, IEEE 1149.1, recommends that JTAG_TMS should be held at 1 while the signal applied at JTAG_TRST_N changes from 0 to 1. Otherwise, a race may occur if JTAG_TRST_N is deasserted (going from low to high) on a rising edge of JTAG_TCK when JTAG_TMS is low, because the TAP controller might go to either the Run-Test/Idle state or stay in the Test-Logic-Reset state.

2. The values for this symbol were determined by calculation, not by testing.

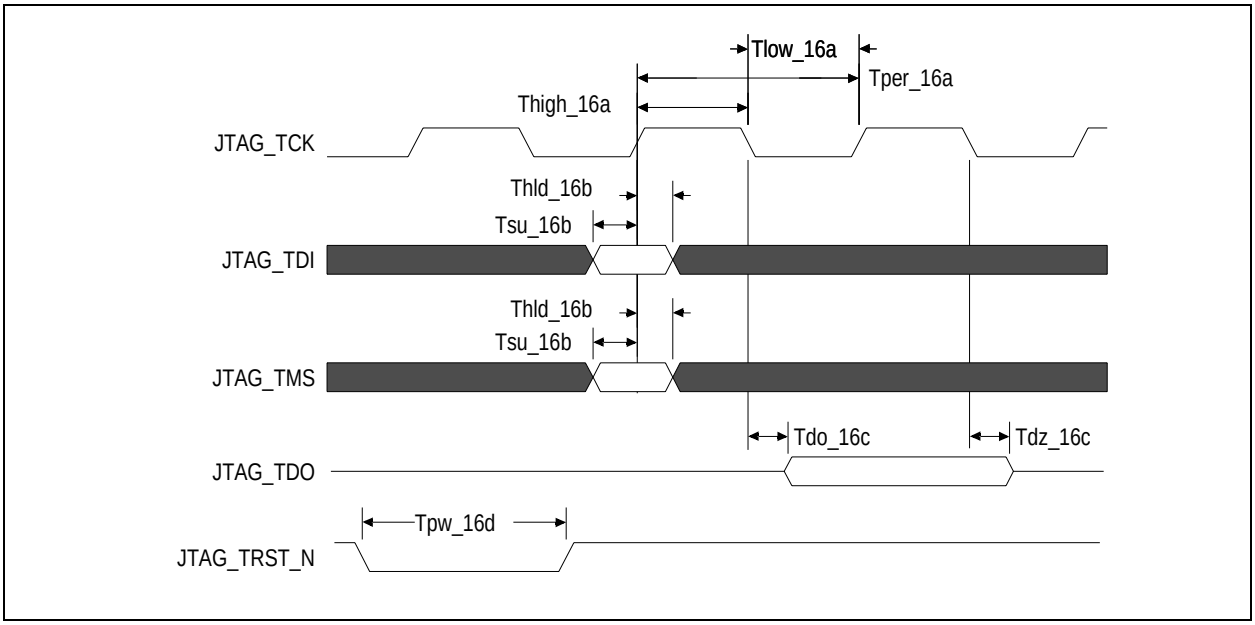


Figure 5 JTAG AC Timing Waveform

Recommended Operating Supply Voltages

Symbol	Parameter	Minimum	Typical	Maximum	Unit
V_{DD}CORE	Internal logic supply	0.9	1.0	1.1	V
V_{DD}I/O	I/O supply except for SerDes LVPECL/CML	3.135	3.3	3.465	V
V_{DD}PE	PCI Express Digital Power	0.9	1.0	1.1	V
V_{DD}APE	PCI Express Analog Power	0.9	1.0	1.1	V
V_{TT}PE	PCI Express Serial Data Transmit Termination Voltage	1.425	1.5	1.575	V
V_{SS}	Common ground	0	0	0	V

Table 12 PES4T4 Operating Voltages

Power-Up/Power-Down Sequence

This section describes the sequence in which various voltages must be applied to the part during power-up to ensure proper functionality. For the PES4T4, the power-up sequence must be as follows:

1. V_{DD}I/O — 3.3V
2. V_{DD}Core, V_{DD}PE, V_{DD}APE — 1.0V
3. V_{TT}PE — 1.5V

When powering up, each voltage level must ramp and stabilize prior to applying the next voltage in the sequence to ensure internal latch-up issues are avoided. There are no maximum time limitations in ramping to valid power levels.

The power-down sequence must be in the reverse order of the power-up sequence.

Recommended Operating Temperature

Grade	Temperature
Commercial	0°C to +70°C Ambient

Table 13 PES4T4 Operating Temperatures

Power Consumption

Parameter		Typ.	Max.	Unit	Conditions
I_{DD}I/O		tbd	tbd	mA	$T_{ambient}$ = 25^{o}C Max. values use the maximum voltages listed in Table 12. Typical values use the typical voltages listed in that table.
I_{DD}Core	Normal mode	tbd	tbd	mA	
	Standby mode[1]	tbd	—	mA	
I_{DD}PE,		tbd	tbd	mA	
I_{DD} APE		tbd	tbd	mA	
I_{TT}PE		tbd	tbd	mA	
Power Dissipation	Normal mode	tbd	tbd	W	
	Standby mode[1]	tbd	—	W	

Table 14 PES4T4 Power Consumption

1. All ports in D1 state.

DC Electrical Characteristics

Values based on systems running at recommended supply voltages, as shown in Table 12.

Note: See Table 7, Pin Characteristics, for a complete I/O listing.

I/O Type	Parameter	Description	Min[1]	Typ[1]	Max[1]	Unit	Conditions
Serial Link	PCIe Transmit						
	$V_{TX-DIFFp-p}$	Differential peak-to-peak output voltage	800		1200	mV	
	$V_{TX-DE-RATIO}$	De-emphasized differential output voltage	-3		-4	dB	
	$V_{TX-DC-CM}$	DC Common mode voltage	-0.1	1	3.7	V	
	$V_{TX-CM-ACP}$	RMS AC peak common mode output voltage			20	mV	
	$V_{TX-CM-DC-active-idle-delta}$	Abs delta of DC common mode voltage between L0 and idle			100	mV	
	$V_{TX-CM-DC-line-delta}$	Abs delta of DC common mode voltage between D+ and D-			25	mV	
	$V_{TX-Idle-DiffP}$	Electrical idle diff peak output			20	mV	
	$V_{TX-RCV-Detect}$	Voltage change during receiver detection			600	mV	
	$RL_{TX-DIFF}$	Transmitter Differential Return loss	12			dB	
	RL_{TX-CM}	Transmitter Common Mode Return loss	6			dB	
	$Z_{TX-DEFF-DC}$	DC Differential TX impedance	80	100	120	Ω	
	Z_{OSE}	Single ended TX Impedance	40	50	60	Ω	
	Transmitter Eye Diagram	TX Eye Height (De-emphasized bits)	505	650		mV	
	Transmitter Eye Diagram	TX Eye Height (Transition bits)	800	950		mV	
	PCIe Receive						
	$V_{RX-DIFFp-p}$	Differential input voltage (peak-to-peak)	175		1200	mV	
	$V_{RX-CM-AC}$	Receiver common-mode voltage for AC coupling			150	mV	
	$RL_{RX-DIFF}$	Receiver Differential Return Loss	15			dB	
	RL_{RX-CM}	Receiver Common Mode Return Loss	6			dB	
	$Z_{RX-DIFF-DC}$	Differential input impedance (DC)	80	100	120	Ω	
	$Z_{RX-COMM-DC}$	Single-ended input impedance	40	50	60	Ω	
	$Z_{RX-COMM-HIGH-Z-DC}$	Powered down input common mode impedance (DC)	200k	350k		Ω	
	$V_{RX-IDLE-DET-DIFFp-p}$	Electrical idle detect threshold	65		175	mV	
PCIe REFCLK							
	C_{IN}	Input Capacitance	1.5	—		pF	

Table 15 DC Electrical Characteristics (Part 1 of 2)

I/O Type	Parameter	Description	Min[1]	Typ[1]	Max[1]	Unit	Conditions
Other I/Os							
LOW Drive Output	I_{OL}		—	2.5	—	mA	V_{OL} = 0.4v
	I_{OH}		—	-5.5	—	mA	V_{OH} = 1.5V
High Drive Output	I_{OL}		—	12.0	—	mA	V_{OL} = 0.4v
	I_{OH}		—	-20.0	—	mA	V_{OH} = 1.5V
Schmitt Trigger Input (STI)	V_{IL}		-0.3	—	0.8	V	—
	V_{IH}		2.0	—	V_{DD}I/O + 0.5	V	—
Input	V_{IL}		-0.3	—	0.8	V	—
	V_{IH}		2.0	—	V_{DD}I/O + 0.5	V	—
Capacitance	C_{IN}		—	—	8.5	pF	—
Leakage	Inputs		—	—	± 10	µA	V_{DD}I/O (max)
	$I/O_{LEAK\ W/O}$ Pull-ups/downs		—	—	± 10	µA	V_{DD}I/O (max)
	$I/O_{LEAK\ WITH}$ Pull-ups/downs		—	—	± 80	µA	V_{DD}I/O (max)

Table 15 DC Electrical Characteristics (Part 2 of 2)

1. Minimum, Typical, and Maximum values meet the requirements under PCI Specification 1.1.

Package Pinout — 144-BGA Signal Pinout for PES4T4

The following table lists the pin numbers and signal names for the PES4T4 device.

Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt
A1	V_{SS}		C11	V_{DD}CORE		F9	V_{DD}CORE		J7	V_{SS}	
A2	V_{DD}I/O		C12	V_{SS}		F10	V_{DD}I/O		J8	V_{DD}CORE	
A3	APWRDISN		D1	JTAG_TDO		F11	V_{DD}I/O		J9	V_{SS}	
A4	V_{TT}PE		D2	MSMBCLK		F12	GPIO_01	1	J10	V_{SS}	
A5	V_{TT}PE		D3	V_{DD}CORE		G1	V_{SS}		J11	V_{DD}I/O	
A6	PE0TP00		D4	V_{SS}		G2	JTAG_TRST_N		J12	GPIO_09	1
A7	V_{DD}PE		D5	V_{SS}		G3	V_{SS}		K1	V_{SS}	
A8	PE0RP00		D6	V_{SS}		G4	V_{DD}CORE		K2	V_{DD}CORE	
A9	V_{DD}I/O		D7	V_{DD}CORE		G5	V_{SS}		K3	V_{DD}I/O	
A10	SWMODE_0		D8	V_{SS}		G6	V_{DD}CORE		K4	V_{DD}CORE	
A11	SWMODE_1		D9	V_{SS}		G7	V_{SS}		K5	V_{DD}PE	
A12	V_{SS}		D10	V_{SS}		G8	V_{DD}CORE		K6	V_{SS}	
B1	V_{DD}CORE		D11	PERSTN		G9	V_{SS}		K7	V_{DD}PE	
B2	WAKEN		D12	RSTHALT		G10	V_{DD}CORE		K8	V_{SS}	
B3	CCLKUS		E1	JTAG_TDI		G11	V_{SS}		K9	V_{DD}CORE	
B4	V_{DD}PE		E2	MSMBDAT		G12	GPIO_02	1	K10	V_{DD}I/O	
B5	V_{DD}PE		E3	V_{DD}I/O		H1	PEREFCLKP		K11	V_{SS}	
B6	PE0TN00		E4	V_{DD}CORE		H2	V_{DD}I/O		K12	V_{SS}	
B7	V_{DD}PE		E5	V_{SS}		H3	V_{DD}APE		L1	PE2RN00	
B8	PE0RN00		E6	V_{DD}CORE		H4	V_{SS}		L2	V_{SS}	
B9	CCLKDS		E7	V_{SS}		H5	V_{SS}		L3	PE2TP00	
B10	SWMODE_2		E8	V_{SS}		H6	V_{SS}		L4	V_{SS}	
B11	V_{SS}		E9	V_{SS}		H7	V_{DD}CORE		L5	PE3TN00	
B12	V_{SS}		E10	V_{DD}CORE		H8	V_{SS}		L6	V_{DD}APE	
C1	JTAG_TMS		E11	V_{SS}		H9	V_{SS}		L7	PE3RN00	
C2	V_{SS}		E12	GPIO_00	1	H10	V_{DD}CORE		L8	V_{TT}PE	
C3	V_{SS}		F1	JTAG_TCK		H11	V_{SS}		L9	PE4RP00	
C4	V_{DD}CORE		F2	V_{DD}I/O		H12	GPIO_07	1	L10	V_{SS}	
C5	V_{DD}APE		F3	V_{DD}CORE		J1	PEREFCLKN		L11	PE4TN00	
C6	V_{DD}APE		F4	V_{SS}		J2	V_{SS}		L12	V_{DD}CORE	
C7	V_{SS}		F5	V_{DD}CORE		J3	V_{SS}		M1	PE2RP00	
C8	V_{DD}CORE		F6	V_{SS}		J4	V_{SS}		M2	V_{SS}	
C9	V_{DD}CORE		F7	V_{DD}CORE		J5	V_{SS}		M3	PE2TN00	
C10	V_{SS}		F8	V_{SS}		J6	V_{DD}CORE		M4	V_{TT}PE	

Table 16 PES4T4 144-pin Signal Pin-Out (Part 1 of 2)

Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt
M5	PE3TP00		M7	PE3RP00		M9	PE4RN00		M11	PE4TP00	
M6	V_{SS}		M8	V_{DD}APE		M10	V_{SS}		M12	V_{SS}	

Table 16 PES4T4 144-pin Signal Pin-Out (Part 2 of 2)

Alternate Signal Functions

Pin	GPIO	Alternate
E12	GPIO_00	P2RSTN
F12	GPIO_01	P4RSTN
G12	GPIO_02	IOEXPINTN0
H12	GPIO_07	GPEN
J12	GPIO_09	P3RSTN

Table 17 PES4T4 Alternate Signal Functions

Power Pins

V_{DD}Core	V_{DD}Core	V_{DD}I/O	V_{DD}PE	V_{DD}APE	V_{TT}PE
B1	F9	A2	A7	C5	A4
C4	G4	A9	B4	C6	A5
C8	G6	E3	B5	H3	L8
C9	G8	F2	B7	L6	M4
C11	G10	F10	K5	M8	
D3	H7	F11	K7		
D7	H10	H2			
E4	J6	J11			
E6	J8	K3			
E10	K2	K10			
F3	K4				
F5	K9				
F7	L12				

Table 18 PES4T4 Power Pins

Ground Pins

V_{ss}	V_{ss}	V_{ss}	V_{ss}
A1	D10	G11	K1
A12	E5	H4	K6
B11	E7	H5	K8
B12	E8	H6	K11
C2	E9	H8	K12
C3	E11	H9	L2
C7	F4	H11	L4
C10	F6	J2	L10
C12	F8	J3	M2
D4	G1	J4	M6
D5	G3	J5	M10
D6	G5	J7	M12
D8	G7	J9	
D9	G9	J10	

Table 19 PES4T4 Ground Pins

Signals Listed Alphabetically

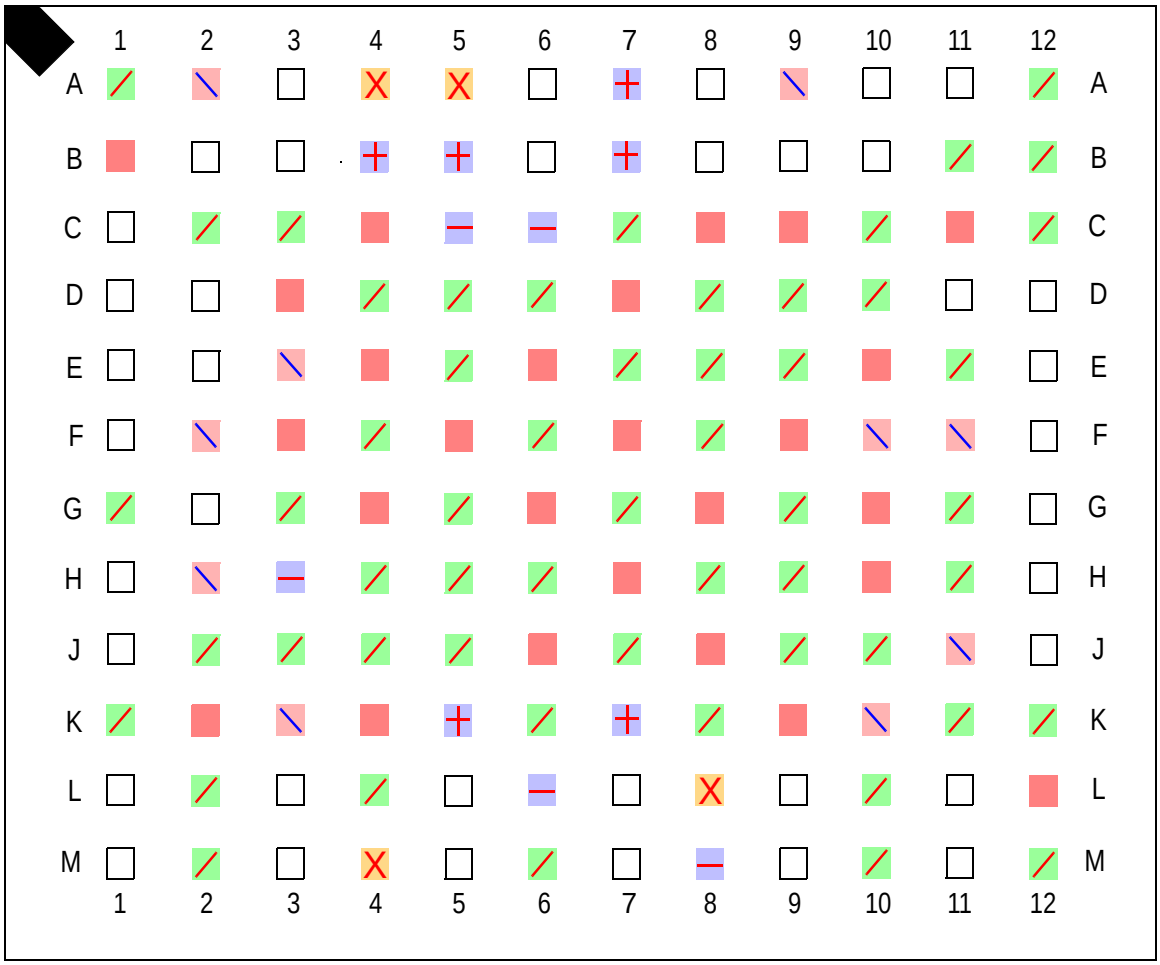
Signal Name	I/O Type	Location	Signal Category
APWRDISN	I	A3	System
CCLKDS	I	B9	
CCLKUS	I	B3	
GPIO_00	I/O	E12	General Purpose Input/Output
GPIO_01	I/O	F12	
GPIO_02	I/O	G12	
GPIO_07	I/O	H12	
GPIO_09	I/O	J12	
JTAG_TCK	I	F1	JTAG
JTAG_TDI	I	E1	
JTAG_TDO	I	D1	
JTAG-TMS	O	C1	
JTAG-TRST_N	I	G2	
MSMBCLK	I/O	D2	SMBus
MSMBDAT	I/O	E2	

Table 20 89PES4T4 Alphabetical Signal List (Part 1 of 2)

Signal Name	I/O Type	Location	Signal Category
PE0RN00	I	B8	PCI Express
PE0RP00	I	A8	
PE0TN00	O	B6	
PE0TP00	O	A6	
PE2RN00	I	L1	
PE2RP00	I	M1	
PE2TN00	O	M3	
PE2TP00	O	L3	
PE3RN00	I	L7	
PE3RP00	I	M7	
PE3TN00	O	L5	
PE3TP00	O	M5	
PE4RN00	I	M9	
PE4RP00	I	L9	
PE4TN00	O	L11	
PE4TP00	O	M11	
PEREFCLKN	I	J1	
PEREFCLKP	I	H1	
PERSTN	I	D11	System
RSTHALT	I	D12	System
SWMODE_0	I	A10	
SWMODE_1	I	A11	
SWMODE_2	I	B10	
WAKEN	I/O	B2	
V_{DD}CORE, V_{DD}APE, V_{DD}I/O, V_{DD}PE, V_{TT}PE	See Table 18 for a listing of power pins.		
V_{SS}	See Table 19 for a listing of ground pins.		

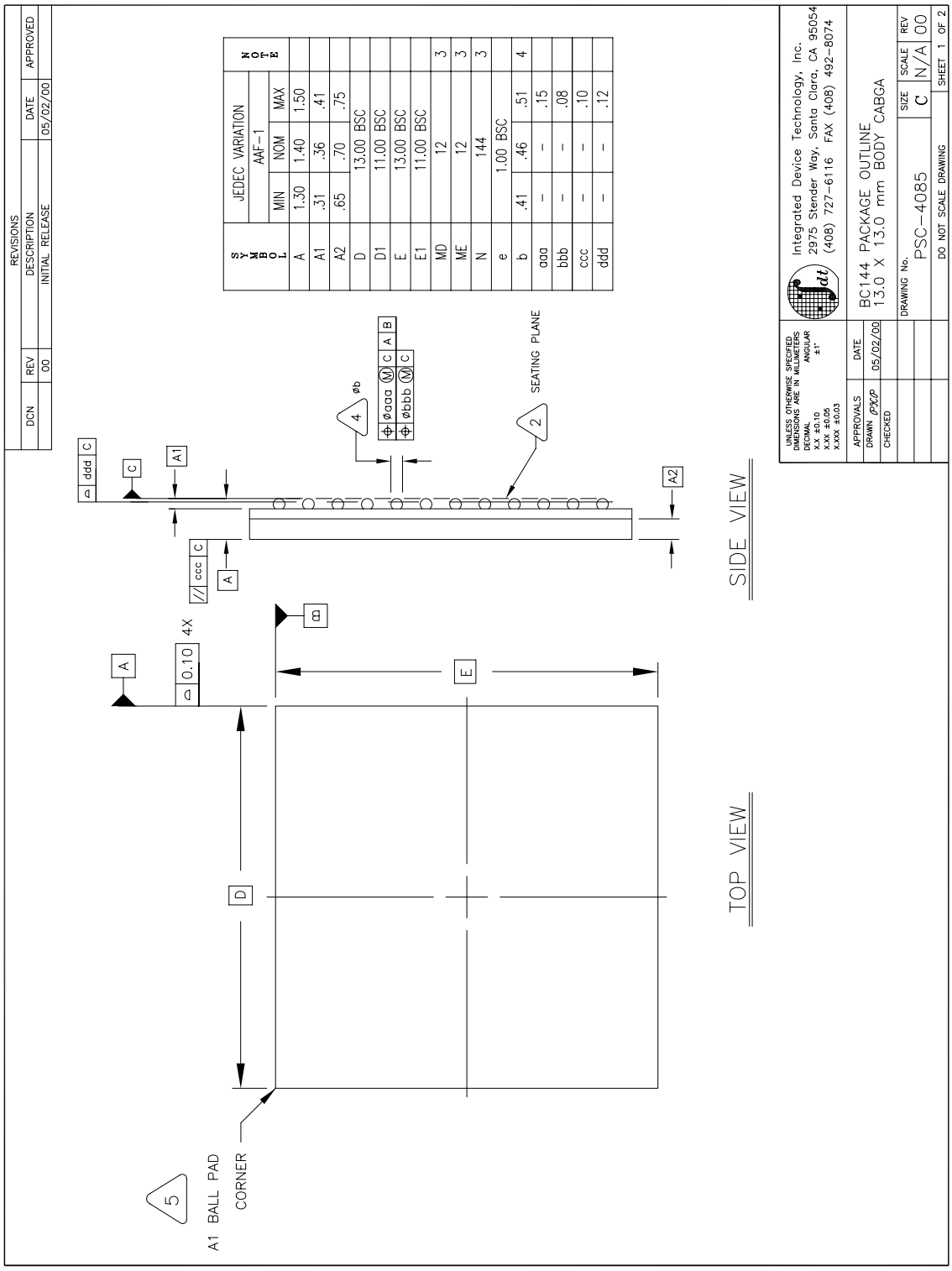
Table 20 89PES4T4 Alphabetical Signal List (Part 2 of 2)

PES4T4 Pinout — Top View



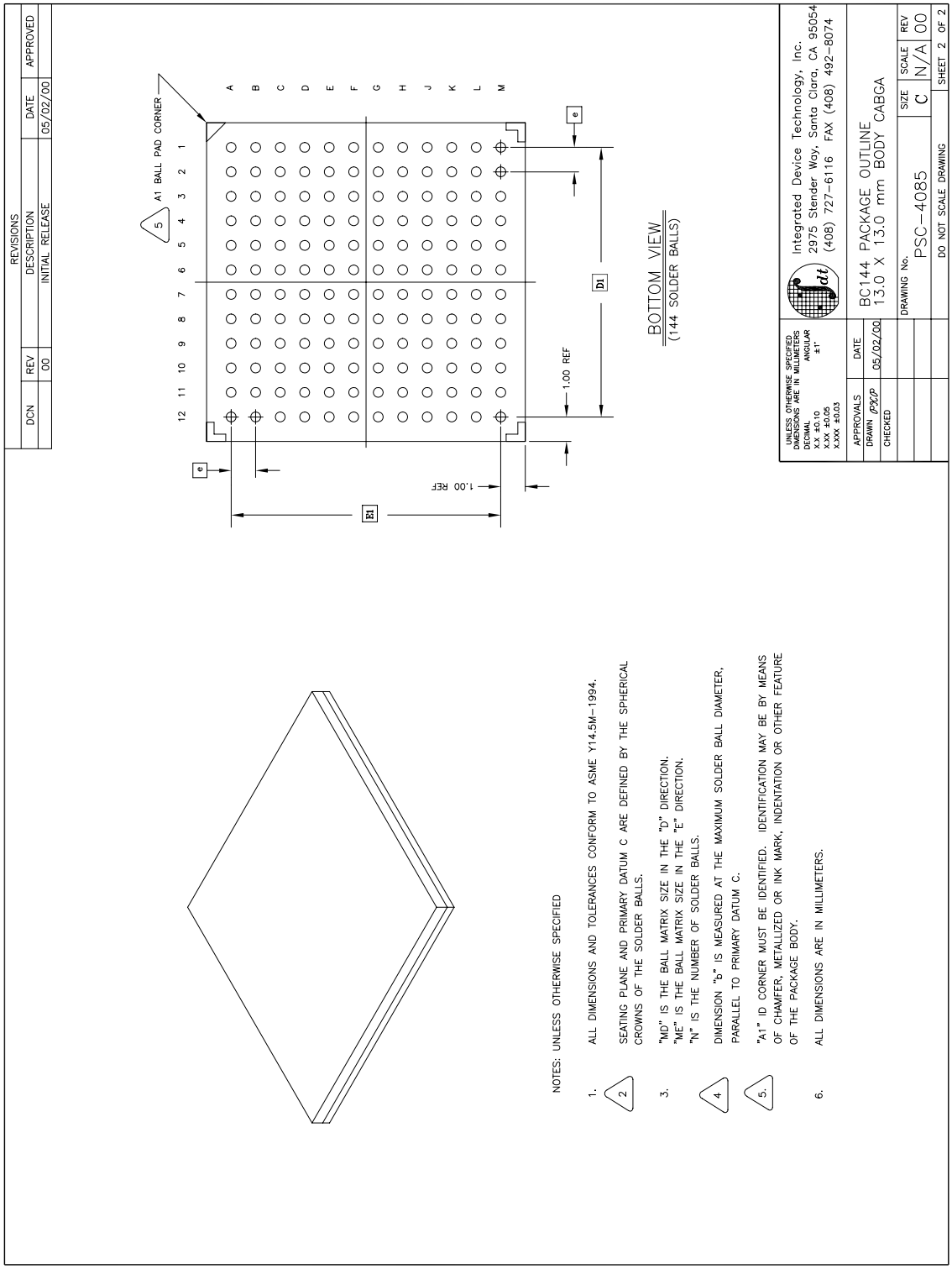
Advance Information

PES4T4 Package Drawing — 144-Pin BC144/BCG144



Advance Information

PES4T4 Package Drawing — Page Two



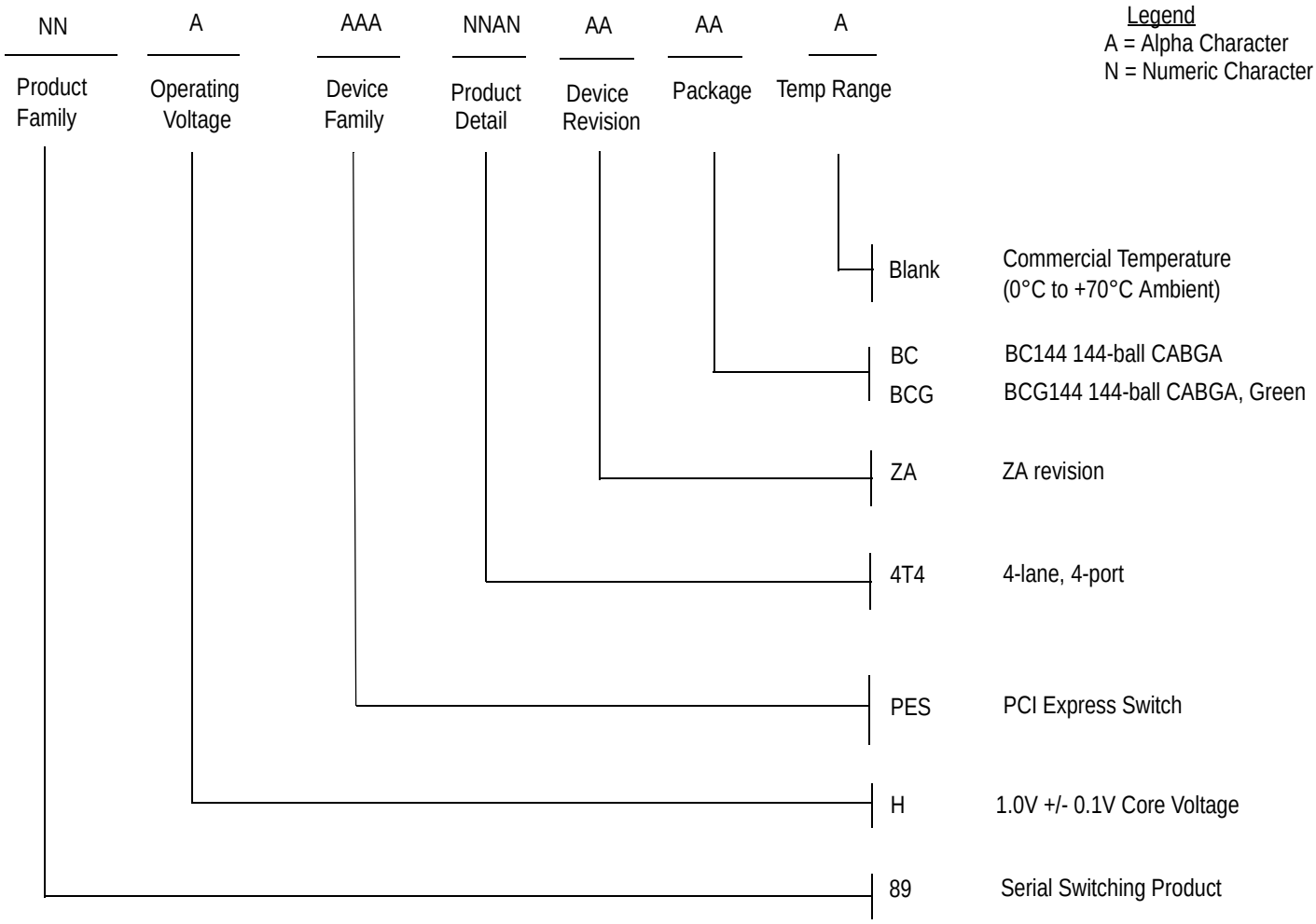
Advance Information

Revision History

August 16, 2007: Initial publication of advanced data sheet.

September 7, 2007: Added Power-Up/Power Down Sequence.

Ordering Information



Advance Information

Valid Combinations

89HPES4T4ZABC	144-pin BC144 package, Commercial Temperature
89HPES4T4ZABCG	144-pin Green BC144 package, Commercial Temperature

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