P54/74FCT861AT/BT/CT—P54/74FCT863AT/BT/CT P54/74FCT864AT/BT/CT BUS INTERFACE TRANSCEIVERS

FEATURES

- Function, Pinout and Drive Compatible with the FCT, F Logic and AM29861/863/864
- FCT-C speed at 5.1ns max. (Com'l) FCT-B speed at 6.0ns max. (Com'l)
- Reduced V_{OH} (typically = 3.3V) versions of Equivalent FCT functions
- Edge-rate Control Circuitry for Significantly Improved Noise Characteristics
- ESD protection exceeds 2000V
- Power-off disable feature
- Matched Rise and Fall times
- Fully Compatible with TTL Input and Output Logic Levels
- 64 mA Sink Current (Com'l), 32 mA (Mil) 15 mA Source Current (Com'l), 12 mA (Mil)
- Buffered Common Clear and Preset Input
- High Speed Parallel Latches
- Buffered Common Latch Enable Input
- Manufactured in 0.7 micron PACE Technology™

DESCRIPTION

The 'FCT860T bus interface transceivers provide high-performance interface buffering for wide data/address paths or buses carrying parity. The 'FCT861T is a non-inverting, 10-bit transceiver. The 'FCT863Tand 'FCT864T are 9-bit transceivers having NAND-ed output enables for maximum control flexibility. The 'FCT864T is the inverting version of the 'FCT863T.

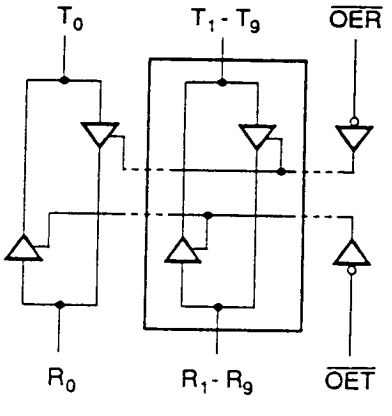
The 'FCT800T high performance interface family is designed for high-capacitance load drive capability while providing low-capacitance bus loading at both inputs and outputs. All inputs have clamp diodes and all outputs are designed for low-capacitance bus loading in the high impedance state.

The 'FCT800T interface family are manufactured using PACE Technology™ which is Performance Advanced CMOS Engineered to use 0.7 micron effective channel lengths giving 400 picosecond loaded* internal gate delays. PACE Technology includes two-level metal and epitaxial substrates. In addition to very high performance and very high density, the technology features latch-up protection, single event upset protection, and is supported by a Class 1 environment volume production facility.

* For a fan-in/fan-out of 4, at 85°C junction temperature and 5.0V.

FUNCTIONAL BLOCK DIAGRAMS

'FCT861T



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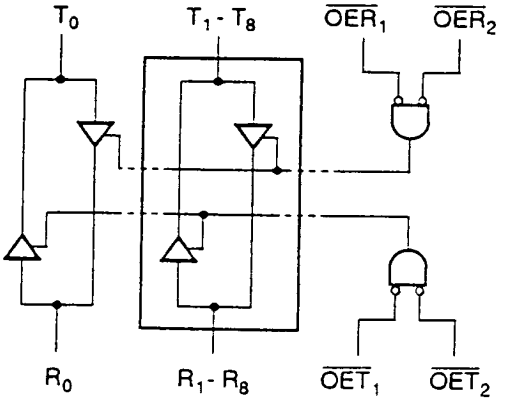
'FCT863T



* 'FCT864T is inverting

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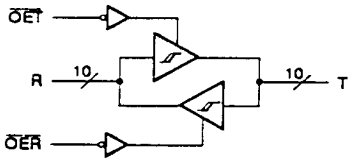
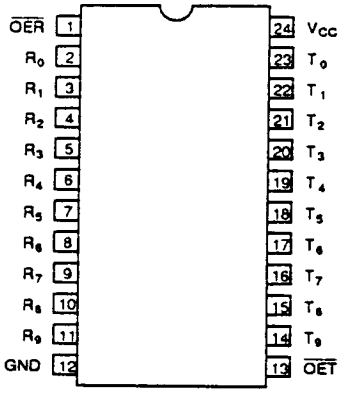
LOGIC SYMBOLS

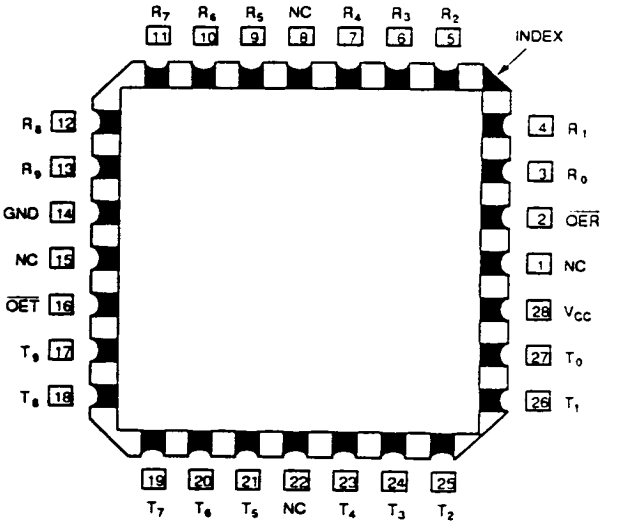
PIN CONFIGURATIONS

'FCT861T 10-BIT TRANSCEIVER





DIP (D4, P4), SOIC (S4)



LCC (L5-1)

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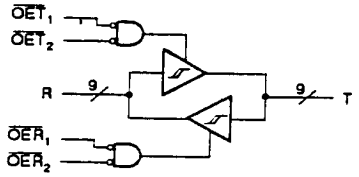
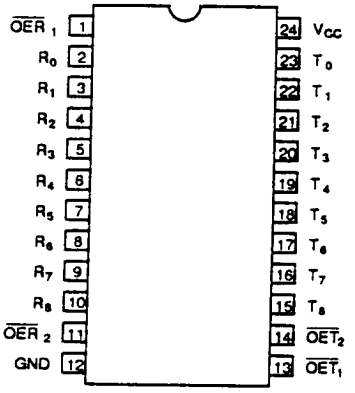
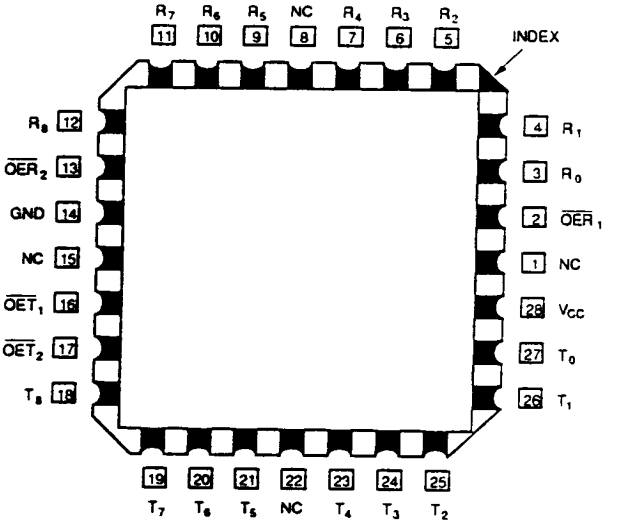
'FCT863T/864T 9-BIT TRANSCEIVER



* 'FCT864T is inverting



DIP (D4, P4), SOIC (S4)



LCC (L5-1)

1720 04

2/13/92 - 3

PIN DESCRIPTION

Name	I/O	Description
'FCT861T		
$\overline{OER}$	I	When LOW in conjunction with $\overline{OET}$ HIGH activates the RECEIVE mode.
$\overline{OET}$	I	When LOW in conjunction with $\overline{OER}$ HIGH activates the TRANSMIT mode.
R_I	I/O	10-bit RECEIVE input/output.
T_I	I/O	10-bit TRANSMIT input/output.
'FCT863T/864T		
$\overline{OER}_I$	I	When LOW in conjunction with $\overline{OET}_I$ HIGH activates the RECEIVE mode.
$\overline{OET}_I$	I	When LOW in conjunction with $\overline{OER}_I$ HIGH activates the TRANSMIT mode.
R_I	I/O	9-bit RECEIVE input/output.
T_I	I/O	9-bit TRANSMIT input/output.

1720 Tbl 01

TRUTH TABLE[1]

'FCT861T/863T (Non-Inverting)

Inputs				Outputs		Function
$\overline{OET}$	$\overline{OER}$	R_I	T_I	R_I	T_I	
L	H	L	N/A	N/A	L	Transmitting
L	H	H	N/A	N/A	H	Transmitting
H	L	N/A	L	L	N/A	Receiving
H	L	N/A	H	H	N/A	Receiving
H	H	X	X	Z	Z	High-Z

1720 Tbl 02

NOTE:

1. H = HIGH, L = LOW, Z = Impedance, X = Don't Care, N/A = Not Applicable.

ABSOLUTE MAXIMUM RATINGS[1,2]

Symbol	Parameter	Value	Unit
T_{STG}	Storage Temperature	–65 to +150	°C
T_A	Ambient Temperature Under Bias	–65 to +135	°C
V_{CC}	V_{CC} Potential to Ground	–0.5 to +7.0	V
P_T	Power Dissipation	0.5	W

1720 Tbl 03

Symbol	Parameter	Value	Unit
I_{OUTPUT}	Current Applied to Output	120	mA
V_{IN}	Input Voltage	–0.5 to +7.0	V
V_{OUT}	Voltage Applied to Output	–0.5 to +7.0	V

1720 Tbl 04

Notes:

1. Operation beyond the limits set forth in the above table may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.
2. Unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.

RECOMMENDED OPERATING CONDITIONS

Free Air Ambient Temperature	Min	Max
Military	–55°C	+125°C
Commercial	0°C	+70°C

1720 Tbl 05

Supply Voltage (V_{CC})	Min	Max
Military	+3.1V	+3.5V
Commercial	+3.1V	+3.5V

1720 Tbl 06

DC ELECTRICAL CHARACTERISTICS (Over recommended operating conditions)

Symbol	Parameter		Min	Typ[1]	Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage		2.0			V		
V_{IL}	Input LOW Voltage				0.8	V		
V_H	Hysteresis			0.35		V		All inputs
V_{IK}	Input Clamp Diode Voltage			–0.7	–1.2	V	MIN	I_{IN} = –18mA
V_{OH}	Output HIGH Voltage	Military	2.4	3.3		V	MIN	I_{OH} = –12mA
		Commercial	2.4	3.3		V	MIN	I_{OH} = –15mA
V_{OL}	Output LOW Voltage	Military		0.3	0.5	V	MIN	I_{OL} = 32mA
		Commercial		0.3	0.5	V	MIN	I_{OL} = 48mA
		Commercial		0.3	0.5	V	MIN	I_{OL} = 64mA
I_I	Input HIGH Current				20	µA	MAX	V_{IN} = V_{CC}
I_{IH}	Input HIGH Current				5	µA	MAX	V_{IN} = 2.7V
I_{IL}	Input LOW Current				–5	µA	MAX	V_{IN} = 0.5V
I_{OZH}	Off State I_{OUT} HIGH-Level Output Current				10	µA	MAX	V_{OUT} = 2.7V
I_{OZL}	Off State I_{OUT} LOW-Level Output Current				–10	µA	MAX	V_{OUT} = 0.5V
I_{OS}	Output Short Circuit Current[2]		–60	–120	–225	mA	MAX	V_{OUT} = 0.0V
I_{OFF}	Power-off Disable				100	µA	0V	V_{OUT} = 4.5V
C_{IN}	Input Capacitance[3]			5	10	pF	MAX	All inputs
C_{OUT}	Output Capacitance[3]			9	12	pF	MAX	All outputs
I_{CC}	Quiescent Power Supply Current			0.2	1.5	mA	MAX	$V_{IN} \leq 0.2V$, $V_{IN} \geq V_{CC}-0.2V$

1720 Tbl 07

Notes:

1. Typical limits are at V_{CC} = 3.3V, T_A = +25°C ambient.
2. Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{os} tests should be performed last.
3. This parameter is guaranteed but not tested.

DC CHARACTERISTICS (Over recommended operating conditions unless otherwise specified.)

Symbol	Parameter	Typ[1]	Max	Units	Conditions
ΔI_{CC}	Quiescent Power Supply Current (TTL inputs)	0.2	2.0	mA	V_{CC} = MAX, V_{IN} = 2.7V[2], f_1 = 0, Outputs Open
I_{CCD}	Dynamic Power Supply Current[3]	0.15	0.25	mA/ mHz	V_{CC} = MAX, One Input Toggling, 50% Duty Cycle, Outputs Open, $\overline{OER}$ or $\overline{OET}$ = GND, $V_{IN} \le 0.2V$ or $V_{IN} \ge V_{CC} - 0.2V$
I_C	Total Power Supply Current[5]	1.7	4.0	mA	V_{CC} = MAX, 50% Duty Cycle, Outputs Open, One Bit Toggling at f_1 = 10MHz, $\overline{OER}$ or $\overline{OET}$ = GND, $V_{IN} \le 0.2V$ or $V_{IN} \ge V_{CC} - 0.2V$
		2.0	5.0	mA	V_{CC} = MAX, 50% Duty Cycle, Outputs Open, One Bit Toggling at f_1 = 10mHz, $\overline{OER}$ or $\overline{OET}$ = GND, V_{IN} = 2.7V or V_{IN} = GND
		3.2	6.5[4]	mA	V_{CC} = MAX, 50% Duty Cycle, Outputs Open, Eight Bits Toggling at f_1 = 2.5MHz, $\overline{OER}$ or $\overline{OET}$ = GND, $V_{IN} \le 0.2V$ or $V_{IN} \ge V_{CC} - 0.2V$
		5.2	14.5[4]	mA	V_{CC} = MAX, 50% Duty Cycle, Outputs Open, Eight Bits Toggling at f_1 = 2.5MHz, $\overline{OER}$ or $\overline{OET}$ = GND, V_{IN} = 2.7V or V_{IN} = GND

1720 Tbl 08

Notes:

1. Typical values are at V_{CC} = 3.3V, +25°C ambient.
2. Per TTL driven input (V_{IN} = 2.7V); all other inputs at V_{CC} or GND.
3. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
4. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
5. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD}(f_0/2 + f_1 N_1)$
   I_{CC} = Quiescent Current with CMOS input levels
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 2.7V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_0 = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_1 = Input Frequency
   N_1 = Number of Inputs at f_1
   All currents are in milliamps and all frequencies are in megahertz.

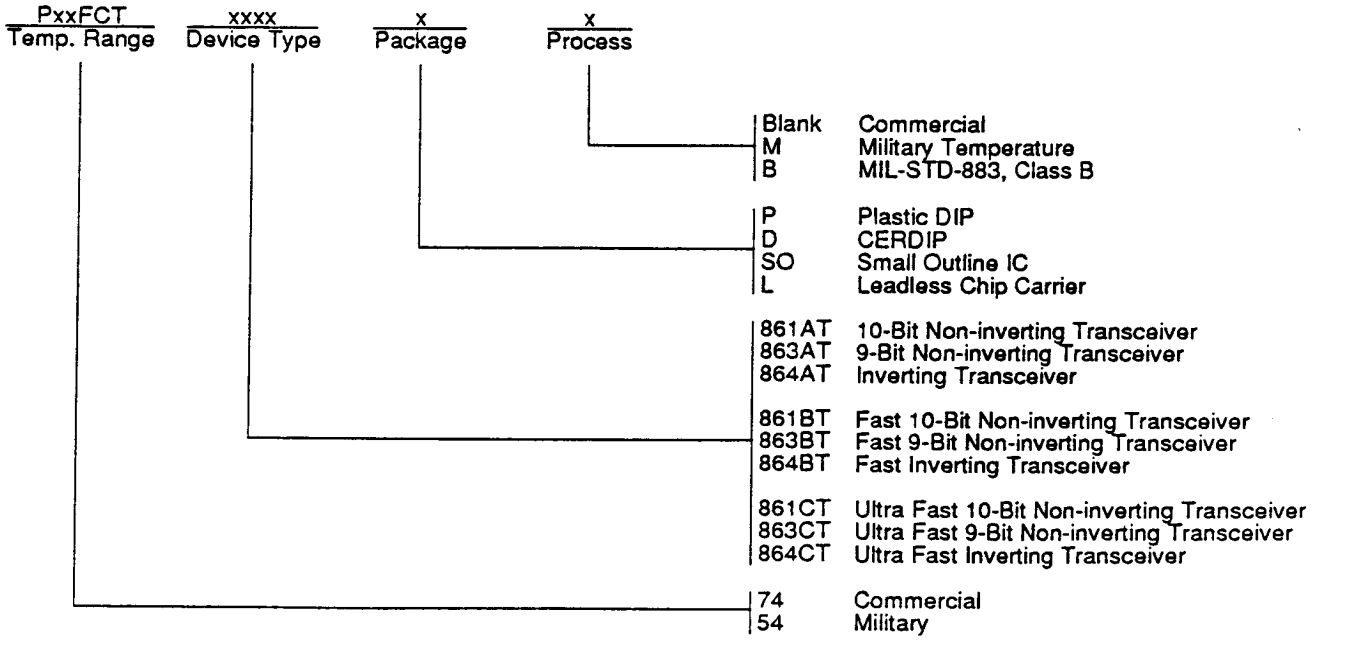
SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Sym.	Parameter	Test Conditions[1]	FCT861AT/863AT/864AT				FCT861BT/863BT/864BT				FCT861CT/863CT/864CT				Units
			MIL		COM'L		MIL		COM'L		MIL		COM'L		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
t_{PLH} t_{PHL}	Propagation Delay R_I to T_I or T_I to R_I 'FCT861T/863T	C_L = 50pF R_L = 500Ω	—	9.0	—	8.0	—	6.5	—	6.0	2.0	5.6	2.0	5.1	ns
		C_L = 300pF[3] R_L = 500Ω	—	17.0	—	15.0	—	14.0	—	13.0	4.0	13.0	4.0	12.0	ns
t_{PLH} t_{PHL}	Propagation Delay R_I to T_I or T_I to R_I 'FCT864T	C_L = 50pF R_L = 500Ω	—	9.0	—	7.5	—	6.5	—	5.5	2.0	5.3	2.0	4.7	ns
		C_L = 300pF[3] R_L = 500Ω	—	16.0	—	14.0	—	14.0	—	13.0	4.0	12.5	4.0	11.5	ns
t_{PZH} t_{PZL}	Output Enable Time $\overline{OET}$ to T_I or $\overline{OER}$ to R_I	C_L = 50pF R_L = 500Ω	—	13.0	—	12.0	—	9.0	—	8.0	2.0	7.6	2.0	6.8	ns
		C_L = 300pF[3] R_L = 500Ω	—	22.0	—	20.0	—	16.0	—	15.0	4.0	15.0	4.0	14.0	ns
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OET}$ to T_I or $\overline{OER}$ to R_I	C_L = 5pF[3] R_L = 500Ω	—	9.0	—	9.0	—	7.0	—	6.0	1.5	6.1	1.5	5.1	ns
		C_L = 50pF R_L = 500Ω	—	10.0	—	10.0	—	8.0	—	7.0	2.0	6.6	2.0	5.6	ns

1720 Tbl 09

Notes:
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. This parameters are guaranteed but not tested.

ORDERING INFORMATION



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