P/Active™ High Performance GTL/ECL Local Termination Network

Features

- Designed especially for Pentium Pro and RISC-based computers/servers
- Provides high speed bus termination
- Reduces ground bounce with center ground pin placement
- Terminates 22 lines in a QSOP package
- Saves board space and reduces assembly cost

Applications

- Pentium Pro servers
- Pentium Pro desk top systems
- GTL, ECL terminator for embedded processor busses

Refer to AP-201 Termination Application Note and AP-203 GTL+ Termination Application Note for further information.

Product Description

CAMD's P/Active RG GTL+ Local Bus Terminator is ideal for Pentium Pro and related high speed bus termination applications where a resistor approach is deemed suitable. This device also meets the high-speed bus termination demands of microprocessors like Motorola's PowerPC, DEC's Alpha, Sun's SPARC, and SGI's MIPs processor, as well as other high performance RISC processors for embedded control applications.

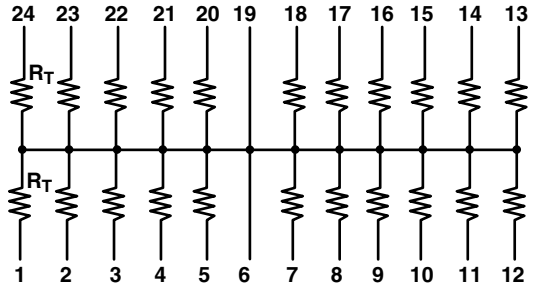
The PACRG offers 22 terminations per package and meets all related Intel specifications for Pentium Pro termination requirements. Four popular values are available for a variety of bus termination applications and line impedance requirements: 47, 50, 56 and 68 ohms.

The P/Active RG Termination Networks provide high performance, high reliability, and low cost through manufacturing efficiency. The termination resistor elements are fabricated using proprietary state-of-the-art thin film technology. CAMD's highly integrated solution is silicon-based and has the same enhanced reliability characteristics as today's microprocessor products. The thin film resistors have very high stability over a wide temperature range, over applied voltage, and over life. In addition, the QSOP industry standard packaging is manufacturing-friendly and yields the high reliability of other semiconductor components. The P/Active RG Pentium Pro Termination Network provides a complete 300 point termination solution in only 14 QSOP packages.

STANDARD SPECIFICATIONS	
Absolute Tolerance (R)	±5%
Operating Temperature Range	0°C to 70°C
Power Rating/Resistor	100mW
Storage Temperature	–65°C to 150°C
Package Power Rating	1.00w, Max

STANDARD VALUES	
R (Ω)	**Code**
47	470
50	500
56	560
68	680

PIN DIAGRAM



STANDARD PART ORDERING INFORMATION					
	Package		Ordering Part Number		
R Code	**Pins**	**Style**	**Tubes**	**Tape & Reel**	**Part Marking**
470(1%)	24	QSOP	PAC470RGQ/T	PAC470RGQ/R	PAC470RGQ
500(1%)	24	QSOP	PAC500RGQ/T	PAC500RGQ/R	PAC500RGQ
560(1%)	24	QSOP	PAC560RGQ/T	PAC560RGQ/R	PAC560RGQ
680(1%)	24	QSOP	PAC680RGQ/T	PAC680RGQ/R	PAC680RGQ

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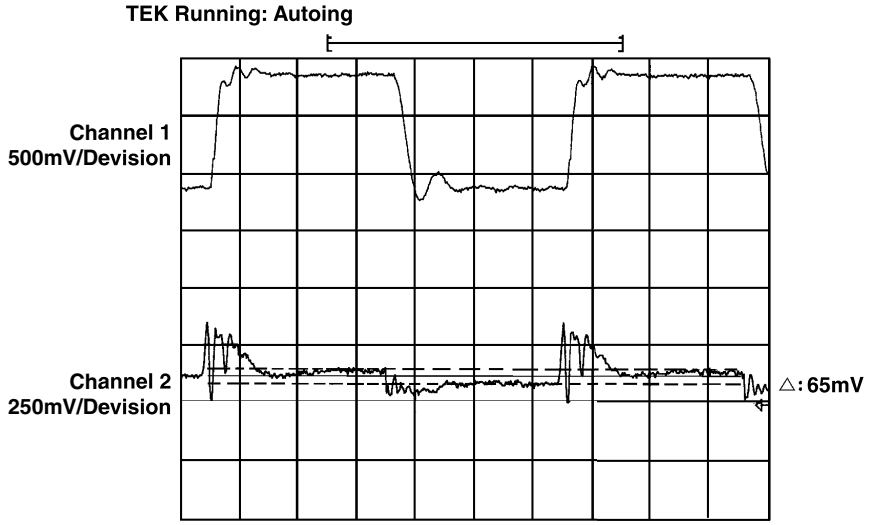
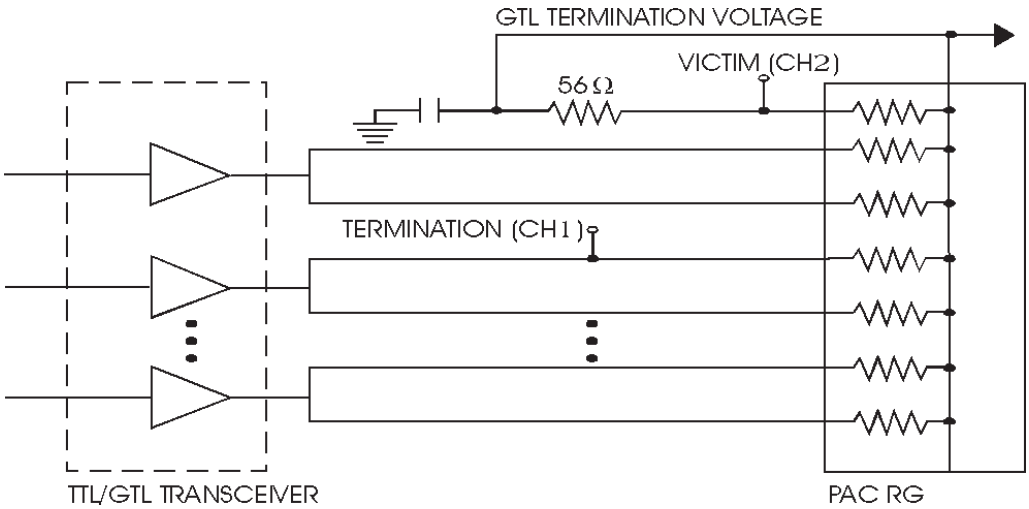
Signal at Termination and Victim Line (TA=25^{O}C) (See Test Circuit)

Channel 1 (500mV/division) Termination Signal, Channel 2 (250mV/division) Victim Voltage. The victim voltage crosstalk measures 65mV in the critical areas around the system clock. The system clock occurs approximately 4ns before each data transition. The horizontal dashed lines are 65mV apart. The time scale is 5.0ns/division. The signal voltage rise and fall times have been adjusted at the driver to conform to Intel specifications.) Measurements made using Tektronix TDS820 6 GHz Digitizing Oscilloscope with P6207 FET Probes.



Test Circuit Block Diagram



Test Circuit