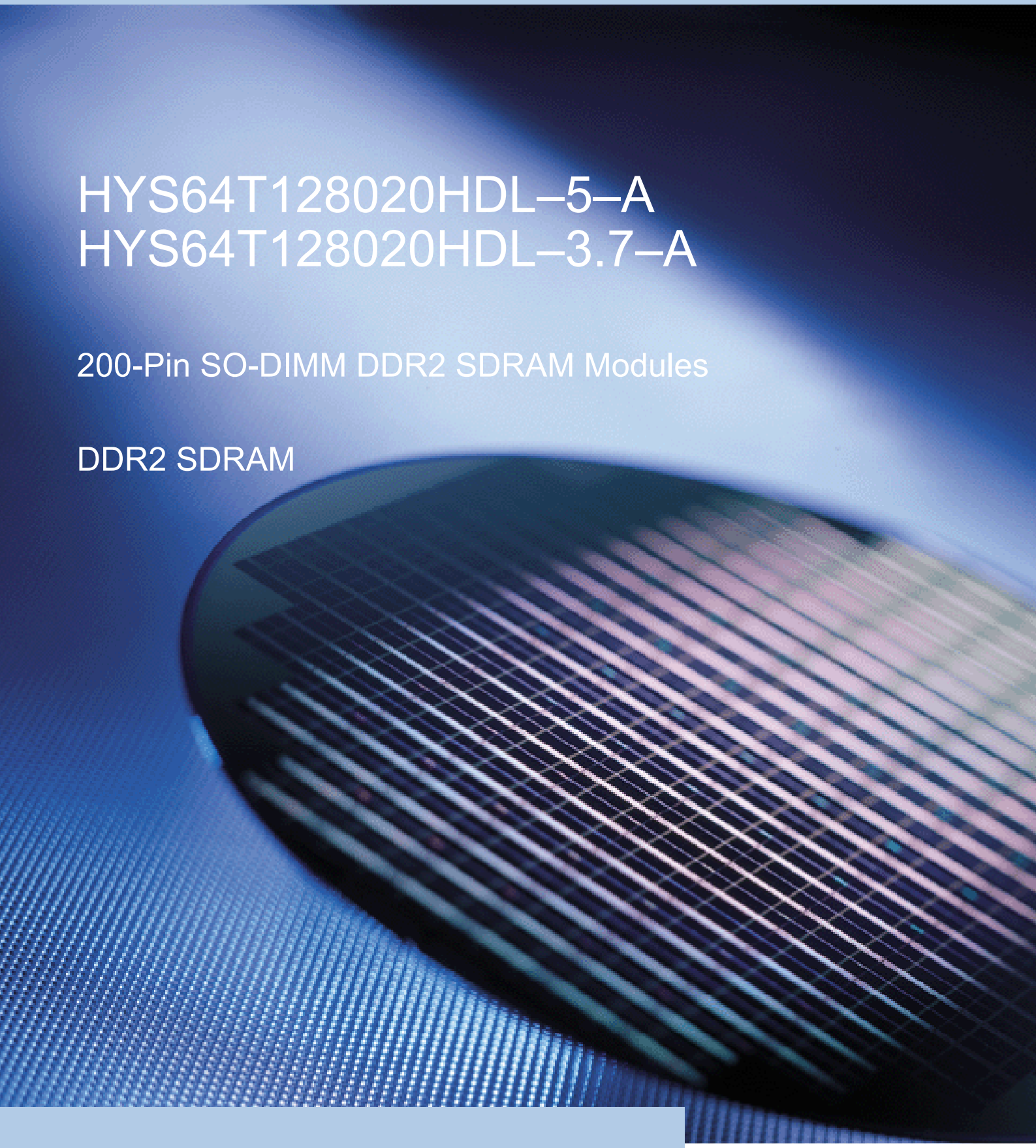
HYS64T128020HDL–5–A
HYS64T128020HDL–3.7–A

200-Pin SO-DIMM DDR2 SDRAM Modules

DDR2 SDRAM



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Page	Subjects (major changes since last revision)
18,**19**	adjusted low power I_{DD} values

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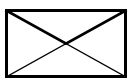

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1 Overview

This chapter gives an overview of the 200-Pin SO-DIMM DDR2 SDRAM Modules product family and describes its main characteristics.

1.1 Features

- 200-pin PC2-4200 and PC2-3200 DDR2 SDRAM memory modules for use as main memory when installed in systems such as mobile personal computers.
- 128M × 64 module organization, and 64M × 16 chip organization
- JEDEC standard Double-Data-Rate-Two Synchronous DRAMs (DDR2 SDRAM) with a single + 1.8 V (± 0.1 V) power supply
- Built with 1 Gb DDR2 SDRAMs in P-TFBGA-92 chipsize packages
- Programmable CAS Latencies (3, 4 and 5), Burst Length (8 & 4) and Burst Type
- Burst Refresh, Distributed Refresh and Self Refresh
- All inputs and outputs SSTL_18 compatible
- OCD (Off-Chip Driver Impedance Adjustment) and ODT (On-Die Termination)
- Serial Presence Detect with E^2PROM
- SO-DIMM Dimensions (nominal): 30 mm high, 67.6 mm wide
- Based on JEDEC standard reference layouts Raw Card “A”
- RoHS Compliant Products[1)]

Table 1 Performance

Product Type Speed Code			–3.7	–5	Units
Speed Grade			PC2–4200 4–4–4	PC2–3200 3–3–3	—
max. Clock Frequency	@CL5	f_{CK5}	266	200	MHz
	@CL4	f_{CK4}	266	200	MHz
	@CL3	f_{CK3}	200	200	MHz
min. RAS-CAS-Delay		t_{RCD}	15	15	ns
min. Row Pre charge Time		t_{RP}	15	15	ns
min. Row Active Time		t_{RAS}	45	40	ns
min. Row Cycle Time		t_{RC}	60	55	ns

1.2 Description

The INFINEON HYS64T128020HDL–[3.7/5]–A module family are low profile SO-DIMM modules with 30,0 mm height based on DDR2 technology. DIMMs are available as non-ECC modules in 128M × 64 (1GB)organisation and density, intended for mounting into 200 pin connector sockets.

The memory array is designed with 1Gb Double Data Rate (DDR2) Synchronous DRAMs for Non-ECC applications. Decoupling capacitors are mounted on the PCB board. The DIMMs feature serial presence detect based on a serial E^2PROM device using the 2-pin I^2C protocol. The first 128 bytes are programmed with configuration data and the second 128 bytes are available to the customer.

1)RoHS Compliant Product: Restriction of the use of certain hazardous substances (RoHS) in electrical and electronic equipment as defined in the directive 2002/95/EC issued by the European Parliament and of the Council of 27 January 2003. These substances include mercury, lead, cadmium, hexavalent chromium, polybrominated biphenyls and polybrominated biphenyl ethers.

Table 2 Ordering Information

Product Type	Compliance Code	Description	SDRAM Technology
PC2–3200			green Product
HYS64T128020HDL-5-A	1GB 2R×16 PC2–3200S–333–11–A0	2 ranks, Non-ECC	1 Gbit (×16)
PC2–4200			
HYS64T128020HDL–3.7–A	1GB 2R×16 PC2–4200S–444–11–A0	2 ranks, Non-ECC	1 Gbit (×16)

Note:

1. *All part numbers end with a place code, designating the silicon die revision. Example: HYS64T128020HDL–3.7–A, indicating Rev. "A" dies are used for DDR2 SDRAM components. For all INFINEON DDR2 module and component nomenclature see section 8 of this data sheet.*
2. *The Compliance Code is printed on the module label and describes the speed grade, f.e. "PC2-4200S-444-11-A", where 4200S means Small Outline DIMM modules with 4.26 GB/sec Module Bandwidth and "444-11" means CAS latency = 4, t_{RCD} latency = 4 and t_{RP} latency = 4 using the latest JEDEC SPD Revision 1.1 and produced on the Raw Card "A".*

Table 3 Address Format

DIMM Density	Module Organization	Memory Ranks	ECC/ Non-ECC	# of SDRAMs	# of row/bank/columns bits	Raw Card
1 GB	128M ×64	2	Non-ECC	8	13/3/10	A

Table 4 Components on Modules [1)2)]

Part Number	DRAM components reference data sheet	DRAM Density	DRAM Organization
HYS64T128020HDL	HYB18T1G160AF	1 Gbit	64Mb ×16

1) For a detailed description of all functions of the DRAM components on these modules see the referenced component data sheet.

2) Green Product

2 Pin Configuration

The pin configuration of the Small Outline DDR2 SDRAM DIMM is listed by function in **Table 5** (200 pins). The abbreviations used in columns Pin and Buffer Type are explained in **Table 6** and **Table 7** respectively. The pin numbering is depicted in **Figure 1**

Table 5 Pin Configuration of SO-DIMM

Pin#	Name	Pin Type	Buffer Type	Function
Clock Signals				
30	CK0	I	SSTL	**Clock Signals 2:0, Complement Clock Signals 2:0**
164	CK1	I	SSTL	*Note: The system clock inputs. All address and command lines are sampled on the cross point of the rising edge of CK and the falling edge of $\overline{CK}$. A Delay Locked Loop (DLL) circuit is driven from the clock inputs and output timing for read operations is synchronized to the input clock.*
32	$\overline{CK0}$	I	SSTL	
166	$\overline{CK1}$	I	SSTL	
79	CKE0	I	SSTL	**Clock Enable Rank 1:0**
80	CKE1	I	SSTL	*Note: Activates the DDR2 SDRAM CK signal when HIGH and deactivates the CK signal when LOW. By deactivating the clocks, CKE LOW initiates the Power Down Mode or the Self Refresh Mode.* *Note: 2 Ranks module*
	NC	NC	—	*Note: 1-rank module*
Control Signals				
110	$\overline{S0}$	I	SSTL	**Chip Select Rank 1:0**
115	$\overline{S1}$	I	SSTL	*Note: Enables the associated DDR2 SDRAM command decoder when LOW and disables the command decoder when HIGH. When the command decoder is disabled, new commands are ignored but previous operations continue. Rank 0 is selected by $\overline{S0}$; Rank 1 is selected by $\overline{S1}$. Ranks are also called "Physical banks".* *Note: 2 Ranks module*
	NC	NC	—	*Note: 1-rank module*
108	$\overline{RAS}$	I	SSTL	**Row Address Strobe** *Note: When sampled at the cross point of the rising edge of CK,and falling edge of $\overline{CK}$, $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ define the operation to be executed by the SDRAM.*
113	$\overline{CAS}$	I	SSTL	**Column Address Strobe**
109	$\overline{WE}$	I	SSTL	**Write Enable**
Address Signals				
107	BA0	I	SSTL	**Bank Address Bus 2:0**
106	BA1	I	SSTL	*Note: Selects which DDR2 SDRAM internal bank of four or eight is activated.*

Table 5 Pin Configuration of SO-DIMM (cont'd)

Pin#	Name	Pin Type	Buffer Type	Function
85	BA2	I	SSTL	**Bank Address Bus 2** *Note: greater than 512Mb DDR2 SDRAMS*
	NC	I	SSTL	*Note: less than 1Gb DDR2 SDRAMS*
102	A0	I	SSTL	**Address Bus 12:0**
101	A1	I	SSTL	*Note: During a Bank Activate command cycle, defines the row address when sampled at the crosspoint of the rising edge of CK and falling edge of $\overline{CK}$. During a Read or Write command cycle, defines the column address when sampled at the cross point of the rising edge of CK and falling edge of $\overline{CK}$. In addition to the column address, AP is used to invoke autoprecharge operation at the end of the burst read or write cycle. If AP is HIGH, autoprecharge is selected and BA0-BAn defines the bank to be precharged. If AP is LOW, autoprecharge is disabled. During a Precharge command cycle, AP is used in conjunction with BA0-BAn to control which bank(s) to precharge. If AP is HIGH, all banks will be precharged regardless of the state of BA0-BAn inputs. If AP is LOW, then BA0-BAn are used to define which bank to precharge.*
100	A2	I	SSTL	
99	A3	I	SSTL	
98	A4	I	SSTL	
97	A5	I	SSTL	
94	A6	I	SSTL	
92	A7	I	SSTL	
93	A8	I	SSTL	
91	A9	I	SSTL	
105	A10	I	SSTL	
	AP	I	SSTL	
90	A11	I	SSTL	
89	A12	I	SSTL	**Address Signal 12** *Note: Module based on 256 Mbit or larger dies*
116	A13	I	SSTL	**Address Signal 13** *Note: 1 Gbit based module*
	NC	NC	—	*Note: Module based on 512 Mbit or smaller dies*
Data Signals				
5	DQ0	I/O	SSTL	**Data Bus 63:0**
7	DQ1	I/O	SSTL	Note: Data Input/Output pins
17	DQ2	I/O	SSTL	
19	DQ3	I/O	SSTL	
4	DQ4	I/O	SSTL	
6	DQ5	I/O	SSTL	
14	DQ6	I/O	SSTL	
16	DQ7	I/O	SSTL	
23	DQ8	I/O	SSTL	
25	DQ9	I/O	SSTL	
35	DQ10	I/O	SSTL	
37	DQ11	I/O	SSTL	
20	DQ12	I/O	SSTL	
22	DQ13	I/O	SSTL	
36	DQ14	I/O	SSTL	

Table 5 Pin Configuration of SO-DIMM (cont'd)

Pin#	Name	Pin Type	Buffer Type	Function
38	DQ15	I/O	SSTL	**Data Bus 63:0**
43	DQ16	I/O	SSTL	
45	DQ17	I/O	SSTL	
55	DQ18	I/O	SSTL	
57	DQ19	I/O	SSTL	
44	DQ20	I/O	SSTL	
46	DQ21	I/O	SSTL	
56	DQ22	I/O	SSTL	
58	DQ23	I/O	SSTL	
61	DQ24	I/O	SSTL	
63	DQ25	I/O	SSTL	
73	DQ26	I/O	SSTL	
75	DQ27	I/O	SSTL	
62	DQ28	I/O	SSTL	
64	DQ29	I/O	SSTL	
74	DQ30	I/O	SSTL	
76	DQ31	I/O	SSTL	
123	DQ32	I/O	SSTL	
125	DQ33	I/O	SSTL	
135	DQ34	I/O	SSTL	
137	DQ35	I/O	SSTL	
124	DQ36	I/O	SSTL	
126	DQ37	I/O	SSTL	
134	DQ38	I/O	SSTL	
136	DQ39	I/O	SSTL	
141	DQ40	I/O	SSTL	
143	DQ41	I/O	SSTL	
151	DQ42	I/O	SSTL	
153	DQ43	I/O	SSTL	
140	DQ44	I/O	SSTL	
142	DQ45	I/O	SSTL	
152	DQ46	I/O	SSTL	
154	DQ47	I/O	SSTL	
157	DQ48	I/O	SSTL	
159	DQ49	I/O	SSTL	
173	DQ50	I/O	SSTL	
175	DQ51	I/O	SSTL	
158	DQ52	I/O	SSTL	
160	DQ53	I/O	SSTL	
174	DQ54	I/O	SSTL	

Table 5 Pin Configuration of SO-DIMM (cont'd)

Pin#	Name	Pin Type	Buffer Type	Function
176	DQ55	I/O	SSTL	**Data Bus 63:0**
179	DQ56	I/O	SSTL	
181	DQ57	I/O	SSTL	
189	DQ58	I/O	SSTL	
191	DQ59	I/O	SSTL	
180	DQ60	I/O	SSTL	
182	DQ61	I/O	SSTL	
192	DQ62	I/O	SSTL	
194	DQ63	I/O	SSTL	
Data Strobe Signals				
13	DQS0	I/O	SSTL	**Data Strobe Bus 7:0**
11	$\overline{\text{DQS0}}$	I/O	SSTL	*Note: The data strobes, associated with one data byte, sourced with data transfers. In Write mode, the data strobe is sourced by the controller and is centered in the data window. In Read mode the data strobe is sourced by the DDR2 SDRAM and is sent at the leading edge of the data window. $\overline{\text{DQS}}$ signals are complements, and timing is relative to the crosspoint of respective DQS and $\overline{\text{DQS}}$. If the module is to be operated in single ended strobe mode, all $\overline{\text{DQS}}$ signals must be tied on the system board to V_{SS} and DDR2 SDRAM mode registers programmed appropriately.*
31	DQS1	I/O	SSTL	
29	$\overline{\text{DQS1}}$	I/O	SSTL	
51	DQS2	I/O	SSTL	
49	$\overline{\text{DQS2}}$	I/O	SSTL	
70	DQS3	I/O	SSTL	
68	$\overline{\text{DQS3}}$	I/O	SSTL	
131	DQS4	I/O	SSTL	
129	$\overline{\text{DQS4}}$	I/O	SSTL	
148	DQS5	I/O	SSTL	
146	$\overline{\text{DQS5}}$	I/O	SSTL	
169	DQS6	I/O	SSTL	
167	$\overline{\text{DQS6}}$	I/O	SSTL	
188	DQS7	I/O	SSTL	
186	$\overline{\text{DQS7}}$	I/O	SSTL	
Data Mask Signals				
10	DM0	I	SSTL	**Data Mask Bus 7:0**
26	DM1	I	SSTL	*Note: The data write masks, associated with one data byte. In Write mode, DM operates as a byte mask by allowing input data to be written if it is LOW but blocks the write operation if it is HIGH. In Read mode, DM lines have no effect.*
52	DM2	I	SSTL	
67	DM3	I	SSTL	
130	DM4	I	SSTL	
147	DM5	I	SSTL	
170	DM6	I	SSTL	
185	DM7	I	SSTL	
EEPROM				
197	SCL	I	CMOS	**Serial Bus Clock** Note: This signal is used to clock data into and out of the SPD EEPROM.

Table 5 Pin Configuration of SO-DIMM (cont'd)

Pin#	Name	Pin Type	Buffer Type	Function
195	SDA	I/O	OD	**Serial Bus Data** *Note: This is a bidirectional pin used to transfer data into or out of the SPD EEPROM. A resistor must be connected from SDA to to V_{DDSPD} on the motherboard to act as a pull-up.*
198	SA0	I	CMOS	**Serial Address Select Bus 2:0**
200	SA1	I	CMOS	*Note: Address pins used to select the Serial Presence Detect base address.*
Power Supplies				
1	V_{REF}	AI	—	**I/O Reference Voltage** *Note: Reference voltage for the SSTL-18 inputs.*
199	V_{DDSPD}	PWR	—	**EEPROM Power Supply** *Note: Power supplies for core, I/O, Serial Presence Detect, and ground for the module.*
81,82,87,88,95,96,103,104, 111,112,117,118	V_{DD}	PWR	—	**Power Supply** *Note: Power supplies for core, I/O, Serial Presence Detect, and ground for the module.*
2,3,8,9,12,15,18,21,24,27,28, 33,34,39,40,41,42,47,48,53, 54,59,60,65,66,71,72,77,78, 121,122,127,128,132,133,138, 139,144,145,149,150,155,156, 161,162,165,171,172,177, 178,183,184,187,190,193,196	V_{SS}	GND	—	**Ground Plane** *Note: Power supplies for core, I/O, Serial Presence Detect, and ground for the module.*
Other Pins				
114	ODT0	I	SSTL	**On-Die Termination Control 1:0**
119	ODT1	I	SSTL	**On-Die Termination Control 1** *Note: Asserts on-die termination for DQ, DM, DQS, and $\overline{DQS}$ signals if enabled via the DDR2 SDRAM mode register.* *Note: 2 Rank modules*
	NC	NC	—	*Note: 1 Rank modules*
50,69,83,84,120,163,168	NC	NC	—	**Not connected** *Note: Pins not connected on Infineon SO-DIMMs*

Table 6 Abbreviations for Pin Type

Abbreviation	Description
I	Standard input-only pin. Digital levels.
O	Output. Digital levels.
I/O	I/O is a bidirectional input/output signal.
AI	Input. Analog levels.
PWR	Power
GND	Ground
NC	Not Connected

Table 7 Abbreviations for Buffer Type

Abbreviation	Description
SSTL	Serial Stub Terminated Logic (SSTL_18)
LV-CMOS	Low Voltage CMOS
CMOS	CMOS Levels
OD	Open Drain. The corresponding pin has 2 operational states, active low and tristate, and allows multiple devices to share as a wire-OR.

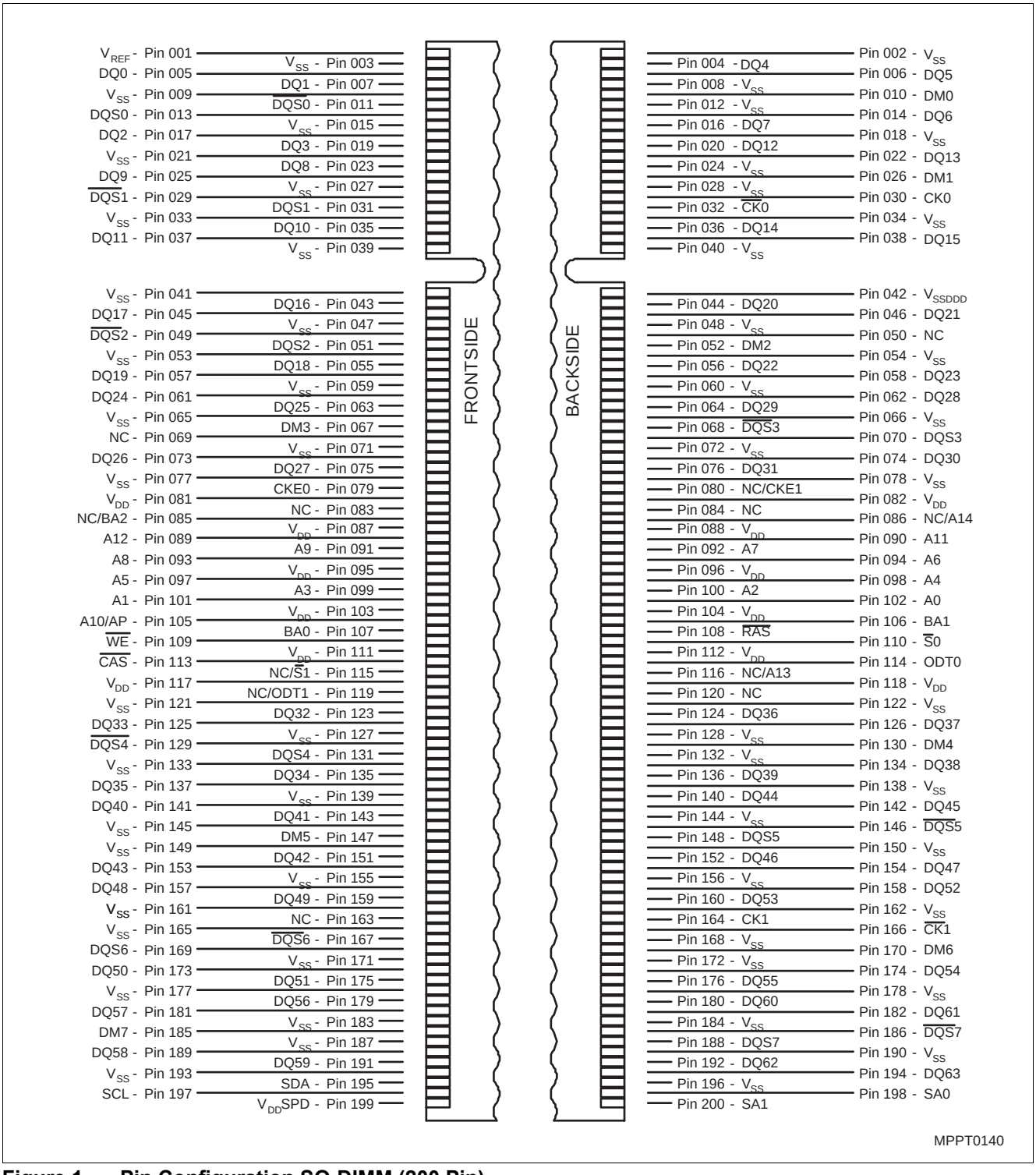

Figure 1 Pin Configuration SO-DIMM (200 Pin)

2.1 Block Diagrams

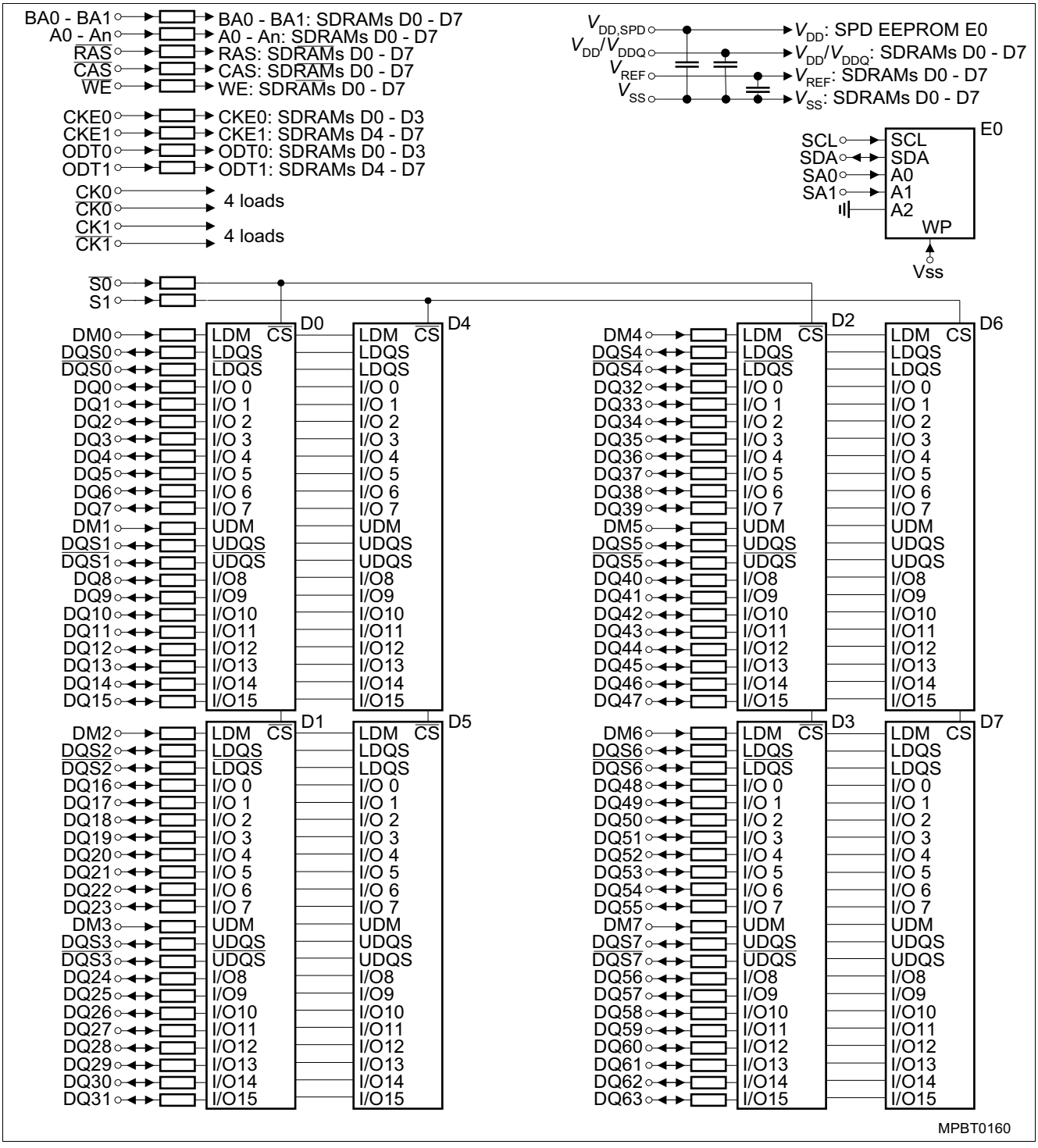

Figure 2 Block Diagram Raw Card A SO-DIMM (×64, 2 Ranks, ×16)

Notes

1. *DQ, DQS, DM resistors are 22 Ω ±5 %*
2. *$\overline{S0}$, $\overline{S1}$, BAn, An, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, ODTO, ODT1, CKEO, CKE1 resistors are 3 Ω ±5 %*

3 I_{DD} Specifications and Conditions

Table 8 I_{DD} Measurement Conditions[1)2)3)4)5)6)]

Parameter	Symbol
Operating Current 0 One bank Active - Precharge; $t_{CK} = t_{CK.MIN}$, $t_{RC} = t_{RC.MIN}$, $t_{RAS} = t_{RAS.MIN}$, CKE is HIGH, $\overline{CS}$ is HIGH between valid commands. Address and control inputs are SWITCHING, Databus inputs are SWITCHING.	I_{DD0}
Operating Current 1 One bank Active - Read - Precharge; I_{OUT} = 0 mA, BL = 4, $t_{CK} = t_{CK.MIN}$, $t_{RC} = t_{RC.MIN}$, $t_{RAS} = t_{RAS.MIN}$, $t_{RCD} = t_{RCD.MIN}$, AL = 0, CL = $CL_{.MIN}$; CKE is HIGH, $\overline{CS}$ is HIGH between valid commands. Address and control inputs are SWITCHING, Databus inputs are SWITCHING.	I_{DD1}
Precharge Power-Down Current Other control and address inputs are STABLE, Data bus inputs are FLOATING.	I_{DD2P}
Precharge Standby Current All banks idle; $\overline{CS}$ is HIGH; CKE is HIGH; $t_{CK} = t_{CK.MIN}$; Other control and address inputs are SWITCHING, Data bus inputs are SWITCHING.	I_{DD2N}
Precharge Quiet Standby Current All banks idle; $\overline{CS}$ is HIGH; CKE is HIGH; $t_{CK} = t_{CK.MIN}$; Other control and address inputs are STABLE, Data bus inputs are FLOATING.	I_{DD2Q}
Active Power-Down Current All banks open; $t_{CK} = t_{CK.MIN}$, CKE is LOW; Other control and address inputs are STABLE, Data bus inputs are FLOATING. MRS A12 bit is set to LOW (Fast Power-down Exit);	$I_{DD3P(0)}$
Active Power-Down Current All banks open; $t_{CK} = t_{CK.MIN}$, CKE is LOW; Other control and address inputs are STABLE, Data bus inputs are FLOATING. MRS A12 bit is set to HIGH (Slow Power-down Exit);	$I_{DD3P(1)}$
Active Standby Current Burst Read: All banks open; Continuous burst reads; BL = 4; AL = 0, CL = $CL_{.MIN}$; $t_{CK} = t_{CK.MIN}$; $t_{RAS} = t_{RAS.MAX}$, $t_{RP} = t_{RP.MIN}$; CKE is HIGH, $\overline{CS}$ is HIGH between valid commands. Address inputs are SWITCHING; Data Bus inputs are SWITCHING; I_{OUT} = 0 mA.	I_{DD3N}
Operating Current Burst Read: All banks open; Continuous burst reads; BL = 4; AL = 0, CL = $CL_{.MIN}$; $t_{CK} = t_{CK.MIN}$; $t_{RAS} = t_{RAS.MAX.}$, $t_{RP} = t_{RP.MIN}$; CKE is HIGH, $\overline{CS}$ is HIGH between valid commands. Address inputs are SWITCHING; Data Bus inputs are SWITCHING; I_{OUT} = 0 mA.	I_{DD4R}
Operating Current Burst Write: All banks open; Continuous burst writes; BL = 4; AL = 0, CL = $CL_{.MIN}$; $t_{CK} = t_{CK.MIN}$; $t_{RAS} = t_{RAS.MAX.}$, $t_{RP} = t_{RP.MAX}$; CKE is HIGH, $\overline{CS}$ is HIGH between valid commands. Address inputs are SWITCHING; Data Bus inputs are SWITCHING;	I_{DD4W}
Burst Refresh Current $t_{CK} = t_{CKmin.}$, Refresh command every $t_{RFC} = t_{RFC.MIN}$ interval, CKE is HIGH, $\overline{CS}$ is HIGH between valid commands, Other control and address inputs are SWITCHING, Data bus inputs are SWITCHING.	I_{DD5B}
Distributed Refresh Current $t_{CK} = t_{CKmin.}$, Refresh command every $t_{RFC} = t_{REFI}$ interval, CKE is LOW and $\overline{CS}$ is HIGH between valid commands, Other control and address inputs are SWITCHING, Data bus inputs are SWITCHING.	I_{DD5D}

Table 8 I_{DD} Measurement Conditions[1)2)3)4)5)6)]

Parameter	Symbol
Self-Refresh Current CKE ≤ 0.2 V; external clock off, CK and $\overline{CK}$ at 0 V; Other control and address inputs are FLOATING, Data bus inputs are FLOATING. I_{DD6} current values are guaranteed up to T_{CASE} of 85 °C max.	I_{DD6}
All Bank Interleave Read Current All banks are being interleaved at minimum t_{RC} without violating t_{RRD} using a burst length of 4. Control and address bus inputs are STABLE during DESELECTS. I_{out} = 0 mA.	I_{DD7}

1) V_{DDQ} = 1.8 V ± 0.1 V; V_{DD} = 1.8 V ± 0.1 V
2) I_{DD} specifications are tested after the device is properly initialized and I_{DD} parameter are specified with ODT disabled.
3) Definitions for I_{DD}:
   LOW is defined as $V_{IN} \le V_{IL(ac).MAX}$, HIGH is defined as $V_{IN} \ge V_{IH(ac).MIN}$
   STABLE is defined as: inputs are stable at a HIGH or LOW level
   FLOATING is defined as: inputs are $V_{REF} = V_{DDQ}/2$
   SWITCHING is defined as: inputs are changing between HIGH and LOW every other clock (once per 2 cycles) for address and control signals, and inputs changing between HIGH and LOW every other data transfer (once per cycle) for DQ signals not including mask or strobes.
4) I_{DD1}, I_{DD4R} and I_{DD7} current measurements are defined with the outputs disabled (I_{OUT} = 0 mA). To achieve this on module level the output buffers can be disabled using an EMRS(1) (Extended Mode Register Command) by setting A12 bit to HIGH.
5) For two rank modules: for all active current measurements the other rank is in Precharge Power-Down Mode I_{DD2P}
6) For details and notes see the relevant INFINEON component data sheet

Table 9 I_{DD} Specification for HYS64T128020HDL–3.7–A

Product Type	HYS64T128020HDL–3.7–A	Unit	Notes[1]
Organization	1 GB		
	2 Ranks		
	×64		
	–37		
Symbol	Max.		
I_{DD0}	340	mA	2)
I_{DD1}	400	mA	2)
I_{DD2P}	40	mA	3)
I_{DD2N}	370	mA	3)
I_{DD2Q}	260	mA	3)
$I_{DD3P(MRS=0)}$	140	mA	3)
$I_{DD3P(MRS=1)}$	50	mA	3)
I_{DD3N}	400	mA	3)
I_{DD4R}	540	mA	2)
I_{DD4W}	680	mA	2)
I_{DD5B}	760	mA	2)
I_{DD5D}	60	mA	3)
I_{DD6}	32	mA	3)
I_{DD7}	1100	mA	2)

1) Calculated values from component data. ODT disabled. I_{DD1}, I_{DD4R} and I_{DD7} are defined with the outputs disabled

2) The other rank is in I_{DD2P} Pre charge Power-Down Standby Current mode

3) Both ranks are in the same I_{DD} current mode

Table 10 I_{DD} Specification for HYS64T128020HDL–5–A

Product Type	HYS64T128020HDL–5–A	Unit	Notes[1)]
Organization	**1 GB**		
	2 Ranks		
	×64		
	–5		
Symbol	**Max.**		
I_{DD0}	320	mA	2)
I_{DD1}	380	mA	2)
I_{DD2P}	40	mA	3)
I_{DD2N}	280	mA	3)
I_{DD2Q}	220	mA	3)
$I_{DD3P(MRS=0)}$	100	mA	3)
$I_{DD3P(MRS=1)}$	40	mA	3)
I_{DD3N}	320	mA	3)
I_{DD4R}	440	mA	2)
I_{DD4W}	540	mA	2)
I_{DD5B}	740	mA	2)
I_{DD5D}	60	mA	3)
I_{DD6}	32	mA	3)
I_{DD7}	1040	mA	2)

1) Calculated values from component data. ODT disabled. I_{DD1}, I_{DD4R} and I_{DD7} are defined with the outputs disabled

2) The other rank is in I_{DD2P} Pre charge Power-Down Standby Current mode

3) Both ranks are in the same I_{DD} current mode

3.1 I_{DD} Test Conditions

For testing the I_{DD} parameters, the following timing parameters are used:

Table 11 I_{DD} Measurement Test Conditions

Parameter		Symbol	–3.7	–5	Unit
			PC2-4200-4-4-4	PC2-3200-3-3-3	
CAS Latency		$CL_{(IDD)}$	4	3	t_{CK}
Clock Cycle Time		$t_{CK(IDD)}$	3.75	5	ns
Active to Read or Write delay		$t_{RCD(IDD)}$	15	15	ns
Active to Active / Auto-Refresh command period		$t_{RC(IDD)}$	60	55	ns
Active bank A to Active bank B command delay	×8[1)]	$t_{RRD(IDD)}$	7.5	7.5	ns
	×16[2)]	$t_{RRD(IDD)}$	10	10	ns
Active to Precharge Command		$t_{RAS.MIN(IDD)}$	45	40	ns
		$t_{RAS.MAX(IDD)}$	70000	70000	ns
Precharge Command Period		$t_{RP(IDD)}$	15	15	ns
Auto-Refresh to Active / Auto-Refresh command period		$t_{RFC(IDD)}$	127.5	127.5	ns
Average periodic Refresh interval		t_{REFI}	7.8	7.8	µs

1) *For modules based on ×8 components*

2) *For modules based on ×16 components*

3.2 ODT (On Die Termination) Current

The ODT function adds additional current consumption to the DDR2 SDRAM when enabled by the EMRS(1). Depending on address bits A6 & A2 in the EMRS(1) a “week” or “strong” termination can be selected. The current consumption for any terminated input pin, depends on the input pin is in tristate or driving 0 or 1, as long a ODT is enabled during a given period of time.

Table 12 ODT current per terminated pin:

Parameter	Symbol	Min.	Type.	Max.	Unit	EMRS(1) State
Enabled ODT current per DQ added IDDQ current for ODT enabled; ODT is HIGH; Data Bus inputs are FLOATING	I_{ODTO}	5	6	7.5	mA/DQ	A6 = 0, A2 = 1
		2.5	3	3.75	mA/DQ	A6 = 1, A2 = 0
Active ODT current per DQ added IDDQ current for ODT enabled; ODT is HIGH; worst case of Data Bus inputs are STABLE or SWITCHING.	I_{ODTT}	10	12	15	mA/DQ	A6 = 0, A2 = 1
		5	6	7.5	mA/DQ	A6 = 1, A2 = 0

Note: For power consumption calculations the ODT duty cycle has to be taken into account

4 Electrical Characteristics

4.1 Operating Conditions

Table 13 Absolute Maximum Ratings

Parameter	Symbol	Limit Values		Unit	Note/Test Condition
		Min.	Max.		
Voltage on any pins relative to V_{SS}	V_{IN}, V_{OUT}	– 0.5	2.3	V	1)
Voltage on V_{DD} relative to V_{SS}	V_{DD}	– 1.0	2.3	V	1)
Voltage on $V_{DD\,Q}$ relative to V_{SS}	V_{DDQ}	– 0.5	2.3	V	1)
Storage Humidity (without condensation)	H_{STG}	5	95	%	1)

1) Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Table 14 Operating Conditions

Parameter	Symbol	Limit Values		Unit	Notes
		Min.	Max.		
DIMM Module Operating Temperature Range (ambient)	T_{OPR}	0	+55	°C	
DRAM Component Case Temperature Range	T_{CASE}	0	+95	°C	1)2)3)4)
Storage Temperature	T_{STG}	– 50	+100	°C	
Barometric Pressure (operating & storage)	PBar	+69	+105	kPa	5)
Operating Humidity (relative)	H_{OPR}	10	90	%	

1) DRAM Component Case Temperature is the surface temperature in the center on the top side of any of the DRAMs

2) Within the DRAM Component Case Temperature range all DRAM specification will be supported.

3) Above 85°C DRAM case temperature the Auto-Refresh command interval has to be reduced to t_{REFI} = 3.9 µs.

4) Self-Refresh period is hard-coded in the DRAMs and therefore it is imperative that the system ensures the DRAM is below 85°C case temperature before initiating self-refresh operation.

5) Up to 3000 m.

Table 15 Supply Voltage Levels and DC Operating Conditions

Parameter	Symbol	Limit Values			Unit	Notes
		Min.	Nom.	Max.		
Device Supply Voltage	V_{DD}	1.7	1.8	1.9	V	-
Output Supply Voltage	V_{DDQ}	1.7	1.8	1.9	V	1)
Input Reference Voltage	V_{REF}	0.49 x V_{DDQ}	0.5 x V_{DDQ}	0.51 x V_{DDQ}	V	2)
SPD Supply Voltage	V_{DDSPD}	1.7	–	3.6	V	
DC Input Logic High	$V_{IH\,(DC)}$	V_{REF} + 0.125	–	V_{DDQ} + 0.3	V	
DC Input Logic Low	$V_{IL\,(DC)}$	– 0.30	–	V_{REF} – 0.125	V	

1) *Under all conditions, V_{DDQ} must be less than or equal to V_{DD}*

2) *Peak to peak AC noise on V_{REF} may not exceed ± 2% V_{REF} (DC). V_{REF} is also expected to track noise variations in V_{DDQ}.*

Table 16 Speed Grade Definition Speed Bins

Speed Grade			DDR2–533C		DDR2–400B		Unit	Notes
IFX Sort Name			–3.7		–5			
CAS-RCD-RP latencies			4–4–4		3–3–3		t_{CK}	
Parameter		Symbol	Min.	Max.	Min.	Max.	—	
Clock Frequency	@ CL = 3	t_{CK}	5	8	5	8	ns	1)2)3)4)
	@ CL = 4	t_{CK}	3.75	8	5	8	ns	1)2)3)4)
	@ CL = 5	t_{CK}	3.75	8	5	8	ns	1)2)3)4)
Row Active Time		t_{RAS}	45	70000	40	70000	ns	1)2)3)4)5)
Row Cycle Time		t_{RC}	60	—	55	—	ns	1)2)3)4)
RAS-CAS-Delay		t_{RCD}	15	—	15	—	ns	1)2)3)4)
Row Precharge Time		t_{RP}	15	—	15	—	ns	1)2)3)4)

1) Timings are guaranteed with CK/$\overline{CK}$ differential Slew Rate of 2.0 V/ns. For DQS signals timings are guaranteed with a differential Slew Rate of 2.0 V/ns in differential strobe mode and a Slew Rate of 1 V/ns in single ended mode. Timings are further guaranteed for normal OCD drive strength (EMRS(1) A1 = 0) only.

2) The CK/$\overline{CK}$ input reference level (for timing reference to CK/$\overline{CK}$) is the point at which CK and $\overline{CK}$ cross. The DQS / $\overline{DQS}$, RDQS / $\overline{RDQS}$, input reference level is the crosspoint when in differential strobe mode

3) Inputs are not recognized as valid until V_{REF} stabilizes. During the period before V_{REF} stabilizes, CKE = 0.2 x V_{DDQ} is recognized as low.

4) The output timing reference voltage level is V_{TT}.

5) $t_{RAS.MAX}$ is calculated from the maximum amount of time a DDR2 device can operate without a refresh command which is equal to 9 x t_{REFI}.

Table 17 Timing Parameter by Speed Grade - DDR2-400B & DDR2-533C

Parameter	Symbol	–3.7 DDR2–533 4–4–4		–5 DDR2–400 3–3–3		Unit	Notes[1)]
		Min.	Max.	Min.	Max.		
DQ output access time from CK / $\overline{CK}$	t_{AC}	–500	+500	–600	+600	ps	
$\overline{CAS}$ A to $\overline{CAS}$ B command period	t_{CCD}	2	—	2	—	t_{CK}	
CK, $\overline{CK}$ high-level width	t_{CH}	0.45	0.55	0.45	0.55	t_{CK}	
CKE minimum high and low pulse width	t_{CKE}	3	—	3	—	t_{CK}	
CK, $\overline{CK}$ low-level width	t_{CL}	0.45	0.55	0.45	0.55	t_{CK}	
Auto-Precharge write recovery + precharge time	t_{DAL}	WR + t_{RP}	—	WR + t_{RP}	—	t_{CK}	
Minimum time clocks remain ON after CKE asynchronously drops LOW	t_{DELAY}	t_{IS} + t_{CK} + t_{IH}	—	t_{IS} + t_{CK} + t_{IH}	—	ns	
DQ and DM input hold time (differential data strobe)	t_{DH}(base)	225	—	275	—	ps	
DQ and DM input hold time (single ended data strobe)	t_{DH1}(base)	–25	—	25	—	ps	
DQ and DM input pulse width (each input)	t_{DIPW}	0.35	—	0.35	—	t_{CK}	
DQS output access time from CK / $\overline{CK}$	t_{DQSCK}	–450	+450	–500	+500	ps	
DQS input low (high) pulse width (write cycle)	$t_{DQSL,H}$	0.35	—	0.35	—	t_{CK}	
DQS-DQ skew (for DQS & associated DQ signals)	t_{DQSQ}	—	300	—	350	ps	
Write command to 1st DQS latching transition	t_{DQSS}	WL – 0.25	WL + 0.25	WL – 0.25	WL + 0.25	t_{CK}	
DQ and DM input setup time (differential data strobe)	t_{DS}(base)	100	—	150	—	ps	
DQ and DM input setup time (single ended data strobe)	t_{DS1}(base)	–25	—	25	—	ps	
DQS falling edge hold time from CK (write cycle)	t_{DSH}	0.2	—	0.2	—	t_{CK}	
DQS falling edge to CK setup time (write cycle)	t_{DSS}	0.2	—	0.2	—	t_{CK}	
Four Activate Window period	t_{FAW}	37.5	—	37.5	—	ns	2)3)
		50	—	50	—	ns	4)
Clock half period	t_{HP}	MIN. (t_{CL}, t_{CH})		MIN. (t_{CL}, t_{CH})			
Data-out high-impedance time from CK / $\overline{CK}$	t_{HZ}	—	$t_{AC.MAX}$	—	$t_{AC.MAX}$	ps	
Address and control input hold time	t_{IH}(base)	375	—	475	—	ps	
Address and control input pulse width (each input)	t_{IPW}	0.6	—	0.6	—	t_{CK}	

Table 17 Timing Parameter by Speed Grade - DDR2-400B & DDR2-533C (cont'd)

Parameter	Symbol	–3.7 DDR2–533 4–4–4		–5 DDR2–400 3–3–3		Unit	Notes[1)]
		Min.	Max.	Min.	Max.		
Address and control input setup time	t_{IS}(base)	250	—	350	—	ps	
DQ low-impedance time from CK / $\overline{CK}$	$t_{LZ(DQ)}$	$2 \times t_{AC.MIN}$	$t_{AC.MAX}$	$2 \times t_{AC.MIN}$	$t_{AC.MAX}$	ps	
DQS low-impedance from CK / $\overline{CK}$	$t_{LZ(DQS)}$	$t_{AC.MIN}$	$t_{AC.MAX}$	$t_{AC.MIN}$	$t_{AC.MAX}$	ps	
Mode register set command cycle time	t_{MRD}	2	—	2	—	t_{CK}	
OCD drive mode output delay	t_{OIT}	0	12	0	12	ns	
Data output hold time from DQS	t_{QH}	$t_{HP} - t_{QHS}$	—	$t_{HPQ} - t_{QHS}$	—		
Data hold skew factor	t_{QHS}	—	400	—	450	ps	
Average periodic refresh Interval	t_{REFI}	—	7.8	—	7.8	µs	5)
		—	3.9	—	3.9	µs	6)
Auto-Refresh to Active/Auto-Refresh command period	t_{RFC}	127.5	—	127.5	—	ns	
Precharge-All (8 banks) command period	t_{RP}	15 + 1t_{CK}	—	15 + 1t_{CK}	—	ns	
Read preamble	t_{RPRE}	0.9	1.1	0.9	1.1	t_{CK}	
Read postamble	t_{RPST}	0.40	0.60	0.40	0.60	t_{CK}	
Active bank A to Active bank B command period	t_{RRD}	7.5	—	7.5	—	ns	
		10	—	10	—	ns	
Internal Read to Precharge command delay	t_{RTP}	7.5	—	7.5	—	ns	
Write preamble	t_{WPRE}	0.35xt_{CK}	—	0.35xt_{CK}	—	t_{CK}	
Write postamble	t_{WPST}	0.40	0.60	0.40	0.60	t_{CK}	
Write recovery time for write without Auto-Precharge	t_{WR}	15	—	15	—	ns	
Write recovery time for write with Auto-Precharge	WR	t_{WR}/t_{CK}		t_{WR}/t_{CK}		t_{CK}	
Internal Write to Read command delay	t_{WTR}	7.5	—	10	—	ns	
Exit power down to any valid command (other than NOP or Deselect)	t_{XARD}	2	—	2	—	t_{CK}	
Exit active power-down mode to Read command (slow exit, lower power)	t_{XARDS}	6 – AL	—	6 – AL	—	t_{CK}	
Exit precharge power-down to any valid command (other than NOP or Deselect)	t_{XP}	2	—	2	—	t_{CK}	
Exit Self-Refresh to non-Read command	t_{XSNR}	t_{RFC} +10	—	t_{RFC} +10	—	ns	
Exit Self-Refresh to Read command	t_{XSRD}	200	—	200	—	t_{CK}	

1) For details and notes see the relevant INFINEON component data sheet
2) ×4 & ×8 (1k page size)
3) 8 bank device Sequential Activation Restriction. No more than 4 banks may be activated in a rolling t_{FAW} window.
4) ×16 (2k page size), not on 256 Mbit component
5) $0 \leq T_{CASE} \leq 85$ °C
6) 85 °C < $T_{CASE} \leq 95$ °C

Table 18 ODT AC Electrical Characteristics and Operating Conditions

Symbol	Parameter / Condition	Values		Unit	Notes
		Min.	Max.		
t_{AOND}	ODT turn-on delay	2	2	t_{CK}	
t_{AON}	ODT turn-on	$t_{AC.MIN}$	$t_{AC.MAX}$ + 1 ns	ns	1)
t_{AONPD}	ODT turn-on (Power-Down Modes)	$t_{AC.MIN}$ + 2 ns	2 t_{CK} + $t_{AC.MAX}$ + 1 ns	ns	
t_{AOFD}	ODT turn-off delay	2.5	2.5	t_{CK}	
t_{AOF}	ODT turn-off	$t_{AC.MIN}$	$t_{AC.MAX}$ + 0.6 ns	ns	2)
t_{AOFPD}	ODT turn-off (Power-Down Modes)	$t_{AC.MIN}$ + 2 ns	2.5 t_{CK} + $t_{AC.MAX}$ + 1 ns	ns	
t_{ANPD}	ODT to Power Down Mode Entry Latency	3	—	t_{CK}	
t_{AXPD}	ODT Power Down Exit Latency	8	—	t_{CK}	

1) ODT turn on time min. is when the device leaves high impedance and ODT resistance begins to turn on. ODT turn on time max is when the ODT resistance is fully on. Both are measure from t_{AOND}.
2) ODT turn off time min. is when the device starts to turn off ODT resistance. ODT turn off time max is when the bus is in high impedance. Both are measured from t_{AOFD}.

5 SPD Codes

Table 19 SPD Codes for HYS64T128020HDL–[3.7/5]–A

Product Type		HYS64T128020HDL–3.7–A	HYS64T128020HDL–5–A
Organization		**1 GByte**	**1 GByte**
		×64	**×64**
		2 Ranks (×16)	**2 Ranks (×16)**
Label Code		**PC2–4200S–444**	**PC2–3200S–333**
JEDEC SPD Revision		**Rev. 1.1**	**Rev. 1.1**
Byte#	**Description**	**HEX**	**HEX**
0	Programmed SPD Bytes in EEPROM	80	80
1	Total number of Bytes in EEPROM	08	08
2	Memory Type (DDR2)	08	08
3	Number of Row Addresses	0D	0D
4	Number of Column Addresses	0A	0A
5	DIMM Rank and Stacking Information	61	61
6	Data Width	40	40
7	Not used	00	00
8	Interface Voltage Level	05	05
9	t_{CK} @ CL_{max} (Byte 18) [ns]	3D	50
10	t_{AC} SDRAM @ CL_{max} (Byte 18) [ns]	50	60
11	Error Correction Support (non-ECC, ECC)	00	00
12	Refresh Rate and Type	82	82
13	Primary SDRAM Width	10	10
14	Error Checking SDRAM Width	00	00
15	Not used	00	00
16	Burst Length Supported	0C	0C
17	Number of Banks on SDRAM Device	08	08
18	Supported CAS Latencies	38	38
19	DIMM Mechanical Characteristics	00	00
20	DIMM Type Information	04	04
21	DIMM Attributes	00	00
22	Component Attributes	01	01
23	t_{CK} @ CL_{max} -1 (Byte 18) [ns]	3D	50
24	t_{AC} SDRAM @ CL_{max} -1 [ns]	50	60

Table 19 SPD Codes for HYS64T128020HDL–[3.7/5]–A (cont'd)

Product Type		**HYS64T128020HDL–3.7–A**	**HYS64T128020HDL–5–A**
Organization		**1 GByte**	**1 GByte**
		×64	**×64**
		2 Ranks (×16)	**2 Ranks (×16)**
Label Code		**PC2–4200S–444**	**PC2–3200S–333**
JEDEC SPD Revision		**Rev. 1.1**	**Rev. 1.1**
Byte#	**Description**	**HEX**	**HEX**
25	t_{CK} @ CL_{max} -2 (Byte 18) [ns]	50	50
26	t_{AC} SDRAM @ CL_{max} -2 [ns]	60	60
27	$t_{RP.min}$ [ns]	3C	3C
28	$t_{RRD.min}$ [ns]	28	28
29	$t_{RCD.min}$ [ns]	3C	3C
30	$t_{RAS.min}$ [ns]	2D	28
31	Module Density per Rank	80	80
32	$t_{AS.min}$ and $t_{CS.min}$ [ns]	25	35
33	$t_{AH.min}$ and $t_{CH.min}$ [ns]	37	47
34	$t_{DS.min}$ [ns]	10	15
35	$t_{DH.min}$ [ns]	22	27
36	$t_{WR.min}$ [ns]	3C	3C
37	$t_{WTR.min}$ [ns]	1E	28
38	$t_{RTP.min}$ [ns]	1E	1E
39	Analysis Characteristics	00	00
40	t_{RC} and t_{RFC} Extension	00	00
41	$t_{RC.min}$ [ns]	3C	37
42	$t_{RFC.min}$ [ns]	7F	7F
43	$t_{CK.max}$ [ns]	80	80
44	$t_{DQSQ.max}$ [ns]	1E	23
45	$t_{QHS.max}$ [ns]	28	2D
46	PLL Re-lock Time	00	00
47	$T_{CASE.max}$ Delta / ΔT_{4R4W} Delta	57	55
48	Psi(T-A) DRAM	58	58
49	ΔT_0 (DT0)	36	32
50	ΔT_{2N} (DT2N, UDIMM) or ΔT_{2Q} ((DT2Q, RDIMM)	26	1D
51	ΔT_{2P} (DT2P)	1C	1C

Table 19 SPD Codes for HYS64T128020HDL–[3.7/5]–A (cont'd)

Product Type		**HYS64T128020HDL–3.7–A**	**HYS64T128020HDL–5–A**
Organization		**1 GByte**	**1 GByte**
		×64	**×64**
		2 Ranks (×16)	**2 Ranks (×16)**
Label Code		**PC2–4200S–444**	**PC2–3200S–333**
JEDEC SPD Revision		**Rev. 1.1**	**Rev. 1.1**
Byte#	**Description**	**HEX**	**HEX**
52	ΔT_{3N} (DT3N)	1C	16
53	$\Delta T_{3P.fast}$ (DT3P fast)	1C	16
54	$\Delta T_{3P.slow}$ (DT3P slow)	14	11
55	ΔT_{4R} (DT4R) / $\Delta T_{4R4W\ S}$ Sign (DT4R4W)	36	2C
56	ΔT_{5B} (DT5B)	1F	1E
57	ΔT_{7} (DT7)	2D	2B
58	Psi(ca) PLL	00	00
59	Psi(ca) REG	00	00
60	ΔT_{PLL} (DTPLL)	00	00
61	ΔT_{REG} (DTREG) / Toggle Rate	00	00
62	SPD Revision	11	11
63	Checksum of Bytes 0-62	D4	23
64	JEDEC ID Code of Infineon (1)	C1	C1
65 - 71	JEDEC ID Code of Infineon (2 - 8)	00	00
72	Module Manufacturer Location	xx	xx
73	Product Type, Char 1	36	36
74	Product Type, Char 2	34	34
75	Product Type, Char 3	54	54
76	Product Type, Char 4	31	31
77	Product Type, Char 5	32	32
78	Product Type, Char 6	38	38
79	Product Type, Char 7	30	30
80	Product Type, Char 8	32	32
81	Product Type, Char 9	30	30
82	Product Type, Char 10	48	48
83	Product Type, Char 11	44	44
84	Product Type, Char 12	4C	4C

Table 19 SPD Codes for HYS64T128020HDL–[3.7/5]–A (cont'd)

Product Type		**HYS64T128020HDL–3.7–A**	**HYS64T128020HDL–5–A**
Organization		**1 GByte**	**1 GByte**
		×64	**×64**
		2 Ranks (×16)	**2 Ranks (×16)**
Label Code		**PC2–4200S–444**	**PC2–3200S–333**
JEDEC SPD Revision		**Rev. 1.1**	**Rev. 1.1**
Byte#	**Description**	**HEX**	**HEX**
85	Product Type, Char 13	33	35
86	Product Type, Char 14	2E	41
87	Product Type, Char 15	37	20
88	Product Type, Char 16	41	20
89	Product Type, Char 17	20	20
90	Product Type, Char 18	20	20
91	Module Revision Code	1x	1x
92	Test Program Revision Code	xx	xx
93	Module Manufacturing Date Year	xx	xx
94	Module Manufacturing Date Week	xx	xx
95 - 98	Module Serial Number (1 - 4)	xx	xx
99 - 127	Not used	00	00

6 Package Outlines

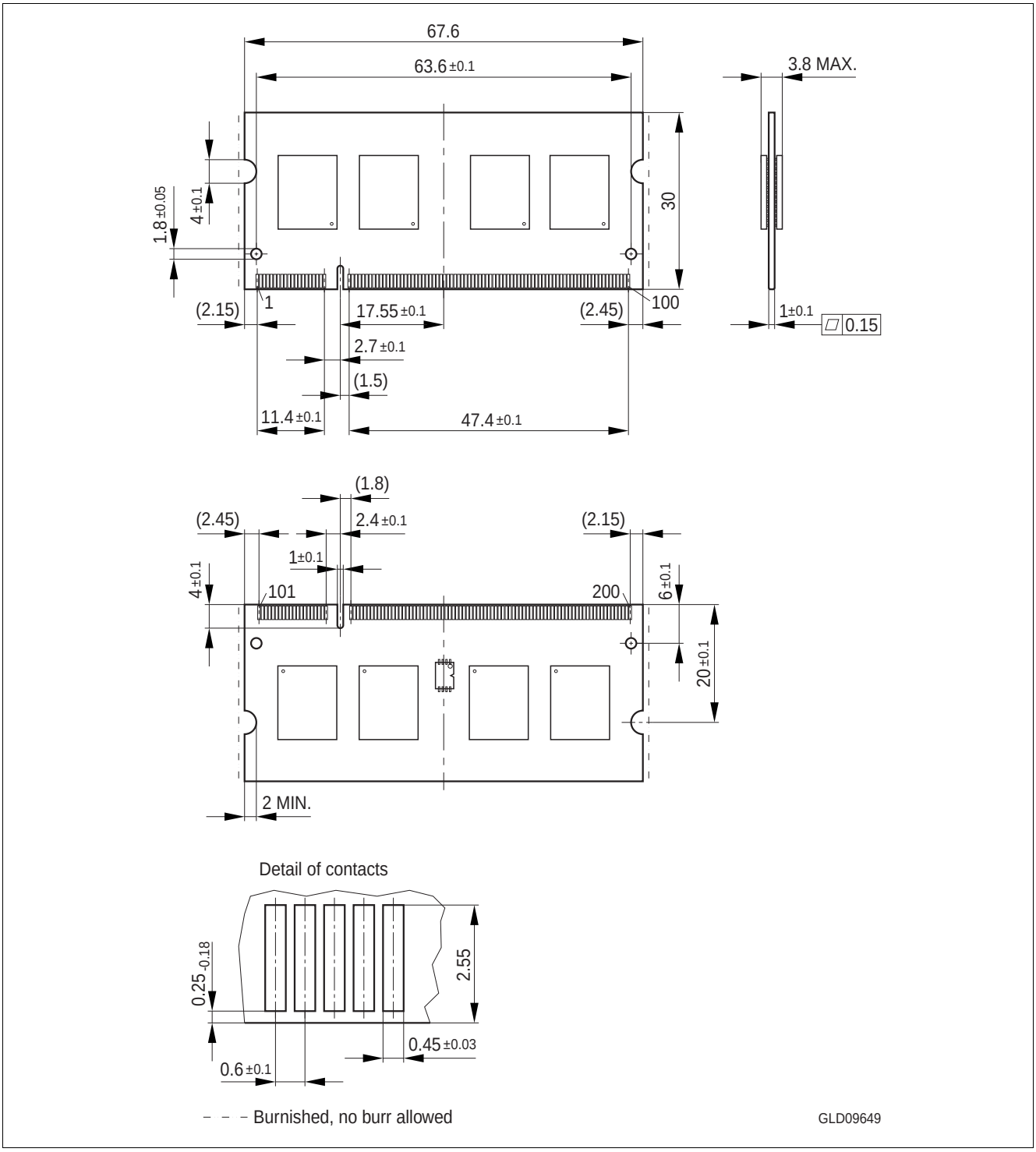

Figure 3 Package Outline Raw Card A – L-DIM-200-31

7 Product Type Nomenclature (DDR2 DRAMs and DIMMs)

Infineon's nomenclature uses simple coding combined with some proprietary coding. Table 20 provides examples for module and component product type number as well as the field number. The detailed field description together with possible values and coding explanation is listed for modules in Table 21 and for components in Table 22.

Table 20 Nomenclature Fields and Examples

Example for	Field Number										
	1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**
Micro-DIMM	HYS	64	T	128	0	2	0	K	M	–5	–A
DDR2 DRAM	HYB	18	T	1G	16		0	A	C	–5	

Table 21 DDR2 DIMM Nomenclature

Field	Description	Values	Coding
1	INFINEON Modul Prefix	HYS	Constant
2	Module Data Width [bit]	64	Non-ECC
		72	ECC
3	DRAM Technology	T	DDR2
4	Memory Density per I/O [Mbit]; Module Density[1)]	32	256 MByte
		64	512 MByte
		128	1 GByte
		256	2 GByte
5	Raw Card Generation	0 .. 9	look up table
6	Number of Module Ranks	0, 2, 4	1, 2, 4
7	Product Variations	0 .. 9	look up table
8	Package, Lead-Free Status	A .. Z	look up table
9	Module Type	D	SO-**D**IMM
		M	**M**icro-DIMM
		R	**R**egistered
		U	**U**nbuffered
10	Speed Grade	–3.7	PC2–4200 4–4–4
		–5	PC2–3200 3–3–3
11	Die Revision	–A	First
		–B	Second

1) Multiplying "Memory Density per I/O" with "Module Data Width" and dividing by 8 for Non-ECC and 9 for ECC modules gives the overall module memory density in MBytes as listed in column "Coding".

Table 22 DDR2 DRAM Nomenclature

Field	Description	Values	Coding
1	INFINEON Component Prefix	HYB	Constant
2	Interface Voltage [V]	18	SSTL1.8
3	DRAM Technology	T	DDR2
4	Component Density [Mbit]	256	256 Mbit
		512	512 Mbit
		1G	1 Gbit
		2G	2 Gbit
5+6	Number of I/Os	40	×4
		80	×8
		16	×16
7	Product Variations	0 .. 9	look up table
8	Die Revision	A	First
		B	Second
9	Package, Lead-Free Status	C	FBGA, lead-containing
		F	FBGA, lead-free
10	Speed Grade	–3.7	DDR2-533C
		–5	DDR2-400B
11	N/A for Components		

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