Audio Conversion Systems Noise Calculations and Requirements

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1. Introduction

The skills required to predict the dynamic range of a combined Analog-to-Digital converter (ADC) and Digital-to-Analog converter (DAC) system, as well as determine the noise requirements for the analog input and output stages, should be considered essential for an audio systems designer. The techniques required are relatively basic in that they are generally covered in the first analog circuit analysis class in most engineering programs. However, applying these techniques to the conversion processes often generates some level of confusion. This discussion will detail the steps required to apply these techniques and determine this critical system performance parameter.

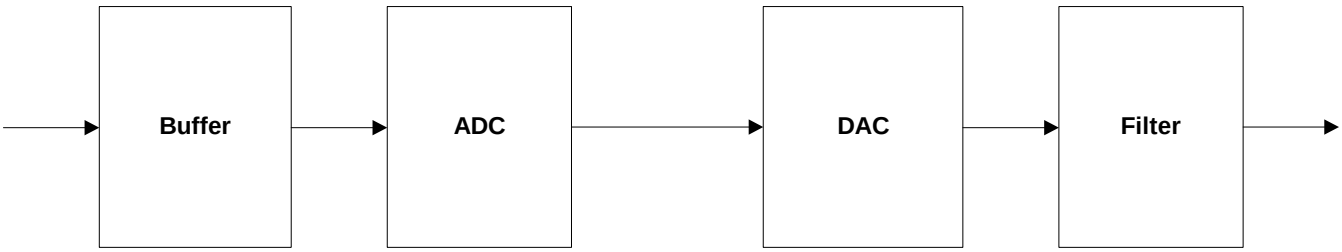

Figure 1. Conversion System Block Diagram

The ADC and DAC system, Figure 1, contains four primary noise sources that must be considered. These include the analog input buffer, ADC, DAC and the analog output buffer/ filter stage. Noise generated in each of these stages adds as the “square root of the sum of the squares” as shown below. This fundamental relationship will be used throughout this discussion.

$$V_{total} = \sqrt{V_1^2 + V_2^2 + V_3^2 + V_4^2}$$

The analysis requires several initial assumptions and setting of limits.

1) The bandwidth is set to 20 kHz. This constraint is purely for convenience and allows the use of a common converter data sheet specification. The results can easily be scaled to other bandwidths as long as assumption #2 remains valid.
2) The spectral content of the noise is “white”. This assumes that the contribution of 1/f noise is negligible and the noise sources within the converters remain “white” to the upper limit of the analysis. A word

of warning, the spectral noise content of digital-to-analog converters often do not retain this characteristic at bandwidths well beyond 20 kHz when operated at 96 kHz or 192 kHz sample rates.

3) The noise contribution of the analog input and output stages are negligible. This assumption simplifies the initial analysis but requires further investigation to ensure accuracy.

2. Combined ADC and DAC Dynamic Range Calculation

2.1 Converter Equivalent Noise Calculation

Dynamic Range (DR) is a specification that can be found in any ADC or DAC data sheet. This specification is defined as the ratio of the RMS voltage of a full-scale analog input (V_{fsadc}) or output (V_{fsdac}) sine wave to the RMS noise voltage of the converter over a 20 kHz bandwidth. DR is generally specified in dB and the equation for dynamic range is shown below. Notice that there are three variables in this equation, where the DR and V_{fs} are common data sheet specifications. The equation can be easily rearranged to allow the calculation of the equivalent RMS noise voltage (V_n) of the converter.

$$DR = 20 \times \log\left(\frac{V_{fs}}{V_n}\right)$$

$$V_n = \frac{V_{fs}}{10^{\left(\frac{DR}{20}\right)}}$$

However, adjustments to the data sheet Dynamic Range and full-scale input/output specifications are often required prior to the calculation.

1) Dynamic Range specifications are often A-weighted and the equivalent noise calculation requires the use of un-weighted numbers. Fortunately, A-weighted specifications can easily be converted to an approximate unweighted specification. A conservative estimate can be determined by simply degrading the A-weighted data sheet specification by 3 dB.
2) The full scale input or output voltage specifications in converter data sheets are commonly represented as either volts peak-to-peak, volts peak or RMS. The full scale input or output voltage must be converted to a RMS value for this calculation to be valid.

2.2 Conversion System Gain

Another requirement is that the noise sources within the system must be referenced to the same system node. Assume that the ADC and DAC system operates as a single block with analog input and analog output. Due to the differences in the conversion processes and the corresponding differences in the analog input voltage and the analog output voltage, the block has either gain or attenuation. The system must be modeled to reflect this gain with the gain coefficient (K), as shown in Figure 2.

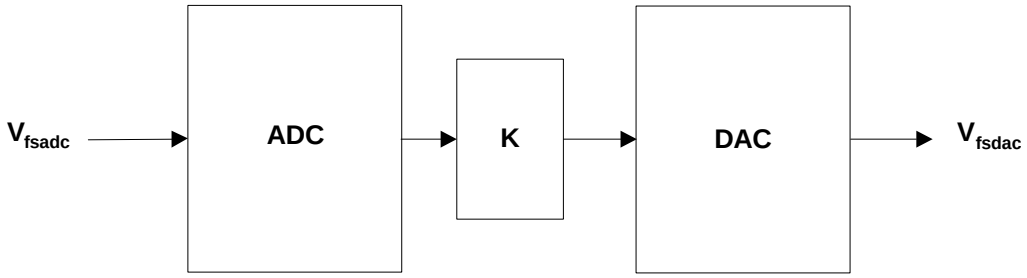

Figure 2. Effective Conversion System Gain

$$K = \frac{V_{fsdac}}{V_{fsadc}}$$

2.3 Equivalent System Noise Calculation

The output referred system noise voltage (V_{nsys}) can be calculated using the expressions for the gain coefficient, equivalent ADC and DAC noise voltages.

$$V_{nsys} = \sqrt{(V_{ndac}{}^2 + (K \times V_{nadc})^2)}$$

Where:

$$V_{ndac} = \frac{V_{fsdac}}{10^{\left(\frac{DR_{dac}}{20}\right)}}$$

$$V_{nadc} = \frac{V_{fsadc}}{10^{\left(\frac{DR_{adc}}{20}\right)}}$$

$$K = \frac{V_{fsdac}}{V_{fsadc}}$$

Following substitution and simplification:

$$V_{nsys} = V_{fsdac}\sqrt{10^{-\left(\frac{DR_{dac}}{10}\right)} + 10^{-\left(\frac{DR_{adc}}{10}\right)}}$$

2.4 System Dynamic Range Calculation

The un-weighted system dynamic range (in dB) can be calculated using the equation for the equivalent system noise voltage. Conversion to A-weighting requires the addition of 3 dB to the un-weighted number.

$$unweighted \qquad DR_{sys} = 20 \times \log \frac{V_{fsdac}}{V_{nsys}}$$

Substituting and simplifying the equation yields;

$$unweighted \qquad DR_{sys} = -10 \times \log \left[10^{-\left(\frac{DR_{dac}}{10}\right)} + 10^{-\left(\frac{DR_{adc}}{10}\right)} \right]$$

A-weighted DR_{sys} = unweighted DR_{sys} + 3 dB

3. Converter and Buffer Noise Analysis

One of the initial assumptions was that the buffer noise was negligible in relation to the converter noise. Of the assumptions during the initial analysis, this has the greatest potential of being invalid. Though this assumption proves to be acceptable for many applications and converter products, it becomes questionable as converter dynamic range improves.

The calculation of the equivalent noise voltages for the ADC input buffers and DAC output buffers / filters is beyond the scope of this paper. However, care needs to be taken to ensure that the converter and buffer noise sources are referred to the appropriate system node. The converters themselves can be considered unity gain devices and their noise can be referred to either the input or output of the converter. It's generally best to refer the ADC buffer noise to the input of the ADC. In the case of the DAC, it is most convenient to refer the noise of the DAC and buffer to the output of the buffer.

To illustrate the technique let's take a look at the combination of an input buffer and ADC, Figure 3. The combined converter + buffer noise equation is shown below, assuming the buffer noise is referred to the input of the ADC. The equivalent converter noise voltage can be calculated as previously shown.

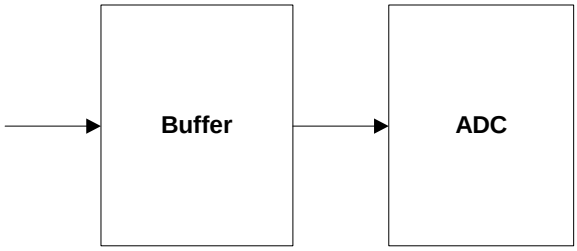

Figure 3. Input Buffer and ADC Block Diagram

$$V_{nT} = \sqrt{V_{nadc}^2 + V_{nbuffer}^2}$$

3.1 Generalized Noise Error

It is very informative to create a generalized noise relationship and a “rule-of-thumb” design goal such that the noise contribution of the buffer can be considered negligible. Taking the total noise equation, and dividing each of the contributing noise sources by the converter noise as shown below can easily accomplish this. Converting the normalized noise to dB, creates a very informative relationship in that the deviation from 0 dB can now interpreted as the normalized error function.

$$V_{nT_{normalized}} = \sqrt{\left(\frac{V_{nconverter}}{V_{nconverter}}\right)^2 + \left(\frac{V_{nbuffer}}{V_{nconverter}}\right)^2}$$

$$V_{nT_{normalized}} = \sqrt{1 + \left(\frac{V_{nbuffer}}{V_{nconverter}}\right)^2}$$

$$Error = 20 \times \log \sqrt{1 + \left(\frac{V_{nbuffer}}{V_{nconverter}}\right)^2}$$

Figure 4 shows the normalized noise error as a function of ratio of buffer to converter noise. The X-axis shows the ratio and the Y-axis displays the deviation from 0 dB. Notice that as the ratio approaches 1, where the buffer noise is equivalent to the converter noise, the error is 3 dB. The graph also indicates that an error of approximately 1 dB is introduced when the noise of the buffer noise is 1/2 that of the converter. Figure 5 shows the previous normalized noise error with a change in the scaling of the X-axis and Y-axis. Notice that at the point where buffer noise is 10% that of the converter noise, the error is approximately 0.05 dB. This error can probably be considered negligible for even the most demanding of applications. It is also convenient that a ratio of 0.1 is equivalent to a buffer noise voltage that is 20 dB below the converter noise voltage. This indicates that a conservative and convenient “rule-of-thumb” design goal is for the buffer noise to be 20 dB below that of the converter. However, the ultimate decision on the minimum required buffer noise is based on systems performance and cost requirements and may differ from this “rule-of-thumb”.

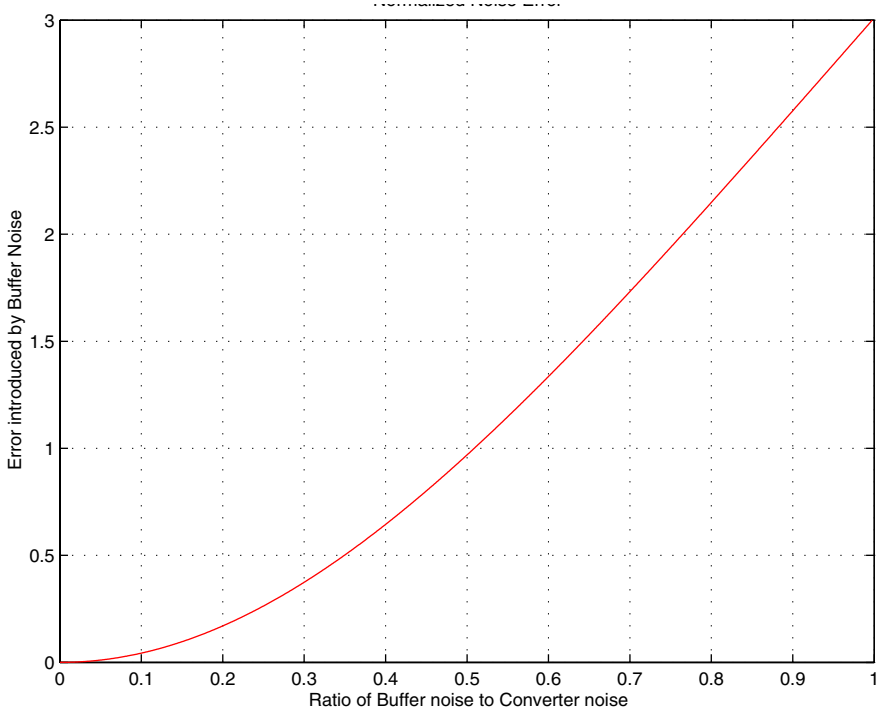

Figure 4. Normalized Noise Error - Wide View

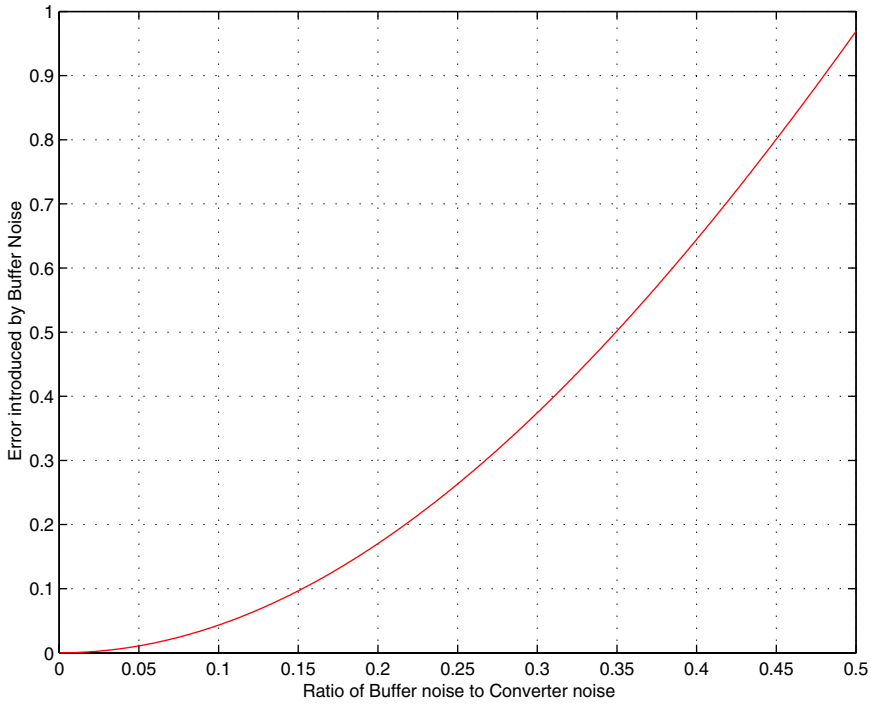

Figure 5. Normalized Noise Error - Zoomed View

3.1.1 Illustrative Noise Budget Calculation

Let's calculate the required buffer noise for the CS5381 to meet the assumption of negligible noise contribution using the “rule-of-thumb” design goal. The equivalent noise of the CS5381 can be calculated as previously shown using the relevant data sheet specifications, where the un-weighted Dynamic Range is 117 dB and the full-scale differential input is 2 Vrms. This calculation shows that the equivalent noise for the CS5381 is 2.83 μV. Based on the “rule-of-thumb” noise requirement, the buffer noise should be 20 dB below the equivalent converter noise, or 0.283 μV.

It is informative and enlightning to compare this noise voltage to the equivalent noise generated by a resistor at room temperature (25 degrees C). The following is the equation used to calculate the noise for a resistor.

$$V_{n_{resistor}} = \sqrt{4kTBR}$$

Where:

- k = 1.38 x 10-23 Joules / degree (Boltzman's Constant)
- T = Absolute temperature of the resistor
- B = effective bandwidth (20 kHz for this example)
- R = resistance value

Solving this equation for the resistance and inserting the buffer noise voltage design goal indicates that the noise contribution of the buffer must be equal to or less than the equivalent noise of a 243 ohm resistor! It's apparent that in the case of high-dynamic range converters, the noise contribution of the input and output buffers cannot be assumed to be negligible. Low noise design techniques for the analog buffers must be employed to achieve the full performance capabilities of leading edge converters.

3.2 Combined Converter and Buffer Dynamic Range from a different perspective

It is interesting to look at this relationship from the perspective of the deviation from ideal as the converter dynamic range increases and the buffer noise remains constant. This has been a relatively common occurrence over the past few years as systems designers have been assigned the goal of updating an existing product by increasing the system dynamic range. The obvious solution is to replace the existing converters with higher dynamic range converters. Unfortunately, the assumption is often made that the noise contribution of the existing buffer design is negligible, which often leads to disappointing results and subsequent redesign.

Figure 6 displays the results of this situation with a hypothetical D/A and filter design. The X-axis of the graph indicates the converter dynamic range and the Y-axis indicates the dynamic range of the combined filter / buffer and D/A converter. The upper plot indicates the ideal dynamic range where the buffer noise is zero. The remaining plots indicate the degradation in performance with a fixed buffer noise contribution for four different converter full-scale output voltages. Notice that, for this example, the deviation from ideal for the converters with dynamic ranges in the 100 to 105 dB range is minimal. However, as converter performance exceeds 105 dB the deviation becomes significant.

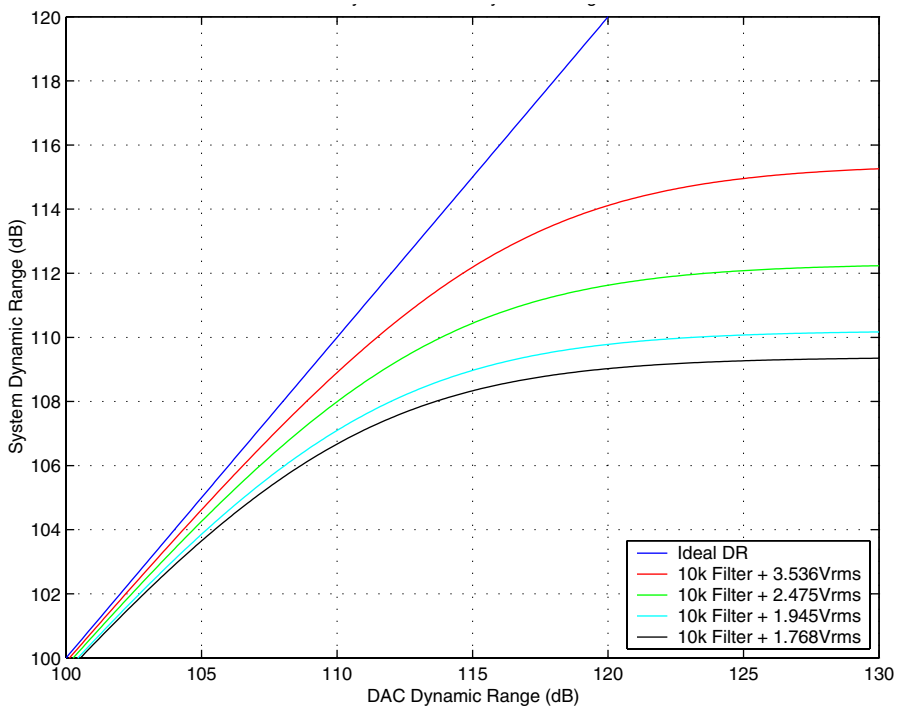

Figure 6. System vs. DAC Dynamic Range - 10K Filter

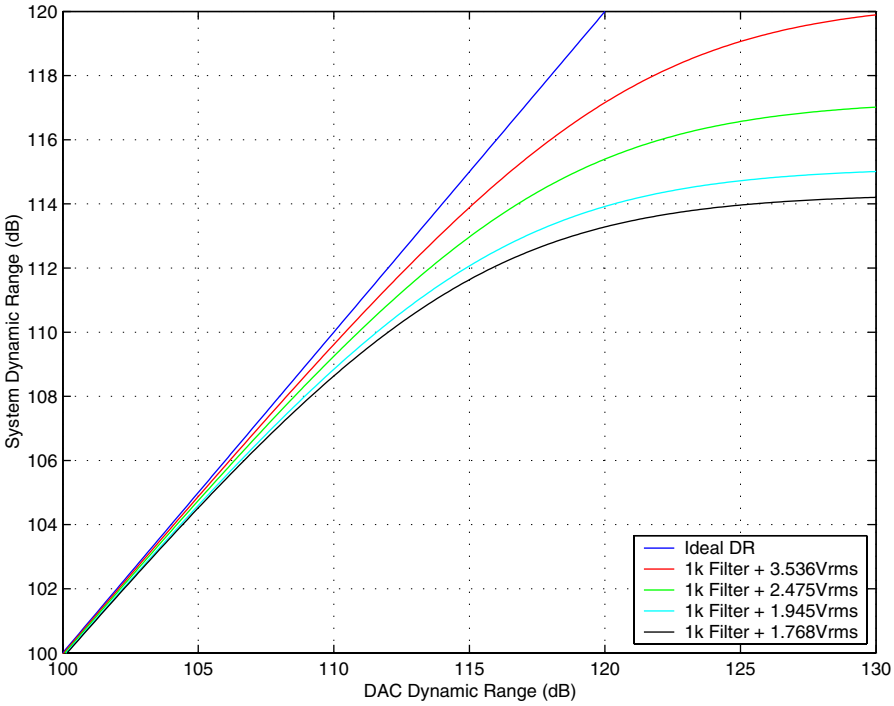

Figure 7. System vs. DAC Dynamic Range - 1K Filter

Figure 7 displays a similar series of plots where the filter/ buffer circuit has been redesigned to scale the resistors to 10% of the previous values. Notice the improvements in the deviation from the ideal. With these impedance changes, the deviation from the ideal remains minimal up to approximately 110 dB.

4. Conclusion

It is a relatively straightforward process to calculate and predict the system dynamic range for any combination of analog-to-digital and digital-to-analog converter, as well as the maximum allowable analog buffer and filter noise to achieve these targets. The difficulty is designing low noise analog buffers and filters that meet the requirements of today's leading edge converters. The combination of high-dynamic range and the limited full-scale signal amplitudes typical of today's converters create a challenging enviroment for the systems designer. The first steps are to recognize and understand the challenge.

Revision	Date	Changes
1	18 Oct 2004	Initial Release

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