Preliminary

Am3020/3030/3042/3064/3090

Am3000 Series Family of Programmable Gate Arrays

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **Second generation user-programmable gate array**
- **Flexible array architecture**
- **High performance**
  - 50, 70, 100 MHz commercial products
  - 50, 70 MHz military products
- **Improved interconnection resources**
- **Density of up to 9000 gates**
- **100% factory pre-tested**
- **Selectable configuration modes**
- **100% compatibility with AMD PGA development tools**
- **Standard PROM file interface**
- **Off the shelf availability**

GENERAL DESCRIPTION

The Am3000 Series Logic Cell™ Array (LCA) is a high-performance, second generation user-programmable gate array. The array contains three types of configurable elements that are customized in accordance with the user-defined system design; a perimeter of Input/Output Blocks (IOBs), a core array of Configurable Logic Blocks (CLBs), and interconnection resources.

The final configuration of the three main programmable elements is determined by the user and easily implemented by AMD user-programmable gate array design tools.

AMD's development tools let users produce a complete design, from schematic capture through device customization, on an IBM PC-AT™ compatible computer. LCA macro libraries and interface software are also available to support schematic capture and simulation on popular CAE workstations.

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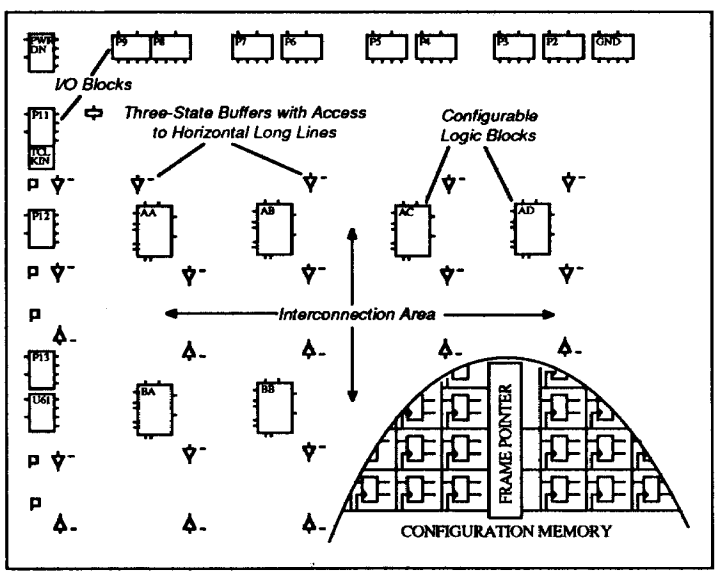
BLOCK DIAGRAM



Logic Cell is a trademark of Xilinx, Inc.
IBM PC-AT is a trademark of International Business Machines Corp.

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PRODUCT SELECTOR GUIDE

BASIC ARRAY	LOGIC CAPACITY (USABLE GATES)	CONFIGURABLE LOGIC BLOCKS	USER I/OS	PROGRAM DATA (BITS)
Am3020	2000	64	64	14779
Am3030	3000	100	80	22176
Am3042	4200	144	96	30784
Am3064	6400	224	120	46064
Am3090	9000	320	144	64160

ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The ordering number (Valid Combination) is formed by a combination of:

a. Device Number
b. Speed Option (if applicable)
c. Package Type
d. Temperature Range
e. Number of Pins

AM3020 -50 J C 068

e. NUMBER OF PINS
068 (68 pins)
084 (84 pins)
132 (132 pins)*
175 (175 pins)

d. TEMPERATURE RANGE
C = Commercial (0°C to 70°C)
I = Industrial (-40°C to +85°C)

c. PACKAGE TYPE
J = Plastic Leaded Chip Carrier
G = Pin Grid Array

b. SPEED OPTION
-50 (50 MHz toggle rate)
-70 (70 MHz toggle rate)
-100 (100 MHz toggle rate)

a. DEVICE NUMBER/DESCRIPTION
Am3000 Series of Programmable Gate Arrays
Am3020 (2000 gates)
Am3030 (3000 gates)
Am3042 (4200 gates)
Am3064 (6400 gates)
Am3090 (9000 gates)

Package Availability Guide

	68-pin PLCC	68-pin PGA	84-pin PLCC	84-pin PGA	175-pin PGA
3020	x	x	x	x	
3030			x	x	
3042			x	x	
3064	**	**	**	**	**
3090					x

*In development

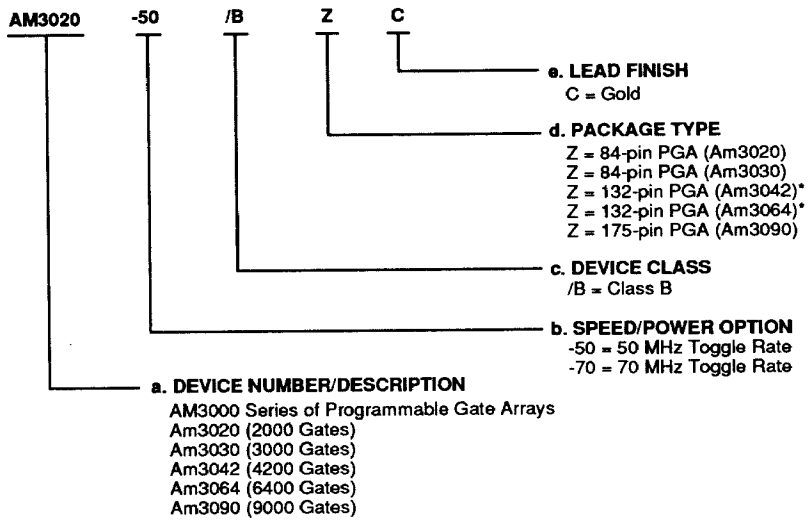
** Package types for the Am3064 are to be determined

ORDERING INFORMATION

Military APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) for APL products is formed by a combination of:

a. Device Number
b. Speed/Power Option (if applicable)
c. Device Class
d. Package Type
e. Lead Finish



Valid Combinations	
Am3020-50	/BZC
Am3020-70	
Am3030-50	
Am3030-70	
Am3042-50	
Am3042-70	
Am3064-50	
Am3064-70	
Am3090-50	
Am3090-70	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

Group A Tests

Group A Tests consist of Subgroups 1, 2, 3, 7, 8, 9, 10, 11.

Military Burn-In

Military burn-in is in accordance with the current revision of MIL–STD–883, Test Method 1015, Conditions A through E. Test conditions are selected at AMD's option.

*In development

ARCHITECTURE

Functional Description

The perimeter of configurable IOBs provides a programmable interface between the internal logic array and the device package pins. The array of CLBs performs user-specified logic functions. The interconnections are programmed to form networks, carrying logic signals among blocks. This is analogous to printed circuit board traces connecting MSI/SSI packages.

The logic functions of these blocks are determined by programmed look-up tables. Functional options are performed by program-controlled multiplexers. Interconnecting networks between blocks are composed of metal segments joined by program-controlled pass transistors. These LCA functions are activated by a configuration bit stream that is loaded into an internal, distributed array of configuration memory cells. The configuration bit stream is loaded into the LCA device at power-up and can be reloaded on command. The LCA device includes logic and control signals for automatic or passive configuration. Configuration data can be either bit serial or byte parallel. The PGA Development System generates the configuration bit stream used to configure the LCA device. The memory loading process is independent of the user logic functions.

Configuration Memory

The static memory cell used for the LCA's configuration memory has been designed specifically for high reliability and noise immunity, ensuring integrity even under adverse conditions. Static memory provides the best combination of high density, high performance, high reliability, and comprehensive testability. As shown below, the basic memory cell consists of two CMOS inverters and a pass transistor, which is used for writing and reading cell data. The cell is only written during configuration and only read during readback. During normal operation, the pass transistor is off and does not affect the stability of the cell. This is quite different from the operation of conventional memory devices, in which the cells are frequently read and re-written.

A static configuration memory cell is loaded with one bit of the configuration bit stream and controls one data selection in the LCA device. The memory cell outputs Q and $\overline{Q}$ use full Ground and V_{CC} levels and provide continuous, direct control. The additional capacitive load, together with the absence of address decoding and sense amplifiers, gives the cell high stability.

Due to the structure of the configuration memory cells, they are not affected by extreme power supply excursions or very high levels of alpha particle radiation. No soft errors have been observed in reliability testing, even in the presence of very high doses of alpha radiation.

The method of loading the configuration data is selectable. Two methods use serial data, while three use byte-wide data. The internal configuration logic uses framing information, which is embedded in the configuration data by the PGA Development System, to direct memory cell loading. The serial data framing and length count preamble provide synchronous, serial, or daisy-chained compatibility with various AMD programmable gate arrays.

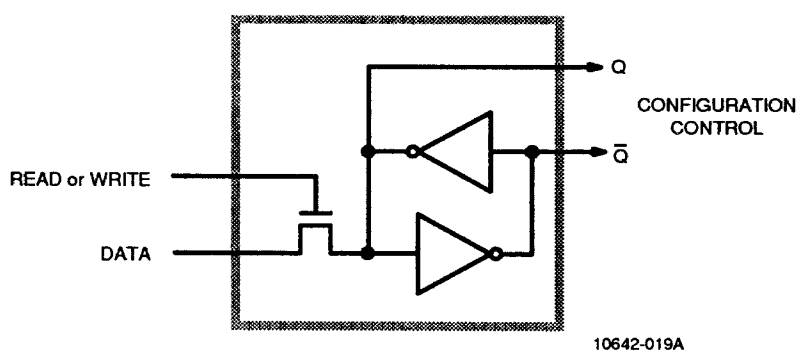


Figure 1. Basic Memory Cell

Input/Output Blocks

Each user-configurable IOB, shown below, provides an interface between the device's external package pin and the internal user logic. Each IOB includes both registered and direct input paths and each provides a programmable three-state output buffer that can be driven by a registered or direct output signal. Configuration options allow a choice of polarity on the output and three-state control signals, a controlled slew rate, and a high impedance pull-up. Each input circuit provides input clamping diodes for electrostatic protection, and circuits to inhibit latch-up produced by input currents.

The input buffer portion of each IOB provides threshold detection to translate external signals applied to the package pin to internal logic levels. The global input-buffer threshold of the IOBs can be programmed for TTL or CMOS voltage levels. The buffered input signal drives the data input of a storage element that can be configured as a positive edge-triggered D flip-flop, or a level-transparent latch. The sense of the clock can be inverted (negative edge/high transparent) as long as all IOBs on the same clock net use the same clock sense. Clock/load signals, IOB pins .ik and .ok, can be chosen from either of two available metal lines along each die edge. I/O storage elements are reset during configuration or by the active low chip $\overline{\text{RESET}}$ input. Both direct input from IOB pin .i, and registered input from IOB pin .q signals are available for interconnect.

For reliable operation, inputs should have transition times less than 100 ns and should not be left undriven, or floating. Unused CMOS input-pin circuits can be at threshold and produce oscillations. This produces additional power dissipation and system noise. A typical hysteresis of about 300 mV reduces input noise sensitivity. Each user IOB includes a programmable high impedance pull-up resistor that can be selected by the bit stream and which provides a constant HIGH for otherwise undriven package pins. Although the LCA device provides circuitry for input protection against electrostatic discharge, normal CMOS handling precautions should be observed.

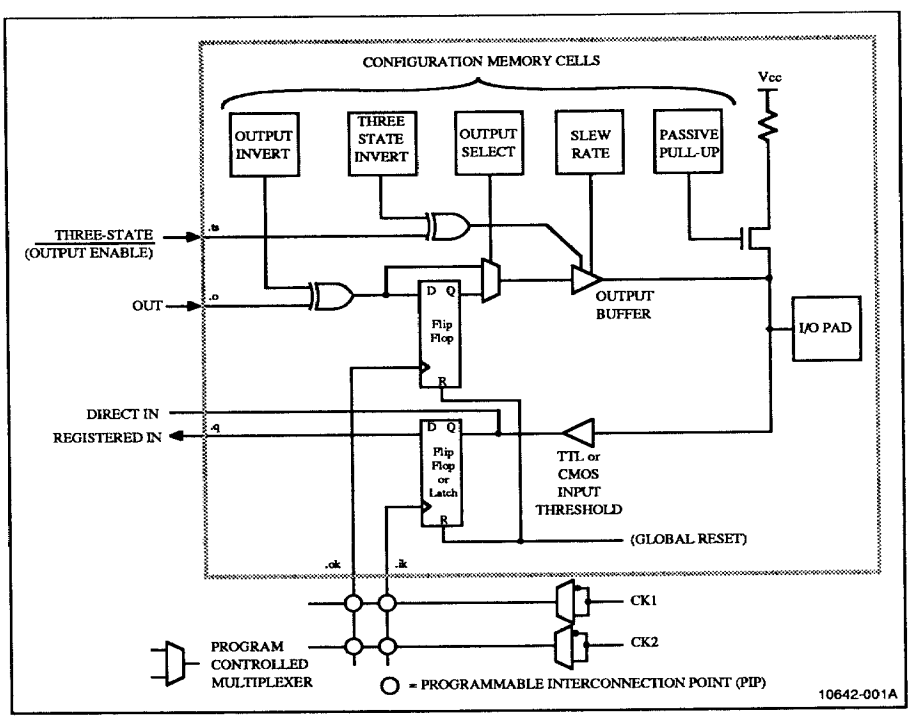


Figure 2. Input/Output Block

Flip-flop loop delays for the IOB and logic block flip-flops are about 3 ns. This increases reliability, especially for asynchronous clock and data conditions. Short loop delays minimize the probability of a metastable condition, which can result from assertion of the clock during data transitions. Because of the short loop delay in LCA devices, the I/O flip-flops can be used to synchronize external signals applied to the device. Once synchronized in the IOB, the signals can be used internally without regard to their clock-relative timing, except as it applies to the internal logic and routing path delays.

Output buffers of the IOBs provide CMOS-compatible 4 mA source-or-sink drive for high fan-out CMOS or TTL compatible signal levels. The network driving IOB pin .o becomes the registered or direct data source for the output buffer. The three-state control signal, IOB pin .ts, can control output activity. An open-drain type output can be obtained by using the same signal for driving the output and three-state signal nets, so that the buffer output is enabled only for a LOW.

The configuration memory cells, shown in Figure 2, control the optional output register and logical signal inversion, as well as the three-state and slew rate configuration bits. A choice of two clocks is available on each die edge. All user inputs are programmed for TTL or CMOS thresholds.

The IOB includes input and output storage elements and the following I/O options selected by configuration memory cells.

- Logical **Inversion of the output** is controlled by one configuration bit per IOB.
- Logical **three-state control** of each IOB output buffer is determined by the states of the configuration data bits that turn the buffer on/off or select the output buffer three-state control interconnection, IOB pin .ts. When this IOB output control signal is HIGH, or logic 1, the buffer is disabled and the package pin is high impedance. Inversion of the buffer three-state control logic sense, output enable, is controlled by an additional configuration data bit.
- **Direct or registered output** is selectable for each IOB. The register uses a positive-edge, clocked flip-flop. The clock source, IOB pin .ok, can be supplied by either of two metal lines, which are available along each die edge. Each of these lines is driven by an invertible buffer.
- Increased **output transition speed** can be selected to satisfy critical nets. Slower transitions reduce capacitive load peak currents of non-critical outputs and minimize system noise.
- A high impedance **pull-up resistor** can be used to prevent floating, unused inputs.

The table below summarizes the I/O options.

INPUTS	OUTPUTS
Direct	Direct/registered
Flip-flop/latch	Inverted/true
CMOS/TTL threshold (chip inputs)	Full speed/slew limited
Optional pull-up resistor	Optional three-state control

Configurable Logic Blocks

CLBs are the functional elements from which the user's logic is constructed. The logic blocks are arranged in a matrix within the perimeter of IOBs. The Am3020 has 64 such blocks arranged in eight rows and eight columns. The PGA Development System compiles the configuration data, which defines the operation and interconnection of each block. Users can define CLBs and their interconnecting networks by automatic translation from a schematic capture logic diagram or, optionally, by installing library or user macros.

Each CLB has a combinational logic section, two flip-flops, and an internal control section. As shown in the following figure, there are five logic inputs (.a, .b, .c, .d, and .e), a common clock input (.k), an asynchronous direct reset input (.rd), and a clock enable (.ec). All can be driven from the interconnection resources adjacent to the blocks. Each CLB also has two outputs (.x and .y) that can drive interconnection networks.

Data input for either flip-flop within a CLB is supplied from the F or G function outputs of the combinational logic, or the direct data input, .di. Both flip-flops in each CLB share the asynchronous reset, .rd, which, when enabled and HIGH, is dominant over clocked inputs. All flip-flops are reset by the active-LOW chip input, $\overline{\text{RESET}}$, or during the configuration process. The flip-flops share the clock enable (.ec), which, when LOW, recirculates the present states of the flip-flops and inhibits response to the data-in or combinational function inputs on a CLB. The user can enable these control inputs and select their sources. The user also can select the clock net input (.k) and its active sense in each logic block. This programmable inversion eliminates the need to route both phases of a clock signal throughout the device. Flexible routing allows use of common or individual CLB clocking.

The combinational logic portion of the CLB uses a 32-by-1 look-up table to perform Boolean functions. Variables selected from the five logic inputs and two internal block flip-flops are used as table address inputs. The combinational propagation delay through the network is independent of the logic function generated and is spike free for changes in single input variables.

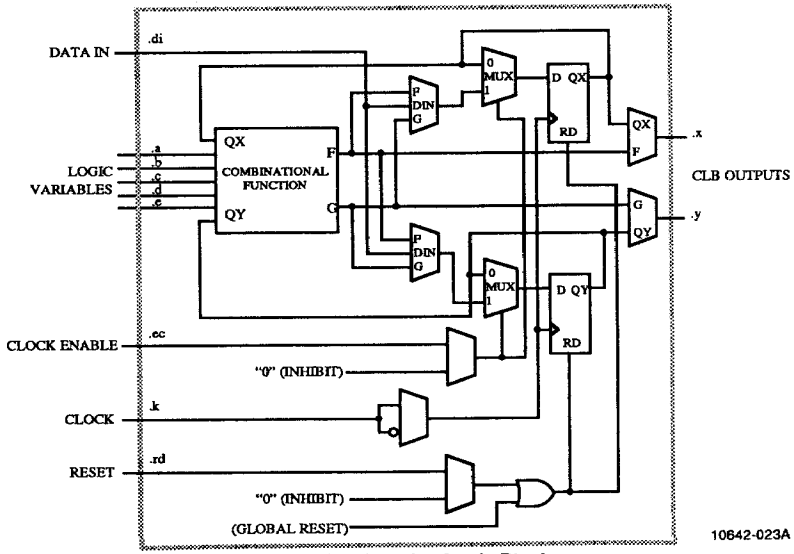


Figure 3. Configurable Logic Block

This technique can generate a single function of five variables, as shown below.

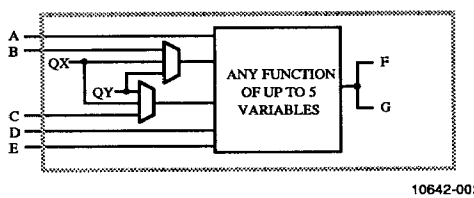


Figure 4. Combinatorial Logic Option 1

It can also generate any two logic functions of up to four variables each.

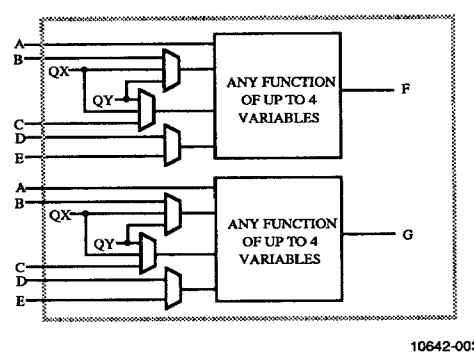


Figure 5. Combinatorial Logic Option 2

It can also generate some functions of seven variables, as shown in the next figure.

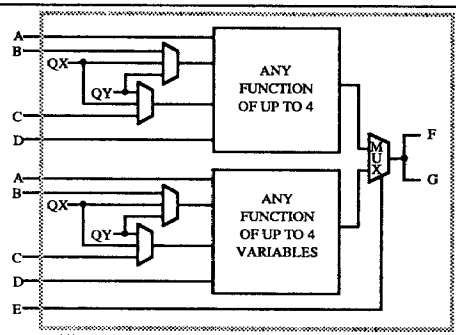


Figure 6. Combinatorial Logic Option 3

The partial functions of six or seven variables are generated by the input variable, .e, which dynamically selects between two functions of four different variables. For the two functions of four variables each, the independent results, F and G, can be used as data inputs to either flip-flop or either logic block output. For the single function of five variables and merged functions of six or seven variables, the F and G outputs are identical. Symmetry of the F and G functions and the flip-flops helps optimize the routing of the networks connecting the logic blocks and IOBs.

The next figure shows a modulo 8 binary counter with parallel enable. It uses one CLB of each type.

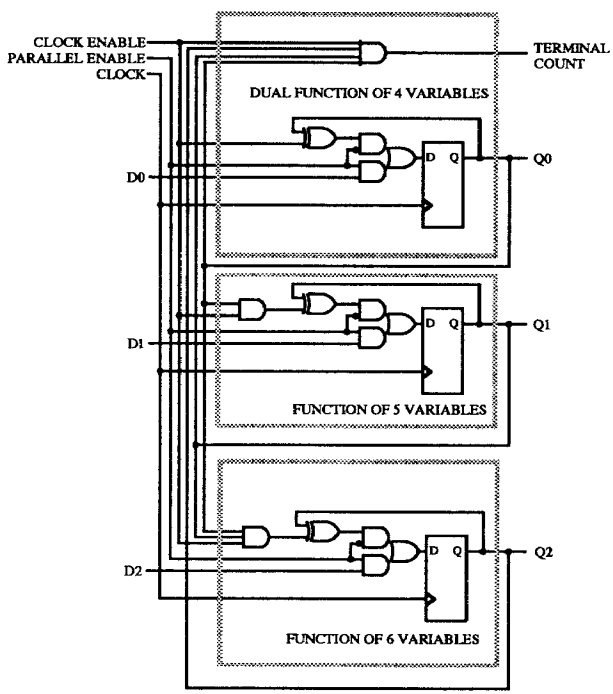


Figure 7. C8BCP Macro (modulo 8 binary counter with parallel enable and clock enable)

INTERCONNECTIONS

Programmable Interconnections

Programmable interconnection resources in the LCA device provide routing paths to connect inputs and outputs of the I/O and logic blocks into logical networks. Interconnections between blocks are composed of two-layer grid of metal segments. Specially designed pass transistors, each controlled by a configuration bit, form programmable interconnect points (PIPs) and switching matrices used to implement the necessary connections between selected metal segments and block pins. The figure below provides an example of a routed net.

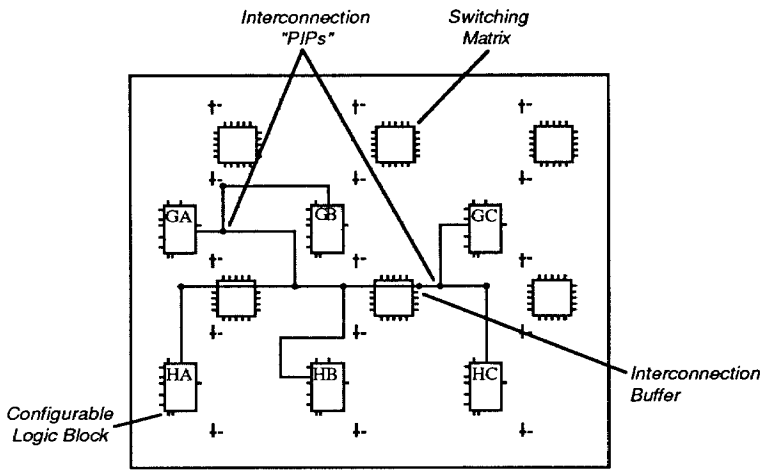


Figure 8. Routing Resources

The PGA Development System automatically routes these interconnections. Interactive routing can also be done to optimize the design. The inputs of the CLB or IOB are multiplexers that can be programmed to select an input network from the adjacent interconnection segments.

Note: The switch connections to block inputs are usable only for input connection, and not for routing, because they are unidirectional (as are block outputs).

The figure below illustrates routing access to logic block input variables, control inputs, and block outputs.

Three types of metal resources are available for network interconnections.

- General-Purpose Interconnection
- Direct Connection
- Long Lines

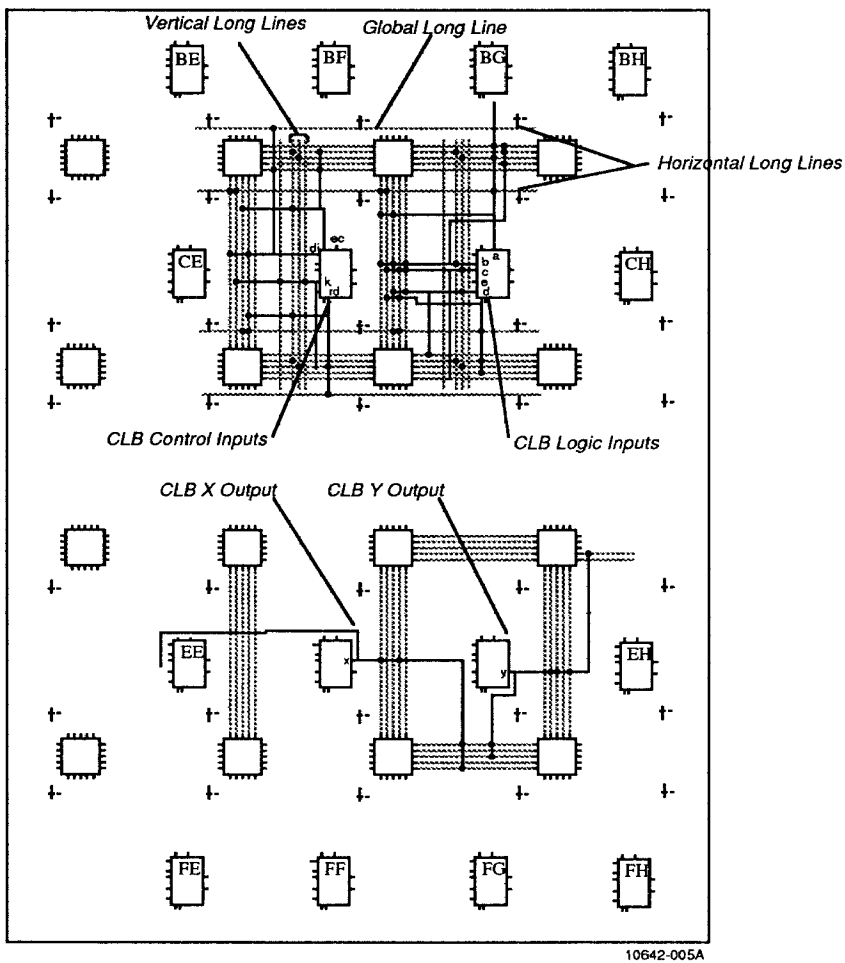


Figure 9. Routing Access to Inputs, Outputs

General-Purpose Interconnections

A general-purpose interconnection, as shown below, consists of a grid of five horizontal and five vertical metal segments located between the rows and columns of CLBs and IOBs. These segments can be connected through switch matrices to form networks for CLB and IOB inputs and outputs.

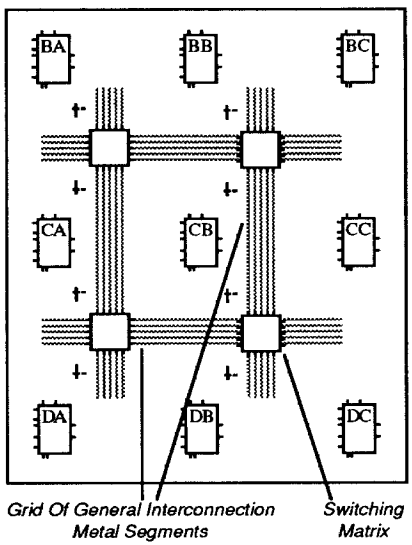


Figure 10. General Purpose Interconnections

Each segment is the height or width of a logic block. Switching matrices join the ends of these segments and allow programmed interconnections between the metal grid segments of adjoining rows and columns. The switches of an unprogrammed device are all non-conducting. The connections through the switch matrix can be made by automatic routing, or by using Editnet to select the desired pairs of matrix pins that are to be connected or disconnected. The legitimate switching matrix combinations for each pin are shown in the next figure, and may be highlighted by the use of the SHOW MATRIX command.

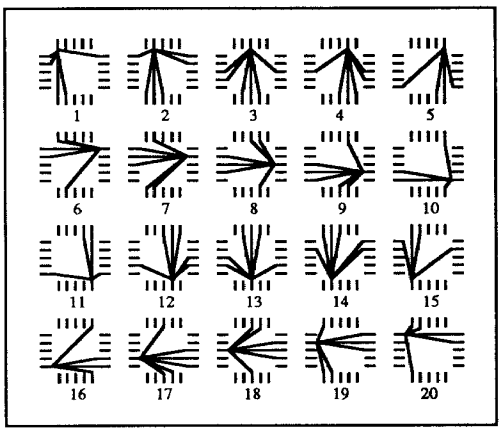


Figure 11. Switch Matrix Interconnection Options

Special buffers in the general interconnection areas are inserted automatically to provide periodic signal isolation and restoration, thus improving performance of lengthy nets. The interconnection buffers can propagate signals in either direction on a general interconnection segment. These bidirectional buffers are above and to the right of the switching matrices, and can be highlighted by the use of the SHOW MATRIX command. The other PIPs adjacent to the matrices are gateways to and from long lines.

The PGA Development System automatically defines the buffer direction based on the location of the interconnection network source. The delay calculator of the PGA Development System automatically calculates and displays the block, interconnection, and buffer delays for the selected paths. It can also generate the simulation net list with a worst-case delay model.

Direct Interconnections

A direct interconnection, shown below, provides the most efficient implementation of networks between adjacent CLBs or IOBs. The .x and .y outputs of each CLB have single contact, direct access to inputs of adjacent CLBs.

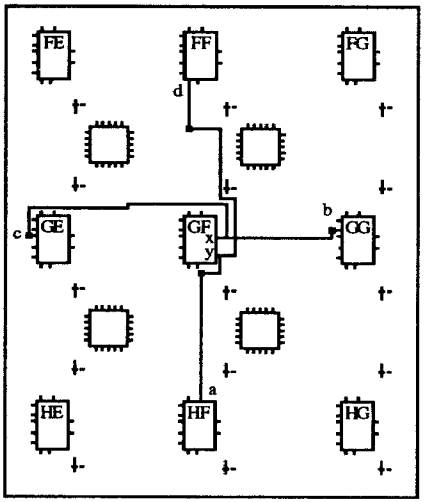


Figure 12. Direct Interconnection

Signals routed from block to block by direct interconnection show minimum interconnection propagation and use no general interconnection resources. For each CLB, the .x output can be connected directly to the .b input of the CLB to its right, and to the .c input of the CLB to its left. The .y output can use a direct interconnection to drive the .d input of the block above, and the .a input of the block below.

Direct interconnection should be used to maximize the speed of high performance portions of logic. Where CLBs are adjacent to IOBs, a direct connection is provided alternately to the IOB inputs (.i) and outputs (.o) on all four edges of the die. The right edge provides additional connections from CLB outputs to adjacent IOBs. Direct interconnections of IOBs and CLBs are shown in the next figure.

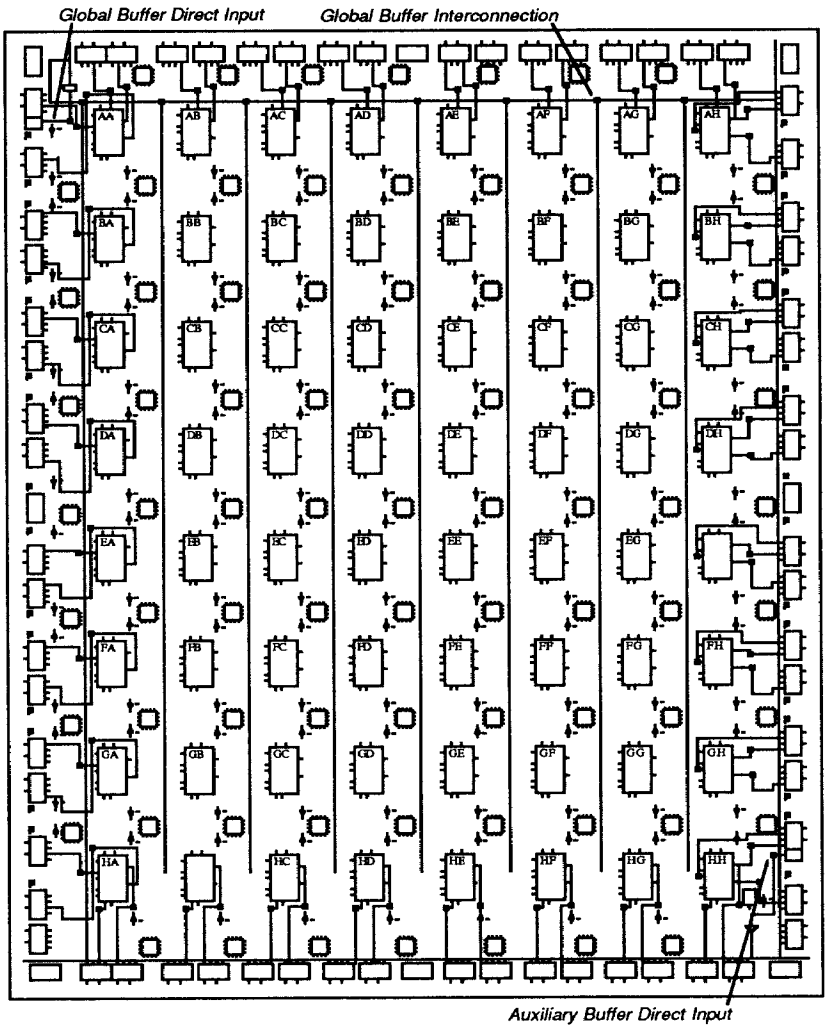


Figure 13. IOB and CLB Direct Interconnections

Long Lines

Long lines, which bypass the switch matrices, are intended primarily for signals that must travel a long distance, or that must have minimum skew among multiple destinations. Long lines, shown below, run the height or width of the interconnection area. Each interconnection column has three vertical long lines, and each interconnection row has two horizontal long lines. Two additional long lines are adjacent to the outer sets of switching matrices. On the Am3020, the outermost long lines are connectable half-length lines. In all other devices, the vertical long lines in each column are also connectable half-length.

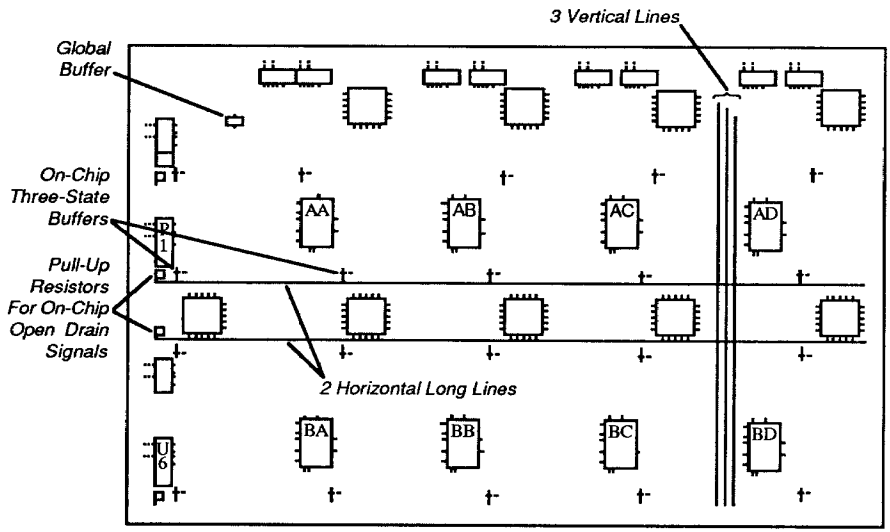


Figure 14. Long Lines

Horizontal and vertical long lines provide high fan-out, low-skew signal distribution in each row and column. The programmable interconnection of long lines is provided at the edges of the routing area. Long lines can be driven by a CLB or IOB output on a column-by-column basis. This provides a common low skew control or clock line within each column of logic blocks. Interconnections of these long lines are shown in the following figure. Isolation buffers are provided at each input to a long line and are enabled automatically by the PGA Development System when a connection is made.

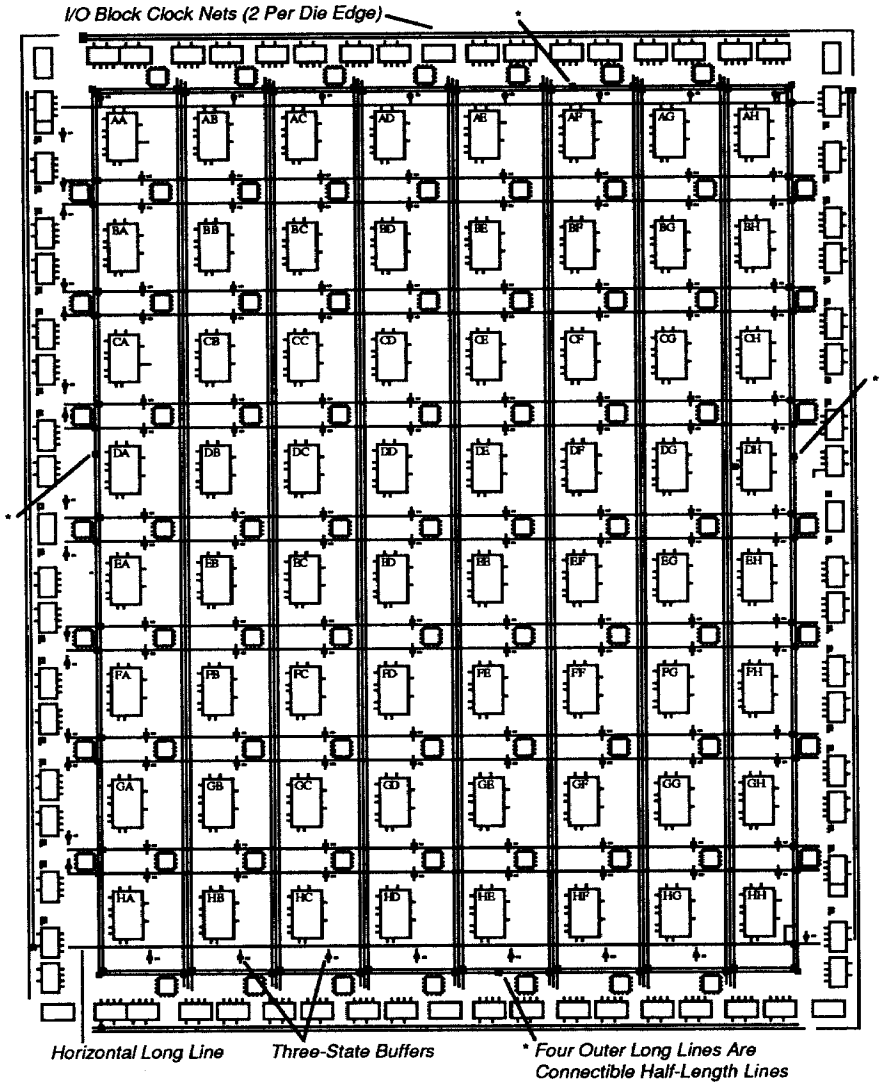


Figure 15. Interconnection of Long Lines

A buffer in the upper left corner of the LCA chip drives a global net available to all .k inputs of logic blocks. Using this global buffer for a clock signal provides a skew free, high fan-out, synchronized clock for use at any, or all, of the I/O and logic blocks. Configuration bits for the .k input to each logic block can select this global line or another routing resource as the clock source for its flip-flops. This net can also be programmed to drive the die edge clock lines for IOB use. TCLKIN is an enhanced speed, CMOS threshold, direct access to this buffer that is available at the second pad from the top of the left die edge.

A buffer in the lower right corner of the array drives a horizontal long line, which can drive programmed connections to a vertical long line in each interconnection column. This alternate buffer also is low skew and high fan-out. The network formed by this alternate buffer's long lines can be selected to drive the .k inputs of the logic blocks. The CMOS threshold, high-speed access to this buffer, BCLKIN, is at the third pad from the bottom of the right die edge.

Internal Busses

A pair of three-state buffers are located adjacent to each CLB. These let logic drive the horizontal long lines. Any three-state buffer input can be selected to drive the horizontal long line bus by applying a low logic level on its three-state control line. Logical operation of the three-state buffer controls lets them implement wide multiplexing functions. When data drives the inputs, and separate signals drive the three-state control lines, these buffers form multiplexers (three-state buses), as shown below. In this case, care must be used to prevent contention through multiple active buffers of conflicting levels on a common line.

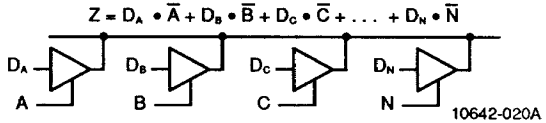


Figure 16. Three-State Buffers Implement a Multiplexer

Control of the three-state input by the same signal that drives the buffer input creates an open drain wired-AND function, as shown below. A logical HIGH on both buffer inputs creates a high impedance with no contention. A logical LOW enables the buffer to drive the long line low. Pull-up resistors are available at each end of the long line to provide a HIGH output when all connected buffers are non-conducting.

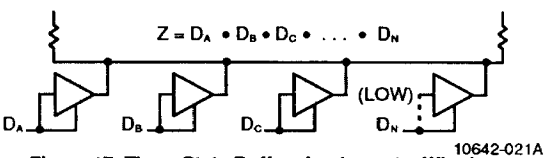


Figure 17. Three-State Buffers Implement a Wired – AND Function

These buffers allow fast, wide gating, optimum speed, and efficient routing of high fan-out signals. The following figure shows three-state buffers, long lines, and pull-up resistors.

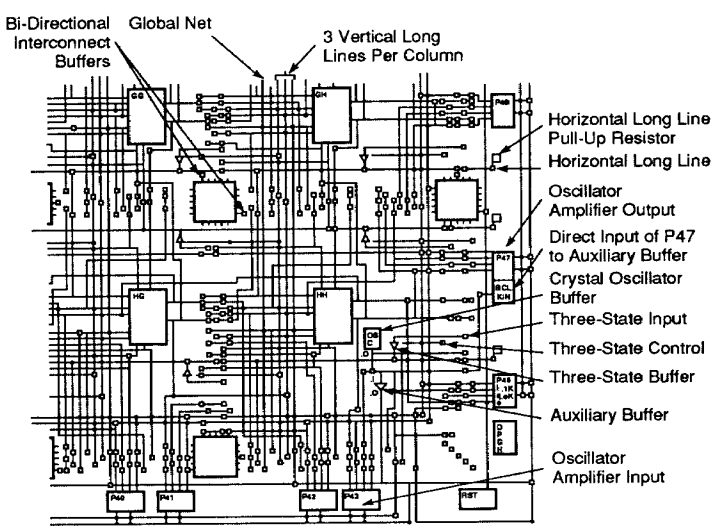


Figure 18. Possible Interconnections in the Lower Right Corner of the Am3020