CYPRESS SEMICONDUCTOR

PRELIMINARY **CYM1400**

32K x 8 SRAM Module

Features

- **Very high speed 256K SRAM module**
  - **Access time of 10 nsec.**
- **300-mil-wide hermetic DIP package**
- **Low active power**
  - **2.1W (max.)**
- **SMD technology**
- **TTL-compatible inputs and outputs**
- **On-chip decode for speed and density**
- **JEDEC pinout—compatible with 7C199 monolithic SRAMs**
- **Small PCB footprint**
  - **0.42 sq. in.**

Functional Description

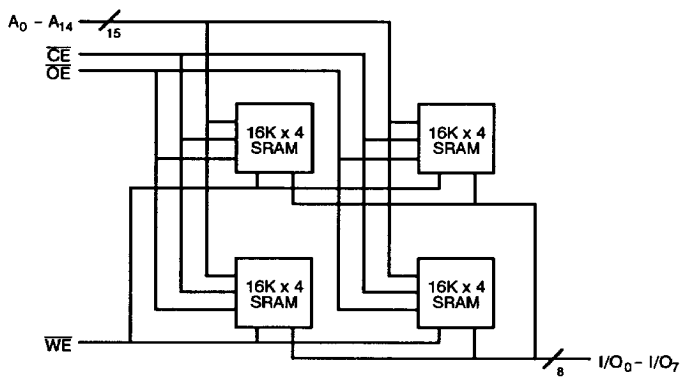
The CYM1400 is an extremely high performance 256-kilobit static RAM module organized as 32,768 words by 8 bits. This module is constructed using four 16K x 4 static RAMs in LCC packages mounted on a 300-mil-wide ceramic substrate. Extremely high speed and density are achieved by using BiCMOS SRAMs containing internal address decoding logic.

Writing to the module is accomplished when the chip enable ($\overline{CE}$) and write enable ($\overline{WE}$) inputs are both LOW. Data on the eight input pins (I/O_0 through I/O_7) of the device is written into the memory location specified on the address pins (A_0 through A_{14}).

Reading the device is accomplished by taking the chip enable ($\overline{CE}$) and output enable ($\overline{OE}$) LOW, while write enable ($\overline{WE}$) remains inactive or HIGH. Under these conditions, the contents of the memory location specified on the address pins (A_0 through A_{14}) will appear on the eight output pins (I/O_0 through I/O_7).

The data output pins remain in a high-impedance state unless the module is selected, outputs are enabled, and write enable ($\overline{WE}$) is HIGH.

Logic Block Diagram



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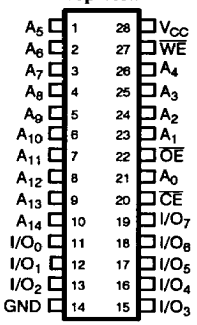
Pin Configuration

DIP
Top View



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Selection Guide

		1400HD-10	1400HD-12	1400HD-15	1400HD-20
Maximum Access Time (ns)		10	12	15	20
Maximum Operating Current (mA)	Commercial	375	375	375	
	Military		425	425	425
Maximum Standby Current (mA)	Commercial	200	200	200	
	Military		250	250	250

Maximum Ratings

(Above which the useful life may be impaired)

Storage Temperature ..... –65°C to +150°C

Ambient Temperature with Power Applied ..... –55°C to +125°C

Supply Voltage to Ground Potential ..... –0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... –0.5V to +7.0V

DC Input Voltage ..... –0.5V to +7.0V

Output Current into Outputs (Low) ..... 20 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Military	–55°C to +125°C	5V ± 10%

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Electrical Characteristics Over the Operating Range

Parameters	Description	Test Conditions		CYM1220HD Min.	CYM1220HD Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = –4.0 mA		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4	V
V_{IH}	Input HIGH Voltage			2.2	V_{CC}	V
V_{IL}	Input LOW Voltage [1]			–0.5	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}		–20	+20	µA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled		–20	+20	µA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, $\overline{CE}$ ≤ V_{IL}	Commercial		375	mA
			Military		425	
I_{SB1}	Automatic $\overline{CE}$ Power-Down Current	V_{CC} = Max., $\overline{CE}$ ≥ V_{IH}, Min. Duty Cycle = 100%	Commercial		200	mA
			Military		250	
I_{SB2}	Automatic $\overline{CE}$ Power-Down Current	V_{CC} = Max., $\overline{CE}$ ≥ V_{CC} – 0.2V, V_{IN} ≥ V_{CC} – 0.2V or V_{IN} ≤ 0.2V	Commercial		200	mA
			Military		250	

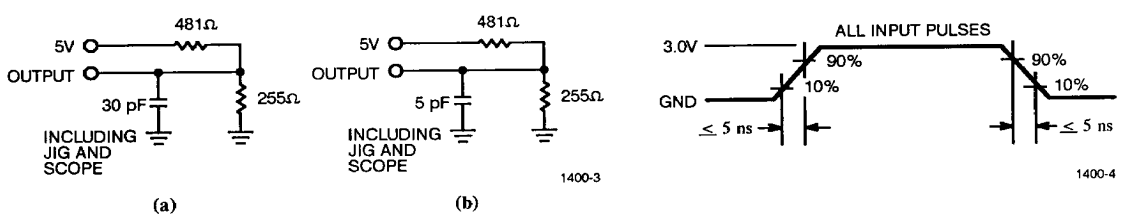
Capacitance[2]

Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	25	pF
C_{OUT}	Output Capacitance		30	pF

Notes:

1. $V_{IL(MIN)}$ = –3.0V for pulse widths less than 20 ns.
2. Tested on a sample basis.

AC Test Loads and Waveforms



Switching Characteristics Over the Operating Range [3]

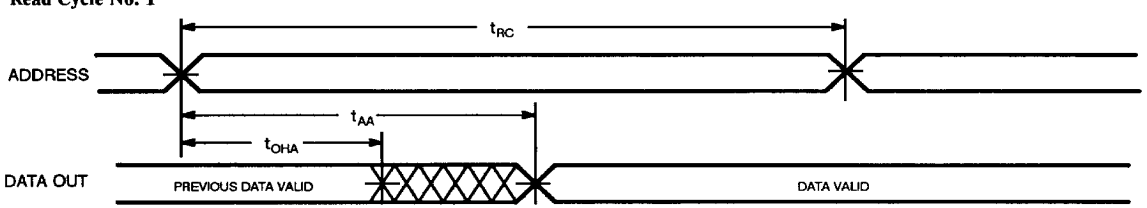
Parameters	Description	1400HD-10		1400HD-12		1400HD-15		1400HD-20		Units
		Min.	Max.	Min.	Max.	Min.	Max.	MIn.	Max.	
READ CYCLE										
t_{RC}	Read Cycle Time	10		12		15		20		ns
t_{AA}	Address to Data Valid		10		12		15		20	ns
t_{OHA}	Data Hold from Address Change	2		3		3		3		ns
t_{ACS}	$\overline{CE}$ LOW to Data Valid		10		12		15		20	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		8		10		10		10	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z	2		2		3		3		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z		8		9		9		9	ns
t_{LZCE}	$\overline{CE}$ LOW to Low Z	2		3		3		3		ns
t_{HZCE}	$\overline{CE}$ HIGH to High Z[4]		6		8		8		8	ns
t_{PU}	$\overline{CE}$ LOW to Power-Up	0		0		0		0		ns
t_{PD}	$\overline{CE}$ HIGH to Power-Down		10		12		15		20	ns
WRITE CYCLE										
t_{WC}	Write Cycle Time	10		12		15		20		ns
t_{SCE}	$\overline{CE}$ LOW to Write End	8		10		12		15		ns
t_{AW}	Address Set-Up to Write End	8		10		12		15		ns
t_{HA}	Address Hold from Write End	1		1		1		1		ns
t_{SA}	Address Set-Up from Write Start	0		0		0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	8		10		12		15		ns
t_{SD}	Data Set-Up to Write End	8		10		10		10		ns
t_{HD}	Data Hold from Write End	1		1		1		1		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z	3		5		5		5		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[4]	0	5	0	7	0	7	0	10	ns

Notes:

3. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
4. t_{HZCS} and t_{HZWE} are specified with C_L = 5 pF as in part (b) of AC Test Loads. Transition is measured ± 500 mV from steady state voltage.
5. The internal write time of the memory is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
6. $\overline{WE}$ is HIGH for read cycle.
7. Device is continuously selected, $\overline{CE}$ = V_I.
8. Address valid prior to or coincident with $\overline{CE}$ transition low.
9. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.

Switching Waveforms

Read Cycle No. 1[6, 7]



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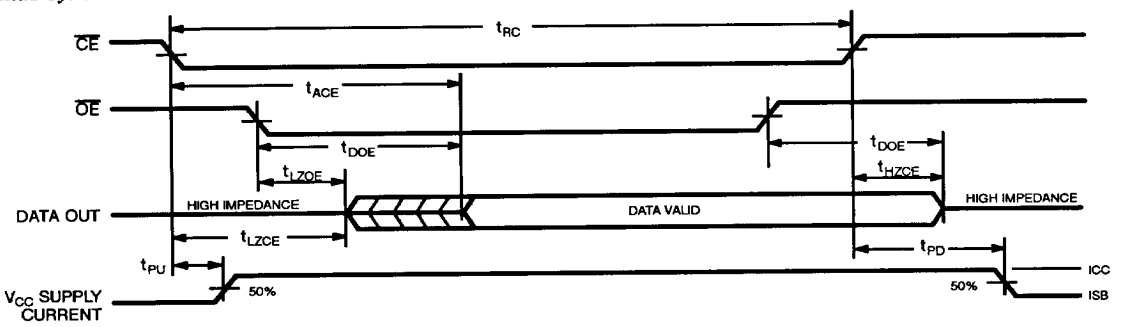
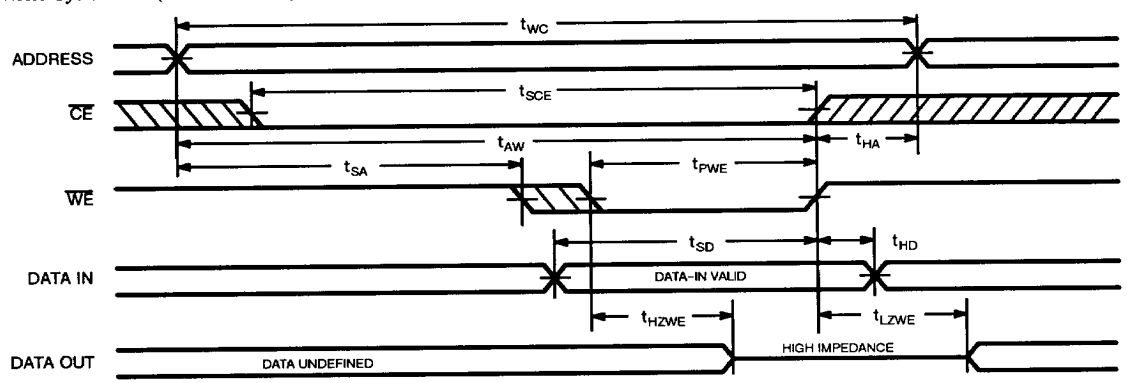
Switching Waveforms (continued)

Read Cycle No. 2[6, 8]



1400-6

Write Cycle No. 1 ($\overline{WE}$ Controlled)[5]



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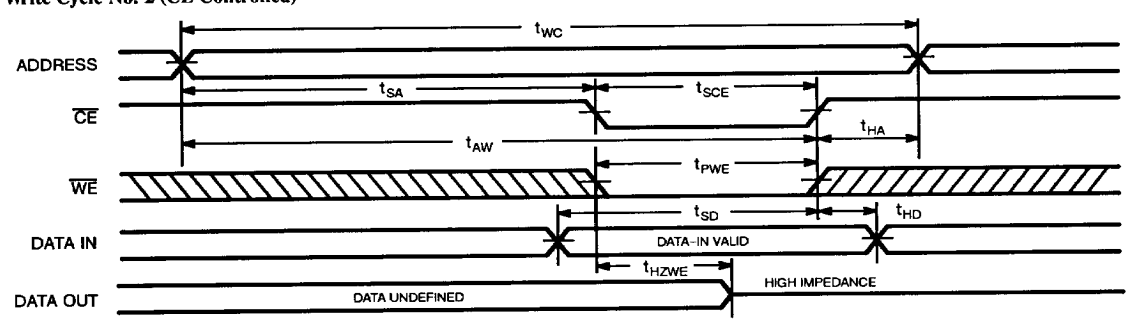
Write Cycle No. 2 ($\overline{CE}$ Controlled)[5, 9]



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Truth Table

$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	Inputs/Outputs	Mode
H	X	X	High Z	Deselect/Power-Down
L	H	L	Data Out	Read Word
L	L	X	Data In	Write Word
L	H	H	High Z	Deselect

Ordering Information

Speed	Ordering Code	Package Type	Operating Range
10	CYM1400HD-10C	HD09	Commercial
12	CYM1400HD-12C	HD09	Commercial
	CYM1400HD-12MB		Military
15	CYM1400HD-15C	HD09	Commercial
	CYM1400HD-15MB		Military
20	CYM1400HD-20MB	HD09	Military

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