# CYM74P435

## 512K Level II Extended Cache Module

### Features

- **512K Cache Module with Extended Cache ability**
- **Synchronous configuration with presence and configuration detect pins**
- **66 MHz operation**
- **Uses high-performance synchronous SRAMs**
- **160-position Burndy DIMM CELP2X80SC3Z48 connector**
- **3.3V compatible inputs/data outputs**

### Functional Description

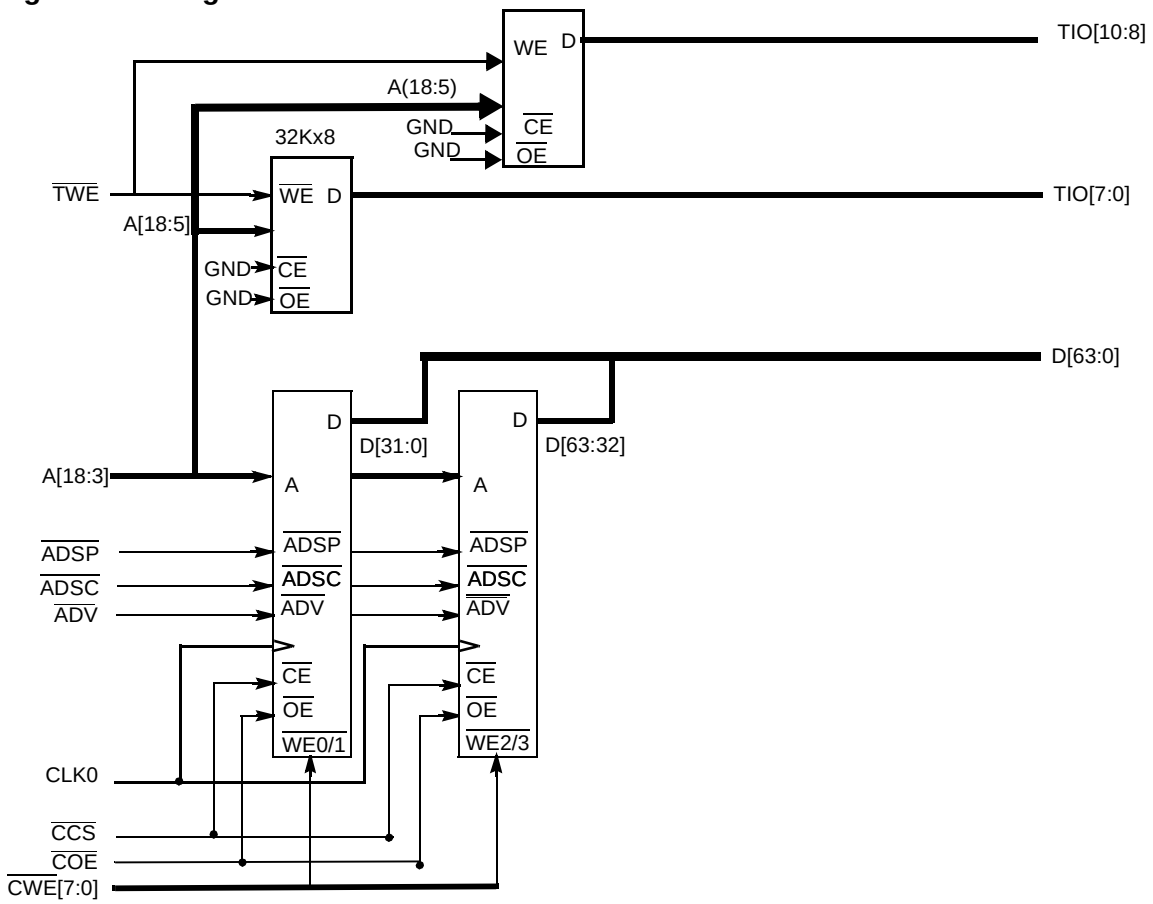
This family of secondary cache modules is designed for Intel P54C systems with the 82430FX (Triton) chipset.

The CYM74P435 is a 512-KB module, organized as 64K by 64-bits with two 32Kx8 tag RAMS that supports 3-1-1-1 read and 4-2-2-2 write cycles at CPU bus speeds up to 66 MHz.

The synchronous modules are available with low cost synchronous pipelined RAMs. The synchronous pipelined modules are based on a 64K x 32 RAM. Multiple ground pins and on-board decoupling capacitors ensure high performance with maximum noise immunity.

All components on the cache modules are surface mounted on a multi-layer epoxy laminate (FR-4) substrate. The contact pins are plated with 150 micro-inches of nickel covered by 10 micro-inches of gold flash.

### Logic Block Diagram - CYM74P435

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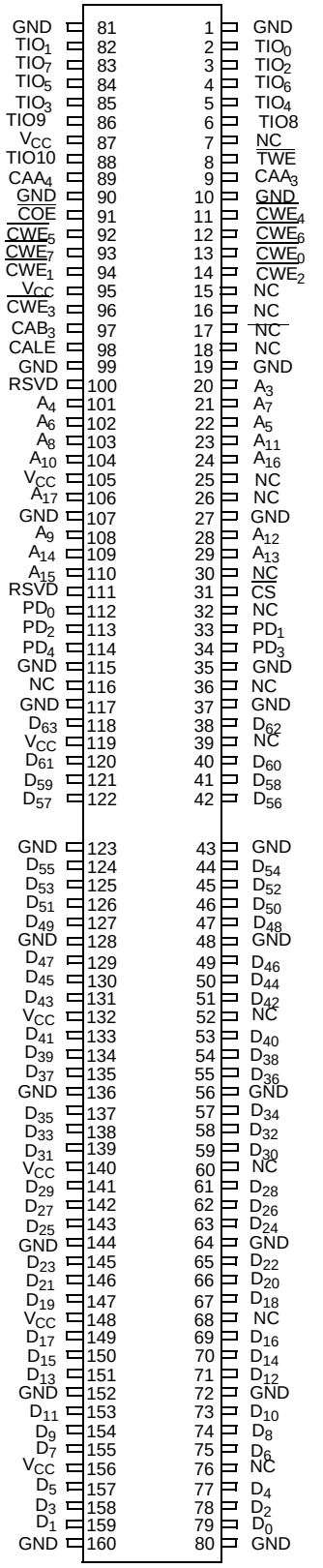
| Part Number | 74P435-66 |
|---|---|
| Cache Size | |
| Ram Type | 512K |
| System Clock (MHz) | 66 |
| Data $t_{CDV}$ | 8.5 ns |
| Tag $t_{AA}$ | 15 ns |

## Pin Configuration

**Dual Read-Out SIMM (DIMM)**
**Top View**




74B435–5

## Pin Definitions

| Common Signals | Description |
|---|---|
| $V_{CC}$ | 3.3V supply |
| GND | Ground |
| A[18:3] | Addresses from processor |
| $\overline{COE}$ | Output Enable |
| $\overline{CWE}$[7:0] | Byte Write Enables |
| $PD_0$-$PD_4$ | Presence Detect output pins |
| D[63:0] | Data lines from processor |
| TIO[10:0] | Tag data bits |
| $\overline{TWE}$ | Tag Write Enable signal |
| NC | Signal not connected on module |
| RSVD | Reserved |
| $V_{CCQ}$ | 3.3V Supply |
| $\overline{ADSP}$ | Processor Address Strobe |
| $\overline{ADSC}$ | Cache Controller Address Strobe |
| $\overline{ADV}$ | Burst Address Advance |
| $\overline{CCS}$ | Chip Select |
| CLK[1:0] | Clock signals, CLK1 not used on CYM74P435 |

## Presence Detect Pins

| | $PD_4$ | $PD_3$ | $PD_2$ | $PD_1$ | $PD_0$ |
|---|---|---|---|---|---|
| Synchronous Burst - CYM74P435 | NC | GND | GND | NC | GND |

## Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature –55°C to +125°C

Ambient Temperature
with Power Applied –0°C to +70°C

3.3V Supply Voltage to Ground Potential –0.5V to +5.25V

5V Supply Voltage to Ground Potential –0.5V to +5.25V

DC Voltage Applied to Outputs
in High Z State –0.5V to +4.6V

DC Input Voltage –0.5V to +4.6V

Output Current into Outputs (LOW)20 mA

## Operating Range

| Range | Ambient Temperature | $V_{CC}$ | $V_{CCQ}$ |
|---|---|---|---|
| Commercial | 0°C to +70°C | 3.3V ± 10% | 3.3V/2.5V +/- 10% |

## Electrical Characteristics Over the Operating Range

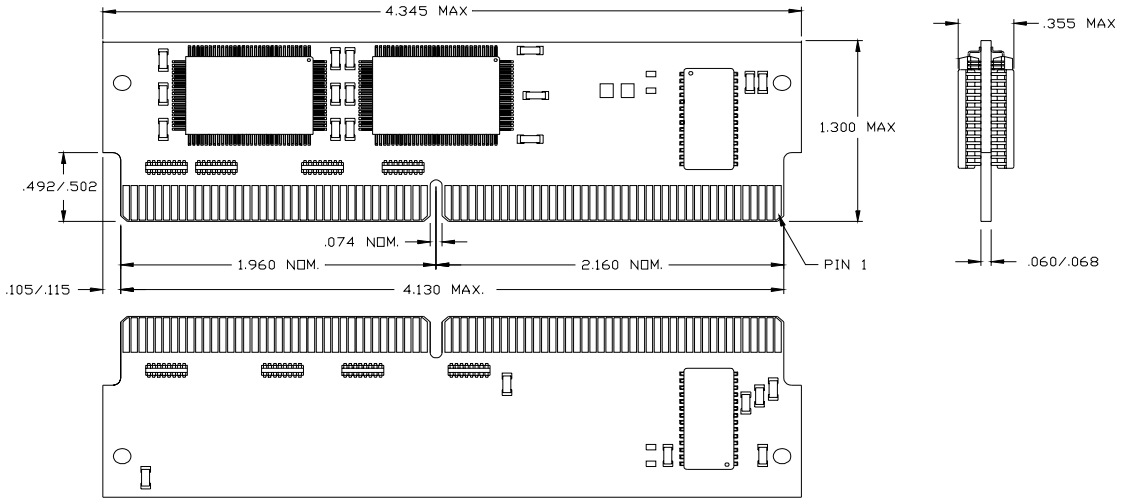
| Parameter | Description | Test Condition | Min. | Max. | Unit |
|---|---|---|---|---|---|
| $V_{IH}$ | Input HIGH Voltage | | 2.2 | $V_{CC}$ + 0.3 | V |
| $V_{IL}$ | Input LOW Voltage | | –0.3 | 0.8 | V |
| $V_{OH}$ | Output HIGH Voltage | $V_{CC}$ = Min. $I_{OH}$ = –4 mA | 2.4 | | V |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$ = Min. $I_{OL}$ = 8 mA | | 0.4 | V |
| $I_{CC}$ (74P435) | $V_{CC}$ Operating Supply Current | $V_{CC}$ = Max., $I_{OUT}$ = 0 mA, f = $f_{MAX}$ = $1/t_{RC}$ | | 1400 | mA |

## Ordering Information

| Speed (MHz) | Ordering Code | Package Name | Package Type | Description | Operating Range |
|---|---|---|---|---|---|
| 66 | CYM74P435CPM-66C | PM49 | 160-pin Dual Read-Out S(D)IMM | Sync pipelined 512 KB | Commercial |

## Package Diagrams

**160-pin Dual Read-Out S(D)IMM PM49**



| Document Title: CYM74P435 512 Level II Extended Cache Module<br>Document Number: 38-05007 | | | | |
|---|---|---|---|---|
| **REV.** | **ECN NO.** | **Issue Date** | **Orig. of Change** | **Description of Change** |
| ** | 106010 | 05/07/01 | MEG | New Spec |