PRELIMINARY

160-common x 132-segment 4-level Gray Scale BITMAP LCD DRIVER

■ GENERAL DESCRIPTION

The **NJU6682** is a 160-common x 132-segment 4-level gray scale bit map LCD driver to display graphics or characters.

It contains 84,480-bit display data RAM, microprocessor interface circuits, instruction decoder, and common and segment drivers.

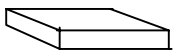
An image data from CPU through the serial or 8-bit/16-bit parallel interface are stored into the 84,480 bits internal display data RAM and are displayed on the LCD panel through the commons and segments drivers.

The **NJU6682** features 4-level gray scale display function creating 4 types of gray scale (white / light gray / dark gray / black) and black & white display function.

The **NJU6682** contains a built-in OSC circuit for reducing external components. And it features Partial Display Function containing selectable active display block(s) (two blocks max.) and optimizing the duty cycle ratio. This function dramatically reduces the operating current, setting the optimum boosted voltage combined with a programmable voltage booster circuit and an electrical variable resister. As result, it reduces the operating current.

The operating voltage from 2.4V to 3.3V and low operating current are suitable for small size battery operation items.

■ PACKAGE OUTLINE



NJU6682CJ

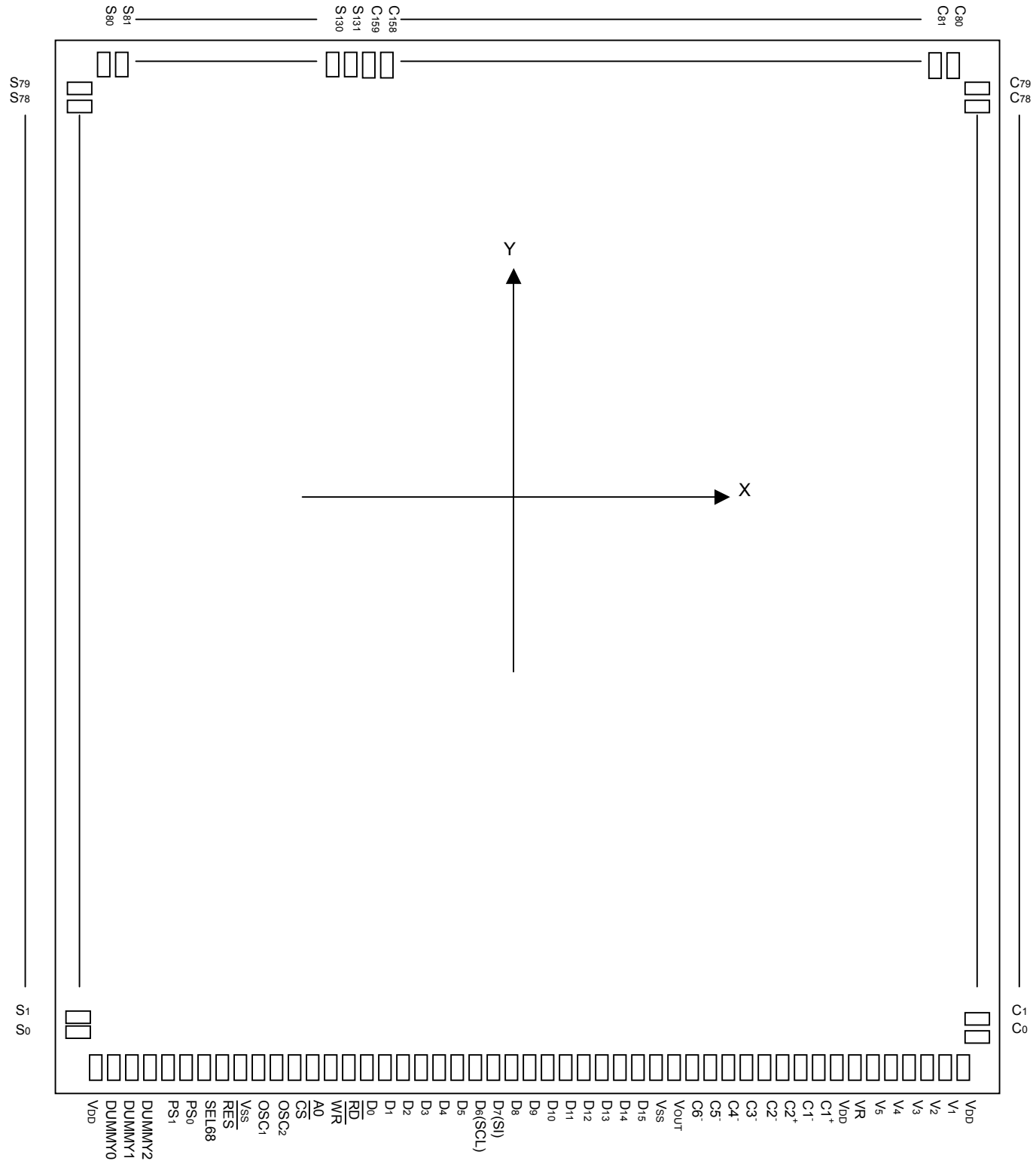
■ FEATURES

- Direct Correspondence of Display Data RAM to LCD Pixel
- Display Method – 4 level Gray Scale / Black & White
- Display Data RAM – 84,480 bits ;(160-Com x 132-Seg) x 2 (double of the display size) x 2bit
- LCD drivers – 160-common and 132-segment
- Direct connection to 8-bit / 16-bit Microprocessor interface for both of 68 and 80 type MPU
- Serial Interface (SI, SCL, A0, $\overline{CS}$)
- Partial Display Function (Two limited active display blocks setting. Duty ratio set automatically.)
- Variable RAM Mapping
  – The display screen can be composed from the RAM area in a maximum of 8 blocks discontinuity.
- Easy Vertical Scroll by setting the start line address of over size display data RAM
  (This function doesn't work in Variable RAM Mapping mode)
- Programmable Bias ratio selection ; 1/4, 1/5, 1/6, 1/7, 1/8, 1/9, 1/10, 1/11, 1/12, 1/13, 1/14 bias
- Common Driver Order Assignment by mask option

Version	C_0 to C_{159} (Pin Name)
NJU6682A	COM_0 to COM_{159}
NJU6682B	COM_{159} to COM_0

- Useful Instruction Sets
  Display ON/OFF, Display Start Line-Address Set, Column-Address Set, Row-Address Set, Status Read, Display Data Read/Write, Normal or Reverse Display, Whole display/Normal display, Partial Display, n-Line Inverse Set, EVR Resister Set, Variable RAM Mapping Mode, Gray Scale Level Select, Bias Select, Booster Select (7-times maximum), Read Modify Write, Reset, Power Supply selection, Driver Outputs ON/OFF, Power Save, ADC Select, Display Mode Select, 8-bit / 16-bit Buss Select.
- Power Supply Circuit for LCD; Programmable Booster Circuits (7 times maximum, Voltage boosting polarity : Negative Voltage (V_{DD} Common), Voltage Adjust Circuit, Voltage Follower (x 4))
- Precision Electrical Variable Resistance (201 Step)
- Low Operating Current T.B.D (typ.)
- Operating Voltage 2.4 to 3.3 V
- LCD Driving Voltage 6.0 to 18.0V
- Package Outline Bumped Chip / COF
- C-MOS Technology (Substrate : N)

■ PAD LOCATION



Chip Center	:X=0um,Y=0um
Chip Size	:X=8.27m,Y=5.67mm
Chip Thickness	:675um +/- 30um
Bump Size	:45um x 83um
Pad Pitch	:60um (min)
Bump Height	:17.5um (typ)
Bump Material	:Au

Voltage boosting polarity : Negative Voltage (V_{DD} Common)
Substrate : N

■ **PAD Coordinates**

Chip Size 8.27×5.67mm(Chip Center X=0μm, Y=0μm)

PAD No.	Terminal	X(um)	Y(um)
1	V_{DD}	-3933	-2675
2	DUMMY0	-3863	-2675
3	DUMMY1	-3793	-2675
4	DUMMY2	-3723	-2675
5	PS_1	-3562	-2675
6	PS_0	-3325	-2675
7	SEL68	-3105	-2675
8	$\overline{RES}$	-2869	-2675
9	V_{SS}	-2712	-2675
10	OSC_1	-2555	-2675
11	OSC_2	-2319	-2675
12	$\overline{CS}$	-2098	-2675
13	A0	-1862	-2675
14	$\overline{WR}$	-1641	-2675
15	$\overline{RD}$	-1405	-2675
16	D_0	-1168	-2675
17	D_1	-948	-2675
18	D_2	-727	-2675
19	D_3	-507	-2675
20	D_4	-287	-2675
21	D_5	-66	-2675
22	D_6(SCL)	153	-2675
23	D_7(SI)	374	-2675
24	D_8	594	-2675
25	D_9	814	-2675
26	D_{10}	1035	-2675
27	D_{11}	1255	-2675
28	D_{12}	1476	-2675
29	D_{13}	1696	-2675
30	D_{14}	1916	-2675
31	D_{15}	2137	-2675
32	V_{SS}	2298	-2675
33	V_{OUT}	2368	-2675
34	$C6^-$	2464	-2675
35	$C5^-$	2613	-2675
36	$C4^-$	2683	-2675
37	$C3^-$	2832	-2675
38	$C2^-$	2902	-2675
39	$C2^+$	3050	-2675
40	$C1^-$	3120	-2675
41	$C1^+$	3269	-2675
42	V_{DD}	3339	-2675
43	VR	3519	-2675
44	V_5	3589	-2675
45	V_4	3659	-2675
46	V_3	3729	-2675
47	V_2	3799	-2675
48	V_1	3869	-2675
49	V_{DD}	3939	-2675
50	C_0	3975	-2186

PAD No.	Terminal	X(um)	Y(um)
51	C_1	3975	-2126
52	C_2	3975	-2066
53	C_3	3975	-2006
54	C_4	3975	-1946
55	C_5	3975	-1886
56	C_6	3975	-1826
57	C_7	3975	-1766
58	C_8	3975	-1706
59	C_9	3975	-1646
60	C_{10}	3975	-1586
61	C_{11}	3975	-1526
62	C_{12}	3975	-1466
63	C_{13}	3975	-1406
64	C_{14}	3975	-1346
65	C_{15}	3975	-1286
66	C_{16}	3975	-1226
67	C_{17}	3975	-1166
68	C_{18}	3975	-1106
69	C_{19}	3975	-1046
70	C_{20}	3975	-986
71	C_{21}	3975	-926
72	C_{22}	3975	-866
73	C_{23}	3975	-806
74	C_{24}	3975	-746
75	C_{25}	3975	-686
76	C_{26}	3975	-626
77	C_{27}	3975	-566
78	C_{28}	3975	-506
79	C_{29}	3975	-446
80	C_{30}	3975	-386
81	C_{31}	3975	-326
82	C_{32}	3975	-266
83	C_{33}	3975	-206
84	C_{34}	3975	-146
85	C_{35}	3975	-86
86	C_{36}	3975	-26
87	C_{37}	3975	34
88	C_{38}	3975	94
89	C_{39}	3975	154
90	C_{40}	3975	214
91	C_{41}	3975	274
92	C_{42}	3975	334
93	C_{43}	3975	394
94	C_{44}	3975	454
95	C_{45}	3975	514
96	C_{46}	3975	574
97	C_{47}	3975	634
98	C_{48}	3975	694
99	C_{49}	3975	754
100	C_{50}	3975	814

PAD No.	Terminal	X(um)	Y(um)
101	C_{51}	3975	874
102	C_{52}	3975	934
103	C_{53}	3975	994
104	C_{54}	3975	1054
105	C_{55}	3975	1114
106	C_{56}	3975	1174
107	C_{57}	3975	1234
108	C_{58}	3975	1294
109	C_{59}	3975	1354
110	C_{60}	3975	1414
111	C_{61}	3975	1474
112	C_{62}	3975	1534
113	C_{63}	3975	1594
114	C_{64}	3975	1654
115	C_{65}	3975	1714
116	C_{66}	3975	1774
117	C_{67}	3975	1834
118	C_{68}	3975	1894
119	C_{69}	3975	1954
120	C_{70}	3975	2014
121	C_{71}	3975	2074
122	C_{72}	3975	2134
123	C_{73}	3975	2194
124	C_{74}	3975	2254
125	C_{75}	3975	2314
126	C_{76}	3975	2374
127	C_{77}	3975	2434
128	C_{78}	3975	2494
129	C_{79}	3975	2554
130	C_{80}	3930	2675
131	C_{81}	3870	2675
132	C_{82}	3810	2675
133	C_{83}	3750	2675
134	C_{84}	3690	2675
135	C_{85}	3630	2675
136	C_{86}	3570	2675
137	C_{87}	3510	2675
138	C_{88}	3450	2675
139	C_{89}	3390	2675
140	C_{90}	3330	2675
141	C_{91}	3270	2675
142	C_{92}	3210	2675
143	C_{93}	3150	2675
144	C_{94}	3090	2675
145	C_{95}	3030	2675
146	C_{96}	2970	2675
147	C_{97}	2910	2675
148	C_{98}	2850	2675
149	C_{99}	2790	2675
150	C_{100}	2730	2675

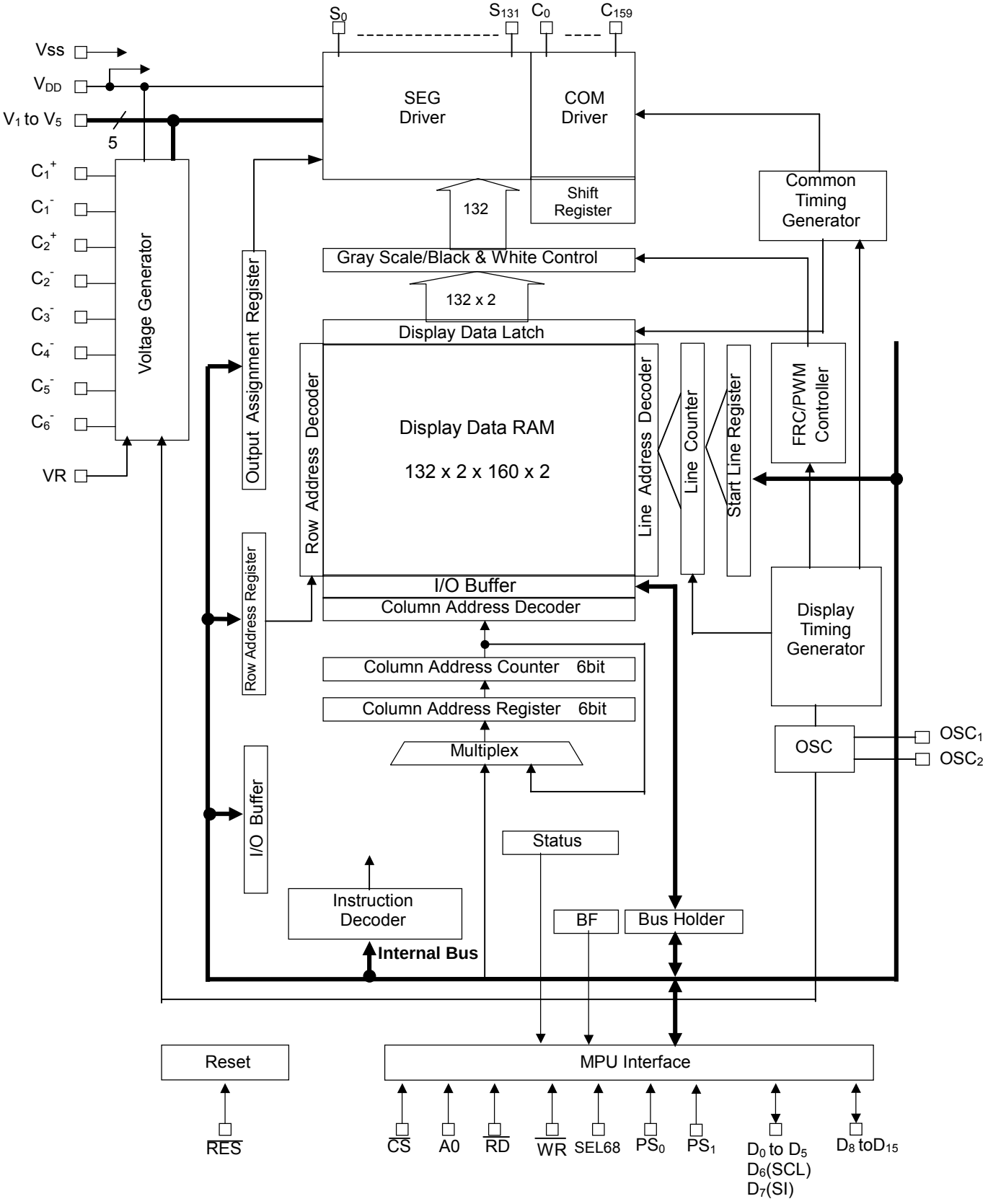
PAD No.	Terminal	X(um)	Y(um)
151	C_{101}	2670	2675
152	C_{102}	2610	2675
153	C_{103}	2550	2675
154	C_{104}	2490	2675
155	C_{105}	2430	2675
156	C_{106}	2370	2675
157	C_{107}	2310	2675
158	C_{108}	2250	2675
159	C_{109}	2190	2675
160	C_{110}	2130	2675
161	C_{111}	2070	2675
162	C_{112}	2010	2675
163	C_{113}	1950	2675
164	C_{114}	1890	2675
165	C_{115}	1830	2675
166	C_{116}	1770	2675
167	C_{117}	1710	2675
168	C_{118}	1650	2675
169	C_{119}	1590	2675
170	C_{120}	1530	2675
171	C_{121}	1470	2675
172	C_{122}	1410	2675
173	C_{123}	1350	2675
174	C_{124}	1290	2675
175	C_{125}	1230	2675
176	C_{126}	1170	2675
177	C_{127}	1110	2675
178	C_{128}	1050	2675
179	C_{129}	990	2675
180	C_{130}	930	2675
181	C_{131}	870	2675
182	C_{132}	810	2675
183	C_{133}	750	2675
184	C_{134}	690	2675
185	C_{135}	630	2675
186	C_{136}	570	2675
187	C_{137}	510	2675
188	C_{138}	450	2675
189	C_{139}	390	2675
190	C_{140}	330	2675
191	C_{141}	270	2675
192	C_{142}	210	2675
193	C_{143}	150	2675
194	C_{144}	90	2675
195	C_{145}	30	2675
196	C_{146}	-30	2675
197	C_{147}	-90	2675
198	C_{148}	-150	2675
199	C_{149}	-210	2675
200	C_{150}	-270	2675

PAD No.	Terminal	X(um)	Y(um)
201	C_{151}	-330	2675
202	C_{152}	-390	2675
203	C_{153}	-450	2675
204	C_{154}	-510	2675
205	C_{155}	-570	2675
206	C_{156}	-630	2675
207	C_{157}	-690	2675
208	C_{158}	-750	2675
209	C_{159}	-810	2675
210	S_{131}	-870	2675
211	S_{130}	-930	2675
212	S_{129}	-990	2675
213	S_{128}	-1050	2675
214	S_{127}	-1110	2675
215	S_{126}	-1170	2675
216	S_{125}	-1230	2675
217	S_{124}	-1290	2675
218	S_{123}	-1350	2675
219	S_{122}	-1410	2675
220	S_{121}	-1470	2675
221	S_{120}	-1530	2675
222	S_{119}	-1590	2675
223	S_{118}	-1650	2675
224	S_{117}	-1710	2675
225	S_{116}	-1770	2675
226	S_{115}	-1830	2675
227	S_{114}	-1890	2675
228	S_{113}	-1950	2675
229	S_{112}	-2010	2675
230	S_{111}	-2070	2675
231	S_{110}	-2130	2675
232	S_{109}	-2190	2675
233	S_{108}	-2250	2675
234	S_{107}	-2310	2675
235	S_{106}	-2370	2675
236	S_{105}	-2430	2675
237	S_{104}	-2490	2675
238	S_{103}	-2550	2675
239	S_{102}	-2610	2675
240	S_{101}	-2670	2675
241	S_{100}	-2730	2675
242	S_{99}	-2790	2675
243	S_{98}	-2850	2675
244	S_{97}	-2910	2675
245	S_{96}	-2970	2675
246	S_{95}	-3030	2675
247	S_{94}	-3090	2675
248	S_{93}	-3150	2675
249	S_{92}	-3210	2675
250	S_{91}	-3270	2675

PAD No.	Terminal	X(um)	Y(um)
251	S_{90}	-3330	2675
252	S_{89}	-3390	2675
253	S_{88}	-3450	2675
254	S_{87}	-3510	2675
255	S_{86}	-3570	2675
256	S_{85}	-3630	2675
257	S_{84}	-3690	2675
258	S_{83}	-3750	2675
259	S_{82}	-3810	2675
260	S_{81}	-3870	2675
261	S_{80}	-3930	2675
262	S_{79}	-3975	2517
263	S_{78}	-3975	2457
264	S_{77}	-3975	2397
265	S_{76}	-3975	2337
266	S_{75}	-3975	2277
267	S_{74}	-3975	2217
268	S_{73}	-3975	2157
269	S_{72}	-3975	2097
270	S_{71}	-3975	2037
271	S_{70}	-3975	1977
272	S_{69}	-3975	1917
273	S_{68}	-3975	1857
274	S_{67}	-3975	1797
275	S_{66}	-3975	1737
276	S_{65}	-3975	1677
277	S_{64}	-3975	1617
278	S_{63}	-3975	1557
279	S_{62}	-3975	1497
280	S_{61}	-3975	1437
281	S_{60}	-3975	1377
282	S_{59}	-3975	1317
283	S_{58}	-3975	1257
284	S_{57}	-3975	1197
285	S_{56}	-3975	1137
286	S_{55}	-3975	1077
287	S_{54}	-3975	1017
288	S_{53}	-3975	957
289	S_{52}	-3975	897
290	S_{51}	-3975	837
291	S_{50}	-3975	777
292	S_{49}	-3975	717
293	S_{48}	-3975	657
294	S_{47}	-3975	597
295	S_{46}	-3975	537
296	S_{45}	-3975	477
297	S_{44}	-3975	417
298	S_{43}	-3975	357
299	S_{42}	-3975	297
300	S_{41}	-3975	237

PAD No.	Terminal	X(um)	Y(um)
301	S_{40}	-3975	177
302	S_{39}	-3975	117
303	S_{38}	-3975	57
304	S_{37}	-3975	-2
305	S_{36}	-3975	-62
306	S_{35}	-3975	-122
307	S_{34}	-3975	-182
308	S_{33}	-3975	-242
309	S_{32}	-3975	-302
310	S_{31}	-3975	-362
311	S_{30}	-3975	-422
312	S_{29}	-3975	-482
313	S_{28}	-3975	-542
314	S_{27}	-3975	-602
315	S_{26}	-3975	-662
316	S_{25}	-3975	-722
317	S_{24}	-3975	-782
318	S_{23}	-3975	-842
319	S_{22}	-3975	-902
320	S_{21}	-3975	-962
321	S_{20}	-3975	-1022
322	S_{19}	-3975	-1082
323	S_{18}	-3975	-1142
324	S_{17}	-3975	-1202
325	S_{16}	-3975	-1262
326	S_{15}	-3975	-1322
327	S_{14}	-3975	-1382
328	S_{13}	-3975	-1442
329	S_{12}	-3975	-1502
330	S_{11}	-3975	-1562
331	S_{10}	-3975	-1622
332	S_9	-3975	-1682
333	S_8	-3975	-1742
334	S_7	-3975	-1802
335	S_6	-3975	-1862
336	S_5	-3975	-1922
337	S_4	-3975	-1982
338	S_3	-3975	-2042
339	S_2	-3975	-2102
340	S_1	-3975	-2162
341	S_0	-3975	-2222

■ BLOCK DIAGRAM



■ TERMINAL DESCRIPTION

<table>
<tr><th>No.</th><th>Symbol</th><th>I/O</th><th>Function</th></tr>
<tr><td>2 – 4</td><td>$DUMMY_0$ – $DUMMY_2$</td><td></td><td>Dummy Terminals
These are open terminals electrically.</td></tr>
<tr><td>1,42,49</td><td>V_{DD}</td><td>Power</td><td>Power Supply Terminal (+2.4V – +3.3V)</td></tr>
<tr><td>9,32</td><td>V_{SS}</td><td>GND</td><td>Ground terminal (0V)</td></tr>
<tr><td>48
47
46
45
44</td><td>V_1
V_2
V_3
V_4
V_5</td><td>Power</td><td>LCD Driving Voltage Supplying Terminals. In case of the external power supply operation without internal power supply operation, each level of LCD driving voltage is supplied from outside fitting with following relation.
$V_{DD} \geq V_1 \geq V_2 \geq V_3 \geq V_4 \geq V_5 \geq V_{OUT}$
In case of the internal power supply, LCD driving voltages V_1-V_4 depending on the Bias selection are supplied as shown in follows;
<table>
<tr><th>Bias</th><th>V_1</th><th>V_2</th><th>V_3</th><th>V_4</th></tr>
<tr><td>1/4Bias</td><td>$V_5+3/4V_{LCD}$</td><td>$V_5+2/4V_{LCD}$</td><td>$V_5+2/4V_{LCD}$</td><td>$V_5+1/4V_{LCD}$</td></tr>
<tr><td>1/5Bias</td><td>$V_5+4/5V_{LCD}$</td><td>$V_5+3/5V_{LCD}$</td><td>$V_5+2/5V_{LCD}$</td><td>$V_5+1/5V_{LCD}$</td></tr>
<tr><td>1/6Bias</td><td>$V_5+5/6V_{LCD}$</td><td>$V_5+4/6V_{LCD}$</td><td>$V_5+2/6V_{LCD}$</td><td>$V_5+1/6V_{LCD}$</td></tr>
<tr><td>1/7Bias</td><td>$V_5+6/7V_{LCD}$</td><td>$V_5+5/7V_{LCD}$</td><td>$V_5+2/7V_{LCD}$</td><td>$V_5+1/7V_{LCD}$</td></tr>
<tr><td>1/8Bias</td><td>$V_5+7/8V_{LCD}$</td><td>$V_5+6/8V_{LCD}$</td><td>$V_5+2/8V_{LCD}$</td><td>$V_5+1/8V_{LCD}$</td></tr>
<tr><td>1/9Bias</td><td>$V_5+8/9V_{LCD}$</td><td>$V_5+7/9V_{LCD}$</td><td>$V_5+2/9V_{LCD}$</td><td>$V_5+1/9V_{LCD}$</td></tr>
<tr><td>1/10Bias</td><td>$V_5+9/10V_{LCD}$</td><td>$V_5+8/10V_{LCD}$</td><td>$V_5+2/10V_{LCD}$</td><td>$V_5+1/10V_{LCD}$</td></tr>
<tr><td>1/11Bias</td><td>$V_5+10/11V_{LCD}$</td><td>$V_5+9/11V_{LCD}$</td><td>$V_5+2/11V_{LCD}$</td><td>$V_5+1/11V_{LCD}$</td></tr>
<tr><td>1/12Bias</td><td>$V_5+11/12V_{LCD}$</td><td>$V_5+10/12V_{LCD}$</td><td>$V_5+2/12V_{LCD}$</td><td>$V_5+1/12V_{LCD}$</td></tr>
<tr><td>1/13Bias</td><td>$V_5+12/13V_{LCD}$</td><td>$V_5+11/13V_{LCD}$</td><td>$V_5+2/13V_{LCD}$</td><td>$V_5+1/13V_{LCD}$</td></tr>
<tr><td>1/14Bias</td><td>$V_5+13/14V_{LCD}$</td><td>$V_5+12/14V_{LCD}$</td><td>$V_5+2/14V_{LCD}$</td><td>$V_5+1/14V_{LCD}$</td></tr>
</table>
($V_{LCD}=V_{DD}-V_5$)</td></tr>
<tr><td>41
40
39
38
37
36
35
34</td><td>$C1^+$
$C1^-$
$C2^+$
$C2^-$
$C3^-$
$C4^-$
$C5^-$
$C6^-$</td><td>O</td><td>Capacitor connecting terminals for Internal Voltage Booster.
Boosting time is programmed by instruction (2 to 7 times)</td></tr>
<tr><td>33</td><td>V_{OUT}</td><td>O</td><td>Boosted voltage output terminal. Connects the capacitor between V_{OUT} terminal and V_{SS}.</td></tr>
<tr><td>43</td><td>VR</td><td>I</td><td>V_{LCD} voltage adjustment terminal. The gain of VLCD setup circuit for V5 level is adjusted by external resistors.</td></tr>
<tr><td>16 – 23
(22,23)</td><td>D_0 – D_7
(SCL, SI)</td><td>I/O</td><td>Data Input/Output terminals.
In Pararel Interface Mode (PS_1="H", PS_0="H"/"L")
•8-bit bus mode*1: I/O terminals of 8-bit bus.
•16-bit bus mode*1: I/O terminals of lower 8-bit of 16-bit bus

*1 8-bit or 16-bit bus is set by the "8-bit / 16-bit Bus Select" instruction

In Serial Interface Mode(PS_1="L", PS_0="H"/"L")
•D_7: Input terminal of serial data (SI).
•D_6: Input terminal of serial data clock (SCL).
D0 to D5 terminals are Hi-impedance

When $\overline{CS}$="H", D_0 to D_7 terminals are Hi-impedance.</td></tr>
<tr><td>24 – 30</td><td>D_8 – D_{15}</td><td>I/O</td><td>Data Input/Output terminals
In 16-bit Bus interface Mode (PS_1="H", PS_0="H"/"L")
•I/O terminals of upper 8-bit of 16-bit bus.
In 8-bit Bus or Serial interface Mode
• D_8 to D_{15} terminals are Hi-impedance</td></tr>
</table>

<table>
<tr><th>No.</th><th>Symbol</th><th>I/O</th><th>Description</th></tr>
<tr><td>13</td><td>A0</td><td>I</td><td>Data discremination signal input terminal. The signal from MPU discreminates transmoitted data between Display data and Instruction.
<table>
<tr><td>A0</td><td>H</td><td>L</td></tr>
<tr><td>Distin.</td><td>Display Data</td><td>Instruction</td></tr>
</table></td></tr>
<tr><td>8</td><td>$\overline{RES}$</td><td>I</td><td>Reset terminal.
When the RES terminal goes to ”L”, the initialization is performed.
Reset operation is executing during “L” state of RES.</td></tr>
<tr><td>12</td><td>$\overline{CS}$</td><td>I</td><td>Chip select signal input terminal.
Data Input/Output are available during $\overline{CS}$=”L”.</td></tr>
<tr><td rowspan="2">15</td><td>$\overline{RD}$</td><td>I</td><td>RD(80 type) or E(68 type) signal input terminal.
•In 80 type MPU mode (PS_1=”H”, SEL68=”L”)
RD signal from 80 type MPU input terminal. Active “L”.
D_0 to D_7 terminals are output during “L” level.</td></tr>
<tr><td>(E)</td><td>I</td><td>•In 68 type MPU mode (PS_1=”H”, SEL68=”H”)
Enable signal from 68 type MPU input terminal. Active “H”.</td></tr>
<tr><td rowspan="2">14</td><td>$\overline{WR}$</td><td>I</td><td>$\overline{WR}$(80 type) or R/W(68 type) signal input terminal
•In 80 type MPU mode (PS_1=”H”, SEL68=”L”)
WR signal from 80 type MPU input terminal. Active “L”.
The data transmitted during WR=”L” are fetched at the rising edge of $\overline{WR}$.</td></tr>
<tr><td>(R/W)</td><td></td><td>•In 68 type MPU mode (PS_1=”H”, SEL68=”H”)
R/W signal from 68 type MPU input terminal.
<table>
<tr><td>R/W</td><td>H</td><td>L</td></tr>
<tr><td>State</td><td>Read</td><td>Write</td></tr>
</table></td></tr>
<tr><td>7</td><td>SEL68</td><td>I</td><td>MPU interface type selection terminal. This terminal must connect to V_{DD} or V_{SS}.
<table>
<tr><td>SEL68</td><td>H</td><td>L</td></tr>
<tr><td>State</td><td>68 Type</td><td>80 Type</td></tr>
</table></td></tr>
<tr><td>6
5</td><td>PS_0
PS_1</td><td>I</td><td>Parallel or Serial interface selection signal input terminal.
<table>
<tr><th>PS_1</th><th>PS_0</th><th>Interface</th><th>Chip Select</th><th>Data/ Instruction</th><th>Data</th><th>Read/ Write</th><th>Serial Clock</th></tr>
<tr><td>H</td><td>L/H</td><td>Parallel</td><td>$\overline{CS}$</td><td>A0</td><td>D_0~D_7,
D_8~D_{15}</td><td>$\overline{RD}$,$\overline{WR}$</td><td>-</td></tr>
<tr><td rowspan="2">L</td><td>H</td><td>Serial 4-wire</td><td>$\overline{CS}$</td><td>A0</td><td>SI(D_7)</td><td>-</td><td>SCL(D_6)</td></tr>
<tr><td>L</td><td>Serial 3-wire</td><td>$\overline{CS}$</td><td>Every 17th data of Serial data is recognized as A0.</td><td>SI(D_7)</td><td>-</td><td>SCL(D_6)</td></tr>
</table>
In case of serial interface(PS_1=”L”,PS_0=”H/L”),
$\overline{RD}$ and $\overline{WR}$ terminals must fix to “H” or “L”. D_0 to D_5 and D_8 to D_{15} terminals are Hi-impedance.</td></tr>
<tr><td>10
11</td><td>OSC_1
OSC_2</td><td>I/O</td><td>External clock input terminal.
In Internal oscillation operation, OSC_1 and OSC_2 terminals should be Open.
In External clock operation, the external clock input to OSC_1 terminal.</td></tr>
</table>

<table>
<tr><th>No.</th><th>Symbol</th><th>I/O</th><th>Function</th></tr>
<tr><td>50
– 209</td><td>C_0 – C_{159}</td><td>O</td><td rowspan="2">LCD driving signal output terminal.
•Common output terminal: C_0 to C_{159}
•Segment output terminal: S_0 to S_{131}

•Common output terminal
Following output voltage is selected by the combination of alternating (FR) signal and Common scanning data.
<table>
<tr><th>Scanning Data</th><th>Alternating (FR)</th><th>Common terminal Output Voltage</th></tr>
<tr><td rowspan="2">H</td><td>H</td><td>V_5</td></tr>
<tr><td>L</td><td>V_{DD}</td></tr>
<tr><td rowspan="2">L</td><td>H</td><td>V_1</td></tr>
<tr><td>L</td><td>V_4</td></tr>
</table>
•Segment output terminal
Following output voltage is selected by the combination of alternating (FR) signal and display data in the DD RAM.
<table>
<tr><th rowspan="2">Scanning Data</th><th rowspan="2">Alternating (FR)</th><th colspan="2">Segment terminal Output Voltage</th></tr>
<tr><th>Normal Display</th><th>Reverse Display</th></tr>
<tr><td rowspan="2">H</td><td>H</td><td>V_{DD}</td><td>V_2</td></tr>
<tr><td>L</td><td>V_5</td><td>V_3</td></tr>
<tr><td rowspan="2">L</td><td>H</td><td>V_2</td><td>V_{DD}</td></tr>
<tr><td>L</td><td>V_3</td><td>V_5</td></tr>
</table>
</td></tr>
<tr><td>341
– 210</td><td>S_0 – S_{131}</td><td>O</td></tr>
</table>

■ Functional Description

(1) Description of each blocks

(1-1) Busy Flag (BF)

The Busy Flag (BF) is set to logical “1” in busy of internal execution by an instruction, and any instruction excepting for the “Status Read” is disable at this time. Busy Flag is outputted through D_7 terminal by “Status Read” instruction. Although another instructions should be inputted after check of Busy Flag, no need to check Busy flag if the system cycle time (t_{CYC}) as shown in “AC Characteristics” is secured completely.

(1-2) Display Start Line Register

The Display Start Line Register is a register to set a display data RAM address corresponding to the COM_0 display line (the top line normally) for the vertical scroll on the LCD, Row address change and so forth. The Display Start Line Address set instruction sets the 9-bit display start address into this register.

(1-3) Line Counter

Line Counter is reset when the internal FR signal is switched and outputs the line address of the display data RAM by count up operation synchronizing with common cycle of **NJU6682**.

(1-4) Column Address Counter

Column Address Counter is the 6-bit preset-able counter to point the column address of the display data RAM (DD RAM) as shown in Figure 1-1 and 1-2. The counter is incremented automatically after the display data read/write instructions execution. When the column address counter reaches to the maximum existing address by the increment operations, the count up operation (increment) is frozen. However, when new address is set to the column address counter again, it restarts the count up operation from a set address. The operation of Column Address Counter is independent against Row Address Register.

By the address inverse instruction (ADC select) as shown in Figure 1-1 and 1-2, Column Address Decoder reverses the correspondence between Column address and Segment output of display data RAM.

(1-5) Row Address Register

Row Address Register assigns the row address of the display data RAM as shown in Figure 1-1 and 1-2. In case of accessing from the MPU with changing the row address, Row Address Set instruction is required.

(1-6) Display data RAM (DD RAM)

The Display data RAM (DD RAM) is the bit map RAM consisting of 84,480 bits to store the display data corresponding to the LCD pixel on LCD panel. Each LCD pixel corresponds to two bits in the display data RAM in gray scale mode and to one bit in black & white mode, display data respectively.

The DD RAM data : "00" = Gray Scale Level 0 (Set by the “Gray Scale Level Select” instruction)
The DD RAM data : "01" = Gray Scale Level 1 (“)
The DD RAM data : "10" = Gray Scale Level 2 (“)
The DD RAM data : "11" = Gray Scale Level 3 (“)

The DD RAM data and the state of the LCD in Black & White Mode:

In Normal Display : "1"=Turn-On Display, "0" =Turn-Off Display
In Reveres Display : "1"=Turn-Off Display, "0" =Turn-On Display

The bus length accessing to the DD RAM is chosen 8-bit access or 16-bit by the 8-bit/16-bit Bus Select instruction. In case of the 16-bit bus length is selected in the gray scale display mode, only upper 8 bits of column address are valid and lower 8 bits (D_7-D_0) are ignored (Fig. 1-1) because of 8-bit addressing RAM area of column address=10_H. When the 16-bit bus length in the Black & White display mode is selected, only upper 4 bits of column address are valid and lower 12 bit (D_{11}-D_0) is ignored because of 4-bit RAM area of column address=08_H(Layer0) or column address=28_H(Layer1)

When the 8-bit bus length in the Black & White display mode is selected, the DD RAM is addressed by only upper 4 bits of column address thus lower 4 bits are also ignored.

DD RAM output 132 x 2 bits parallel data addressed by Line counter then the data latched in the display data latch. Asynchronous data access to the DD RAM is available due to the access to the DD RAM from the MPU and latch to the display data latch operation are done independently.

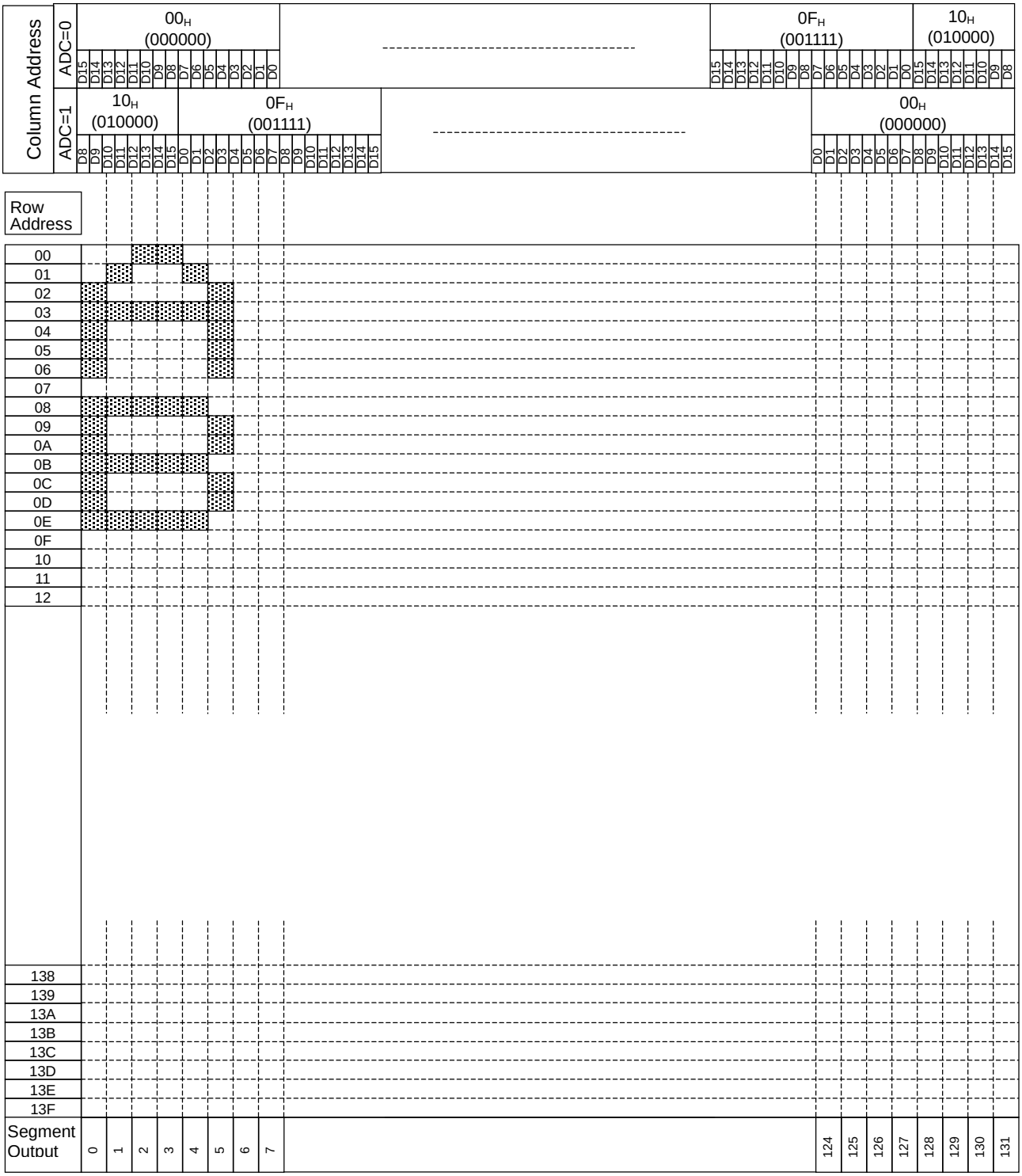


Fig.1-1 DD RAM addressing (Gray scale mode)

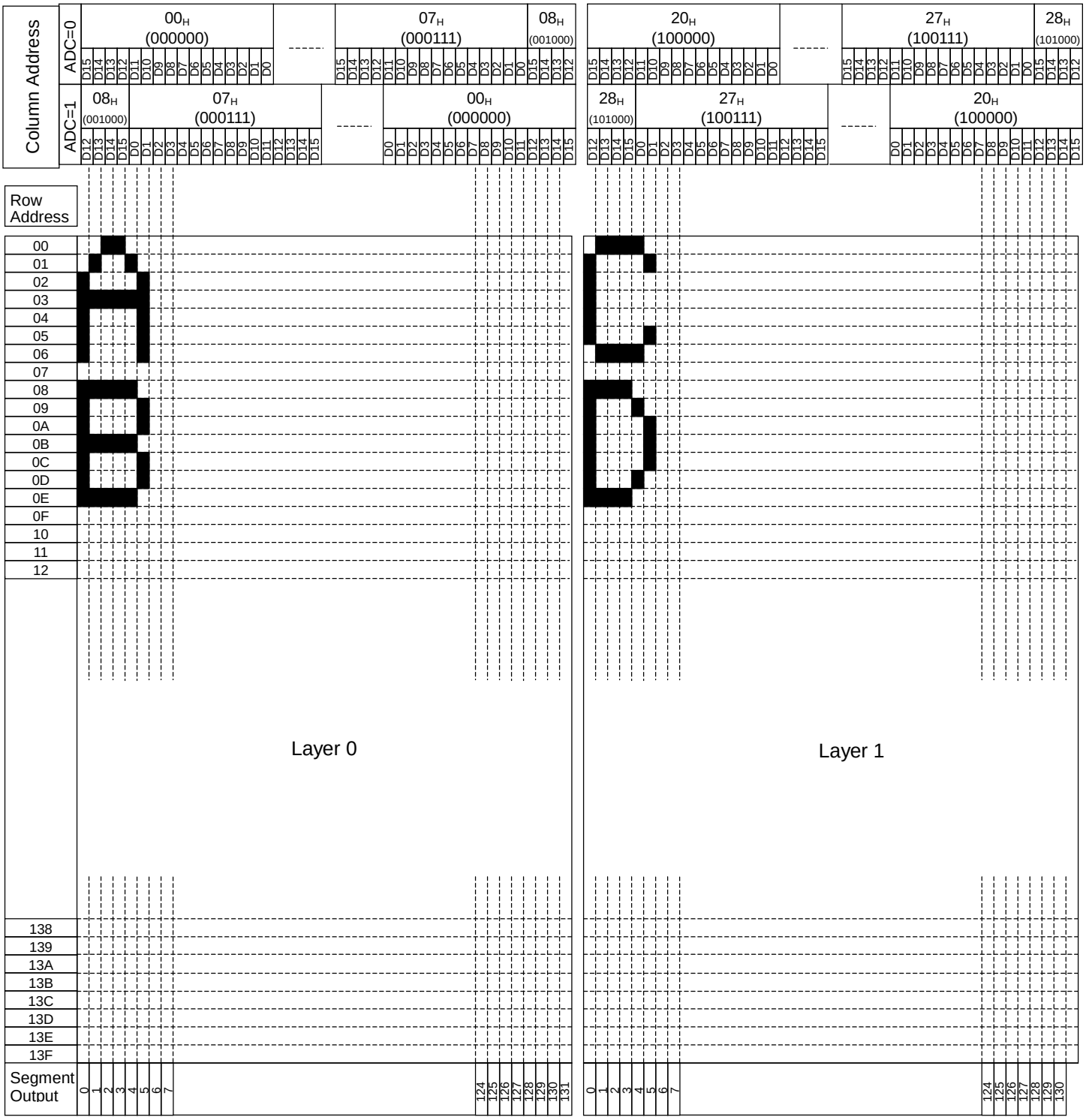


Fig.1-2 DD RAM addressing (Black & White mode)

(1-7) Output Assignment Register

This circuit determines the scanning direction of the common output.

Table 1 Scanning direction of the common output

	Common Output Terminal	
PAD No.	50	209
Terminal Name	C_0	C_{159}
Ver.A	COM_0 ⟶	COM_{159}
Ver.B	COM_{159} ⟵	COM_0

* The Mask fixes the common scanning direction between version A and B that can not be changed by the instruction.

(1-8) Reset Circuit

When the input signal to $\overline{RES}$ terminal goes to "L", the reset circuit executes initialization as below;

-The Initialization state (default)

1. Display mode: 4 level Gray Scale Display Mode.
2. Display off
3. Normal Display (not inverse)
4. ADC selects: Normal
5. Read Modify Write off
6. Voltage Booster off, Voltage Regulator off, Voltage follower off
7. Whole Display / Normal Display
8. Driver output off
9. Clear the data of serial interface register
10. Set the Column Address Counter to 00_H
11. Set the Row Address Register to 00_H
12. Set the Start Line Address to 00_H
13. Set the Gray Scale Level to default value (Refer to (2-1)Descriptions of the Instruction Codes (n)Select Gray Scale Level)
14. The continuous addressing of DDRAM (Variable RAM Mapping Mode off)
15. Set the EVR register to FF_H
16. Set the Duty Ratio to 1/160
17. Bias select D_3, D_2, D_1, D_0 = "1,0,1,0" (1/14 Bias)
18. Voltage Booster Select D_2, D_1, D_0 = "1,0,1" (7 times)
19. Set n-line inverse register to 0_H
20. Set to 8-bit bus interface mode

The $\overline{RES}$ terminal connects to the reset terminal of the MPU synchronization with the MPU initialization as shown in " the MPU interface " in the Application Circuit section. The "L" level input signal as reset signal must keep the period over than 10us as shown in DC Characteristics. The **NJU6682** takes 1us for the reset operation after the rising edge of the $\overline{RES}$ signal.

The reset operation by $\overline{RES}$ ="L" initializes each resister setting as above reset status, but the internal oscillation circuit and output terminals (D_0 to D_{15}) are not affected.

To avoid the lock-up, the reset operation by the $\overline{RES}$ terminal must be required every time when power terns on.

Note1) The reset operation by the reset instruction, function 9 to 20 operations mentioned above is performed.

Note2) The noise into the RES terminal should be eliminated to avoid the error on the application with the careful design.

Note3) The $\overline{RES}$ terminal must be keep "L" level when the power terns on in not use of the built-in LCD power supply circuit for no affect to the internal execution.

(1-9) LCD Driving Circuit

(a) LCD driver

LCD driver is 292 sets of multiplexer consisting of 160 commons and 132 segments drivers to output the 4-level of LCD driving voltage. The common driver outputs the common scan signals formed with the shift register. The segment driver outputs the segment driving signal determined by a combination of display data in the DD RAM, common timing, FR signal, and alternating signal for LCD. The output wave forms of segment/common are shown in "LCD Driving Wave Form".

(b) Display Data Latch Circuit

Display Data Latch Circuit latches the 132 x 2-bit display data outputted from the DD RAM addressed by the Line address counter to LCD driver at every common signal cycle temporarily. The original data in the DD RAM is not changed because of the Normal/Reverse display in Black & White display mode, Display On/Off, Whole Display / Normal Display instruction processes only stored data in this Display Data Latch Circuit.

(c) Gray Scale / Black & White Control Circuit

The Gray Scale control circuit selects the gray scale level data pointed by instruction out of 264 bits display data of the gray scale level signal in Display Data Latch Circuit and outputs to LCD driver Sn.

The Black & White display control circuit selects a layer set by the instruction out of the 264 bits Black & White data latched in Display Data Latch Circuit and outputs to the LCD driver Sn.

(d) Signal forming to Line Counter and Display Data Latch Circuit

The count clock to Line Counter and the latch clock to Display Data Latch Circuit are formed using the internal display clock (CL). The display data of 132 x 2 bits from Display Data RAM pointed by the line address synchronizing with the internal display clock are latched into the Display Data Latch Circuit and are outputted to Gray Scale Control Circuit / Black & White Control Circuit.

The display data read out operation from DD RAM to the LCD Driver Circuit is completely independent operation with an access to the display data RAM from MPU.

(e) Display Timing Generation Circuit

The display timing generation circuit generates the internal timing of the display system by the master clock and the internal FR signal. As for it, the internal FR signal and the LCD alternating signal generate the wave form of 2-frame alternating drive wave form or the n-line inverse drive method for the LCD Driving circuit.

(f) FRC / PWM Control Circuit

The FRC/PWM Control Circuit operates functions of Frame Rate Control (FRC) and Pulse Width Modulation (PWM) for the 4-level gray scale display.

(g) Common Timing Generator

The Common Timing Generator generates the common timing signal from the internal display clock (CL). Figure 2 shows display timing in Black & White mode.

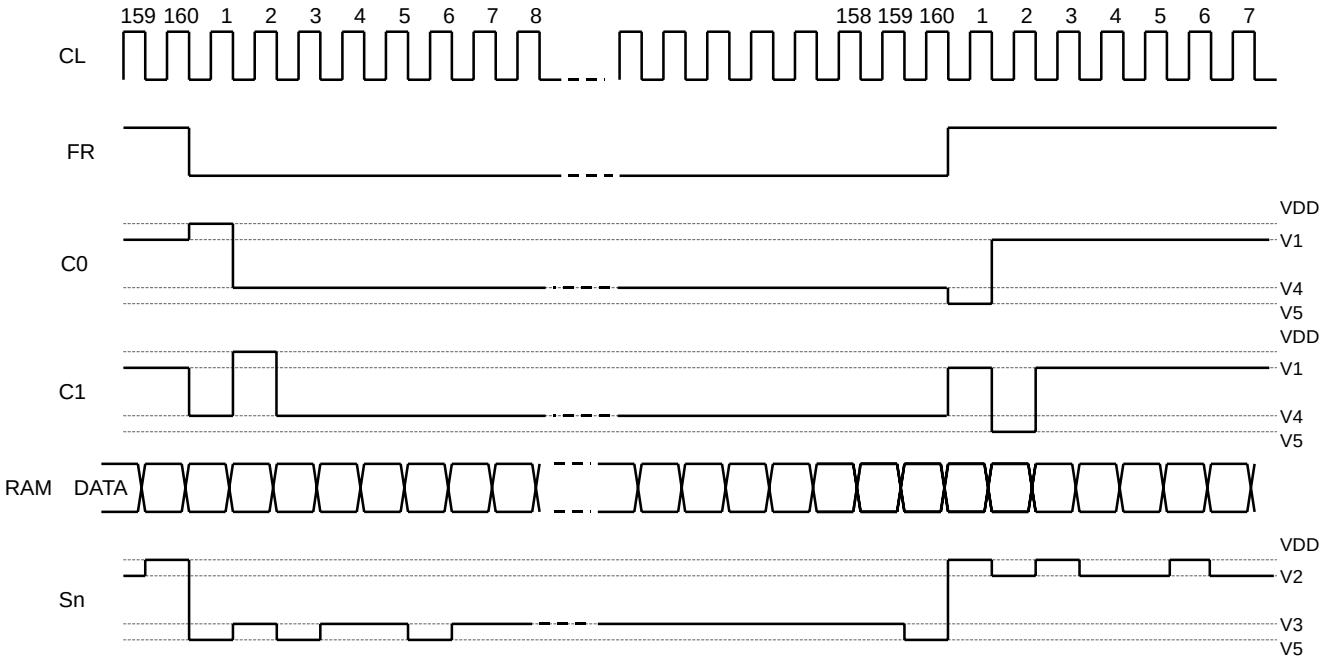


Fig.2-1 2-frame alternating drive mode (line inverting register sets to 0)

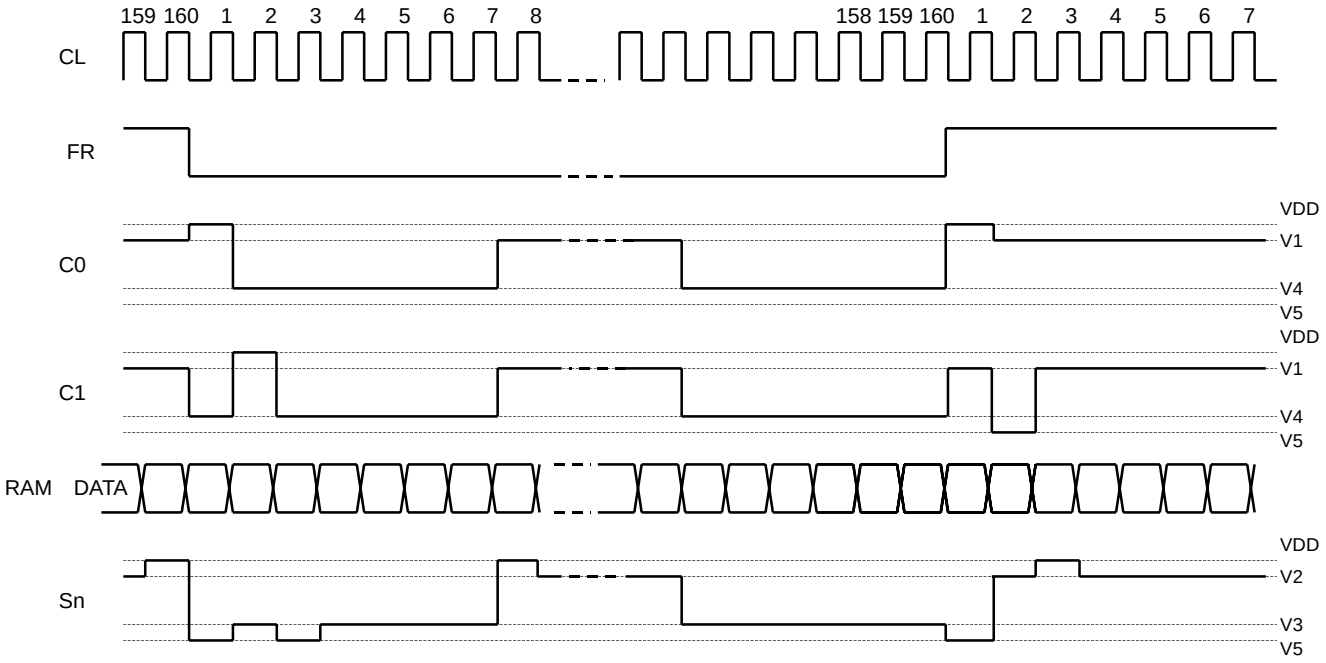


Fig.2-2 n-line inverse drive mode (n=7, line inverting register sets to 6)

(h) Oscillation Circuits

The Oscillation Circuit is a low power type CR oscillator using an internal resistor and capacitor. The oscillator output is using for the display timing clock and for the voltage booster circuit. And the display clock(CL) is generated from this oscillator output frequency by dividing.

Table 2 Relationship between Duty ratio and Dividing

Duty	1/4	1/8	1/12	1/16	1/20	1/24	1/28	1/32	1/36	1/40	1/44, 1/48	1/52, 1/56
Divide	1/1200	1/600	1/405	1/300	1/240	1/195	1/165	1/150	1/135	1/120	1/105	1/90

Duty	1/60, 1/64, 1/68	1/72, 1/76, 1/80, 1/84, 1/88	1/92, 1/96, 1/100, 1/104, 1/108, 1/112, 1/116, 1/120
Divide	1/75	1/60	1/45

Duty	1/124, 1/128, 1/132, 1/136, 1/140, 1/144, 1/148, 1/152, 1/156, 1/160
Divide	1/30

(i) Power Supply Circuits

The internal power supply circuit generates the voltage for driving LCD. It consists of voltage booster circuits (from 2 times to 7 times), voltage adjust circuits, and voltage followers.

The internal power supply Circuits is designed specially for a small-size LCD like as normal cellular phone size LCD panel. When **NJU6682** apply to the large size LCD panel application (large capacitive load), external power supply is required to keep good display condition..

To keep good display condition, external component of the capacitors connecting to the V_1 to V_5 terminals and voltage booster circuits and the feedback resistors for the V_5 operational amplifier must fix each optimized constant after checking various display patterns on LCD panel actually in the application.

The Internal Power Supply Circuits operation is controlled by Internal Power Supply Control Instruction.

A0	$\overline{RD}$	$\overline{WR}$	D_{15}	D_{14}	D_{13}	D_{12}	D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	0	0	0	0	1	0	0	0	1	*	*	*	*	*	DC	VR	VF

*:Don't Care

DC : Voltage Booster Circuit

DC = 1 : Booster Circuit ON

DC = 0 : Booster Circuit OFF (In this time , terminals C_1^+,C_1^-,C_2^+,C_2^-,C_3^-,C_4^-,C_5^- and C_6^- should be open and LCD driving voltage should be supplied to V_{OUT} terminal from outside)

VR : Voltage Adjust Circuit

VR = 1 : Adjust Circuit ON

VR = 0 : Adjust Circuit OFF (In this time, terminal VR should be open, and V_5 should be supplied from outside)

VF : Voltage Follower

VF = 1 : Voltage Follower ON

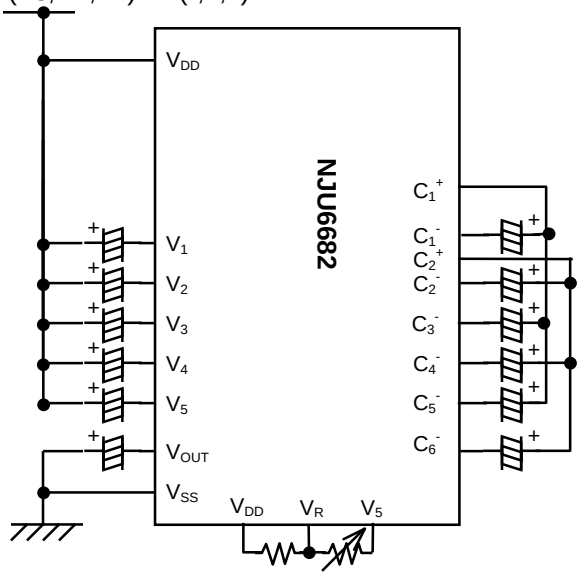
VF = 0 : Voltage Follower OFF (In this time, LCD bias voltage V_1 to V_5 should be supplied to terminals V_1 to V_5 from outside.)

○Power Supply Circuits example

(1) Internal Power Supply Example

All of the Internal Booster, Voltage Adjust Circuit, Voltage Follower using.

(DC, VR, VF) = (1, 1, 1)

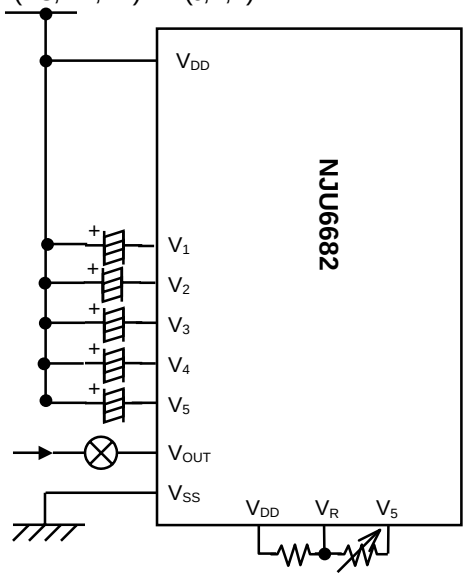


(2) External Power Supply Example

Only V_{OUT} Supply from outside,

Int. Voltage Adjust Circuit, Voltage Follower using.

(DC, VR, VF) = (0, 1, 1)

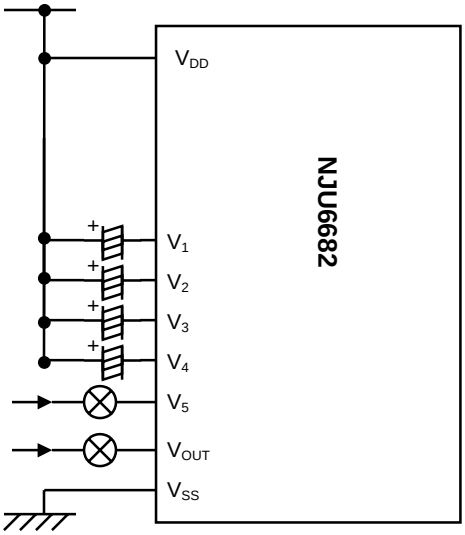


(3) External Power Supply Example

V_{OUT} and V_5 supply from outside,

Internal Voltage Follower using.

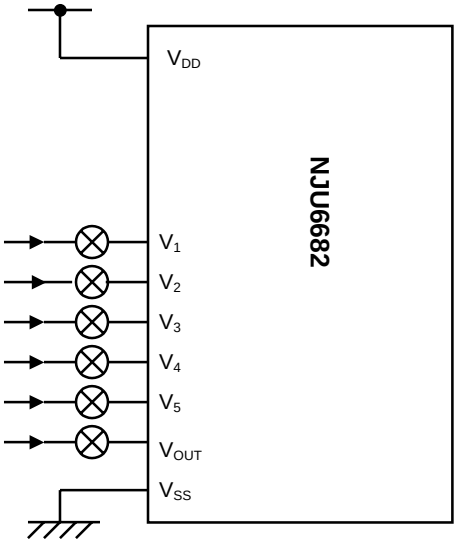
(DC, VR, VF) = (0, 0, 1)



(4) External Power Supply Example

All of V_1 to V_5 and V_{OUT} supply from outside.

(DC, VR, VF) = (0, 0, 0)



(Note)⊗ : These switches should be open or external power supply stops in power-save mode.

(2) Instructions

The **NJU6682** distinguishes the data on the data bus D_0 to D_{15} as an instruction by combination of A0, $\overline{RD}$, and $\overline{WR}$ signals. The decoding of the instruction and exection performes with only high speed internal timing without relation to the external clock.

In case of the serial interface, the data input as MSB(D_{15}) first serially.

Table.3 shows the instruction codes of the **NJU6682**

Table 3. Instruction Codes (*:Don't Care)

Instruction		Code																			Description
		A0	$\overline{RD}$	$\overline{WR}$	D_{15}	D_{14}	D_{13}	D_{12}	D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
(a)	Display ON/OFF	0	1	0	0	0	0	0	0	0	0	0	*							0/1	LCD Display ON/OFF D_0=0:OFF, D_0=1:ON
(b)	Display Start Line Address Set	0	1	0	0	0	1	0	1	0	1	Line Address									Determine the Line Address of DD RAM to the COM_0
(c)	Column Address Set	0	1	0	0	0	1	0	0	0	0	0	*	*	Column Address						Set the Column Address of DD RAM
(d)	Row Address Set	0	1	0	0	0	1	0	1	0	0	Row Address									Set the Row Address of DD RAM
(e)	Status Read	0	0	1	Status							0	Status							0	Read out the internal status
(f)	Write Display Data	1	1	0	Write Data																Write the data into the DD RAM
(g)	Read Display Data	1	0	1	Read Data																Read out the data from the DD RAM
(h)	Normal or Inverse Display	0	1	0	0	0	0	0	0	0	0	1	*							0/1	Normal or Inverse Display D_0=0:Normal, D_0=1:Inverse
(i)	Whole Display/ Normal Display	0	1	0	0	0	0	0	0	0	1	0	*							0/1	Whole Display Turns ON D_0=0:Normal, D_0=1:Whole Display ON
(j)	Partial Display	0	1	0	0	0	1	1	0	0	0	0	*	Start Unit of 1st Block							Set the Display Start Unit of Block1
		0	1	0	0	0	1	1	0	0	0	1	*	Number of unit in 1st Block							Set the Number of Display Unit in Block1
		0	1	0	0	0	1	1	0	0	1	0	*	Start Unit of 2nd Block							Set the Display Start Unit of Block2
		0	1	0	0	0	1	1	0	0	1	1	*	Number of unit in 2nd Block							Set the Number of Display Unit in Block2
		0	1	0	0	0	1	1	0	1	0	0	*							0	Execute the Partial Display
(k)	n-Line Inverse Register Set	0	1	0	0	0	0	0	0	0	1	1	*	The Number of n-line Inverse							Set the n-line inverse number
(l)	EVR Register Set	0	1	0	0	0	0	0	1	0	0	0	EVR Register Data								Set the V_5 output level to the EVR register
(m)	Variable RAM Mapping Mode	0	1	0	0	1	0	0	0	0	0	Row Address of 1st Display Block									Set the Row address of 1st Display block
		0	1	0	0	1	0	0	0	0	1	0	*	Line Number of 1st Block							Set the line number of 1st Display block
		0	1	0	0	1	0	0	0	1	0	Row Address of 2nd Display Block									Set the Row address of 2nd Display block
		0	1	0	0	1	0	0	0	1	1	0	*	Line Number of 2nd Block							Set the line number of 2nd Display block
		0	1	0	0	1	0	0	1	0	0	Row Address of 3rd Display Block									Set the Row address of 3rd Display block
		0	1	0	0	1	0	0	1	0	1	0	*	Line Number of 3rd Block							Set the line number of 3rd Display block
		0	1	0	0	1	0	0	1	1	0	Row Address of 4th Display Block									Set the Row address of 4th Display block
		0	1	0	0	1	0	0	1	1	1	0	*	Line Number of 4th Block							Set the line number of 4th Display block
		0	1	0	0	1	0	1	0	0	0	Row Address of 5th Display Block									Set the Row address of 5th Display block
		0	1	0	0	1	0	1	0	0	1	0	*	Line Number of 5th Block							Set the line number of 5th Display block
		0	1	0	0	1	0	1	0	1	0	Row Address of 6th Display Block									Set the Row address of 6th Display block
		0	1	0	0	1	0	1	0	1	1	0	*	Line Number of 6th Block							Set the line number of 6th Display block
		0	1	0	0	1	0	1	1	0	0	Row Address of 7th Display Block									Set the Row address of 7th Display block
		0	1	0	0	1	0	1	1	0	1	0	*	Line Number of 7th Block							Set the line number of 7th Display block
		0	1	0	0	1	0	1	1	1	0	Row Address of 8th Display Block									Set the Row address of 8th Display block
		0	1	0	0	1	0	1	1	1	1	0	*	Line Number of 8th Block							Set the line number of 8th Display block
		0	1	0	0	1	1	0	0	0	0	0	*							0/1	Variable RAM Mapping Mode D_0=0:ON, D_0=1:OFF

Instruction		Code																		Description
		A0	RD	WR	D_{15}	D_{14}	D_{13}	D_{12}	D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
(n)	Select Gray Scale Level	0	1	0	0	1	1	1	0	0	0	0	PWM Data (1st Frame)				PWM Data (2nd Frame)				Gray Scale Level 0: Set the PWM Data for 1st and 2nd Frames
		0	1	0	0	1	1	1	0	0	0	1	PWM Data (3rd Frame)				PWM Data (4th Frame)				Gray Scale Level 0: Set the PWM Data for 3rd and 4th Frames
		0	1	0	0	1	1	1	0	0	1	0	PWM Data (1st Frame)				PWM Data (2nd Frame)				Gray Scale Level 1: Set the PWM Data for 1st and 2nd Frames
		0	1	0	0	1	1	1	0	0	1	1	PWM Data (3rd Frame)				PWM Data (4th Frame)				Gray Scale Level 1: Set the PWM Data for 3rd and 4th Frames
		0	1	0	0	1	1	1	0	1	0	0	PWM Data (1st Frame)				PWM Data (2nd Frame)				Gray Scale Level 2: Set the PWM Data for 1st and 2nd Frames
		0	1	0	0	1	1	1	0	1	0	1	PWM Data (3rd Frame)				PWM Data (4th Frame)				Gray Scale Level 2: Set the PWM Data for 3rd and 4th Frames
		0	1	0	0	1	1	1	0	1	1	0	PWM Data (1st Frame)				PWM Data (2nd Frame)				Gray Scale Level 3: Set the PWM Data for 1st and 2nd Frames
		0	1	0	0	1	1	1	0	1	1	1	PWM Data (3rd Frame)				PWM Data (4th Frame)				Gray Scale Level 3: Set the PWM Data for 3rd and 4th Frames
(o)	Bias Select	0	1	0	0	0	0	0	1	0	0	1	*				Bias				Select the Bias (11 types)
(p)	Boost level Select	0	1	0	0	0	0	0	1	0	1	0	*					Boost stage			Set the Boost stage :2 to 7 times
(q)	Read Modify Write /End	0	1	0	0	0	0	1	0	0	0	0	*							0/1	Increase Column Address Counter +1 wher writing and no-change when reading D_0=0:ON, D_0=1:END
(r)	Reset	0	1	0	0	0	0	1	0	0	0	1	*							1	Initialize the internal circuits
(s)	Internal Power Supply setting	0	1	0	0	0	0	1	0	0	1	0	*					DC	VR	VF	DC=1: Voltage Booster ON DC=0: Voltage Booster OFF VR=1: Voltage Regurator ON VR=0: Voltage Regurator OFF VF=1: Voltage Follower ON VF=0: Voltage Follower OFF
(t)	LCD Driver Outputs ON/OFF	0	1	0	0	0	0	1	0	0	1	1	*							0/1	LCD Driving wave form outputs ON/OFF D_0=0: LCD Driver Outputs OFF D_0=1: LCD Driver Outputs ON
(u)	Power Save (complex instruction)	0 0	1 1	0 0	0 0	0 0	0 0	0 0	0 0	0 0	0 1	0 0	*							0/1	Set the Power Save mode (Display OFF + Static Drive ON)
(v)	ADC Select	0	1	0	0	0	0	1	1	0	0	0	*							0/1	Output the Display RAM address Sn D_0=0:Normal, D_0=1:Inverse
(w)	Display Mode Select	0	1	0	0	0	0	1	1	0	0	1	*					GS	L1	L0	Set Display mode GB=1: Gray scale mode GB=0: Black and white mode L1=1: Select layer 1 L1=0: Not select layer 1 L0=1: Select layer 0 L0=0: Not select layer 0
(x)	8-/16-bit Bus Interface Select	0	1	0	0	0	0	1	1	0	1	0/1	*								D_8=0: Set 8-bit bus interface D_8=1: Set 16-bit bus interface

(*:Don't Care)

(2-1) Descriptions of the Instruction Codes

(a) Display ON/OFF Control

It executes the ON/OFF control of the whole display without relation to the DD RAM or any internal conditions.

A0	$\overline{RD}$	$\overline{WR}$	D_{15}	D_{14}	D_{13}	D_{12}	D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	0	0	0	0	0	0	0	0	0	*	*	*	*	*	*	*	D

*:Don't Care

D 0: Display OFF
1: Display ON

(b) Display Start Line Address Set (Refer to "Functional Description Fig. 1-1,1-2 DD RAM addressing")

It sets the DD RAM line address corresponding to the COM_0 terminal (normally assigned to the top display line). In this instruction execution, the display area is automatically set by the lines that correspond to the display duty ratio to the upward direction of the line address. Changing the line address by this instruction performs smooth scrolling to a vertical direction. In this time, the DD RAM data are unchanged.

When variable RAM mapping mode is selected, this variable RAM mapping setting takes precedence over the line address setting and Line address Set instruction is ignored.

A0	$\overline{RD}$	$\overline{WR}$	D_{15}	D_{14}	D_{13}	D_{12}	D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	0	0	0	1	0	1	0	1	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0

A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	Start Line Address (HEX)
0	0	0	0	0	0	0	0	0	000
0	0	0	0	0	0	0	0	1	001
				:					:
				:					:
				:					:
1	0	0	1	1	1	1	1	0	13E
1	0	0	1	1	1	1	1	1	13F

(c) Column Address Set (Refer to “Functional Description Fig. 1-1,1-2 DD RAM addressing”)

When MPU access to the DD RAM, a column address is set by Column Address Set instruction before writing the data. The DD RAM becomes accessible by setting both of column address and row address. (Note: the change of row address is not affected to the display.)

The range of column address is determined by the display mode. In gray scale mode, the range of column address is 00_H to 10_H. In black & white mode, 00_H to 08_H(layer 0) and 20_H to 28_H(layer 1). Over range of column address setting is ignored.

When the MPU access to the DD RAM continuously, the column address increments automatically from the set address after each data access. Therefore, the MPU can transmit only the Data continuously without setting the column address at every transmission time. The increment of column address is stopped at the maximum column address plus 1 limited by each display mode. When the column address count up is stopped, the row address is not changed.

A0	$\overline{RD}$	$\overline{WR}$	D_{15}	D_{14}	D_{13}	D_{12}	D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	0	0	0	1	0	0	0	0	0	*	*	A_5	A_4	A_3	A_2	A_1	A_0

*:Don’t Care

A_5	A_4	A_3	A_2	A_1	A_0	Column Address (HEX)		
						Gray Scale Mode	Black & White Mode	
0	0	0	0	0	0	00	Layer 0	00
0	0	0	0	0	1	01		01
0	0	0	0	1	0	02		02
			:			:		:
			:			:		:
0	0	1	0	0	0	:		08
			:				Address Set is Invalid	
			:					
0	0	1	1	1	0	0E		
0	0	1	1	1	1	0F		
0	1	0	0	0	0	10		
			:			Address Set is Invalid		
			:					
			:					
			:					
1	0	0	0	0	0		Layer 1	20
1	0	0	0	0	1			21
								:
								:
1	0	0	1	1	1			27
1	0	1	0	0	0			28
			:				Address Set is Invalid	
			:					
			:					

(d) Row Address Set (Refer to “Functional Description Fig. 1-1,1-2 DD RAM addressing”)

When MPU accesses to the DD RAM , the row address set by Row Address Set instruction is required with the (c) Column Address Set before writing the data.

A0	$\overline{RD}$	$\overline{WR}$	D_{15}	D_{14}	D_{13}	D_{12}	D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	0	0	0	1	0	1	0	0	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0

A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	Row Address (HEX)
0	0	0	0	0	0	0	0	0	000
0	0	0	0	0	0	0	0	1	001
				:					:
				:					:
1	0	0	1	1	1	1	1	0	13E
1	0	0	1	1	1	1	1	1	13F

(e) Status Read

This instruction reads out the intenal status of “BUSY”, “ADC”, “Display ON/OFF”, “RESET”, “GB”, and “LY” described as follows. Even if 8-bit bus interface mode is selected, the status read instruction completes within one cycle only.

A0	$\overline{RD}$	$\overline{WR}$	D_{15}	D_{14}	D_{13}	D_{12}	D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	1	BUSY	ADC	ON/OFF	RESET	GB	LY_1	LY_0	0	BUSY	ADC	ON/OFF	RESET	GB	LY_1	LY_0	0

BUSY : BUSY=1 indicates internal circuits is operating or the Reset cycle.
All instructions can be input after the BUSY status change to “0”.

ADC : Indidates the correspondence of Column Address and Segment Driver.
0: Counterclockwise output (Inverse) Column Address 131-n <--->Segment Driver n
1: Clockwise output (Normal) Column Address n <--->Segment Driver n
(Note) The data “0=Inverse” and “1=Normal” of ADC status is inverted with the ADC Select instruction of “1=Inverse” and “0=Normal”.

ON/OFF : Indicates the display ON/OFF status.
0: Display “ON”
1: Display “OFF”
(Note) The data “0=ON” and “1=OFF” of Display ON/OFF status is inverted with the Display ON/OFF instruction of “1=ON” and ”0=OFF”.

RESET : Indicates the initializing period by $\overline{RES}$ terminal signal or Reset instruction.
0: Not Reset status
1: In the Reset status

GB : Indicates the current Display Mode.
0: Black & White Mode
1: Gray Scale Mode

LY_1 : Indicates the status of Layer 1 when the Black & White Display Mode is selected.
0: Layer 1 is not selected
1: Layer 1 is selected

LY_0 : Indicates the status of Layer 0 when the Black & White Display Mode is selected.
0: Layer 0 is not selected
1: Layer 0 is selected

(f) Write Display Data

It writes the data on the data bus into the DD RAM. Column Address increments automatically after data writing, therefore, the MPU can write the data into the DD RAM continuously without the address setting at every writing time once the starting address is set.

A0	$\overline{RD}$	$\overline{WR}$	D_{15}	D_{14}	D_{13}	D_{12}	D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	1	0	Write Data															

(g) Read Display Data

This instruction reads out the 16-bit data from DD RAM addressed by the row and the column Address. The column address automatically increments after the 16-bit data read out, therefore, the MPU can read the data from the DD RAM continuously without the address setting at every reading time once the starting address is set. Note that the dummy read is required just after setting the column address (see "(5-4) Access to the DD RAM and the Internal Register").

In the serial interface mode, the display data is unable to read out.

A0	$\overline{RD}$	$\overline{WR}$	D_{15}	D_{14}	D_{13}	D_{12}	D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	1	Read Data															

(h) Normal / Inverse Display

It changes the display condition of normal or inverse for entire display area. The execution of this instruction does not change the display data in the DD RAM.

A0	$\overline{RD}$	$\overline{WR}$	D_{15}	D_{14}	D_{13}	D_{12}	D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	0	0	0	0	0	0	0	0	1	*	*	*	*	*	*	*	D

*:Don't Care

Black & White Mode:

D	DD RAM="1"	DD RAM="0"
0 (Normal)	LCD ON	LCD OFF
1 (Inverse)	LCD OFF	LCD ON

Gray Scale Mode:

D	DD RAM="00"	DD RAM="01"	DD RAM="10"	DD RAM="11"
0 (Normal)	Gray Scale Level 0	Gray Scale Level 1	Gray Scale Level 2	Gray Scale Level 3
1 (Inverse)	Gray Scale Level 3	Gray Scale Level 2	Gray Scale Level 1	Gray Scale Level 0

(i) Whole Display / Normal Display

This instruction turns all the pixels ON regardless the data stored in the DD RAM. In this time, the data in DD RAM are remained and unchanged. This instruction is executed prior to the “Normal or Inverse Display” Instruction.

A0	$\overline{RD}$	$\overline{WR}$	D_{15}	D_{14}	D_{13}	D_{12}	D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	0	0	0	0	0	0	0	1	0	*	*	*	*	*	*	*	D

*:Don’t Care

D 0: Normal Display
1: Whole Display Turns ON

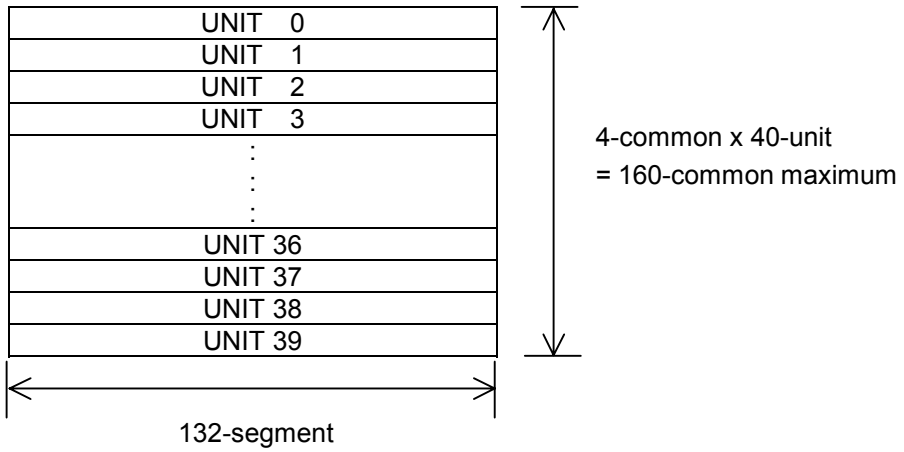
When the “Static Drive ON” instruction is executed at Display OFF status, the **NJU6682** operates in Power Save Mode. (Refer “ Power Save Mode “)

(j) Partial Display

It selects two active display areas on the LCD Panel partially. The display area is divided to 40 units with four commons each and selected two display blocks by setting Unit number and number of Unit required (not overlap, not over than 40 units) to display on the LCD panel. These two display blocks are assigned optionally on the LCD panel. Duty selects an adapted ratio number corresponding to the total number of two display blocks automatically.

Partial Display function adjusts the LCD driving voltage, Voltage boosting times and E.V.R level by the instruction to generate the optimum LCD driving voltage for display quality. As result, the operating current is reduced.

- Display Unit Structure



- Partial Display instruction

When Partial Display functions, both of Top Unit Number of display area (the Start Unit) and the number of the effective continuous unit (Display Unit) from the Start Unit for the first display block and the second. Attention that the first display block and the second definition must not be overlap of display area and not be over than 40 units in total.

In case of whole display (1/160 duty), the first display block defines Start Unit=0 (0,0,0,0,0,0) and Display Unit = 40 (1,0,1,0,0,0) for all of display area selection. In this time, the definition of the second display block is ignored.

In case of only the first block display, the second display block defines Start Unit=0 (0,0,0,0,0,0) and Display Unit = 0 (0,0,0,0,0,0) for no display area.

(1) Set the Start Unit of the 1st partial display block

A0	$\overline{RD}$	$\overline{WR}$	D_{15}	D_{14}	D_{13}	D_{12}	D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	0	0	0	1	1	0	0	0	0	*	*	D	D	D	D	D	D

(2) Set the Display Unit Number of the 1st partial display block

A0	$\overline{RD}$	$\overline{WR}$	D_{15}	D_{14}	D_{13}	D_{12}	D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	0	0	0	1	1	0	0	0	1	*	*	D	D	D	D	D	D

(3) Set the Start Unit of the 2nd partial display block

A0	$\overline{RD}$	$\overline{WR}$	D_{15}	D_{14}	D_{13}	D_{12}	D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	0	0	0	1	1	0	0	1	0	*	*	D	D	D	D	D	D

(4) Set the Display Unit Number of the 2nd partial display block

A0	$\overline{RD}$	$\overline{WR}$	D_{15}	D_{14}	D_{13}	D_{12}	D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	0	0	0	1	1	0	0	1	1	*	*	D	D	D	D	D	D

*:Don't Care

D : The Start Unit (D:000000–100111), or the Display Unit Number(000000–101000)

By input following instruction, the duty ratio is changed automatically and executes the partial display function.

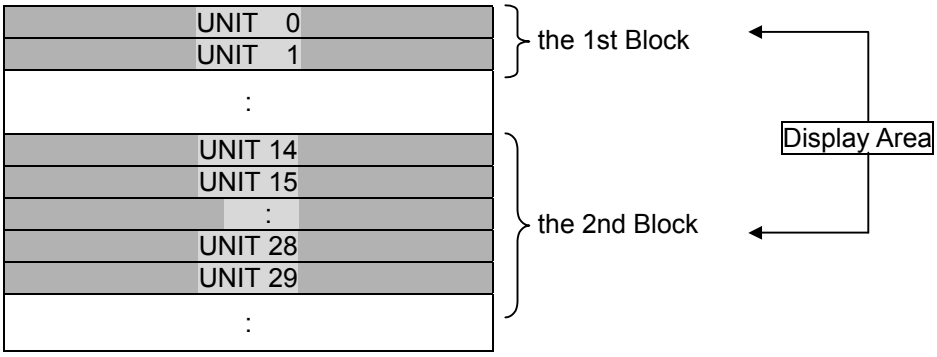
A0	$\overline{RD}$	$\overline{WR}$	D_{15}	D_{14}	D_{13}	D_{12}	D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	0	0	0	1	1	0	1	0	0	*	*	*	*	*	*	*	0

*:Don't Care

(Notes) Attention followings due to prevent from mulfunction.

- The input order of Partial Display instructions must follow above.
- Prohibits the overlap of the 1st partial display block and the 2nd.
- The Start Unit of the 1st partial display block must not be over 39.
- The total Display Unit Number (the sum of the 1st and 2nd partial display block Unit Number) must not be over 40.
- On the LCD panel, no active display area inserts between the 1st display block and the 2nd . However, the display data of the 1st display block and the 2nd must store continuously in the display data RAM.

Example of the Partial Display setting.



The above partial display condition is set as follows:

(1) Set the Start Unit of the 1st partial display block to “0”.

A0	$\overline{RD}$	$\overline{WR}$	D_{15}	D_{14}	D_{13}	D_{12}	D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0

(2) Set the Display Unit Number of the 1st partial display block to “2”.

A0	$\overline{RD}$	$\overline{WR}$	D_{15}	D_{14}	D_{13}	D_{12}	D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	0	0	0	1	1	0	0	0	1	0	0	0	0	0	0	1	0

(3) Set the Start Unit of the 2nd partial display block to “14”.

A0	$\overline{RD}$	$\overline{WR}$	D_{15}	D_{14}	D_{13}	D_{12}	D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	0	0	0	1	1	0	0	1	0	0	0	0	0	1	1	1	0

(4) Set the Display Unit Number of the 2nd partial display block to “16”.

A0	$\overline{RD}$	$\overline{WR}$	D_{15}	D_{14}	D_{13}	D_{12}	D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	0	0	0	1	1	0	0	1	1	0	0	0	1	0	0	0	0

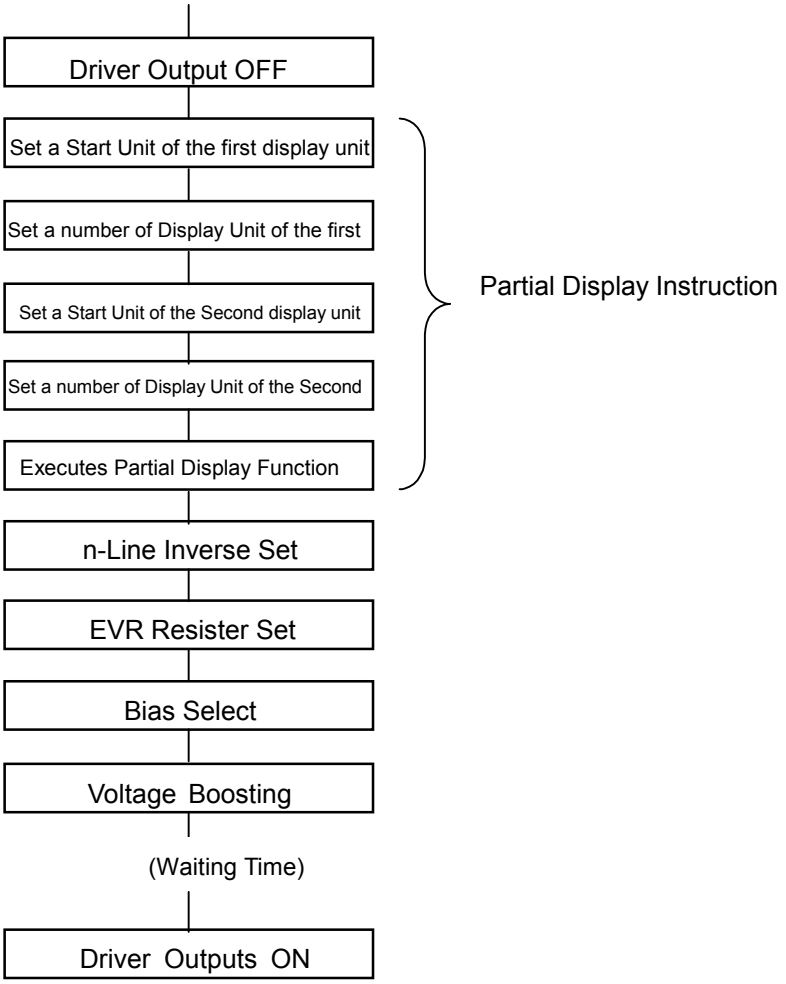
(5) Execute the Partial Display.

A0	$\overline{RD}$	$\overline{WR}$	D_{15}	D_{14}	D_{13}	D_{12}	D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	0	0	0	1	1	0	1	0	0	0	0	0	1	0	0	0	0

The Duty is changed to 1/72 automatically. (Duty = 1/UNIT x 4)

Duty is changed automatically when Partial Display execution. But LCD Driving Voltage, Bias, Driving form like as 2-frame alternating driving or n-line inverse are not changed. Therefore, LCD Driver Output Off should operate before Partial Display execution for prevention of unexpected display, and Voltage Booster Select instruction, E.V.R Register Set, Bias Select and n-line Inverse Driving Set should set optimum conditions for good display in the mean time of Partial Display instruction execution. The optimum conditions should fix refering the result of actual display eveluation.

The Sequence about the Partial Display function



(k) n-Line Inverse Resister Set (refer ■ Functional Description Fig.2-2 n-line Inverse alternative driving wave form)

It sets a line number to inverse the polarity lof common driver and segment.

Set a n-Line Inverse Resister

A0	$\overline{RD}$	$\overline{WR}$	D_{15}	D_{14}	D_{13}	D_{12}	D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	0	0	0	0	0	0	0	1	1	*	*	A_5	A_4	A_3	A_2	A_1	A_0

*:Don't Care

A_5	A_4	A_3	A_2	A_1	A_0	Inverse Line
0	0	0	0	0	0	-(*)
0	0	0	0	0	1	2
0	0	0	0	1	0	3
			:			:
			:			:
1	1	1	1	1	0	63
1	1	1	1	1	1	64

*When A_5 to A_0 are "000000", it set to 2-frame alternating drive mode.

(*) 2-frame alternating drive mode.

(I) EVR Resister Set

It controls the voltage regulator circuit of the internal LCD power supply to adjust the LCD display contrast by changing the LCD driving voltage "V_5". By data setting into the EVR register, the LCD driving voltage "V_5" selects out of 201 steps of regulated voltage. The voltage adjustable range of "V_5" is fixed by the external resistors. For details, refer the section "4-2) Voltage Adjust Circuit".

A0	$\overline{RD}$	$\overline{WR}$	D_{15}	D_{14}	D_{13}	D_{12}	D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	0	0	0	0	0	1	0	0	0	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0

A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	V_{LCD}
0	0	1	1	0	1	1	1	Low
			:					:
			:					:
1	1	1	1	1	1	1	0	:
1	1	1	1	1	1	1	1	High

$V_{LCD}=V_{DD}-V_5$

Set the EVR Register to FF_H (1,1,1,1,1,1,1,1), if not use the EVR.

(m) Variable RAM Mapping Mode

In the variable RAM mapping mode, independent 8 blocks can be defined in the DD RAM. The variable RAM mapping functions to assign the RAM data unconsecutively selectable out of the above 8 blocks (at the maximum); therefore, replacing one part of the display data to another becomes easier (see Figure 3-1, 3-2, 4-1 and 4-2). it is possible to define the RAM area in a maximum of 8-blocks not to continue to display the screen. Therefore, it is easy to replace a part of the Display Data each other(Fig.3-1,3-2, 4-1,4-2).

In the variable RAM mapping mode, Display Start Line Address determined by “2-1 (b) Start Line Address Set instruction” instruction becomes invalid, thus the vertical scroll function also becomes invalid with changing a Line Address will be unable.

The number of the display line for each block is assignable from “1” to “63”; “0” is invalid in this command. And, it is available to define the Display Line Number of each blocks as, but it must not define as “0”.

If the total number of the display line exceeds the duty, the line data in excess of its duty is not displayed.

The initialized state of the resistor regarding the variable RAM mapping is indefinite after reset.

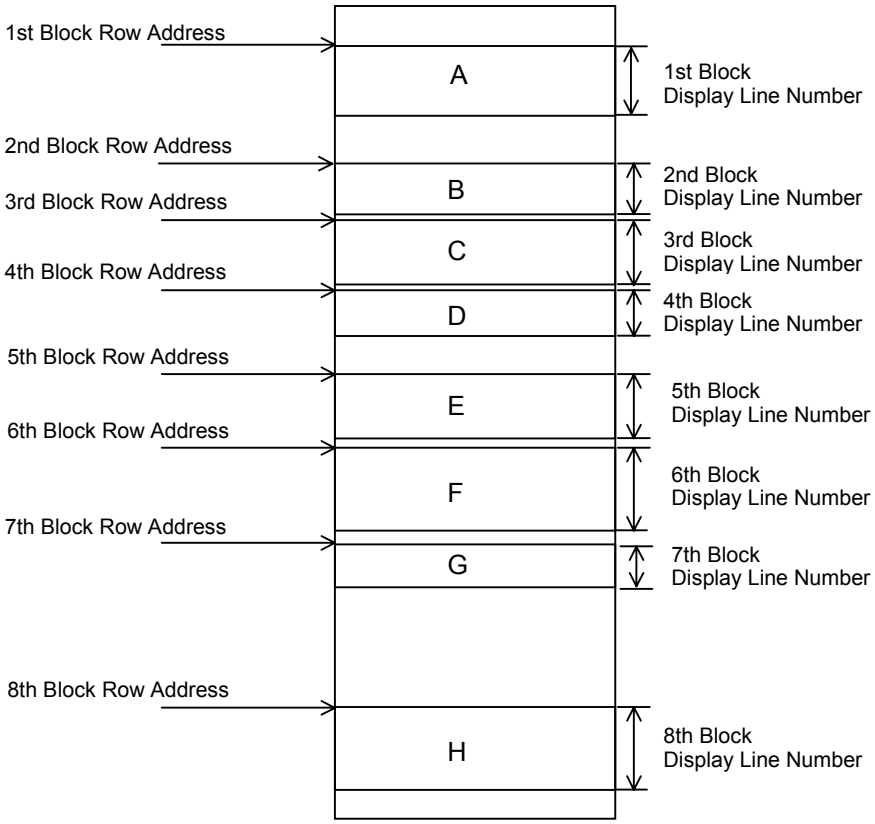


Fig.3-1 Setup the Variable RAM Mapping Mode, and Address Map in the DD RAM

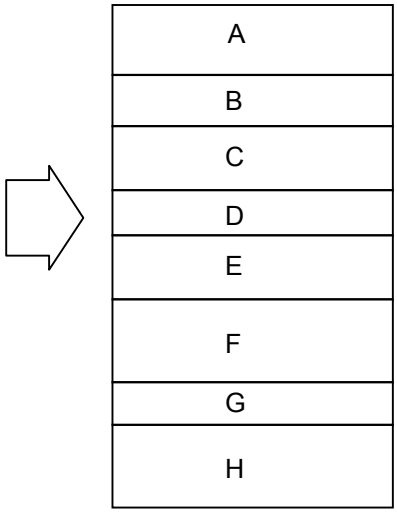


Fig.3-2 Actual Display Image

The Example of Variable RAM Mapping Mode

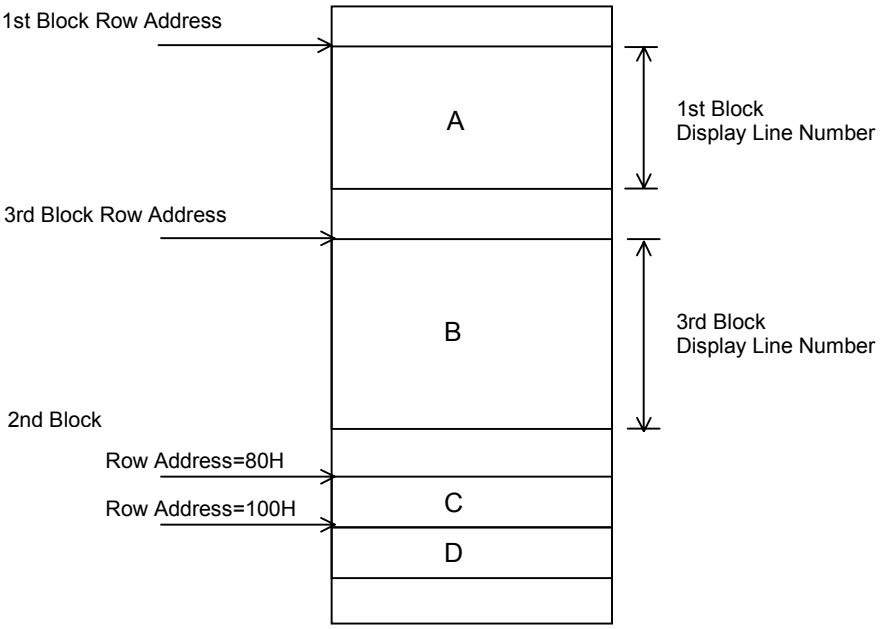


Fig.4-1 The setup of Variable RAM Mapping Mode, and the Address Map

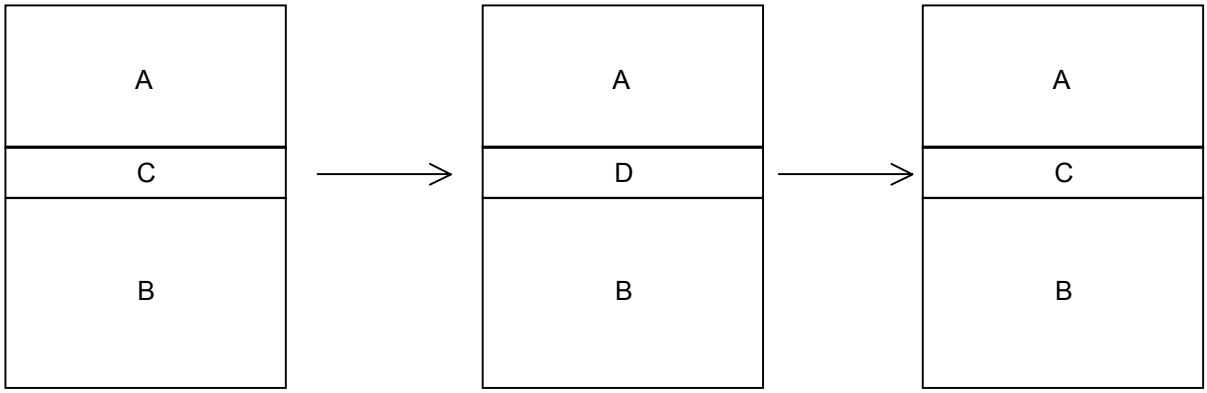


Fig.4-2 The actual Display image when the 2nd Block Row-Address is changed like the sequence of "80"$_H$ -> "100"$_H$ -> "80"$_H$

(1) Set the Row Address of the 1st Display Block

A0	$\overline{RD}$	$\overline{WR}$	D_{15}	D_{14}	D_{13}	D_{12}	D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	0	0	1	0	0	0	0	0	A	A	A	A	A	A	A	A	A

A: the Row Address of the 1st Display Block (0 to 319)

(2) Set the Display Line Number of the 1st Display Block

A0	$\overline{RD}$	$\overline{WR}$	D_{15}	D_{14}	D_{13}	D_{12}	D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	0	0	1	0	0	0	0	1	0	*	*	D	D	D	D	D	D

*:Don't Care

D: the Display Line Number of the 1st Display Block (1 to 63)

(3) Set the Row Address of the 2nd Display Block

A0	$\overline{RD}$	$\overline{WR}$	D_{15}	D_{14}	D_{13}	D_{12}	D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	0	0	1	0	0	0	1	0	A	A	A	A	A	A	A	A	A

A: the Row Address of the 2nd Display Block (0 to 319)

(4) Set the Display Line Number of the 2nd Display Block

A0	$\overline{RD}$	$\overline{WR}$	D_{15}	D_{14}	D_{13}	D_{12}	D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	0	0	1	0	0	0	1	1	0	*	*	D	D	D	D	D	D

*:Don't Care

D: the Display Line Number of the 2nd Display Block (1 to 63)

(5) Set the Row Address of the 3rd Display Block

A0	$\overline{RD}$	$\overline{WR}$	D_{15}	D_{14}	D_{13}	D_{12}	D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	0	0	1	0	0	1	0	0	A	A	A	A	A	A	A	A	A

A: the Row Address of the 3rd Display Block (0 to 319)

(6) Set the Display Line Number of the 3rd Display Block

A0	$\overline{RD}$	$\overline{WR}$	D_{15}	D_{14}	D_{13}	D_{12}	D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	0	0	1	0	0	1	0	1	0	*	*	D	D	D	D	D	D

*:Don't Care

D: the Display Line Number of the 3rd Display Block (1 to 63)

(7) Set the Row Address of the 4th Display Block

A0	$\overline{RD}$	$\overline{WR}$	D_{15}	D_{14}	D_{13}	D_{12}	D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	0	0	1	0	0	1	1	0	A	A	A	A	A	A	A	A	A

A: the Row Address of the 4th Display Block (0 to 319)

(8) Set the Display Line Number of the 4th Display Block

A0	$\overline{RD}$	$\overline{WR}$	D_{15}	D_{14}	D_{13}	D_{12}	D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	0	0	1	0	0	1	1	1	0	*	*	D	D	D	D	D	D

*:Don't Care

D: the Display Line Number of the 4th Display Block (1 to 63)

(9) Set the Row Address of the 5th Display Block

A0	$\overline{RD}$	$\overline{WR}$	D_{15}	D_{14}	D_{13}	D_{12}	D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	0	0	1	0	1	0	0	0	A	A	A	A	A	A	A	A	A

A: the Row Address of the 5th Display Block (0 to 319)

(10) Set the Display Line Number of the 5th Display Block

A0	$\overline{RD}$	$\overline{WR}$	D_{15}	D_{14}	D_{13}	D_{12}	D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	0	0	1	0	1	0	0	1	0	*	*	D	D	D	D	D	D

*:Don't Care

D5: the Display Line Number of the 5th Display Block (1 to 63)

(11) Set the Row Address of the 6th Display Block

A0	$\overline{RD}$	$\overline{WR}$	D_{15}	D_{14}	D_{13}	D_{12}	D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	0	0	1	0	1	0	1	0	A	A	A	A	A	A	A	A	A

A: the Row Address of the 6th Display Block (0 to 319)

(12) Set the Display Line Number of the 6th Display Block

A0	$\overline{RD}$	$\overline{WR}$	D_{15}	D_{14}	D_{13}	D_{12}	D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	0	0	1	0	1	0	1	1	0	*	*	D	D	D	D	D	D

*:Don't Care

D: the Display Line Number of the 6th Display Block (1 to 63)

(13) Set the Row Address of the 7th Display Block

A0	$\overline{RD}$	$\overline{WR}$	D_{15}	D_{14}	D_{13}	D_{12}	D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	0	0	1	0	1	1	0	0	A	A	A	A	A	A	A	A	A

A: the Row Address of the 7th Display Block (0 to 319)

(14) Set the Display Line Number of the 7th Display Block

A0	$\overline{RD}$	$\overline{WR}$	D_{15}	D_{14}	D_{13}	D_{12}	D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	0	0	1	0	1	1	0	1	0	*	*	D	D	D	D	D	D

*:Don't Care

D: the Display Line Number of the 7th Display Block (1 to 63)

(15) Set the Row Address of the 8th Display Block

A0	$\overline{RD}$	$\overline{WR}$	D_{15}	D_{14}	D_{13}	D_{12}	D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	0	0	1	0	1	1	1	0	A	A	A	A	A	A	A	A	A

A: the Row Address of the 8th Display Block (0 to 319)

(16) Set the Display Line Number of the 8th Display Block

A0	$\overline{RD}$	$\overline{WR}$	D_{15}	D_{14}	D_{13}	D_{12}	D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	0	0	1	0	1	1	1	1	0	*	*	D	D	D	D	D	D

*:Don't Care

D: the Display Line Number of the 8th Display Block (1 to 63)

Execute the Variable RAM Mapping Mode, by the following instruction.

A0	$\overline{RD}$	$\overline{WR}$	D_{15}	D_{14}	D_{13}	D_{12}	D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	0	0	1	1	0	0	0	0	0	*	*	*	*	*	*	*	0

*:Don't Care

Return to the normal display status from Variable RAM Mapping Mode by the following instruction execution.

A0	$\overline{RD}$	$\overline{WR}$	D_{15}	D_{14}	D_{13}	D_{12}	D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	0	0	1	1	0	0	0	0	0	*	*	*	*	*	*	*	1

*:Don't Care

(n) Gray Scale Level Select

This instruction sets the 4 levels of the gray scale. The setting of each gray scale level is executed by writing the PWM data (0 to F_H) to the four registers for the 1st to 4th frame.

The glay scale level 0 corresponds to the data (0,0) of the DD RAM, the level 1 is the data (0,1), the level 2 is the data (1,0), and the level 3 is the data (1,1), respectively.

After reset, 4 registers of each level of the gray scale, 16 registers totality, are initialized as follows. See the table below.

PWM Data	HEX	Gray Scale Level
0	00	0/15 (initialized value of level 0)
1	01	1/15
2	02	2/15
3	03	3/15
4	04	4/15
5	05	5/15 (initialized value of level 1)
6	06	6/15
7	07	7/15
8	08	8/15
9	09	9/15
10	0A	10/15 (initialized value of level 2)
11	0B	11/15
12	0C	12/15
13	0D	13/15
14	0E	14/15
15	0F	15/15 (initialized value of level 3)

(1) Set the 1st and 2nd frame PWM Data for the Gray Scale Level 0.

A0	$\overline{RD}$	$\overline{WR}$	D_{15}	D_{14}	D_{13}	D_{12}	D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	0	0	1	1	1	0	0	0	0	D1	D1	D1	D1	D2	D2	D2	D2

D1: the PWM Data for the 1st Frame
D2: the PWM Data for the 2nd Frame

(2) Set the 3rd and 4th frame PWM Data for the Gray Scale Level 0.

A0	$\overline{RD}$	$\overline{WR}$	D_{15}	D_{14}	D_{13}	D_{12}	D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	0	0	1	1	1	0	0	0	1	D3	D3	D3	D3	D4	D4	D4	D4

D3: the PWM Data for the 3rd Frame
D4: the PWM Data for the 4th Frame

(3) Set the 1st and 2nd frame PWM Data for the Gray Scale Level 1.

A0	$\overline{RD}$	$\overline{WR}$	D_{15}	D_{14}	D_{13}	D_{12}	D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	0	0	1	1	1	0	0	1	0	D1	D1	D1	D1	D2	D2	D2	D2

D1: the PWM Data for the 1st Frame
D2: the PWM Data for the 2nd Frame

(4) Set the 3rd and 4th frame PWM Data for the Gray Scale Level 1.

A0	$\overline{RD}$	$\overline{WR}$	D_{15}	D_{14}	D_{13}	D_{12}	D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	0	0	1	1	1	0	0	1	1	D3	D3	D3	D3	D4	D4	D4	D4

D3: the PWM Data for the 3rd Frame
D4: the PWM Data for the 4th Frame

(5) Set the 1st and 2nd frame PWM Data for the Gray Scale Level 2.

A0	$\overline{RD}$	$\overline{WR}$	D_{15}	D_{14}	D_{13}	D_{12}	D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	0	0	1	1	1	0	1	0	0	D1	D1	D1	D1	D2	D2	D2	D2

D1: the PWM Data for the 1st Frame
D2: the PWM Data for the 2nd Frame

(6) Set the 3rd and 4th frame PWM Data for the Gray Scale Level 2.

A0	$\overline{RD}$	$\overline{WR}$	D_{15}	D_{14}	D_{13}	D_{12}	D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	0	0	1	1	1	0	1	0	1	D3	D3	D3	D3	D4	D4	D4	D4

D3: the PWM Data for the 3rd Frame
D4: the PWM Data for the 4th Frame

(7) Set the 1st and 2nd frame PWM Data for the Gray Scale Level 3.

A0	$\overline{RD}$	$\overline{WR}$	D_{15}	D_{14}	D_{13}	D_{12}	D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	0	0	1	1	1	0	1	1	0	D1	D1	D1	D1	D2	D2	D2	D2

D1: the PWM Data for the 1st Frame
D2: the PWM Data for the 2nd Frame

(8) Set the 3rd and 4th frame PWM Data for the Gray Scale Level 3.

A0	$\overline{RD}$	$\overline{WR}$	D_{15}	D_{14}	D_{13}	D_{12}	D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	0	0	1	1	1	0	1	1	1	D3	D3	D3	D3	D4	D4	D4	D4

D3: the PWM Data for the 3rd Frame
D4: the PWM Data for the 4th Frame

(o) Bias Select

This instruction sets the bias voltage. (1/4 to 1/14 Bias)

A0	$\overline{RD}$	$\overline{WR}$	D_{15}	D_{14}	D_{13}	D_{12}	D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	0	0	0	0	0	1	0	0	1	*	*	*	*	A_3	A_2	A_1	A_0

*:Don't Care

A_3	A_2	A_1	A_0	Bias
0	0	0	0	1/4
0	0	0	1	1/5
0	0	1	0	1/6
0	0	1	1	1/7
0	1	0	0	1/8
0	1	0	1	1/9
0	1	1	0	1/10
0	1	1	1	1/11
1	0	0	0	1/12
1	0	0	1	1/13
1	*	1	*	1/14

* : Don't Care

(p) Boost Level Select

This instruction sets the boost level (2 to 7 times). When "Partial Display Instruction" execution, the "Boost Level Select" also must be executed. If the external capasitors are connected as the lower than 6 times boost level, don't set the boost level by the instruction over than the boost level by conecting capasitors. If set the boost level over than it, the device will make malfunction.

A0	$\overline{RD}$	$\overline{WR}$	D_{15}	D_{14}	D_{13}	D_{12}	D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	0	0	0	0	0	1	0	1	0	*	*	*	*	*	A_2	A1	A0

*:Don't Care

A_2	A_1	A_0	Boost Level
0	0	0	2-times
0	0	1	3-times
0	1	0	4-times
0	1	1	5-times
1	0	0	6-times
1	*	1	7-times

* : Don't Care

(q) Read Modify Write / End

This instruction sets the Read Modify Write/End controlling the page address increment. In this mode, the Column Address only increments when execute the display data "Write" instruction; but no change when the display data "Read" Instruction. This status is continued until the End instruction execution. When the End instruction is executed, the Column Adddress goes back to the start address before the execution of this "Read Modify Write" instruction. This function reduces the load of MPU for repeating display data change of the fixed area (ex. cursor blink).

A0	$\overline{RD}$	$\overline{WR}$	D_{15}	D_{14}	D_{13}	D_{12}	D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	0	0	0	0	0	0	0	0	0	*	*	*	*	*	*	*	D

* : Don't Care

D=0: Read Modify Write ON

D=1: End

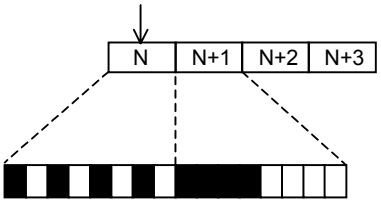
(Note) In this "Read Modify Write" mode, out of display dara "Read"/"Write", any instructions except "Row Address Set" can be executed.

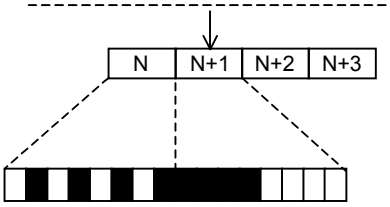
The Example of Read Modify Write Sequence

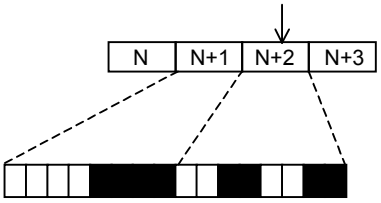
Executed Instructions

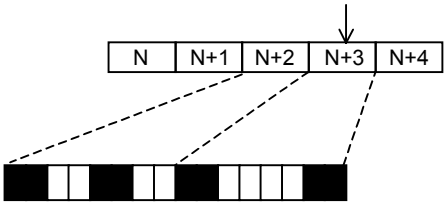
Display Contents

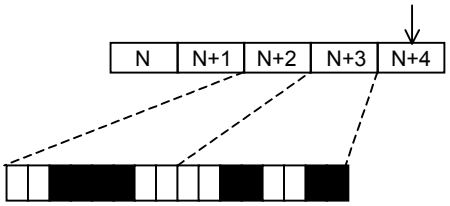
(In 8-bit bus mode, ↓ indicates the column Address)

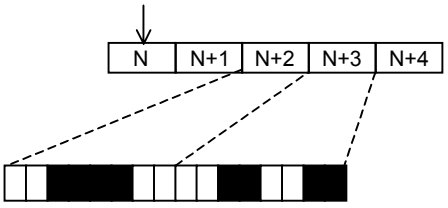




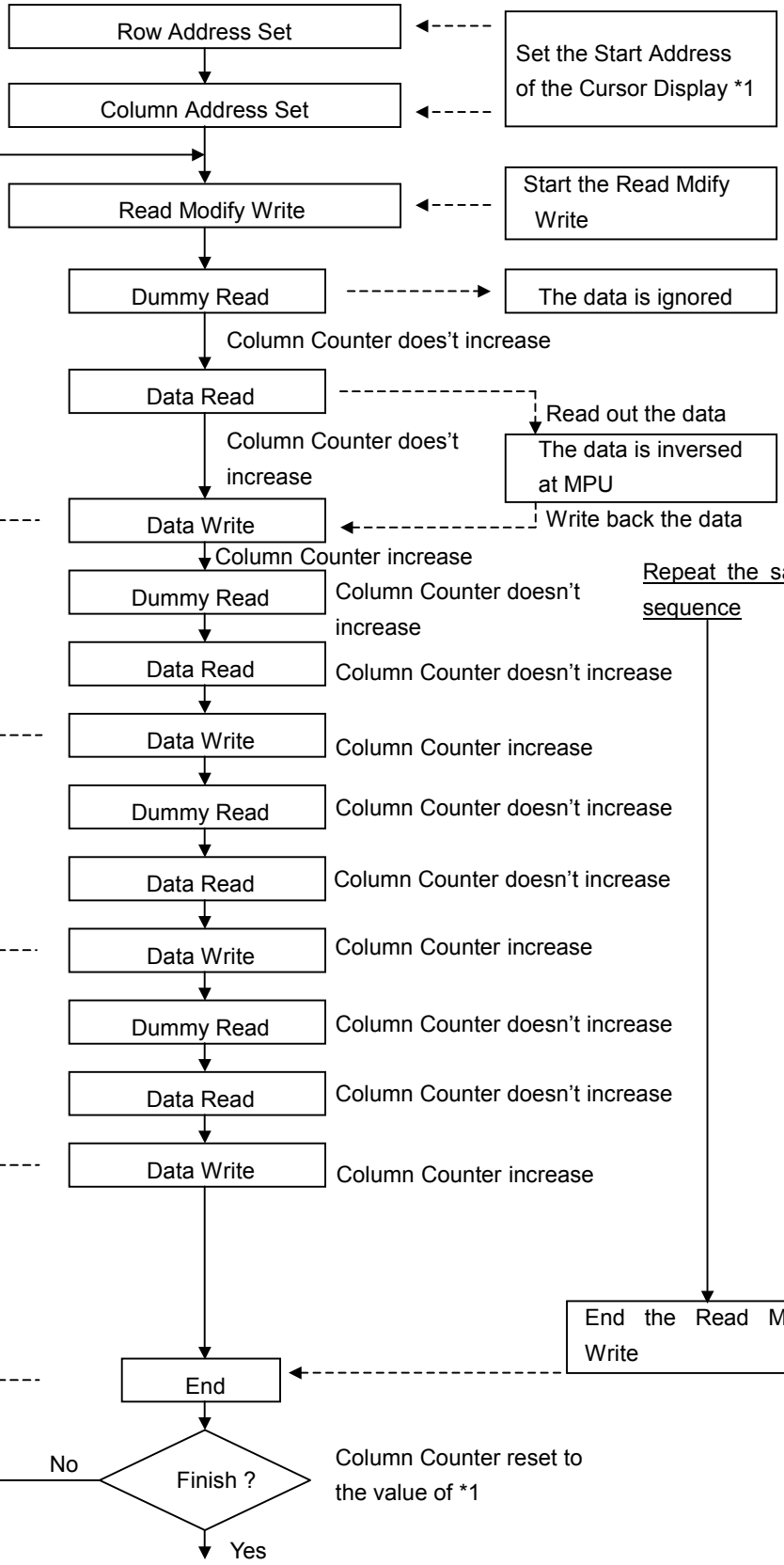








Executed Instructions



(r) Reset

This instruction executes the following initialization

The reset by the reset signal input to the $\overline{RES}$ terminal (hardware reset) is required when power turns on. This reset instruction does not use instead of this hardware reset when power turns on.

Initialization

1: Clear the data in the Selial Interface register.
2: Set the Column Address Counter to 00_H.
3: Set the Row Address Resister to 000_H.
4: Set the Line Address Counter to 000_H
5: Set the Gray Scale Level (refer to "(n))
6: Normal RAM Address Mapping (Variable RAM Mapping Mode OFF).
7: Set the EVR Resister to FF_H.
8: Set the Duty ratio to "1/160"(All ON).
9: Set the Bias ratio to "1/14".
10: Set the Booster Level to 7 times.
11: Set the n-Line Inverse Register to 0_H.
12: Set the 8-bit Bus length for the interface

The DD RAM is not affected in this Initialization.

A0	$\overline{RD}$	$\overline{WR}$	D_{15}	D_{14}	D_{13}	D_{12}	D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	0	0	0	0	1	0	0	0	1	*	*	*	*	*	*	*	D

* : Don't Care

The DD RAM is not affected in this instruction

(s) Internal Power Supply

This instruction control ON and OFF for the internal Voltage Converter, Voltage Regulator and Voltage Follower circuits. For the Booster circuits operation, the oscillation circuits must be in operation.

A0	$\overline{RD}$	$\overline{WR}$	D_{15}	D_{14}	D_{13}	D_{12}	D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	0	0	0	0	1	0	0	1	0	*	*	*	*	*	DC	VR	VF

* : Don't Care

DC=1: Booster ON
DC=0: Booster OFF*1)
VR=1: Voltage Regulator ON
VR=0: Voltage Regulator OFF*2)
VF=1: Voltage Follower ON
VF=0: Voltage Follower OFF*3)

*1) At this time, terminals C_1^+,C_1^-,C_2^+,C_3^-,C_4^-,C_5^- and C_6^- should be open, and supply the V_{OUT} from outside.
*2) At this time, terminal V_R should be open, and supply the V_5 from outside.
*3) At this time, bias voltage of V_1 to V_5 should be supplied from outside.

*The Internal Power Supply rise time is depending on the condition of the Supply Voltage, $V_{LCD}=V_{DD}-V_5$, External Capacitor of Booster, and External Capacitor connected to V_1 to V_5. To know the rise time correctly, test by using the actual LCD module.

(t) Driver Outputs ON/OFF
This instruction controlls ON/OFF of the LCD Driver Outputs.

A0	$\overline{RD}$	$\overline{WR}$	D_{15}	D_{14}	D_{13}	D_{12}	D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	0	0	0	0	1	0	0	1	1	*	*	*	*	*	*	*	D

* : Don't Care

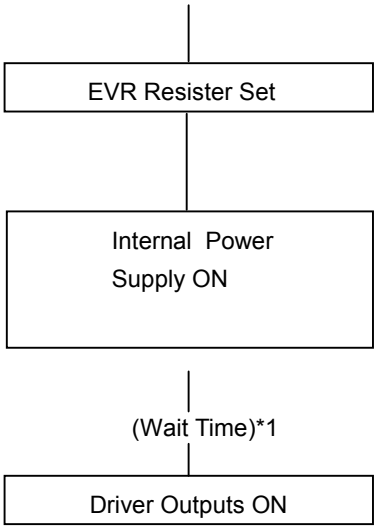
D=0: Driver Outputs OFF(Signai is V_{DD} level)
D=1: Driver Outputs ON (Signal is output)

The NJU6682 implements low power LCD driving voltage generator circuit and requires the following Power Supply ON/OFF sequence.

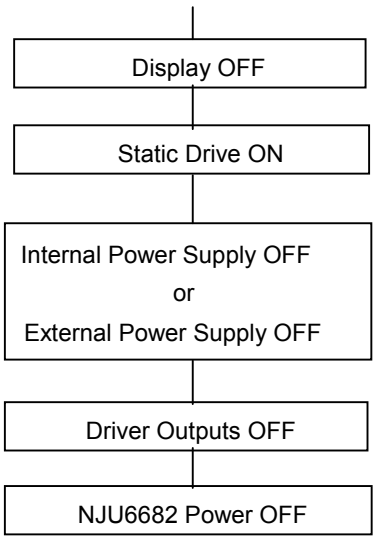
- LCD Driving Power Supply ON/OFF Sequences

The sequences below are required when the power supply turns ON/OFF.
For the power supply turning on operation after the power-save mode, refer the (u) "power save release sequence" mentioned after.

❍Turn ON Sequence



❍Turn OFF Sequence



*1 The Internal Power Supply rise time is depending on the condition of the Supply Voltage, $V_{LCD}=V_{DD}-V_5$, External Capacitor of Booster, and External Capacitor connected to V_1 to V_5. To know the rise time correctly, test by using the actual LCD module.

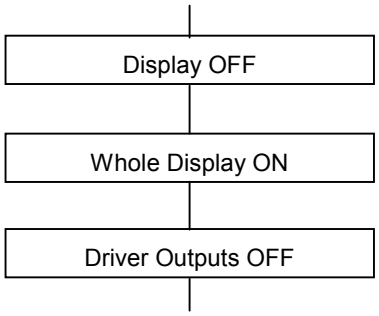
(u) Power Save (complex comand)

When Whole Display ON at the Display OFF status (inverse order also same), the internal circuits goes to the Power Save Mode and the operating current is dramatically reduced, almost same as the standby current.

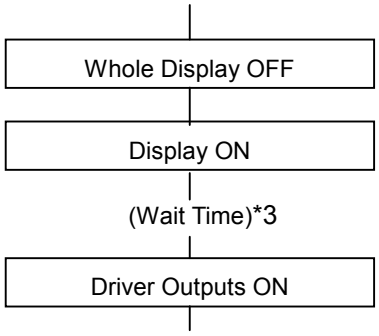
The internal status in the Power Save Mode is shown as follows;

1: The Oscillation Circuits and the Internal Power Supply Circuits stop the operation.
2: LCD driving is stopped. Segment and Common drivers output V_{DD} level voltage.
3: The display data and the internal operating condition are remained and kept as just before enter the Power Save Mode.
4: All the LCD driving bias voltage (V_1 to V_5) is fixed to the V_{DD} level.

❍Power Save Sequence *1



❍Power Save Release Sequence *2



*4

*1 In the Power Save sequence, the Power Save Mode starts after the Static Drive ON command is executed.
*2 In the Power Save Release sequence, the Power Save Mode releases just after the Static Drive OFF instruction execution. The Display ON instruction is allowed to execute at any time after the Static Drive OFF instruction is completed.
*3 The Internal Power Supply rise time is depending on the condition of the Supply Voltage, $V_{LCD}=V_{DD}-V_5$, External Capacitor of Booster, and External Capacitor connected to V_1 to V_5. To know the rise time correctly, test by using the actual LCD module
*4 LCD driving waveform is output after the exection of the Driver Outputs ON instruction execution.
*5 In case of the external power supply operation, the external power supply should be turned off before the Power Save Mode and connected to the V_{DD} for fixing the voltage of Vout terminal.. In this time, V_{OUT} terminal also should be made codition like as connection to the V_{SS} terminal.

(v) ADC Select

This instruction determines the correspondence of Column Address of the DD RAM with the Segment Driver Outputs.(refer to Fig.1-1 DD RAM addressing)

Segment Driver Output order is inverse when this instruction executes, therefore, the placement the NJU6682 against the LCD panel becomes easy.

A0	$\overline{RD}$	$\overline{WR}$	D_{15}	D_{14}	D_{13}	D_{12}	D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	0	0	0	0	1	1	0	0	0	*	*	*	*	*	*	*	D

*:Don't Care

D=0: Clockwise Output (Normal)
D=1: Counterclockwise Output (Inverting)

(w) Display Mode Select

This instruction selects the Display Mode.

A0	$\overline{RD}$	$\overline{WR}$	D_{15}	D_{14}	D_{13}	D_{12}	D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	0	0	0	0	1	1	0	0	1	*	*	*	*	*	GS	L_1	L_0

*:Don't Care

GS=1: Gray Scale Mode
GS=0: Black & White Mode

* When GS=0(Black & White Mode), the following L_1 and L_0 bit are valid.
L_1=1: Select the Layer 1
L_1=0: Not select the Layer 1
L_0=1: Select the Layer 0
L_0=0: Not select the Layer 0
If L_1=L_0=0, the display data becomes 0
And if L1=L0=1, the display data becomes logical OR of the Layer 0 and Layer 1. GS=1: Gray Scale Mode

(x) 8-/16-bit Bus Interface Select

This instruction selects the 8-bit or 16-bit bus interface length.

A0	$\overline{RD}$	$\overline{WR}$	D_{15}	D_{14}	D_{13}	D_{12}	D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	0	0	0	0	1	1	0	1	D	*	*	*	*	*	*	*	*

*:Don't Care

D=0: Select 8-bit bus interface length (D_7 to D_0).
D=1: Select 16-bit bus interface length (D_{15} to D_0)

(4) Internal Power Supply

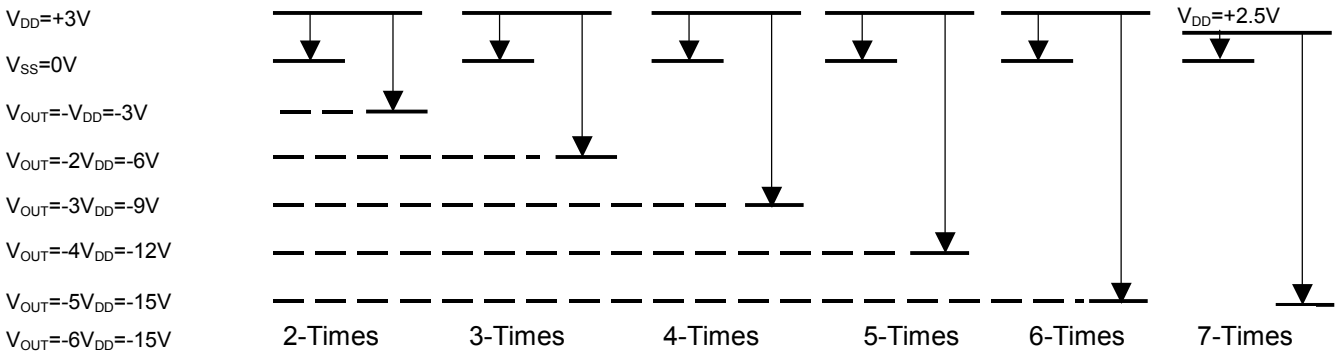
(4-1) 7-Time Voltage Booster circuits

The 7-time voltage booster circuit outputs the negative Voltage(V_{DD} Common) boosted 7 times of V_{DD}-V_{SS} from the V_{OUT} terminal with connecting the seven capacitors between C_1^+ and C_1^-, C_2^+ and C_2^-, C_1^+ and C_3^-, C_2^+ and C_4^-, C_1^+ and C_5^-, C_2^+ and C_6^-,and V_{SS} and V_{OUT}. The boosting time is selected out of 2 times to 7 by the combination of changing the external capacitors connection and "Boost Level Select" instruction. (refer to (2)Instruction (q)Voltage Boost time select)

Voltage Booster circuits requires the clock signals from internal oscillation circuit or the external clock signal. therefore, the internal oscillation circuits or the external clock supplier must be operating when the voltage booster is in operation.

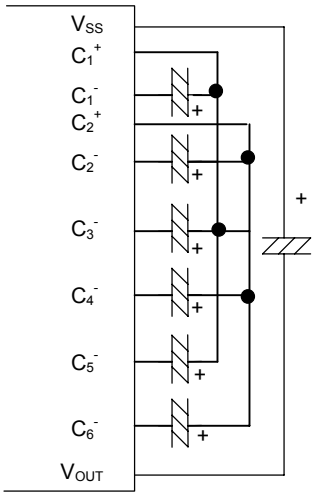
The boosted voltage of V_{DD}-V_{OUT} must be 18V or less.

The boost voltage and the capacitor connection are shown below.

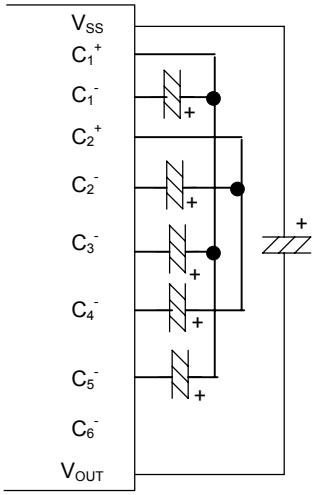


; V_{DD}=+2.5V for voltage limitation

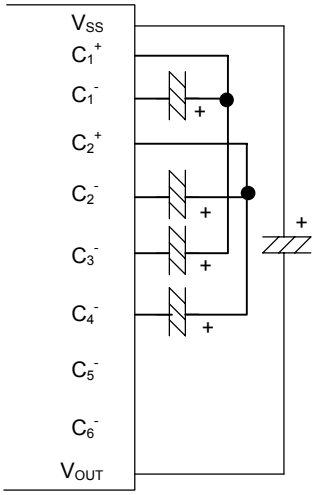
7-Times Voltage



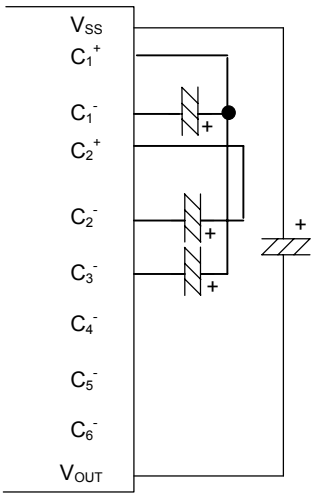
6-Times Voltage



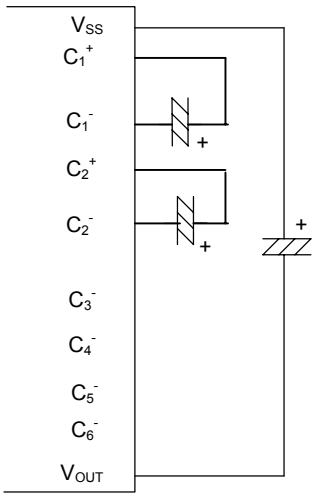
5-Times Voltage



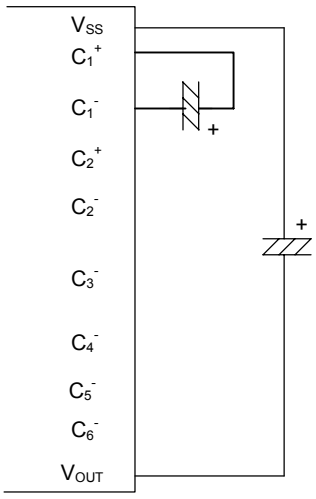
4-Times Voltage



3-Times Voltage



2-Times Voltage



(4-2)Voltage Adjust Circuit

The boosted voltage of V_{OUT} outputs V_5 for LCD driving through the voltage adjust circuits. The output voltage of V_5 is adjusted by Ra and Rb within the range of $|V_5| < |V_{OUT}|$.
The output is calculated by the following formula(1).

$$V_{LCD}=V_{DD}-V_5=(1+Rb/Ra)\bullet V_{REG} \quad \text{----------(1)}$$

The V_{REG} voltage is a reference voltage generated by the built-in bleeder registance. V_{REG} is adjustable by EVR functions (see section 4-3).

For minor adjustment of V_5, it is recommended that the Ra and Rb is composed of R_2 as variable resistor and R_1 and R_3 as fixed resistors, constant should be connected to V_{DD} terminal,VR and V_5 ,as shown below. (refer to Fig.5)

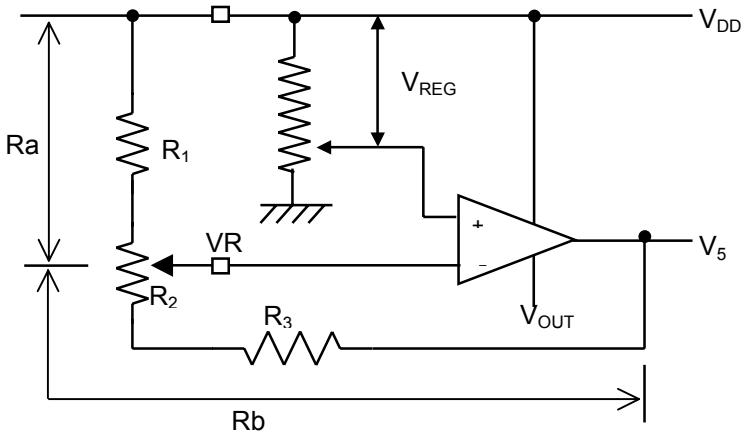


Fig.5 Voltage Adjust Circuit

< Design example for R_1, R_2 and R_3 /Reference >

- $R_1+R_2+R_3=5M\Omega$
  (Determind by the current between V_{DD}-V_5)
- Variable voltage range by the R_2. -7V to -11V ($V_{LCD}=V_{DD}$-V5 : 10V to 12V)
  (Determind by the LCD electrical characteristics)
- V_{REG}=3V
  (In case of V_{DD}=3V and EVR=FF_H)

R_1,R_2 and R_3 are calculated by above conditions and the fomula of(1) to below;

R1=1.5MΩ
R2=0.3MΩ
R3=4.2MΩ

Note) V_5 voltage is generated referencing with V_{REG} voltage beased on the supply voltage (V_{DD} and V_{SS}) as shown in above Figure 5. Therefore, V_{LCD} (V_{DD}-V_5) is affected including the gain (Rb/Ra) by the fluctuation of V_{REG} voltage based on the supply voltage. The power supply voltage should be stabilized for V_5 stable operation.

(4-3)Contrast adjustment by the EVR function

The EVR selects the V_{REG} voltage out of the following 201 conditions by setting 8-bit data into the EVR register. With the EVR function, V_{REG} is controlled, and the LCD display contrast is adjusted. The EVR controls the voltage of V_{REG} by instruction and changes the voltage of V_5.

A step with EVR is set like table shown below.

* If keeping 3% precision set EVR over $4F_H$.

EVR register	V_{REG}
37_H	(100/300) x (V_{DD}-V_{SS})
38_H	(101/300) x (V_{DD}-V_{SS})
39_H	(102/300) x (V_{DD}-V_{SS})
:	:
:	:
:	:
:	:
FD_H	(298/300) x (V_{DD}-V_{SS})
FE_H	(299/300) x (V_{DD}-V_{SS})
FF_H	(300/300) x (V_{DD}-V_{SS})

In use of the EVR function, the voltage adjustment circuit must turn on by the power supply instruction.

● Adjustable range of the LCD driving voltage by EVR function

The adjustable range is decided by the power supply voltage V_{DD} and the ratio of external resistors Ra and Rb.

< Design Example : NJU6682 >

Condition:V_{DD}=3.0V

Ra=1MΩ, Rb=4MΩ (Ra:Rb=1:4)

The adjustable range and step voltage are calculated as follows in the above condition.

In case of setting $4F_H$ in the EVR register,

VLCD=(1+Rb/Ra) x V_{REG}

=(1+4) x (124/300) x 3.0

=6.2V

In case of setting FF(H) in the EVR register,

VLCD=(1+Rb/Ra) x VREG

=(1+4) x (300/300) x 3.0

=15.0V

	(min.)$4F_H$	(max.)FF_H
Adjusutment Renge (V_{LCD})	6.2 ••••••••••••••••••••	15.0 [V]
Step Voltage (V_{LCD})	50	[mV]

* In case of V_{DD}=3V

(4-4)LCD Driving Voltage Generation Circuit

The LCD driving bias voltage of V_1,V_2,V_3,V_4 are generated by dividing the V_{LCD}(V_{LCD}=V_{DD}-V_5) voltage with the internal bleeder resistance and is supplied to the LCD driving circuits after the impedence conversion by the voltage follower.

As shown in Figure 6, five external capacitors are required to connect to each LCD driving voltage terminal for voltage stabilization. The value of capacitors (C_7 to C_{11}) should be determined after the actual LCD panel display evaluation.

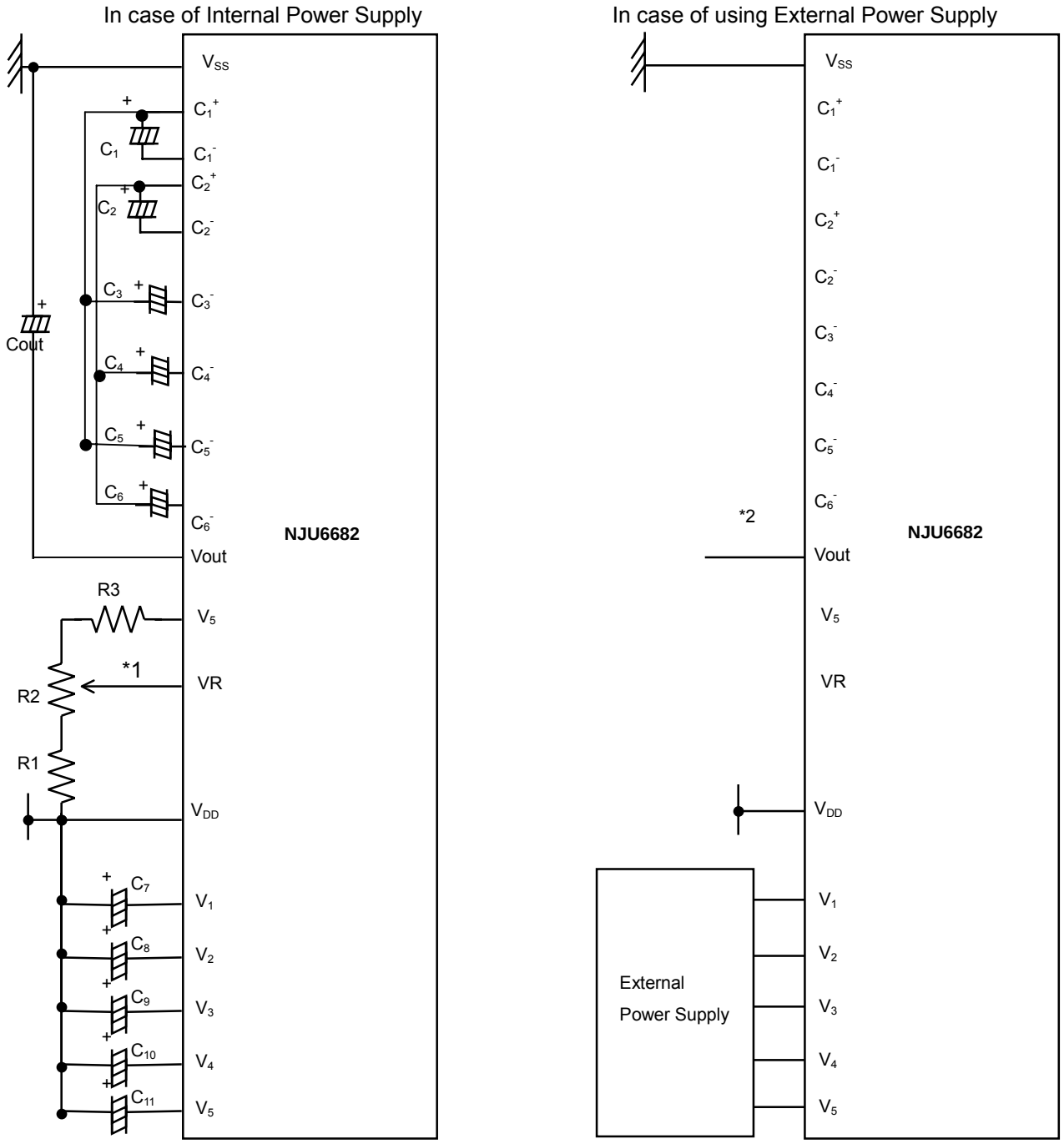


Fig.6 LCD Driving Voltage Generation Circuit

*1 Short wiring or sealed wiring to the VR terminal is required due to the high impedance of VR Terminal.

*2 Following connection of V_{OUT} is required when external power supply using.
When V_{SS}>V_5 --- V_{OUT}=V_5
When V_{SS}≤V_5 --- V_{OUT}=V_{SS}

Reference set up value
V_{LCD}=V_{DD}-V_5≅9.0 to 10.5V

COUT	to 1.0uF
C1 to C6	to 1.0uF
C7 to C11	0.1 to 0.47 uF
R1	2MΩ
R2	500KΩ
R3	2.5MΩ

(5)MPU Interface

(5-1) Interface type selection

Two MPU interface types are available in the NJU6682: by 1) 8/16-bit bi-directional data bus (D_{15} to D_0), 2) serial data input (SI:D_7). The interface type (the 8/16 bit parallel or serial interface) is determined by the condition of the PS_1 and PS_0 terminals connecting to "H" or "L" level as shown in Table 5. In case of the parallel interface, the external bus line selection is set by the “8-bit/16-bit Bus Select” instruction. In case of the serial interface, neither the status read-out nor the RAM data read-out operation is allowed.

Table 5

PS_1	PS_0	Type		$\overline{CS}$	A0	$\overline{RD}$	$\overline{WR}$	SEL68	D_{15}–D_8	D_7	D_6	D_5–D_0
H	*	Parallel	8-bit Bus	$\overline{CS}$	A0	$\overline{RD}$	$\overline{WR}$	SEL68	Hi-Z	D_7	D_6	D_5–D_0
			16-bit Bus	$\overline{CS}$	A0	$\overline{RD}$	$\overline{WR}$	SEL68	D_{15}–D_8	D_7	D_6	D_5–D_0
L	H	Serial (4-wire)		$\overline{CS}$	A0	*	*	*	Hi-Z	SI	SCL	Hi-Z
	L	Serial (3-wire)			*							

*:Don’t care

(5-2)Parallel interface(PS_1=”H”)

The NJU6682 interfaces the 68- or 80-type MPU directly if the parallel interface (PS_1="H") is selected.

The 68-type or 80-type MPU is selected by connecting the SEL68 terminal to "H" or "L" as shown in table 6.

Table 6

SEL68	Type	$\overline{CS}$	A0	$\overline{RD}$	$\overline{WR}$	D_{15}–D_8	D_7–D_0
H	68 type MPU	$\overline{CS}$	A0	E	R/W	D_{15}–D_8	D_7–D_0
L	80 type MPU	$\overline{CS}$	A0	$\overline{RD}$	$\overline{WR}$	D_{15}–D_8	D_7–D_0

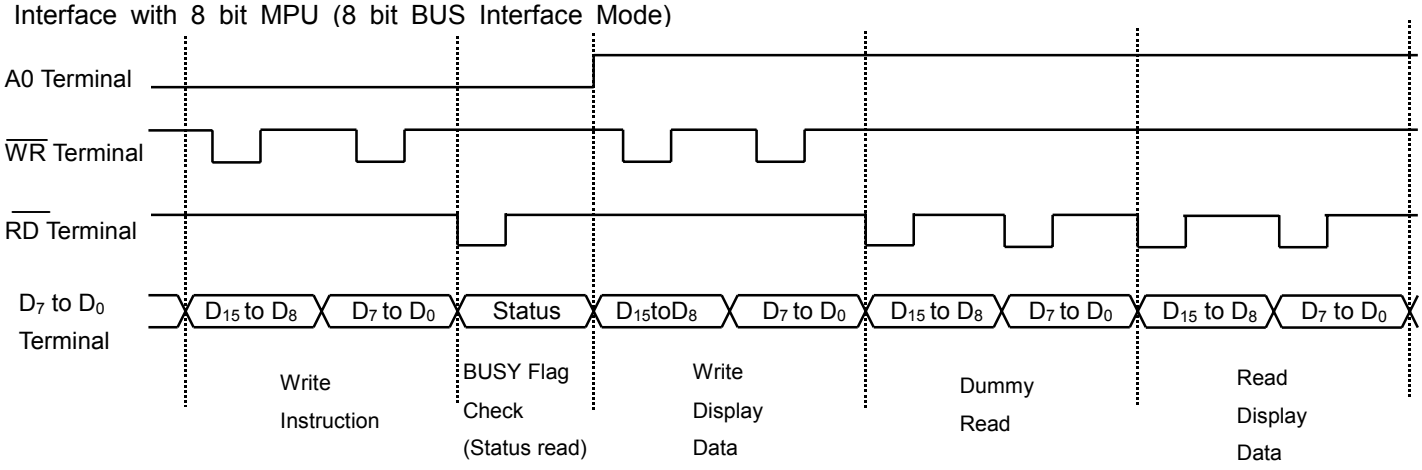
- Interface operation with MPU

The NJU6682 can be connected to MPU with the 8/16-bit interface: transferring data twice by 8-bit ,or Once by 16-bit.

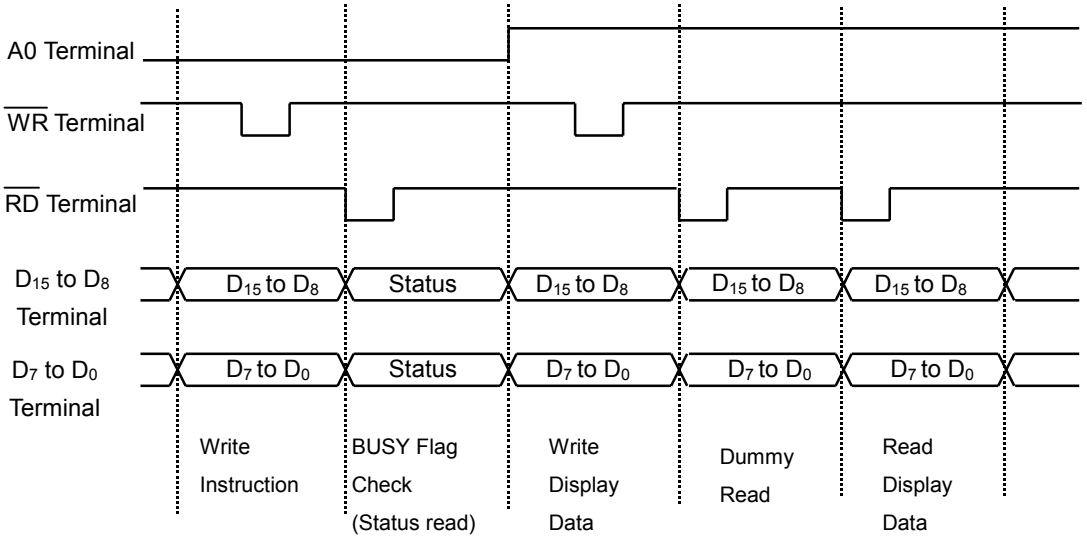
When the 8-bit bus interface is selected, data is transferred only through the D_0–D_7; the D_8–D_{15} lines are not used with this interface. Then, the 8-bit data transmission is performed twice to complete the data transmission.. The data transmisson is executed through the upper 8 bits(D_{15}–D_8) and through the lower 8 bits(D_7–D_0), respectively. If checking the Busy Flag(status read) is required, it should be performed after the 2nd data transmission. In this case, the status read is completed only once.

When 16-bit bus interface is selected, D_0–D_{15} lines as 16-bit bus are used once to complete the data transmission.

(a) Interface with 8 bit MPU (8 bit BUS Interface Mode)



(b) Interface with 16 bit MPU (16 bit BUS Interface Mode)



(5-3) Serial Data Input (PS_1="L")

The serial interface of the NJU6682 consists of the 16-bit shift register and 4-bit counter. In case the chip is selected ($\overline{CS}$=L), the input to D_7(SI) and D_6(SCL) becomes available, and in case that the chip isn't selected, the shift register and the counter are reset to the initial condition.

The data input from the terminal(SI) is MSB first like as the order of D_{15}, D_{14}, ••• D_0 by a serial interface, it is entered into with rise edge of serial clock(SCL). The data converted into parallel data of 16-bit with the rise edge of 16th serial clock and processed.

The serial interface of the NJU6682 can be selected out of the 3-wire or 4-wire type according to the PS_0 terminal. In chosen PS_0 terminal to "H", it becomes 4-wire interface and discriminates display data or instructions by A0 input terminal. A0 is read with rise edge of (16 X n)th of serial clock (SCL), it is recognized display data by A0=H" and instruction by A0="L". A0 input is read in the rise edge of (16 X n)th of serial clock (SCL) after chip select and distinguished.

However,in case of $\overline{RES}$="L" or $\overline{CS}$="H" with trasfered data does not fill 16 bit, attention is necessary because it will processed as there was command input. Always, input the data of (16 X n) style. In chosen PS_0 terminal to "L",it becomes 3-wire interface and discleminate data after the serial data of 16-bit as the A0 data.

Note) The SCL signal must be careful of the termination reflection by the wiring length and the external noise and confirmation by the actual machine is recommended by it.

(a) 4-wired Serial Interface

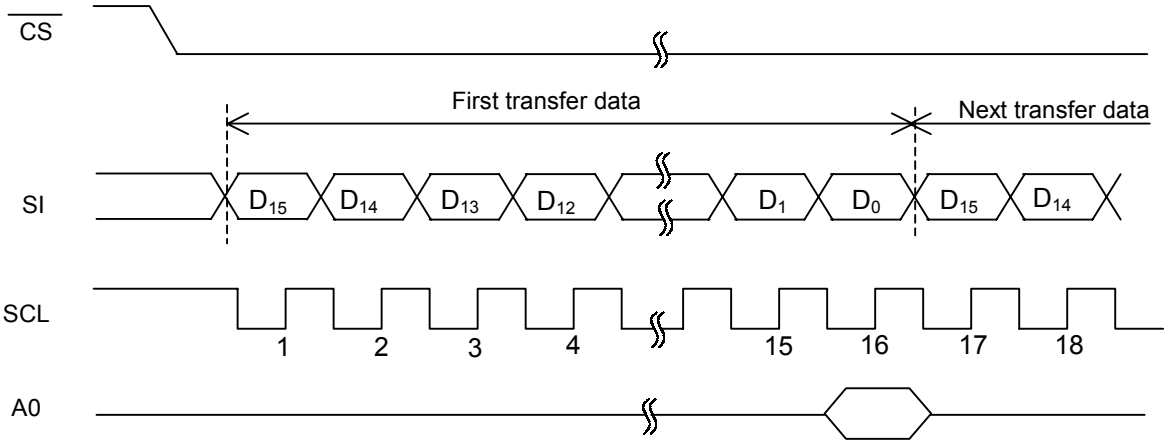


Fig 7-1 4-wired Serial Interface

A0=”H”: Display Data
A0=”L”: Instruction

(b) 3-wire Serial Interface

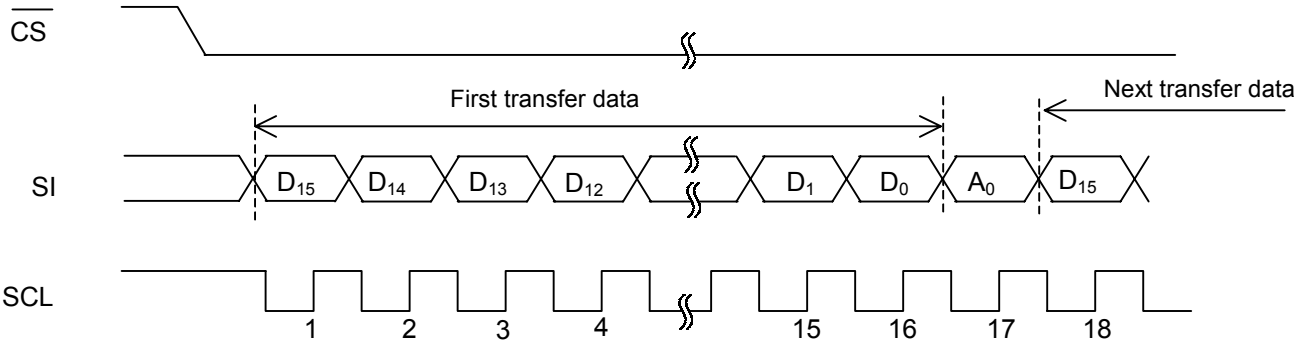


Fig 7-2 3-wire Serial Interface

A0="1":Display Data
A0="0":Instruction

(5-4)Display Data RAM , Access of Internal Register

The **NJU6682** transfers data to the CPU through the bus holder with the internal data bus.

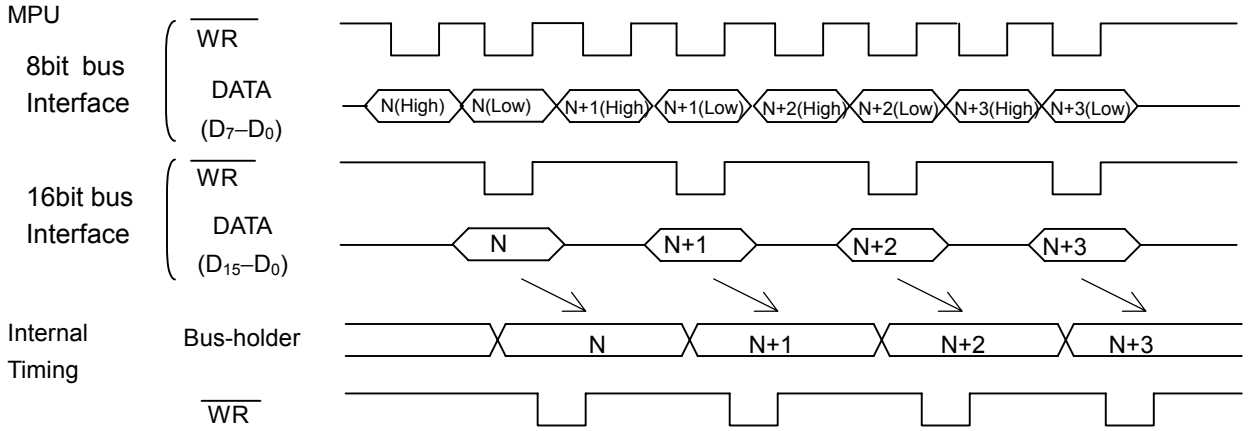
In case of reading out the display data contents in the DD RAM, the data which was read in the first data read cycle (= the dummy read) is memorized in the bus holder. Then the data is read out to the system bus from the bus holder in the next data read cycle. Also, In case that the MPU writes into DD RAM, the data is temporarily stored in the bus holder and is then written into DD RAM by the next data write cycle.

Therefore, the limitation of the access to **NJU6682** from MPU side is not access time (t_{ACC},t_{DS}) of Display Data RAM and the cycle time becomes dominant. With this, speed-up of the data transfer with the MPU becomes possible. In case of cycle time isn't met, the MPU inserts NOP operation only and becomes an equivalent to an execution of wait operation on the sutisfy condition in MPU.

When setting an address, the data of the specified address isn't output immediately by the read operation after setting an address, and the data of the specified address is output at the the 2nd data read operation. Therefore, the dummy read is always necessary once after the address set and the write cycle. (See Fig. 8)

The exsample of Read Modify Write operaion is mentioned in (2-1) Description of the Instruction codesInstruction (q) “ Read Modify Write / End” .)

● Write Operation



● Read Operation

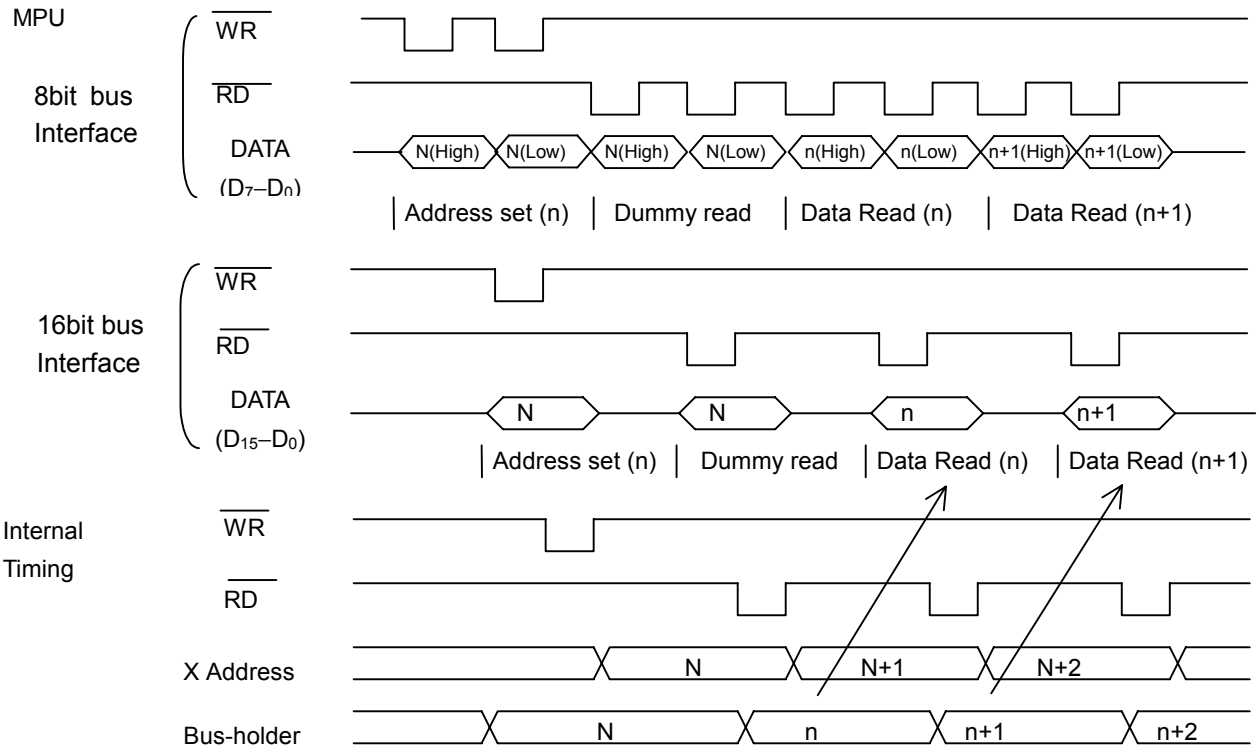


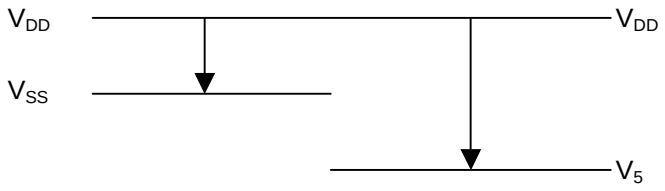
Fig.8 Relation of Display Read/Write and Internal Timing

(5-5) Chip Select

$\overline{CS}$ is the Chip Select terminal. In case of $\overline{CS}$="L", the interface with MPU is available.
In case of CS="H" (Chip is not selected), the terminals of D_0 to D_{15} are high impedance and A0, $\overline{RD}$, $\overline{WR}$, D_7(SI) and D_6(SCL) inputs are ignored. If the serial interface is selected when $\overline{CS}$="H", the shift register and the counter for the serial interface are reset.
However, the reset signal is always input and executed in any conditions of $\overline{CS}$.

■**ABSOLUTE MAXIMUM RATING**

PARAMETER		SYMBOL	RATINGS	UNIT
Supply Voltage(1)		V_{DD}	-0.3 to +5.0	V
Supply Voltage(2)		V_5 , V_{OUT}	V_{DD}-20.0 to V_{DD}+0.3	V
Supply Voltage(3)		V_1,V_2,V_3,V_4	V_5 to V_{DD}+0.3	V
Input Voltage		V_{IN}	-0.3 to V_{DD}+0.3	V
Operating Temperature		T_{OPR}	-30 to +80	°C
Strage Temperature	TCP	T_{STG}	-55 to +100	°C
	Chip		-55 to +125	



(* 1) Voltage value is specified as V_{SS}=0V.
(* 2) The relation of $V_{DD}\geq V_1\geq V_2\geq V_3\geq V_4\geq V_5\geq V_{OUT}$; $V_{DD}>V_{SS}\geq V_{OUT}$ must be maintained.
In case of inputting external LCD driving voltage , the LCD drive voltage should start supplying to **NJU6682** at the mean time of turning on V_{DD} power supply or after turned on V_{DD} .
In use of the voltage boost circuit, the condition that the supply voltage: 18.0V≥V_{DD}-V_{OUT} is necessary.
(* 3) If the LSI are used on condition beyond the absolute maximum rating, the LSI may be destroyed.
Using LSI within electrical characteristics is strongly recommended for normal operation.
Use beyond the erectric characteristics conditions will cause malfunction and poor reliability.
(* 4) Decoupling capacitor should be connected between V_{DD} and V_{SS} due to stabilized operation, especially for the Voltage Converter.

■ELECTRICAL CHARACTERISTICS

(V_{DD}=2.4 to 3.3V, V_{SS}=0V, Ta=-30 to +80°C)

PARAMETER		SYMBOL	CONDITIONS		MIN	TYP	MAX	UNIT	NOTE
Operating voltage(1)		V_{DD}			2.4		3.3	V	5
Operating Voltage(2)		V_5			V_{DD}-18.0V		V_{DD}-6.0V	V	6
		V_1,V_2	V_{LCD}=V_{DD}-V5		V_{DD}-0.5VLCD		V_{DD}		
		V_3,V_4			V5		V_{DD} - 0.5V_{LCD}		
Input Voltage	High Level	V_{IHC1}	A0,D_0-D_{15},$\overline{RD}$,$\overline{WR}$,$\overline{RES}$,$\overline{CS}$ Exclude P/S, SEL68,OSC1 terminal		0.8V_{DD}		V_{DD}	V	
	Low Level	V_{ILC1}			V_{SS}		0.2V_{DD}		
Output Voltage	High Level	V_{HC11}	D_0toD_1 Terminal	I_{OH}=-0.5mA	0.8V_{DD}		V_{DD}	V	
	Low Level	V_{OLC11}		I_{OL}= 0.5mA	V_{SS}		0.2V_{DD}		
Input Leagage Current		I_{LI0}	All input terminal, D_0 to D_{15} Terminal in High Z		-1.0		1.0	µA	
Driver On-resistance		R_{ON}	Ta=25°C V_{LCD}=15V			2.0	3.0	kΩ	7
Stand-by Current		I_{DDQ}	During Power Save Mode			T.B.D	T.B.D	µA	8
Operating Current		I_{DD01}	Display V_{LCD}=16V			T.B.D	T.B.D	µA	8
In use external Power supply		I_{DD02}	Access f_{CYC}=200KHz			T.B.D	TBD	µA	9
Input Terminal Capacitance		CIN	Ta=25°C			10		pF	10
Oscillation Frequency		f_{OSC}	VDD= 3.0V, Ta=25°C			T.B.D		kHz	
Reset Time		t_R	$\overline{RES}$ terminal		1.0			µS	11
Reset "L" level pulse Width		t_{RW}			10			µS	12

Voltage boost output voltage	V_{OUT1}	7-times boost, V_{DD}=2.5V	V_{DD}-17.5V		V_{DD}-17.0V	V	
Voltage boost On-resistance	R_{TRI}	7-times boost, V_{DD}=2.5V,Cout=4.7µF			3.0	kΩ	
Adjustment range of LCD driving Voltage	V_{OUT2}	Voltage boost operation off	V_{DD} - 8.0V		V_{DD} - 6.0V	V	13
Voltage Follower	V_5	Voltage adjustment circuit "OFF"	V_{DD} - 18.0V		V_{DD} - 6.0V	V	
Operating Current In use internal power supply	I_{OUT1}	Display V_{DD}=3V,V_{LCD}=16V, 6-time boost COn/Sn are Open , non-access , Display Checkerd pattern		300	T.B.D	µA	14
Voltage Regulator	V_{REG}%	V_{DD}=3.0V, Ta=25°C			T.B.D	%	

*5:Although the **NJU6682** can operate in wide range of the operating voltage, it shall not be guaranteed in a sudden voltage fluctuation during the access with MPU.

*6:The operating voltage when using external power supply.

*7:R_{ON} is the resistance values in supplying 0.1V voltage-difference beteen power supply terminals (V_1,V_2,V_3,V_4) and each output terminals (common/ segment). This is specified within the range of Operating Voltage(2).

*8,9:Refers to the current consumption of the IC itself; external power supply is used for the LCD driving. In case of not use internal power supply circuit,meaning current of IC's. LCD driving power supply are external power supply.

*8,9:The value of after Driver Output On instruction execution.

*8:Applicable in case of not accessing to the MPU.

*9:The operating current when writing a vertical stripe pattern on the tcyc. Current consumption during the access is approximately proportional to the access frequency. When not accessed, it consumpts only I_{DD01}.

*10:Apply to A0,D_0-D_{15},$\overline{RD}$,$\overline{WR}$,$\overline{CS}$,$\overline{RES}$,SEL68,PS_0,PS_1 terminals

*11:t_R (Reset Time) refers to the reset completion time of the internal circuits from the rise edge of the $\overline{RES}$ signal.

*12:Apply minimum pulse width of the $\overline{RES}$ signal. To reset, the "L" pulse over t_{RW} shall be input. .

*13:The voltage adjustment circuit controls V_5 within the range of the voltage follower operating voltage.

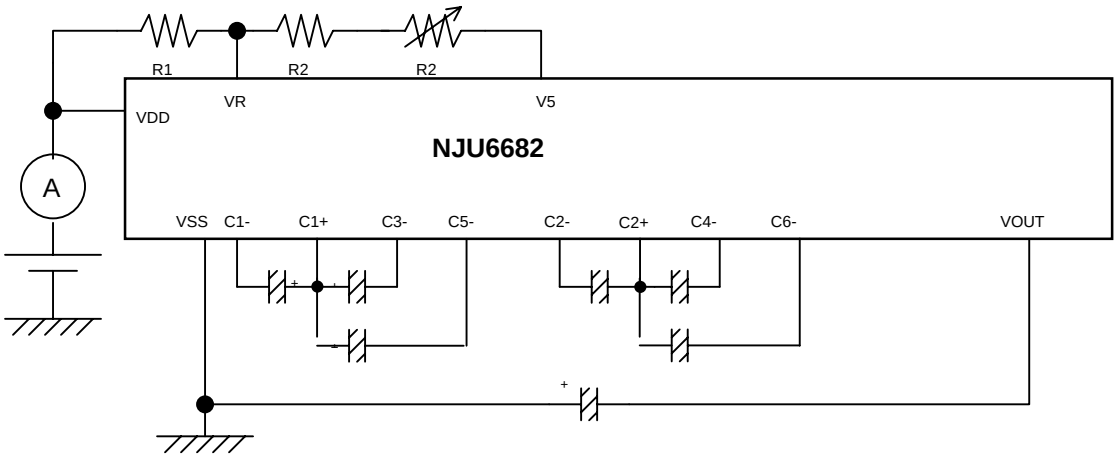
*14:Each operating current shall be defined as being measured in the following condition.

SYMBOL	POWER SUPPLY SET INSTRUCTION			OPERATING CONDITION				EXTERNAL VOLTAGE SUPPLY (INPUT TERMINAL)
	DC	VR	VF	Internal Oscillator	Voltage Booster	Voltage Adjustment	V/F Circuit	
I_{DD1}	1	1	1	Validity	Validity (6-time boost)	Validity	Validity	Unuse

- LCD output terminals are open (No connection).
- Display on,Display checkered pattern,No access from MPU
- Set V_{LCD}=16V
- Set to $R_1+R_2+R_3=2M\Omega$

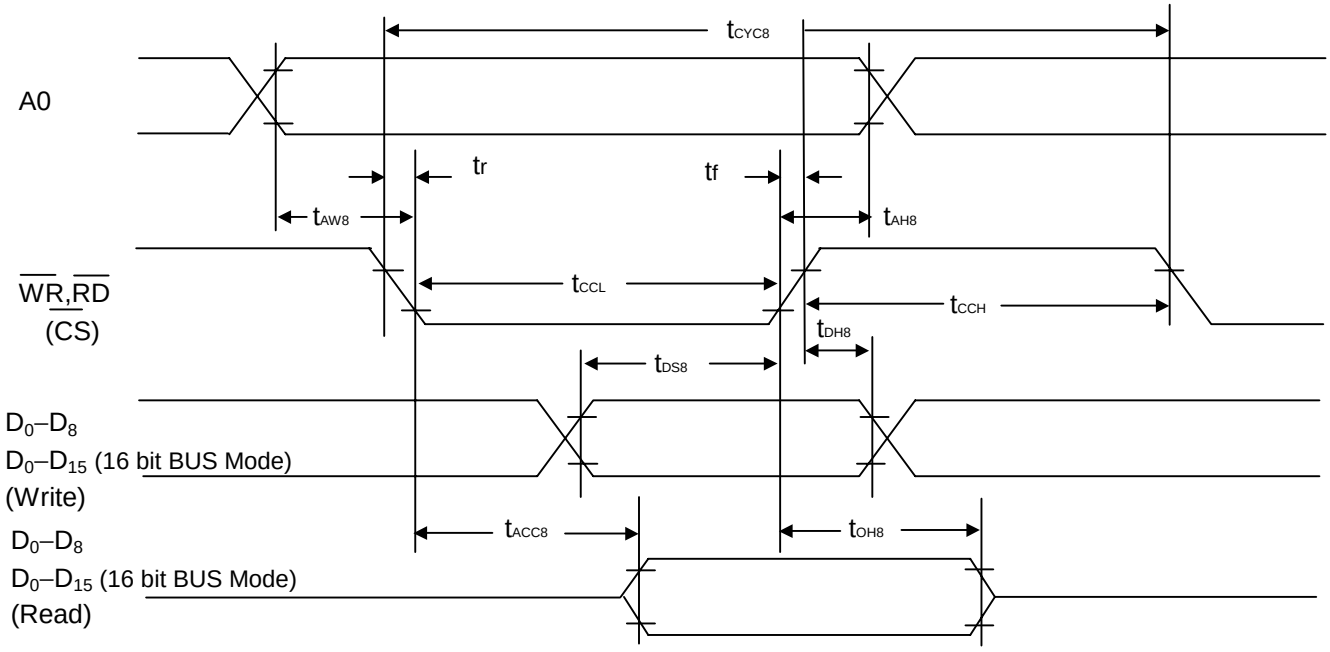
Measurement Block Diagram

:I_{OUT1}



■BUS TIMING CHARACTERISTICS

•Read/Write operation sequence(80 type MPU)

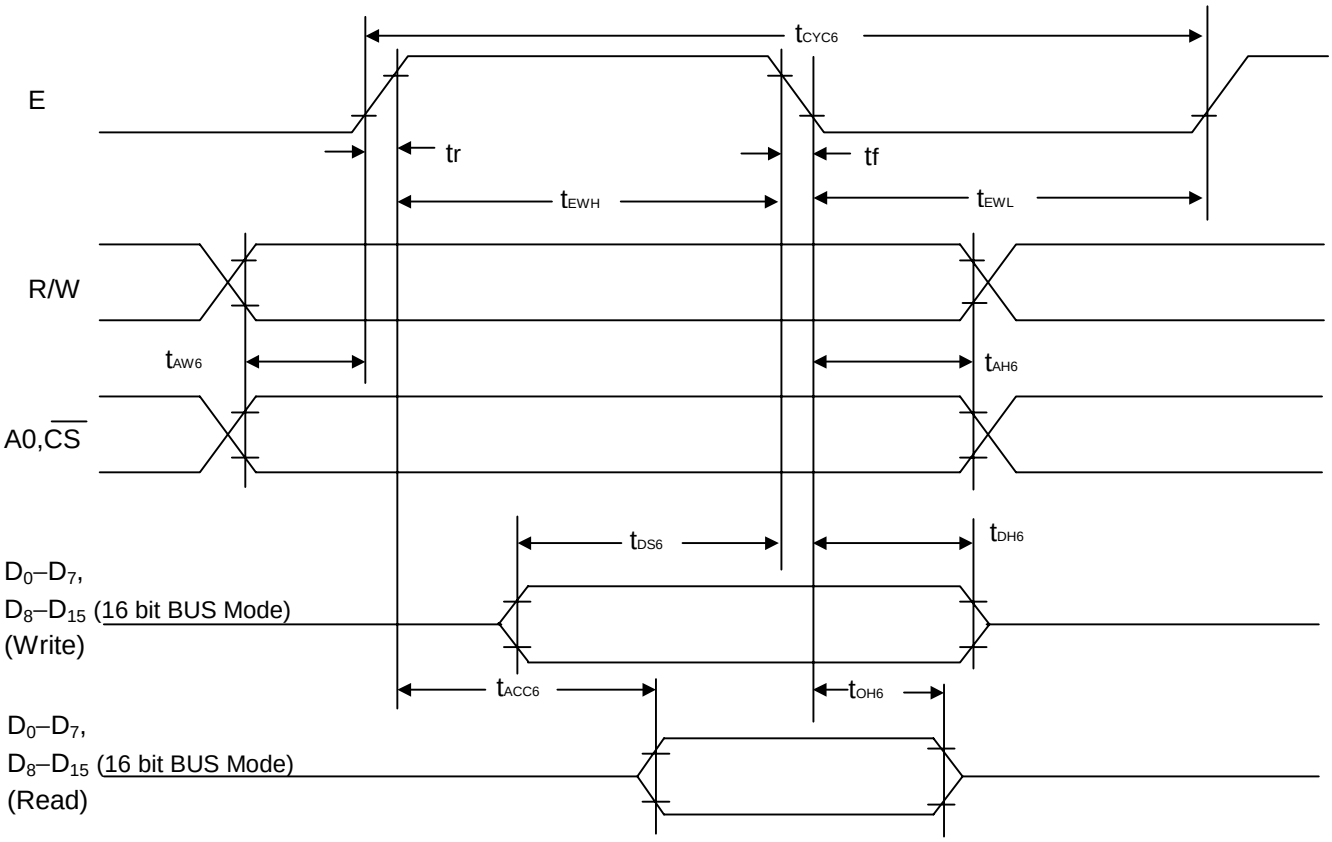


(V_{DD}=2.4V to 3.3V, Ta=-30 to 80°C)

PARAMETER	SIGNAL	SYMBOL	Measurement Condition	MIN	TYP	MAX	UNIT
Address Hold Time	A0,$\overline{CS}$	t_{AH8}		0			ns
Address Set up Time		t_{AW8}		0			
System Cycle Time (WRITE)	$\overline{WR}$	t_{CYC8}(W)		160			
System Cycle Time (READ)	$\overline{RD}$	t_{CYC8}(R)		360			
Control Pulse Width ($\overline{WR}$)		t_{CCL}(W)		50			
Control Pulse Width ($\overline{RD}$)		t_{CCL}(R)		250			
Control “H” Pulse Width	$\overline{WR}$,$\overline{RD}$	t_{CCH}		110			
Data Set Up Time	D_0 to D_7 D_8 to D_{15}	t_{DS8}		30			
Data Hold Time		t_{DH8}		5			
Rdaccess Time		t_{ACC8}	CL=100pF			240	
Output Disable Time		t_{OH8}		0		50	
Rise Time / FallTime	$\overline{CS}$,$\overline{WR}$,$\overline{RD}$	tr, tf				15	

*15 All timing based on 20% and 80% of V_{DD} voltage level.

•System BUS Sequence (Read / Write) (68-type MPU)



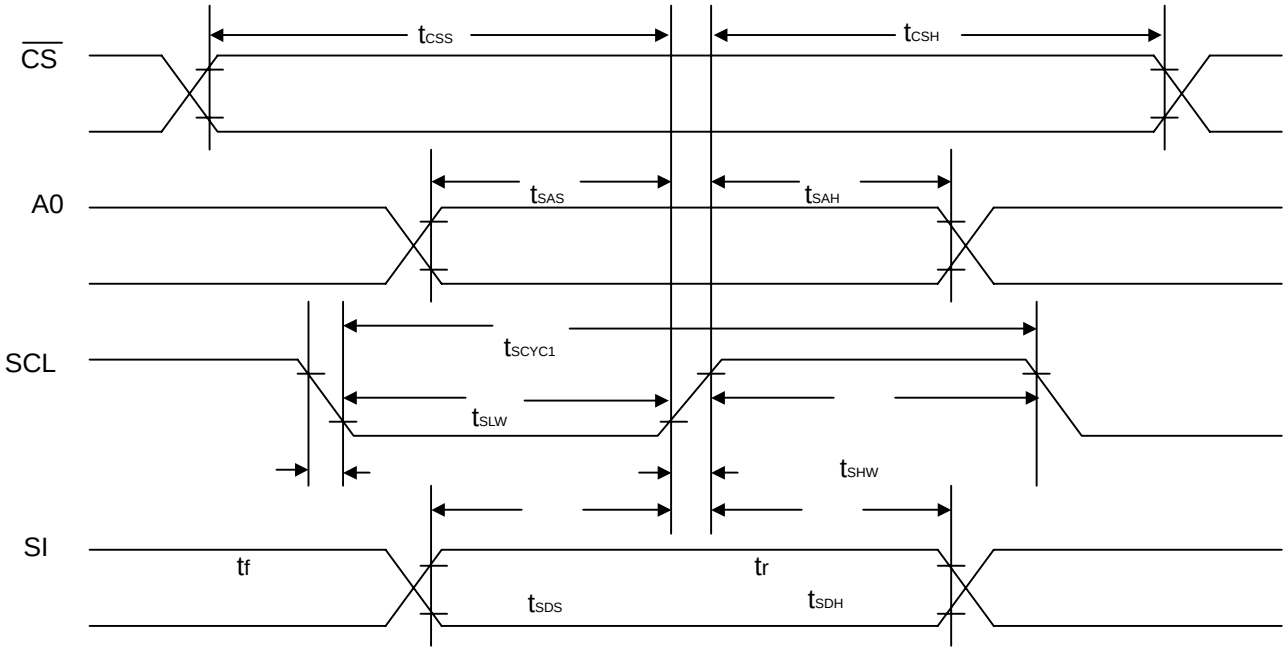
(VDD=2.4V to 3.3V, Ta=-30 to 80°C)

PARAMETER		SIGNAL	SYMBOL	Measurement Condition	MIN	TYP	MAX	UNIT
Address Hold Time		A0,$\overline{CS}$	t_{AH6}		0			ns
Address Set Up time			t_{AW6}		0			
System Cycle Time (WRITE)		R/W	t_{CYC6}(W)		160			
System Cycle Time (READ)			t_{CYC6}(R)		360			
Enable “H” Pulse Width	READ	E	t_{EWH}		250			
	WRITE				50			
Enable “L” PilseWidth (READ/WRITE)			t_{EWL}		110			
Data Set Up Time		D_0 to D_7, D_8 to D_{15}	t_{DS6}		30			
Data Hold Time			t_{DH6}		5			
Access Time			t_{ACC6}	CL=100pF			240	
Output Disable Time			t_{OH6}		0		50	
Rise Time / Fall Time		tr, tf	E				15	

*16 All timing are based on 20% and 80% of V_{DD} voltage level.

*17 t_{CYC6} shows the cycle of the E signal in active $\overline{CS}$.

•Serial Interfave

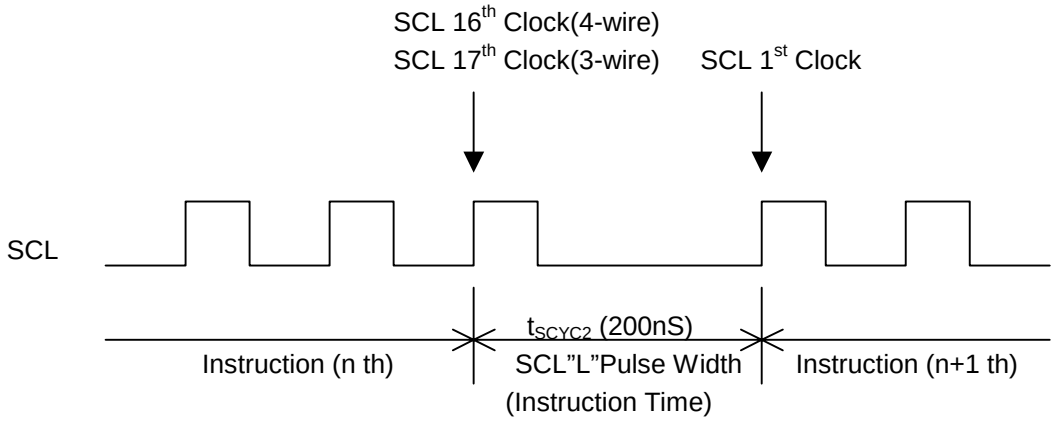


(VDD=2.4V to 3.3V, Ta=-30 to 80°C)

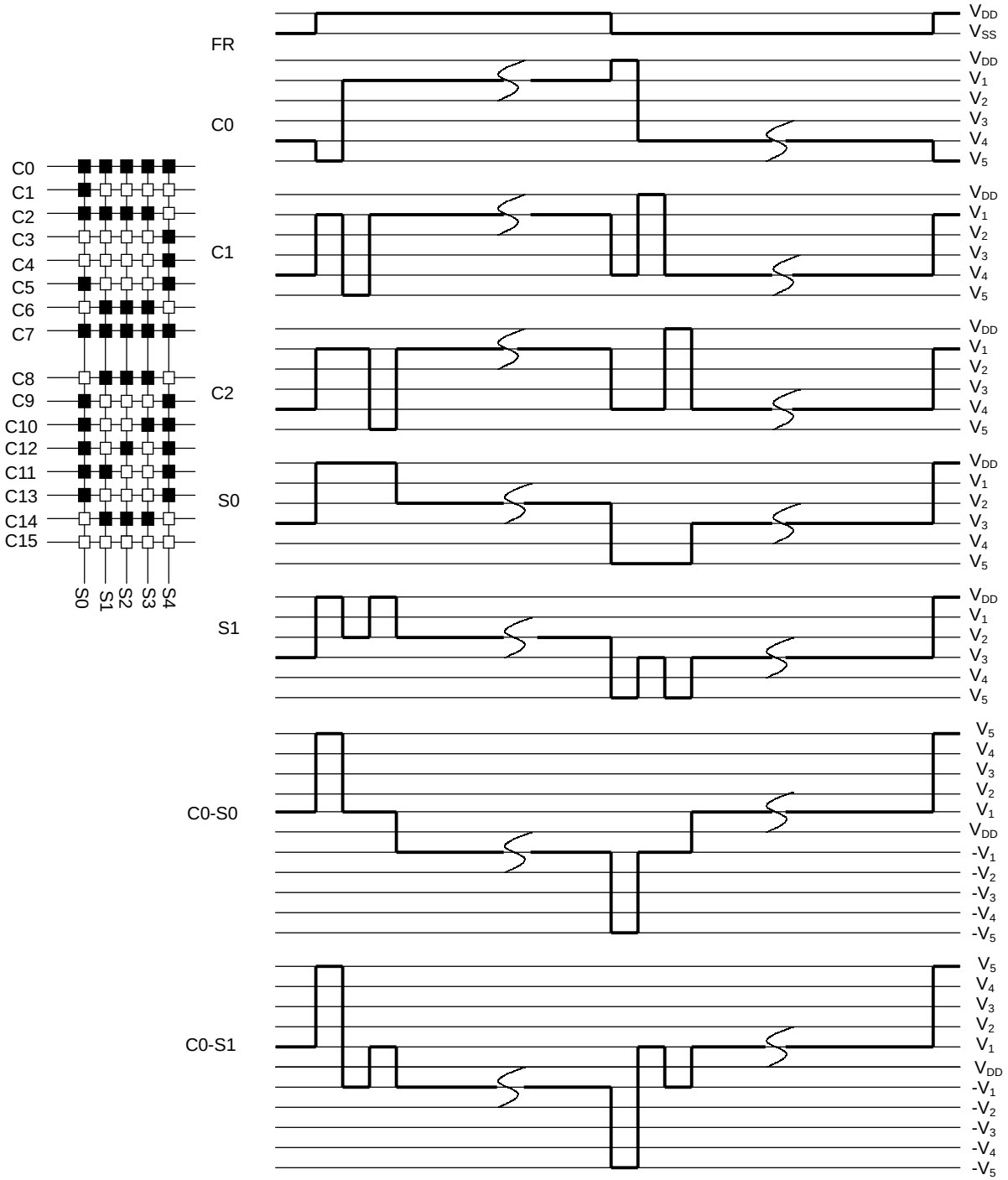
PARAMETER		SIGNAL	SYMBOL	Measurement Condition	MIN	TYP	MAX	UNIT
Serial Clock Cycle	Instruction Input	SCL	t_{SCYC1}		60			ns
	Instruction Time*19)		t_{SCYC2}		200			
SCL"H" Pulse Width			t_{SHW}		30			
SCL"L" Pilse Width			t_{SLW}		30			
Address Set Up Time		A0	t_{SAS}		15			
Address Hold Time			t_{SAH}		15			
Data Set Up Time		SI	t_{SDS}		15			
Data Hold Time			t_{SDH}		15			
$\overline{CS}$-SCLTime		$\overline{CS}$	t_{CSS}		30			
			t_{CSH}		30			
Rise Time / Fall Time		SCL	tf, tr				15	

*18 All timing are based on 20% and 80% of V_{DD} voltage level.

*19 When inputting an instruction continuously, keep 200nS as the cycle of SCL between the instructions as follows



■LCD Driving Wave Form (Black & White Mode)



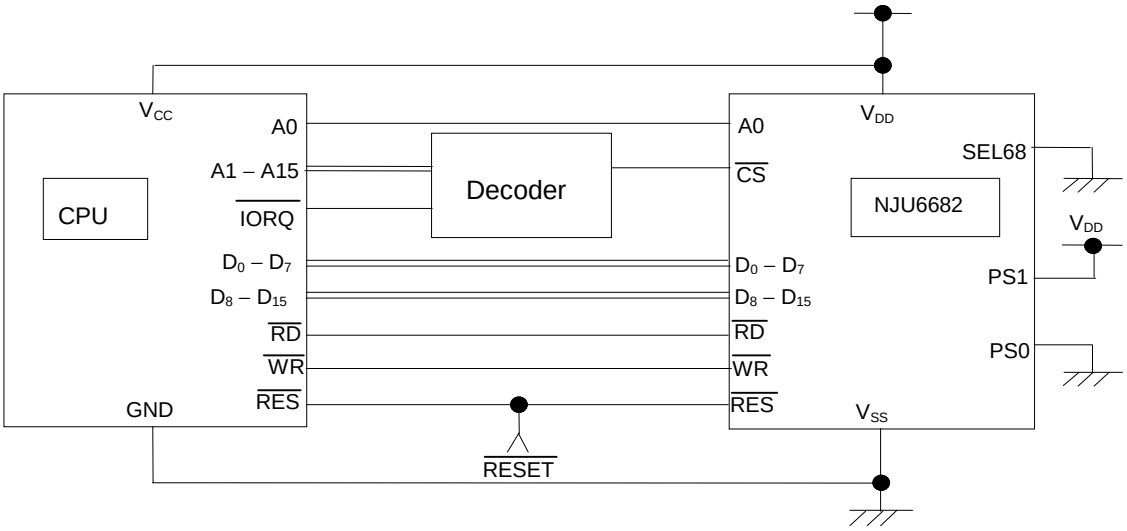
■APPLICATION CIRCUIT

MPU Interface Example

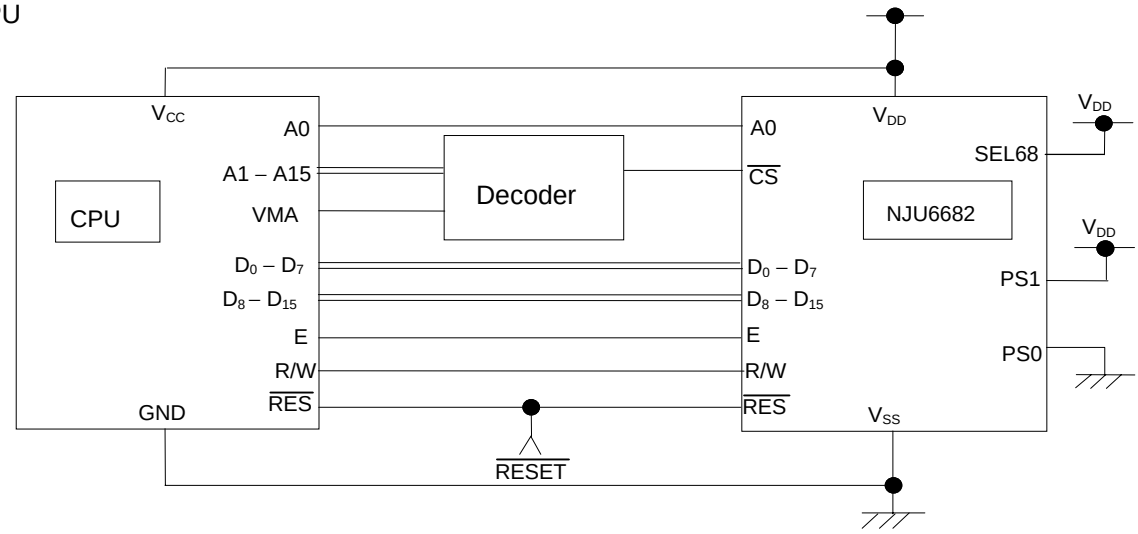
NJU6682 can direct connection with 80 type MPU and 68 type MPU. Moreover, with to use a serial interface, it is possible to control by the signal line with the more small being.

*SEL68 terminal should be connect V_{DD} or V_{SS}

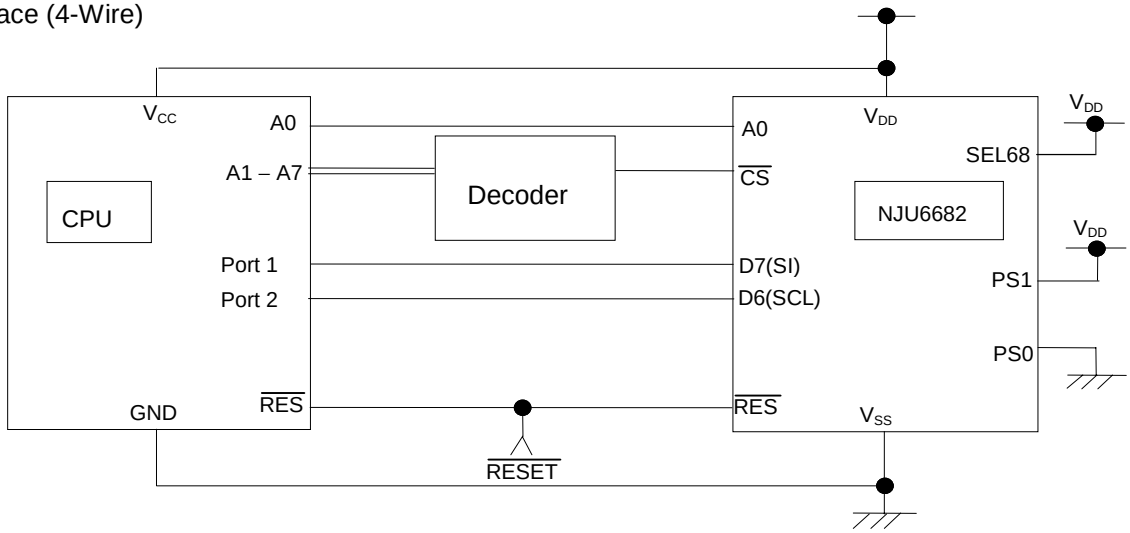
●80 type MPU



●68 type MPU



●Serial Interface (4-Wire)



MEMO