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GS62C101
SYSTEM/DATA CONTROLLER

1. FEATURES

- Clock generation circuit which supports both synchronous and asynchronous operation between CPU local bus and ISA Bus.
- A low power mode which runs the CPU at a reduced clock rate.
- Ideal for reduced power consumption and portable applications.
- DRAM refresh circuit with hidden refresh capability.
- System data bus driver circuit.
- Memory data bus driver circuit.
- X data bus driver circuit.
- Parity generation circuit.
- 8-bits to 16-bits data conversion circuit.
- Sleep mode circuit which reduces system power consumption to the minimum.
- Fast Numerical Coprocessor (80387SX) Interface.
- Built-in 82C59 interrupt controllers (X2).
- Built-in 8254 timer counter.
- B-PORT circuit.
- Speaker circuit.
- Non-maskable interrupt (NMI) register circuit.
- Reset circuit and reset signals distribution.
- Software programmable system configuration registers.
- Low power CMOS VLSI implementation.
- 160 pins QFP package.

2. DESCRIPTION

State Machine

Two state machines (CPU and AT) interface between the CPU and the AT BUS. The CPU state machine is running at the CPU speed to interpret the status: M/IO, D/C and W/R, ADS for 386SX. If FS16 is inactive, CPU state machine will send a trigger to AT BUS state machine, then finish the cycle by READY when the wait state is fully counted.

ISA Bus Implementation

Async/synchronous ISA bus operation is implemented for efficiency and compatibility reasons. The ISA bus runs at the half of the CPU speed or fixed asynchronous speed, depending on the configuration. Two clock modes are built in for reducing power consumptions: the Low Power Mode and the Sleep Mode. In Low Power Mode, the CPU clock are divided down by a factor of 2, 4, 8 or 16. The AT bus, running based on the async or CLK2/2, remains without change. The Sleep Mode is used to stop the clocks when an application is waiting for an external event such as an input from the keyboard or an I/O operation. After the interrupt is serviced, the control is returned to the sleep function to find out if the specified event has occurred. If it has, control is returned to the application; if not, the system falls back to sleep.

The chip set provides quick reset and direct gate A20 function to allow for fast switching between protected and real modes. This function provides a faster OS/2 interface instead of using the keyboard controller for a slower switch between the protected mode and real mode. The memory and bus operation are selected by hardware design options using DIP switches without any BIOS modification. On the other hand, this chip set can be implemented into a motherboard without DIP switches in which case the options are software configured upon power up. Furthermore, the chip set supports a setup ROM to configure the system automatically during power up. With the proper dip switch set, the first CPU address after power up is redirected to the setup ROM. Therefore, the register can be initialized without BIOS modification.

Clock/Reset Generation (Power Down/Sleep)

GS62C101 takes power-on reset and keyboard reset signals, and distributes the reset signals to the ISA-bus, CPU, NP, Keyboard controller and the GS62C102. In addition, GS62C101 manipulates 3 clock inputs to provide all of the needed clock sources for the entire system.

Three clock inputs are described:

- CLK2IN 36-40 MHz: This clock is used to derive the CPU CLOCK and the AT CLOCK during synchronous mode operation.
- X21,X22 14.31818 MHz : The Real Time Clock uses this source. Furthermore, this clock is the source of the OSC pin on the ISA Bus.
- ATCLK 12-20 MHz: This asynchronous clock input is used for the ISA Bus when the ISA Bus is configured to run in the asynchronous mode.

Given the above clock sources, the CPU can be set into two modes of operation: the Fast Mode and the Normal Mode. This CPU speed selection is completely independent of the AT clock speed since they are running asynchronously with each other. These mode are summarized below:

- a. Fast (F/C = 1):
  CPUCLK=CLK2 (36-40Mhz)
  CPU speed: 12-20Mhz
- b. Normal (F/C = 0):
  CPUCLK=CLK2/2 (12-20Mhz).
  CPU speed: 6-10Mhz.

In addition to the above clock generation and configuration circuits, the SYSCLK on the ISA Bus is derived by dividing the AT CLK by 2. Internally, a DMA clock is derived by dividing the SYSCLK by two.

GS62CS03 supports both the low power and portable system designs. Two additional clock modes are provided for low power mode and sleep mode. These two features are ideal for low power lap top designs:

- Low Power Mode: CPUCLK divided down by 2, 4, 8 or 16 selected by configuration register. The CPU and the GS62CS03 is consuming much less power when the CPU clock frequency is reduced. The full ISA Bus compatibility is maintained at all time.
- Sleep mode: The clock oscillation circuit is turned off. Interrupts turn the clock back on without loss of the system data and state.

The configuration needed to set up the above modes of operation are described fully later in this document.

Data Control

GS62C101 controls the data flow among the CPU, the local memory, the ISA bus and the on-board peripherals during the CPU, DMA and MASTER cycles. If 8-bits device is accessed in a 16 bits operation, GS62C101 will automatically split the cycles to do the bus conversion.

NP Interface

A fast Numerical Processor such as 387SX is connected directly to the CPU data bus D15-D0. The address information A9 to A0 from the CPU is internally latched and decoded in the GS62C101. The fast NP command interface runs on the CPU clock. (i.e. CPU match cycle). The GS62CS101 Numerical Processor Interface is faster because the competitors' implementations have the NP on the X bus running on asynchronous bus cycles. GS62C101 can also be programed to run with slower Numerical Processors.

GS62C101 can access the NP using IOR/IOW using zero, 1 or 2 CPU wait state depending on the configuration register setting. The default is 2 wait state. GS62C101 also generates NPCS

signal and monitor the NPBUSY and NPERROR to activate the BUSY and IRQ13 signals respectively. GS62C101 supports the 387SX zero wait state by using READYO from 387SX.

8254 Timer and 8259 Interrupt Controller

One of the 8254 Timer and two of the 8259 Interrupt Controllers are incorporated into the GS62C101.

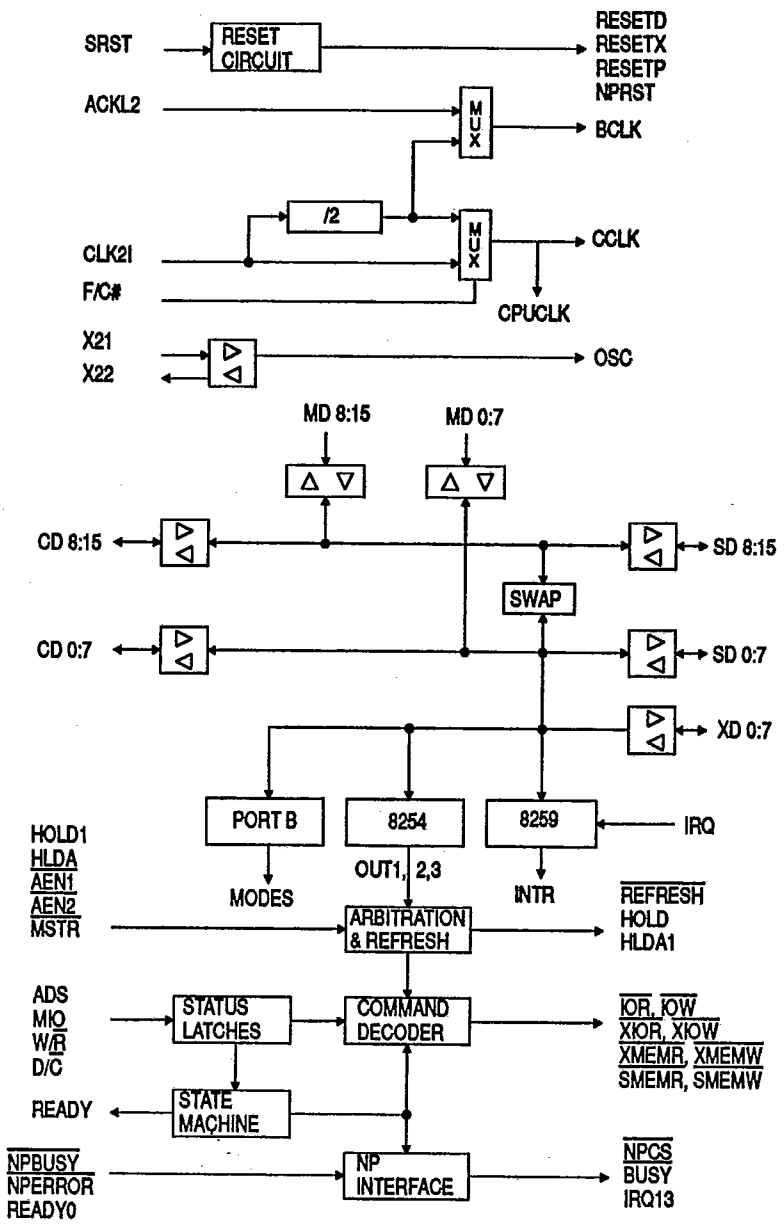
PARITY/NMI

Given the data, GS62C101 generates the parity bits MP1, MP0 in CPU write cycle, and check for even parity in CPU read cycle. When the parity error occurs, or IOCHCK from the AT bus is active, NMI will be asserted. The parity check circuit can be disabled by programming the configuration register.

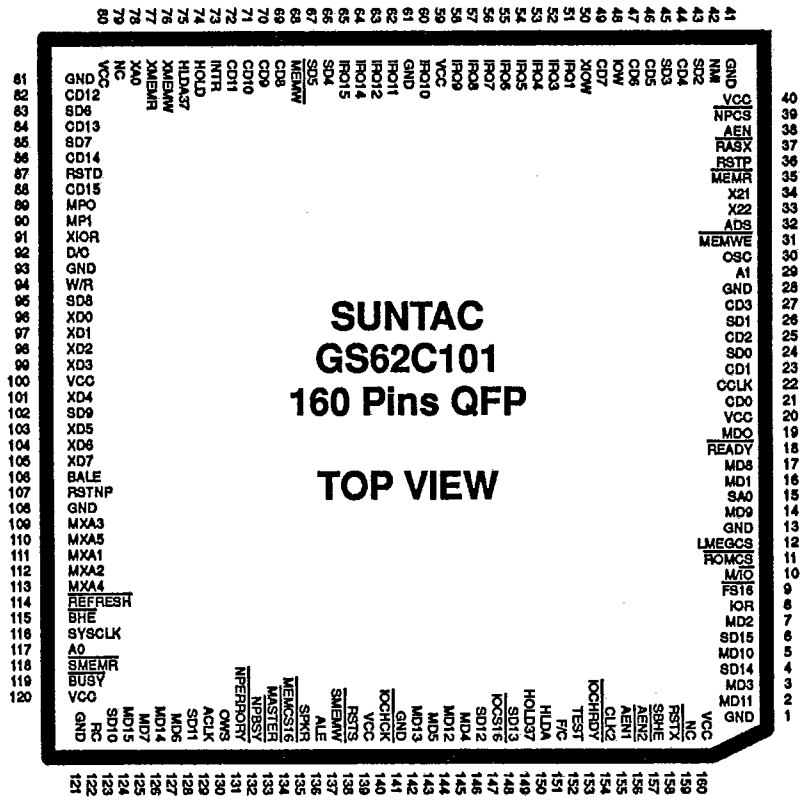
PORT B

The Port B register circuit is located in the GS62C101. It can be read or written to with an I/O command to address 61H. Port B is used to control the speaker and mask out NMI sources. It can be read to find status of $\overline{\text{REFRESH}}$, speaker data and possible sources of NMI.

GS62C101 FUNCTIONAL BLOCK DIAGRAM



GS62C101 PIN DIAGRAM



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PIN DESCRIPTION

Pin Name	Pin No.	Type	Description
CPU Interface			
M/$\overline{IO}$	10	I	Memory/IO status from the CPU.
D/C, W/R	92, 94	I	D/C and W/R status from the CPU. When both D/C and W/R goes low, the TS cycle begins.
CD0:15	21, 23, 25, 27, 44, 46-47, 49, 69, 70, 71, 72, 82, 84, 86, 88	I/O	CPU local data bus. Connect to the data pins of the CPU.
A1	29	I	CPU address bus pin A1.
A0	117	I/O	CPU address bus pin A0.
$\overline{BHE}$	115	I/O	CPU byte-high-enable pin, CD8-CD15 to be valid. This pin is the logic complement of the A0 pin.
CCLK	22	O	Clock to CPU and GS62C102 (CPUCLOCK). This clock will be 40MHz and 32MHz for a 20MHz and 16MHz system, respectively. It can also run at a slower speed when the low power mode is active.
HOLD	74	O	Connects to CPU's Hold request pin.
HLDA	150	I	Connects to CPU's "HLDA" pin.

Pin Name	Pin No.	Type	Description
$\overline{BUSY}$	119	O	BUSY signal to CPU. Indicates a local bus master (e.g. Numerical Processor) is still busy.
$\overline{READY}$	18	I/O	Bus ready to terminate current bus cycle. connects to the "READY" pin of CPU. This output is open drain with a 5K pull up Resister. During the local memory cycle, READY pin is used to detect the end of local memory cycle.
RSTP	36	O	Active High output signal requesting CPU reset. Connects to CPU's "Reset" pin.
INTR	73	O	Interrupt request to CPU. Connects to INTR pin of the CPU.
NMI	42	O	Non-maskable interrupt request to CPU connects to the NMI pin of the CPU.
ADS	32	I	Address Status from CPU indicating valid address. This pin acts as part of the protocol between the CPU and the AT.
GS62C102 Interface			
$\overline{RASX}$	37	O	The memory cycle status for the iAPX 386SX. Active low indicates a memory cycle.
$\overline{FS16}$	9	I	GS62C102 indicates the local memory read/write cycle. High signal indicates either I/O or AT bus access.
ALE	136	O	Address-latch-enable. This signal indicates a valid SA signal because this signal is used to latch CPU address on the system.
HOLD37	149	I	Hold request generated by the DMA controller inside GS62C102.

Pin Name	Pin No.	Type	Description
HLDA37	75	O	Hold acknowledge to the DMA controller inside GS62C102.
$\overline{\text{ROMCS}}$	11	I	ROM chip select. Indicating a ROM access to GS62C101. This pin also connects directly to the ROM chips.
LMEGCS	12	I	Low mega operation to enable SMEMR/SMEMW. Active only for access addresses below 1M Byte.
XMEMR	77	I/O	Memory read command. This pin is connected only to the GS62C102. This command indicates a memory read request from the GS62C101. During the DMA read cycle, this pin is in input mode.
XMEMW	76	I/O	Memory write command. This pin is connected only to the GS62C102. This command indicates a memory write request from the GS62C101. During the DMA write cycle, this pin is in input mode.
$\overline{\text{AEN1,2}}$	155, 156	I	AEN1 and AEN2 from the two DMA controllers. These two pins are only connected to the GS62C102 to indicate 8-bits high byte, 8-bits low byte or 16-bits DMA transfers.
MXA1:5	109-113	I/O	Address input for internal registers Refer to configuration register table. These pins are also connected to the X bus. During I/O cycle, these pins contains the GCH proprietary code for accessing on-board devices. During memory cycle, these address pins are connected to the ROM chips.
MEMORY Interface			
MD0:15	2-3, 5, 7, 14, 16-17, 19, 124-127, 142-145	I/O	Memory data bus is connected only to the local system memory. Local system memory contains both RAMs and ROMs.

Pin Name	Pin No.	Type	Description
MP0 MP1	89, 90	I/O	Memory data parity bit. This pin is connected both to the memory and to the AT Bus.
$\overline{\text{MEMWE}}$	31	O	Memory-write-enable. Active when the CPU command status is decoded as a local memory write.
ISA BUS Interface			
SD0:15	4, 6, 24, 26, 43, 45, 66-67, 83, 85, 95, 102, 123, 128, 146, 148	I/O	System data bus are gated on the system bus when 'BALE' is high and are latched on the falling edge of 'BALE'. These signals are generated by the CPU, DMA and other bus masters.
SA0	15	I/O	System address A0 to the ISA bus.
SBHE	157	I/O	System byte-high-enable. When this signal is active, the SD8:15 pins are valid.
BALE	106	O	Bus address-latch-enable. Indicating data on AT address bus is valid.
SYSCLK	116	O	System clock output. Synchronous with the CPU clock.
OSC	30	O	OSC clock to system bus is a high speed clock (14.31818 MHz), not synchronous with system clock.
$\overline{\text{IOR}}$	8	I/O	IO read command to the AT Bus. The other source of this command is bus master.
$\overline{\text{IOW}}$	48	I/O	IO write command to the AT Bus. The other source of this command is bus master.

Pin Name	Pin No.	Type	Description
$\overline{\text{MEMR}}$	35	I/O	Memory read command to the AT Bus. The other source of this command is bus master.
$\overline{\text{MEMW}}$	68	I/O	Memory write command to the AT Bus. The other source of this command is bus master.
$\overline{\text{SMEMR}}$	118	O	Lower one mega memory read command. Indicating a read command to the lower one megabyte of the physical memory.
$\overline{\text{SMEMW}}$	137	O	Lower one mega memory write command. Indicating a write command to the lower one megabyte of the physical memory.
$\overline{\text{MEMCS16}}$	134	I	16 bits wide 1 wait state Memory bus access. This signal is generated by decoding the LA17:23.
$\overline{\text{IOCS16}}$	147	I	Indicate the present data transfer is 16 bits wide 1 wait state I/O access.
OWS	130	I	Indicates a CPU zero wait state access.
$\overline{\text{IOCHRDY}}$	153	I	I/O channel ready input. Pull low to indicates a slow I/O device.
$\overline{\text{REFRESH}}$	114	I/O	I/O pin indicating a Refresh command. The other source of this pin is other bus masters.
$\overline{\text{MASTER}}$	133	I	Master cycle. Allows for other bus master to gain control of the bus.
AEN	38	O	High when HLDA and MASTER high. Indicates AT DMA controller has the control of the bus and a DMA cycle is active.
$\overline{\text{IOCHCK}}$	140	I	IO channel check for IO slot parity. Indicate unrecoverable system error.

Pin Name	Pin No.	Type	Description
RSTD	87	O	RESET output to the system bus. Reset and initialize on power up.
IRQ3:7	52-56	I	Interrupt request inputs from AT Bus.
IRQ9:12	58, 60 62-63	I	Interrupt request inputs from AT Bus
IRQ14,15	64-65	I	Interrupt request inputs from AT Bus.
Fast NP Interface			
$\overline{\text{NPCS}}$	39	O	NP chip select. Active low means the NP is enabled.
$\overline{\text{NPBUSY}}$	132	O	The "Busy" pin at the CPU interface will be active when the $\overline{\text{NPBUSY}}$ is active.
$\overline{\text{NPERROR}}$	131	I	NP error signal from the 387SX.
RSTNP	107	O	The NP is reset when this pin is active.
SYSTEM Interface			
XA0	78	I/O	X address bus. Contains the buffered version of the A0. During DMA cycle this pins outputs the A0.
XD0:7	96-99, 101, 103-105	I/O	X data bus. This bus is connected to the Real Time Clock(146818), the keyboard controller(8042) and GS62C102.
XIOR	91	I/O	X bus read command for on board I/O devices.
XIOW	50	I/O	X bus write command for on board I/O devices.

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Pin Name	Pin No.	Type	Description
F/$\overline{C}$	151	I	Fast/compatible speed selection.
CLK2	154	I	Clock input. Oscillator for CPU clock.
ACLK	129	I	Asynchronous clock input for AT BUS.
X21	34	I	Crystal input 14.318 Mhz.
X22	33	O	Crystal output 14.318 Mhz.
IRQ1	51	I	Interrupt request input from keyboard. (8742).
IRQ8	57	I	Interrupt request input from real time clock. This pin is connected to the $\overline{IRQ}$ pin of the 146818.
RSTS	138	I	System power on reset. This signal originates from the on board power on circuit.
$\overline{RSTX}$	158	O	Reset output to GS62C102 and KYBRD (8742) controller.
RC	122	I	Reset input from KYBRD (8742) controller.
SPKR	135	O	Output to speaker.
TEST	152	I	Put the GS62C101 into the test mode. Always pull high.

Configuration Description

Index Register #O	
This register contains the I/O address of the index address register and the index data register. The default I/O address for index register is 98H; the default index data register is 99H. The table below shows the index registers.	
Index Register #30	
bit 0	Reserved. Always pull low.
bit 1	0=8-bits ROM 1=16-bits ROM
bit 2	AT Bus clock select: 0=ATCLK 1=CLK2/2
bit 3	Rom Accesses Wait State: 0=3WS 1=1WS
bit 4	0=Page Interleave Mode 1=Gold Mode
bit 5	0=Fast Page Mode 1=Normal Page Mode
bit 6	Gold Mode Wait State: 0=0WS 1=1WS
bit 7	Enable Setup ROM: 0=disabled(use FFFFF0), 1=enabled(remap to setup ROM)
Index Register #20	
bit 0,1	Clock division for Low Power Mode 00= divided by 2 01= divided by 4 10= divided by 8 11= divided by 16
bit 2,3	Clock Selection 00= normal high speed mode 01= low power mode (slow clock) 1-= sleep mode (stop clock)
Index Register #2F	
bit 0	ENPALE (extended ALE for -MEMCS16 decoding time): 0=disable, 1=enable
bit 1	0=IBM Refresh Mode, 1=Hidden Refresh Mode
bit 2-7	Reserved. Always set to zero.

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ISA BUS Reference Timing