SSTU32866

1.8 V 25-bit 1:1 or 14-bit 1:2 configurable registered buffer with parity for DDR2 RDIMM applications

Rev. 01 — 09 July 2004 Objective data

1. Description

The SSTU32866 is a 1.8 V configurable register specifically designed for use on DDR2 memory modules requiring a parity checking function. It is defined in accordance with the JEDEC JESD82-7 standard for the SSTU32864 registered buffer, while adding the parity checking function in a compatible pinout. The JEDEC standard for SSTU32866 is pending publication. The register is configurable (using configuration pins C0 and C1) to two topologies: 25-bit 1:1 or 14-bit 1:2, and in the latter configuration can be designated as Register A or Register B on the DIMM.

The SSTU32866 accepts a parity bit from the memory controller on its parity bit (PAR_IN) input, compares it with the data received on the DIMM-independent D-inputs and indicates whether a parity error has occurred on its open-drain $\overline{\text{QERR}}$ pin (active-LOW). The convention is even parity, i.e., valid parity is defined as an even number of ones across the DIMM-independent data inputs combined with the parity input bit.

The SSTU32866 is packaged in a 96-ball, 6 × 16 grid, 0.8 mm ball pitch LFBGA package (13.5 mm by 5.5 mm).

2. Features

- Configurable register supporting DDR2 Registered DIMM applications
- Configurable to 25-bit 1:1 mode or 14-bit 1:2 mode
- Controlled output impedance drivers enable optimal signal integrity and speed
- Exceeds JESD82-7 speed performance (1.8 ns max. single-bit switching propagation delay; 2.0 ns max. mass-switching)
- Supports up to 450 MHz clock frequency of operation
- Optimized pinout for high-density DDR2 module design
- Chip-selects minimize power consumption by gating data outputs from changing state
- Supports SSTL_18 data inputs
- Checks parity on the DIMM-independent data inputs
- Partial parity output and input allows cascading of two SSTU32866s for correct parity error processing
- Differential clock (CK and $\overline{\text{CK}}$) inputs
- Supports LVCMOS switching levels on the control and $\overline{\text{RESET}}$ inputs
- Single 1.8 V supply operation
- Available in 96-ball, 13.5 × 5.5 mm, 0.8 mm ball pitch LFBGA package

3. Applications

- DDR2 registered DIMMs desiring parity checking functionality

4. Ordering information

Table 1: Ordering information

T_{amb} = 0 °C to +70 °C.

Type number	Package			
	Name	Description	Solder process	Version
SSTU32866EC/G	LFBGA96	plastic low profile fine-pitch ball grid array package; 96 balls; body 13.5 × 5.5 × 1.05 mm	Pb-free (SnAgCu solder ball compound)	SOT536-1
SSTU32866EC	LFBGA96	plastic low profile fine-pitch ball grid array package; 96 balls; body 13.5 × 5.5 × 1.05 mm	SnPb solder ball compound	SOT536-1

5. Pinning information

Table 2: Ball mapping, 1:1 register (C0 = 0, C1 = 0)

96-ball, 6 × 16 grid; top view. DNU denotes 'Do Not Use'. NC denotes a no-connect (ball present but not connected to the die).

	1	2	3	4	5	6
A	DCKE	PPO	V_{REF}	V_{DD}	QCKE	DNU
B	D2	D15	GND	GND	Q2	Q15
C	D3	D16	V_{DD}	V_{DD}	Q3	Q16
D	DODT	$\overline{QERR}$	GND	GND	QODT	DNU
E	D5	D17	V_{DD}	V_{DD}	Q5	Q17
F	D6	D18	GND	GND	Q6	Q18
G	PAR_IN	$\overline{RESET}$	V_{DD}	V_{DD}	C1	C0
H	CK	$\overline{DCS}$	GND	GND	$\overline{QCS}$	DNU
J	$\overline{CK}$	$\overline{CSR}$	V_{DD}	V_{DD}	NC	NC
K	D8	D19	GND	GND	Q8	Q19
L	D9	D20	V_{DD}	V_{DD}	Q9	Q20
M	D10	D21	GND	GND	Q10	Q21
N	D11	D22	V_{DD}	V_{DD}	Q11	Q22
P	D12	D23	GND	GND	Q12	Q23
R	D13	D24	V_{DD}	V_{DD}	Q13	Q24
T	D14	D25	V_{REF}	V_{DD}	Q14	Q25

Table 3: Ball mapping, 1:2 Register A (C0 = 0, C1 = 1)

96-ball, 6 × 16 grid; top view. DNU denotes 'Do Not Use'. NC denotes a no-connect (ball present but not connected to the die).

	1	2	3	4	5	6
A	DCKE	PPO	V_{REF}	V_{DD}	QCKEA	QCKEB
B	D2	DNU	GND	GND	Q2A	Q2B
C	D3	DNU	V_{DD}	V_{DD}	Q3A	Q3B
D	DODT	$\overline{QERR}$	GND	GND	QODTA	QODTB
E	D5	NC	V_{DD}	V_{DD}	Q5A	Q5B
F	D6	NC	GND	GND	Q6A	Q6B
G	PAR_IN	$\overline{RESET}$	V_{DD}	V_{DD}	C1	C0
H	CK	$\overline{DCS}$	GND	GND	$\overline{QCSA}$	$\overline{QCSB}$
J	$\overline{CK}$	$\overline{CSR}$	V_{DD}	V_{DD}	NC	NC
K	D8	DNU	GND	GND	Q8A	Q8B
L	D9	DNU	V_{DD}	V_{DD}	Q9A	Q9B
M	D10	DNU	GND	GND	Q10A	Q10B
N	D11	DNU	V_{DD}	V_{DD}	Q11A	Q11B
P	D12	DNU	GND	GND	Q12A	Q12B
R	D13	DNU	V_{DD}	V_{DD}	Q13A	Q13B
T	D14	DNU	V_{REF}	V_{DD}	Q14A	Q14B

Table 4: Ball mapping, 1:2 Register B (C0 = 1, C1 = 1)

96-ball, 6 × 16 grid; top view. DNU denotes 'Do Not Use'. NC denotes a no-connect (ball present but not connected to the die).

	1	2	3	4	5	6
A	D1	PPO	V_{REF}	V_{DD}	Q1A	Q1B
B	D2	DNU	GND	GND	Q2A	Q2B
C	D3	DNU	V_{DD}	V_{DD}	Q3A	Q3B
D	D4	$\overline{QERR}$	GND	GND	Q4A	Q4B
E	D5	DNU	V_{DD}	V_{DD}	Q5A	Q5B
F	D6	DNU	GND	GND	Q6A	Q6B
G	PAR_IN	$\overline{RESET}$	V_{DD}	V_{DD}	C1	C0
H	CK	$\overline{DCS}$	GND	GND	$\overline{QCSA}$	$\overline{QCSB}$
J	$\overline{CK}$	$\overline{CSR}$	V_{DD}	V_{DD}	NC	NC
K	D8	DNU	GND	GND	Q8A	Q8B
L	D9	DNU	V_{DD}	V_{DD}	Q9A	Q9B
M	D10	DNU	GND	GND	Q10A	Q10B
N	DODT	DNU	V_{DD}	V_{DD}	QODTA	QODTB
P	D12	DNU	GND	GND	Q12A	Q12B
R	D13	DNU	V_{DD}	V_{DD}	Q13A	Q13B
T	DCKE	DNU	V_{REF}	V_{DD}	QCKEA	QCKEB

5.1 Pin description

Table 5: Pin description

Signal name	Type	Description
GND	Ground input	Ground.
V_{DD}	1.8 V nominal	Power supply voltage.
V_{REF}	0.9 V nominal	Input reference voltage.
CK	Differential input	Positive master clock input.
$\overline{\text{CK}}$	Differential input	Negative master clock input.
C0, C1	LVCMOS inputs	Configuration control inputs; Register A or Register B and 1:1 mode or 1:2 mode select.
$\overline{\text{RESET}}$	LVCMOS input	Asynchronous reset input. Resets registers and disables V_{REF} data and clock.
$\overline{\text{CSR}}$, $\overline{\text{DCS}}$	SSTL_18 input	Chip select inputs. Disables D1 to D25[1] outputs switching when both inputs are HIGH.
D1 to D25	SSTL_18 input	Data input. Clocked in on the crossing of the rising edge od CK and the falling edge of $\overline{\text{CK}}$.
DODT	SSTL_18 input	The outputs of this register bit will not be suspended by the $\overline{\text{DCS}}$ and $\overline{\text{CSR}}$ control.
DCKE	SSTL_18 input	The outputs of this register bit will not be suspended by the $\overline{\text{DCS}}$ and $\overline{\text{CSR}}$ control.
PAR_IN	SSTL_18 input	Parity input. Arrives one clock cycle after the corresponding data input.
Q1 to Q25[2]	1.8 V CMOS outputs	Data outputs that are suspended by the $\overline{\text{DCS}}$ and $\overline{\text{CSR}}$ control.
PPO	1.8 V CMOS output	Partial parity out. Indicates odd parity of inputs D1 to D25[1].
$\overline{\text{QCS}}$	1.8 V CMOS output	Data output that will not be suspended by the $\overline{\text{DCS}}$ and $\overline{\text{CSR}}$ control.
QODT	1.8 V CMOS output	Data output that will not be suspended by the $\overline{\text{DCS}}$ and $\overline{\text{CSR}}$ control.
QCKE	1.8 V CMOS output	Data output that will not be suspended by the $\overline{\text{DCS}}$ and $\overline{\text{CSR}}$ control.
$\overline{\text{QERR}}$	Open-drain output	Output error bit. Generated one clock cycle after the corresponding data output
NC		No internal connection.
DNU		Do not use. Inputs are in standby-equivalent mode and outputs are driven LOW.

[1] Data inputs = D2, D3, D5, D6, D8 to D25 when C0 = 0 and C1 = 0.
Data inputs = D2, D3, D5, D6, D8 to D14 when C0 = 0 and C1 = 1.
Data inputs = D1 to D6, D8 to D10, D12, D13 when C0 = 1 and C1 = 1.

[2] Data outputs = Q2, Q3, Q5, Q6, Q8 to Q25 when C0 = 0 and C1 = 0.
Data outputs = Q2, Q3, Q5, Q6, Q8 to Q14 when C0 = 0 and C1 = 1.
Data outputs = Q1 to Q6, Q8 to Q10, Q12, Q13 when C0 = 1 and C1 = 1.

6. Functional description

The SSTU32866 is a 25-bit 1:1 or 14-bit 1:2 configurable registered buffer with parity, designed for 1.7 V to 1.9 V V_{DD} operation.

All clock and data inputs are compatible with the JEDEC standard for SSTL_18. The control and reset ($\overline{\text{RESET}}$) inputs are LVCMOS. All data outputs are 1.8 V CMOS drivers that have been optimized to drive the DDR2 DIMM load, and meet SSTL_18 specifications. The error ($\overline{\text{QERR}}$) output is 1.8 V open-drain driver.

The SSTU32866 operates from a differential clock (CK and $\overline{\text{CK}}$). Data are registered at the crossing of CK going HIGH, and CK going LOW.

The C0 input controls the pinout configuration for the 1:2 pinout from A configuration (when LOW) to B configuration (when HIGH). The C1 input controls the pinout configuration from 25-bit 1:1 (when LOW) to 14-bit 1:2 (when HIGH).

The SSTU32866 accepts a parity bit from the memory controller on its parity bit (PAR_IN) input, compares it with the data received on the DIMM-independent D-inputs and indicates whether a parity error has occurred on its open-drain $\overline{\text{QERR}}$ pin (active-LOW). The convention is even parity, i.e., valid parity is defined as an even number of ones across the DIMM-independent data inputs combined with the parity input bit.

When used as a single device, the C0 and C1 inputs are tied LOW. In this configuration, parity is checked on the PAR_IN input which arrives one cycle after the input data to which it applies. The partial-parity-out (PPO) and $\overline{\text{QERR}}$ signals are produced three cycles after the corresponding data inputs.

When used in pairs, the C0 input of the first register is tied LOW and the C0 input of the second register is tied HIGH. The C1 input of both registers are tied HIGH. Parity, which arrives one cycle after the data input to which it applies, is checked on the PAR_IN input of the first device. The PPO and $\overline{\text{QERR}}$ signals are produced on the second device three clock cycles after the corresponding data inputs. The PPO output of the first register is cascaded to the PAR_IN of the second register. The $\overline{\text{QERR}}$ output of the first register is left floating and the valid error information is latched on the $\overline{\text{QERR}}$ output of the second register.

If an error occurs and the $\overline{\text{QERR}}$ output is driven LOW, it stays latched LOW for two clock cycles or until $\overline{\text{RESET}}$ is driven LOW. The DIMM-dependent signals (DCKE, $\overline{\text{DCS}}$, DODT, and $\overline{\text{CSR}}$) are not included in the parity check computation.

The device supports low-power standby operation. When $\overline{\text{RESET}}$ is LOW, the differential input receivers are disabled, and undriven (floating) data, clock and reference voltage (V_{REF}) inputs are allowed. In addition, when $\overline{\text{RESET}}$ is LOW all registers are reset, and all outputs are forced LOW. The LVCMOS $\overline{\text{RESET}}$ input must always be held at a valid logic HIGH or LOW level.

The device also supports low-power active operation by monitoring both system chip select ($\overline{\text{DCS}}$ and $\overline{\text{CSR}}$) inputs and will gate the Qn and PPO outputs from changing states when both $\overline{\text{DCS}}$ and $\overline{\text{CSR}}$ inputs are HIGH. If either $\overline{\text{DCS}}$ or $\overline{\text{CSR}}$ input is LOW, the Qn and PPO outputs will function normally. The $\overline{\text{RESET}}$ input has priority over the $\overline{\text{DCS}}$ and $\overline{\text{CSR}}$ control and when driven LOW will force the Qn and PPO outputs LOW, and the $\overline{\text{QERR}}$ output HIGH. If the $\overline{\text{DCS}}$ control functionality is not desired, then the

$\overline{\text{CSR}}$ input can be hard-wired to ground, in which case, the set-up time requirement for $\overline{\text{DCS}}$ would be the same as for the other D data inputs. To control the low-power mode with $\overline{\text{DCS}}$ only, then the $\overline{\text{CSR}}$ input should be pulled up to V_{DD} through a pull-up resistor.

To ensure defined outputs from the register before a stable clock has been supplied, $\overline{\text{RESET}}$ must be held in the LOW state during power-up.

In the DDR2 RDIMM application, $\overline{\text{RESET}}$ is specified to be completely asynchronous with respect to CK and $\overline{\text{CK}}$. Therefore, no timing relationship can be guaranteed between the two. When entering reset, the register will be cleared and the Qn outputs will be driven LOW quickly, relative to the time to disable the differential input receivers. However, when coming out of reset, the register will become active quickly, relative to the time to enable the differential input receivers. As long as the data inputs are LOW, and the clock is stable during the time from the LOW-to-HIGH transition of $\overline{\text{RESET}}$ until the input receivers are fully enabled, the design of the SSTU32866 must ensure that the outputs will remain LOW, thus ensuring no glitches on the output.

6.1 Function table

Table 6: Function table (each flip-flop)

Inputs						Outputs		
$\overline{RESET}$	$\overline{DCS}$	$\overline{CSR}$	CK	$\overline{CK}$	Dn, DODTn, DCKEn	Qn	$\overline{QCS}$	QODT, QCKE
H	L	L	↑	↓	L	L	L	L
H	L	L	↑	↓	H	H	L	H
H	L	L	L or H	L or H	X	Qo	Qo	Qo
H	L	H	↑	↓	L	L	L	L
H	L	H	↑	↓	H	H	L	H
H	L	H	L or H	L or H	X	Qo	Qo	Qo
H	H	L	↑	↓	L	L	H	L
H	H	L	↑	↓	H	H	H	H
H	H	L	L or H	L or H	X	Qo	Qo	Qo
H	H	H	↑	↓	L	Qo	H	L
H	H	H	↑	↓	H	Qo	H	H
H	H	H	L or H	L or H	X	Qo	Qo	Qo
L	X or floating	X or floating	X or floating	X or floating	X or floating	L	L	L

Table 7: Parity and standby function table

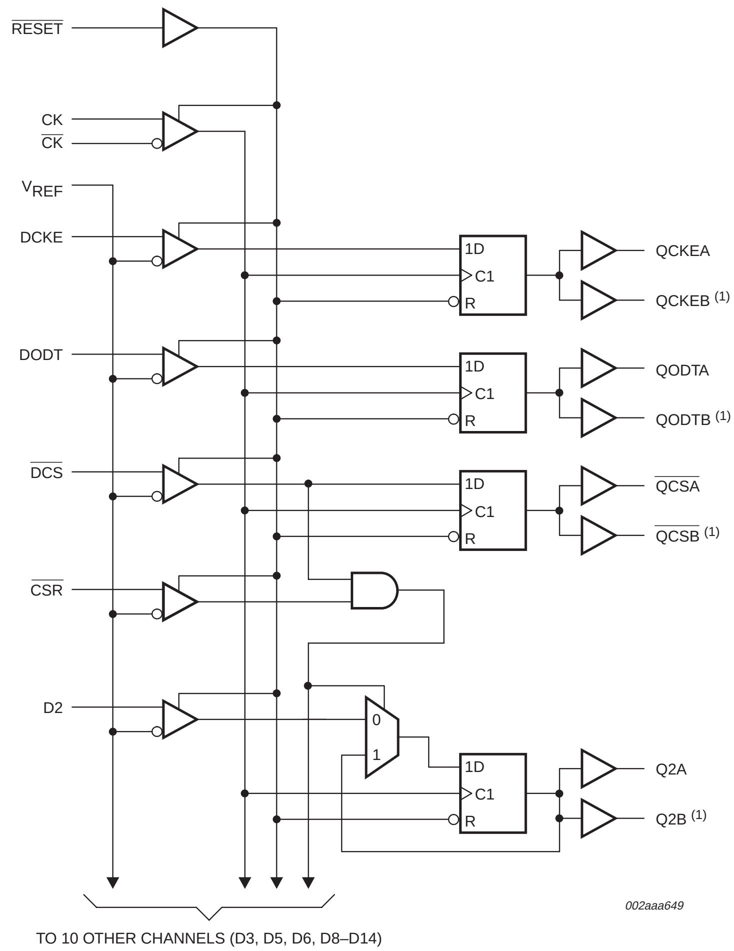
Inputs							Outputs	
$\overline{RESET}$	$\overline{DCS}$	$\overline{CSR}$	CK	$\overline{CK}$	Σ of inputs = H (D1 to D25)	PAR_IN[1]	PPO[2]	$\overline{QERR}$
H	L	X	↑	↓	even	L	L	H
H	L	X	↑	↓	odd	L	H	L
H	L	X	↑	↓	even	H	H	L
H	L	X	↑	↓	odd	H	L	H
H	H	L	↑	↓	even	L	L	H
H	H	L	↑	↓	odd	L	H	L
H	H	L	↑	↓	even	H	H	L
H	H	L	↑	↓	odd	H	L	H
H	H	H	↑	↓	X	X	PPOo	$\overline{QERR}$o
H	X	X	L or H	L or H	X	X	PPOo	$\overline{QERR}$o
L	X or floating	X or floating	X or floating	X or floating	X or floating	X or floating	L	H

[1] Data inputs = D2, D3, D5, D6, D8 to D25 when C0 = 0 and C1 = 0.
Data inputs = D2, D3, D5, D6, D8 to D14 when C0 = 0 and C1 = 1.
Data inputs = D1 to D6, D8 to D10, D12, D13 when C0 = 1 and C1 = 1.

[2] PAR_IN arrives one clock cycle (C0 = 0), or two clock cycles (C0 = 1), after the data to which it applies.

[3] This transition assumes $\overline{QERR}$ is HIGH at the crossing of CK going HIGH and $\overline{CK}$ going LOW. If $\overline{QERR}$ is LOW, it stays latched LOW for two clock cycles or until $\overline{RESET}$ is driven LOW.

6.2 Logic diagram



(1) Disabled in 1:1 configuration.

Fig 1. Logic diagram 1:2 Register A configuration with C0 = 0 and C1 = 1 (positive logic).

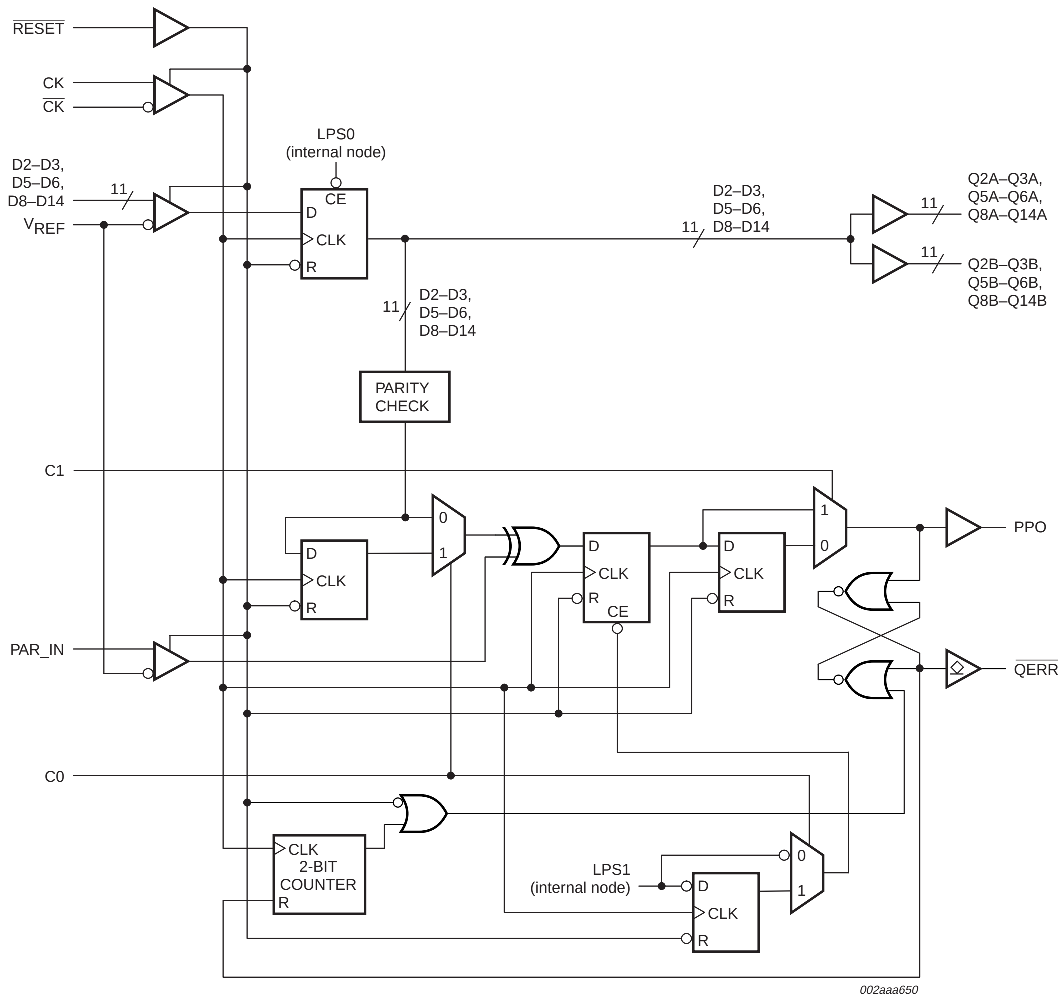


Fig 2. Parity logic diagram for 1:2 Register A configuration (positive logic); C0 = 0, C1 = 1.

7. Limiting values

Table 8: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DD}	supply voltage			–0.5	+2.5	V
V_i	receiver input voltage		[2], [3]	–0.5	+2.5	V
V_o	driver output voltage		[2], [3]	–0.5	V_{DD} + 0.5	V
I_{IK}	input clamp current	$V_i < 0$ or $V_i > V_{DD}$		-	–50	mA
I_{OK}	output clamp current	$V_o < 0$ or $V_o > V_{DD}$		-	±50	mA
I_O	continuous output current	$0 < V_o < V_{DD}$		-	±50	mA
I_{CCC}	continuous current through each V_{DD} or GND pin			-	±100	mA
T_{stg}	storage temperature			–65	+150	°C
ESD_{HBM}	electrostatic discharge	Human Body Model; 1.5 kΩ; 100 pF		>2	-	kV
ESD_{MM}	electrostatic discharge	Machine Model; 0 Ω; 200 pF		>200	-	V

[1] Stresses beyond those listed under ‘absolute maximum ratings’ may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under ‘recommended operating conditions’ is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

[2] The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

[3] This value is limited to 2.5 V maximum.

8. Recommended operating conditions

Table 9: Recommended operating conditions

Symbol	Parameter	Conditions	Min	Nom	Max	Unit
V_{DD}	supply voltage		1.7	-	1.9	V
V_{REF}	reference voltage		$0.49 \times V_{DD}$	$0.50 \times V_{DD}$	$0.51 \times V_{DD}$	V
V_{TT}	termination voltage		V_{REF} – 40 mV	V_{REF}	V_{REF} + 40 mV	V
V_i	input voltage		0	-	V_{DD}	V
V_{IH}	AC HIGH-level input voltage	Data, $\overline{CSR}$, and PAR_IN inputs	V_{REF} + 250 mV	-	-	V
V_{IL}	AC LOW-level input voltage	Data, $\overline{CSR}$, and PAR_IN inputs	-	-	V_{REF} – 250 mV	V
V_{IH}	DC HIGH-level input voltage	Data, $\overline{CSR}$, and PAR_IN inputs	V_{REF} + 125 mV	-	-	V
V_{IL}	DC LOW-level input voltage	Data, $\overline{CSR}$, and PAR_IN inputs	-	-	V_{REF} – 125 mV	V
V_{IH}	HIGH-level input voltage	$\overline{RESET}$, Cn	$0.65 \times V_{DD}$	-	-	V
V_{IL}	LOW-level input voltage	$\overline{RESET}$, Cn	-	-	$0.35 \times V_{DD}$	V
V_{ICR}	common mode input voltage range	CK, $\overline{CK}$	0.675	-	1.125	V
V_{ID}	differential input voltage	CK, $\overline{CK}$	600	-	-	mV

Table 9: Recommended operating conditions *...continued*

Symbol	Parameter	Conditions	Min	Nom	Max	Unit
I_{OH}	HIGH-level output current		-	-	–8	mA
I_{OL}	LOW-level output current		-	-	8	mA
T_{amb}	operating ambient temperature in free air		0	-	+70	°C

[1] The $\overline{RESET}$ and Cn inputs of the device must be held at valid levels (not floating) to ensure proper device operation. The differential inputs must not be floating, unless $\overline{RESET}$ is LOW.

9. Static characteristics

Table 10: DC electrical characteristics

Over recommended operating conditions, unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{OH}	HIGH-level output voltage	I_{OH} = –6 mA; V_{DD} = 1.7 V	1.2	-	-	V
V_{OL}	LOW-level output voltage	I_{OL} = 6 mA; V_{DD} = 1.7 V	-	-	0.5	V
I_i	input current	all inputs; V_i = V_{DD} or GND; V_{DD} = 1.9 V	-	-	±5	µA
I_{DD}	static standby current	$\overline{RESET}$ = GND; I_o = 0 mA; V_{DD} = 1.9 V	-	-	100	µA
	static operating current	$\overline{RESET}$ = V_{DD}; I_o = 0 mA; V_{DD} = 1.9 V; V_i = $V_{IH(AC)}$ or $V_{IL(AC)}$	-	-	40	mA
I_{DDD}	dynamic operating current, clock only	$\overline{RESET}$ = V_{DD}; V_i = $V_{IH(AC)}$ or $V_{IL(AC)}$; CK and $\overline{CK}$ switching at 50% duty cycle. I_o = 0 mA; V_{DD} = 1.8 V	-	16	-	µA / MHz
	dynamic operating current, per each data input, 1:1 mode	$\overline{RESET}$ = V_{DD}; V_i = $V_{IH(AC)}$ or $V_{IL(AC)}$; CK and $\overline{CK}$ switching at 50% duty cycle. One data input switching at half clock frequency, 50% duty cycle. I_o = 0 mA; V_{DD} = 1.8 V	-	11	-	µA / MHz
	dynamic operating current, per each data input, 1:2 mode	$\overline{RESET}$ = V_{DD}; V_i = $V_{IH(AC)}$ or $V_{IL(AC)}$; CK and $\overline{CK}$ switching at 50% duty cycle. One data input switching at half clock frequency, 50% duty cycle. I_o = 0 mA; V_{DD} = 1.8 V	-	19	-	µA / MHz
C_i	input capacitance, data and $\overline{CSR}$ inputs	V_i = V_{REF} ± 250 mV; V_{DD} = 1.8 V	2.5	-	3.5	pF
	input capacitance, CK and $\overline{CK}$ inputs	V_{ICR} = 0.9 V; $V_{i(p-p)}$ = 600 mV; V_{DD} = 1.8 V	2	-	3	pF
	input capacitance, $\overline{RESET}$ input	V_i = V_{DD} or GND; V_{DD} = 1.8 V	3	-	4	pF

10. Dynamic characteristics

Table 11: Timing requirements

Over recommended operating conditions, unless otherwise noted. See Figure 2.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{CLOCK}	clock frequency		-	-	450	MHz
t_W	pulse duration, CK, $\overline{\text{CK}}$ HIGH or LOW		1	-	-	ns
t_{ACT}	differential inputs active time	[1], [2]	-	-	10	ns
t_{INACT}	differential inputs inactive time	[1], [3]	-	-	15	ns
t_{SU}	set-up time	$\overline{\text{DCS}}$ before CK↑, $\overline{\text{CK}}$↓, $\overline{\text{CSR}}$ HIGH; $\overline{\text{CSR}}$ before CK↑, $\overline{\text{CK}}$↓, $\overline{\text{DCS}}$ HIGH	0.7	-	-	ns
		$\overline{\text{DCS}}$ before CK↑, $\overline{\text{CK}}$↓, $\overline{\text{CSR}}$ LOW	0.5	-	-	ns
		DODT, DCKE and data before CK↑, $\overline{\text{CK}}$↓	0.5	-	-	ns
		PAR_IN before CK↑, $\overline{\text{CK}}$↓	0.5	-	-	ns
t_H	hold time	DCS, DODT, DCKE and data after CK↑, $\overline{\text{CK}}$↓	0.5	-	-	ns
		PAR_IN after CK↑, $\overline{\text{CK}}$↓	0.5	-	-	ns

[1] This parameter is not necessarily production tested.

[2] V_{REF} must be held at a valid input voltage level and data inputs must be held LOW for a minimum time of t_{ACT} (max) after $\overline{\text{RESET}}$ is taken HIGH.

[3] V_{REF}, Data and clock inputs must be held at valid levels (not floating) a minimum time of t_{INACT} (max) after $\overline{\text{RESET}}$ is taken LOW.

Table 12: Switching characteristics

Over recommended operating conditions, unless otherwise noted. See Section 11.1.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{MAX}	maximum input clock frequency		450	-	-	MHz
t_{PDM}	propagation delay, single bit switching	from CK↑ and $\overline{\text{CK}}$↓ to Qn [1]	1.41	-	1.8	ns
t_{PD}	propagation delay	from CK↑ and $\overline{\text{CK}}$↓ to PPO	0.5	-	1.8	ns
t_{LH}	LOW-to-HIGH propagation delay	from CK↑ and $\overline{\text{CK}}$↓ to $\overline{\text{QERR}}$	1.2	-	3	ns
t_{HL}	HIGH-to-LOW propagation delay	from CK↑ and $\overline{\text{CK}}$↓ to $\overline{\text{QERR}}$	1	-	2.4	ns
t_{PDMSS}	propagation delay, simultaneous switching	from CK↑ and $\overline{\text{CK}}$↓ to Qn [1], [2]	-	-	2.0	ns
t_{PHL}	HIGH-to-LOW propagation delay	from $\overline{\text{RESET}}$↓ to Qn↓	-	-	3	ns
		from $\overline{\text{RESET}}$↓ to PPO↓	-	-	3	ns
t_{PLH}	LOW-to-HIGH propagation delay	from $\overline{\text{RESET}}$↓ to $\overline{\text{QERR}}$↑	-	-	3	ns

[1] Includes 350 ps of test-load transmission line delay.

[2] This parameter is not necessarily production tested.

Table 13: Data output edge rates

Over recommended operating conditions, unless otherwise noted. See Section 11.2.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
dV/dt_r	rising edge slew rate	from 20% to 80%	1	-	4	V/ns
dV/dt_f	falling edge slew rate	from 80% to 20%	1	-	4	V/ns
dV/dt_Δ[1]	absolute difference between dV/dt_r and dV/dt_f	from 20% or 80% to 80% or 20%	-	-	1	V/ns

[1] Difference between dV/dt_r (rising edge rate) and dV/dt_f (falling edge rate).

10.1 Timing diagrams

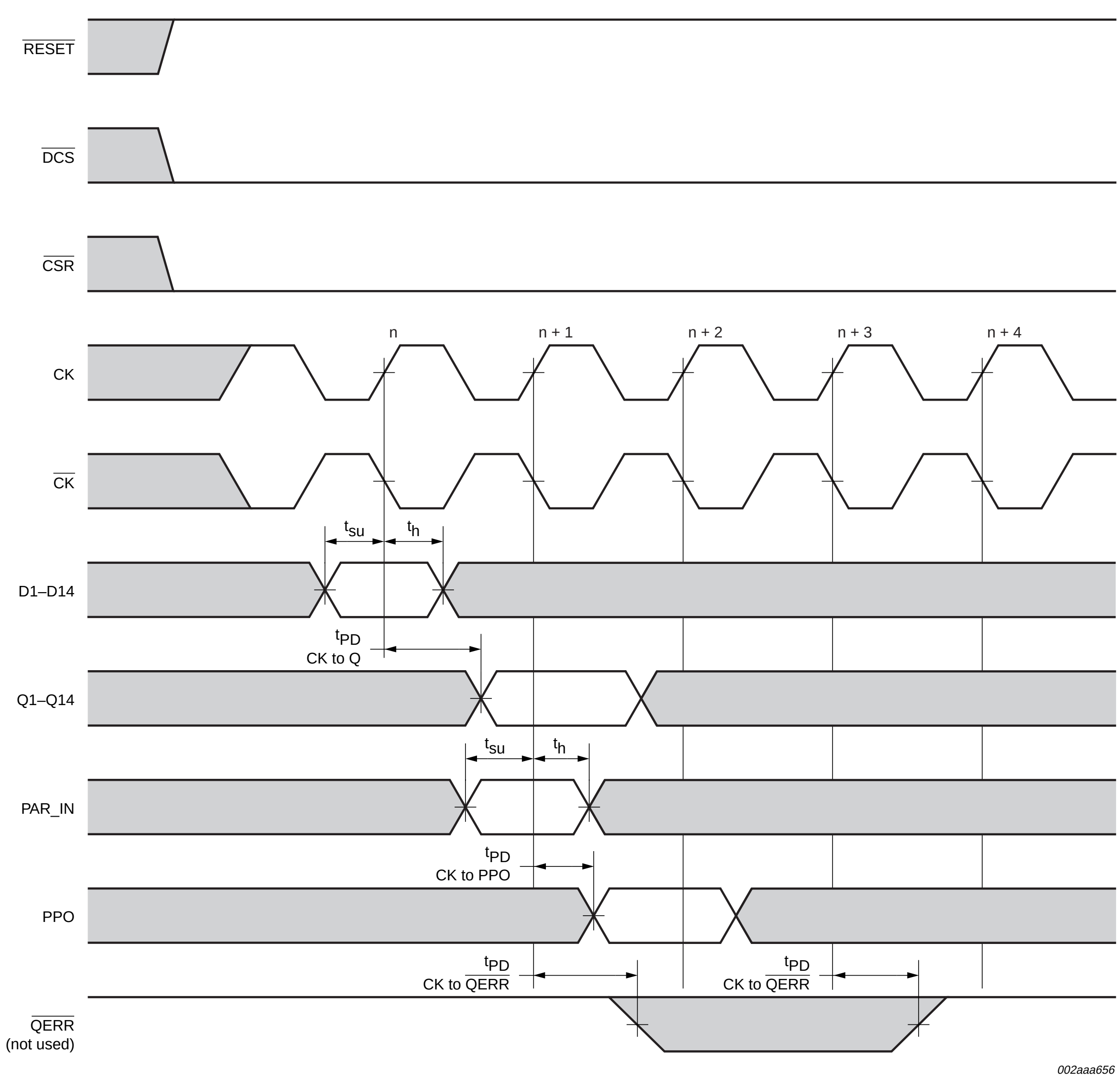


Fig 3. Timing diagram for SSTU32866 used as a single device; C0 = 0, C1 = 0.

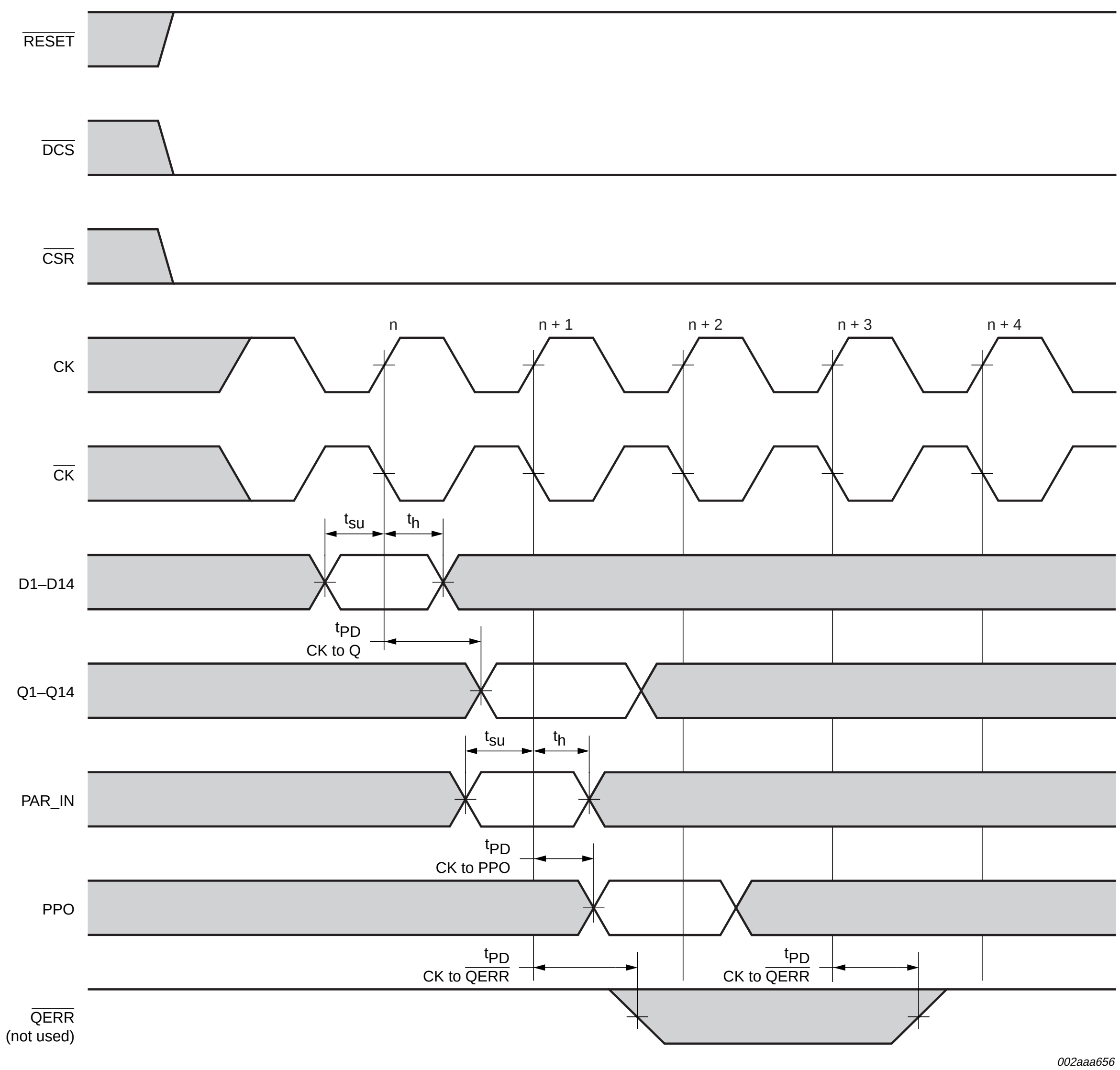
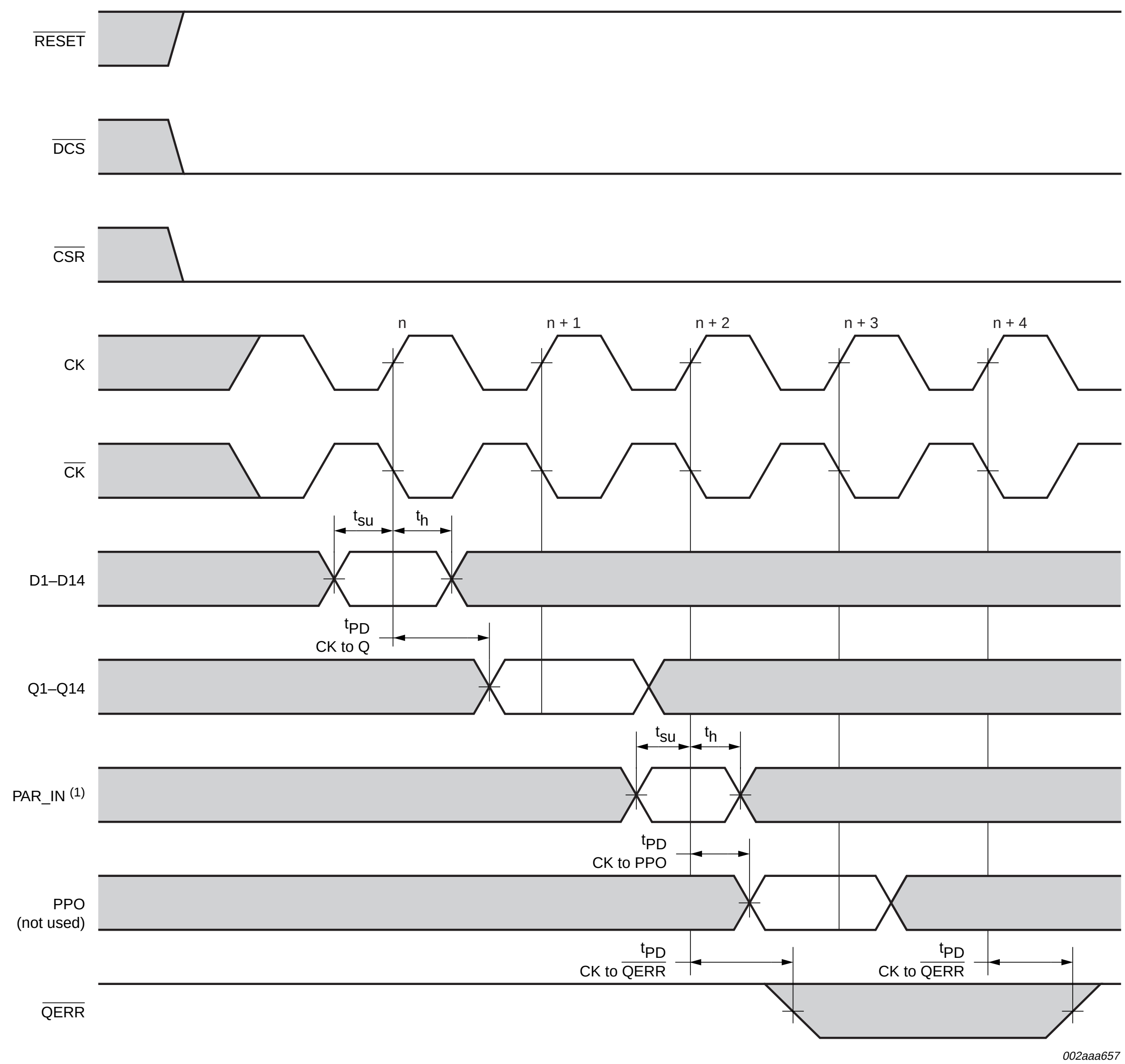


Fig 4. Timing diagram for the first SSTU32866 (1:2 Register A configuration) device used in pair; C0 = 0, C1 = 1.



(1) PAR_IN is driven from PPO of the first SSTU32866 device.

Fig 5. Timing diagram for the second SSTU32866 (1:2 Register B configuration) device used in pair; C0 = 1, C1 = 1.

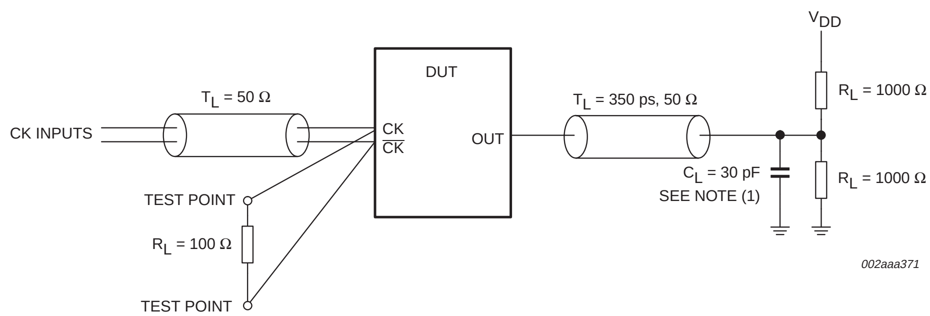
11. Test information

11.1 Parameter measurement information for data output load circuit

V_{DD} = 1.8 V ± 0.1 V.

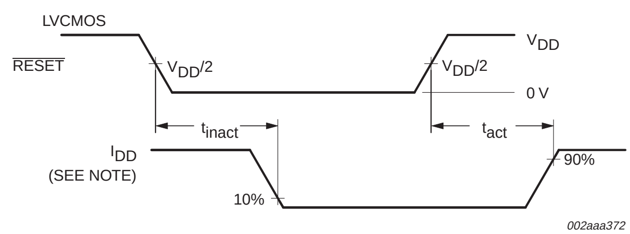
All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz; Z_o = 50 Ω; input slew rate = 1 V/ns ± 20%, unless otherwise specified.

The outputs are measured one at a time with one transition per measurement.



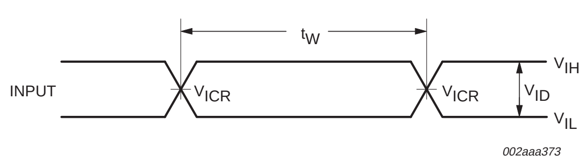
(1) C_L includes probe and jig capacitance.

Fig 6. Load circuit, data output measurements.



I_{DD} tested with clock and data inputs held at V_{DD} or GND, and I_o = 0 mA.

Fig 7. Voltage and current waveforms; inputs active and inactive times.

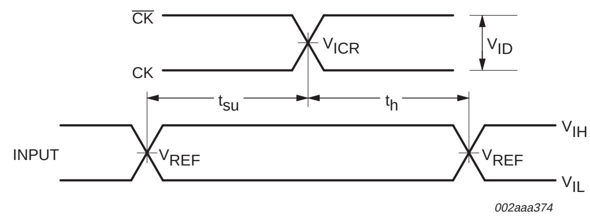


V_{ID} = 600 mV

$V_{IH} = V_{REF}$ + 250 mV (AC voltage levels) for differential inputs. $V_{IH} = V_{DD}$ for LVCMOS inputs.

$V_{IL} = V_{REF}$ – 250 mV (AC voltage levels) for differential inputs. V_{IL} = GND for LVCMOS inputs.

Fig 8. Voltage waveforms; pulse duration.



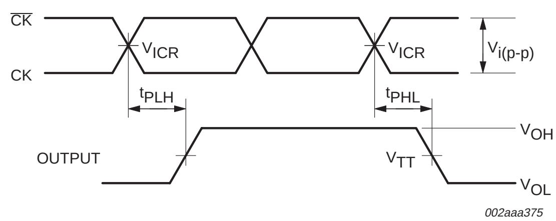
V_{ID} = 600 mV

V_{REF} = V_{DD}/2

V_{IH} = V_{REF} + 250 mV (AC voltage levels) for differential inputs. V_{IH} = V_{DD} for LVCMOS inputs.

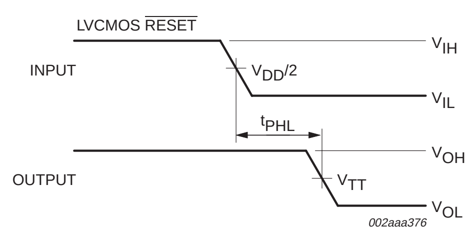
V_{IL} = V_{REF} – 250 mV (AC voltage levels) for differential inputs. V_{IL} = GND for LVCMOS inputs.

Fig 9. Voltage waveforms; set-up and hold times.



t_{PLH} and t_{PHL} are the same as t_{PD}.

Fig 10. Voltage waveforms; propagation delay times.



t_{PLH} and t_{PHL} are the same as t_{PD}.

V_{IH} = V_{REF} + 250 mV (AC voltage levels) for differential inputs. V_{IH} = V_{DD} for LVCMOS inputs.

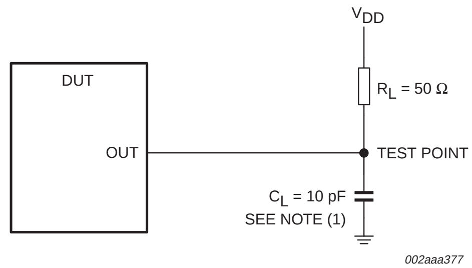
V_{IL} = V_{REF} – 250 mV (AC voltage levels) for differential inputs. V_{IL} = GND for LVCMOS inputs.

Fig 11. Voltage waveforms; propagation delay times.

11.2 Data output slew rate measurement information

V_{DD} = 1.8 V ± 0.1 V.

All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz; Z_o = 50 Ω; input slew rate = 1 V/ns ± 20%, unless otherwise specified.



(1) C_L includes probe and jig capacitance.

Fig 12. Load circuit, HIGH-to-LOW slew measurement.

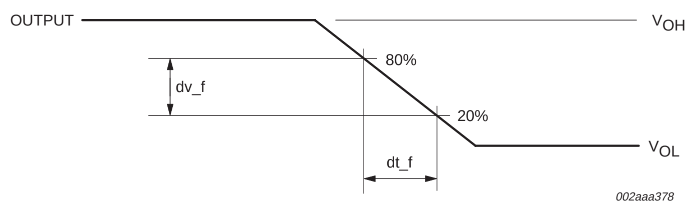
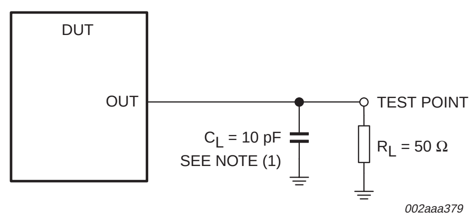


Fig 13. Voltage waveforms, HIGH-to-LOW slew rate measurement.



(1) C_L includes probe and jig capacitance.

Fig 14. Load circuit, LOW-to-HIGH slew measurement.

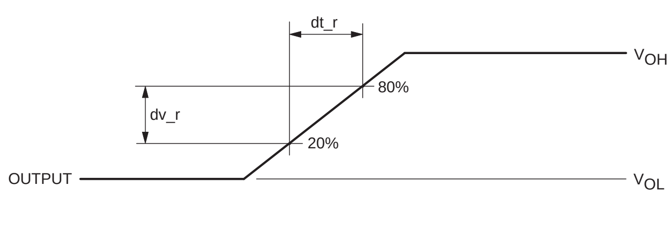
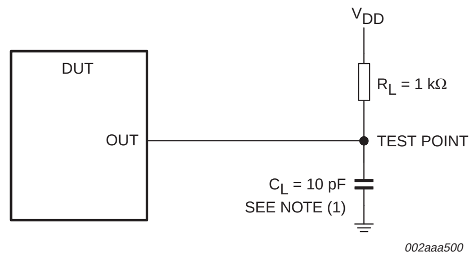


Fig 15. Voltage waveforms, LOW-to-HIGH slew rate measurement.

11.3 Error output load circuit and voltage measurement information

V_{DD} = 1.8 V ± 0.1 V.

All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz; Z_o = 50 Ω; input slew rate = 1 V/ns ± 20%, unless otherwise specified.



(1) C_L includes probe and jig capacitance.

Fig 16. Load circuit, error output measurements.

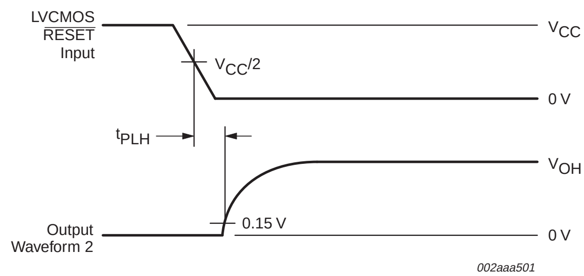


Fig 17. Voltage waveforms, open-drain output LOW-to-HIGH transition time with respect to $\overline{\text{RESET}}$ input.

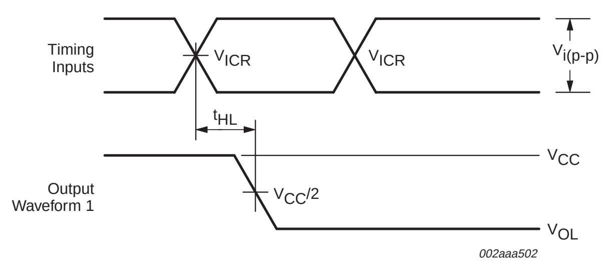


Fig 18. Voltage waveforms, open-drain output HIGH-to-LOW transition time with respect to clock inputs.

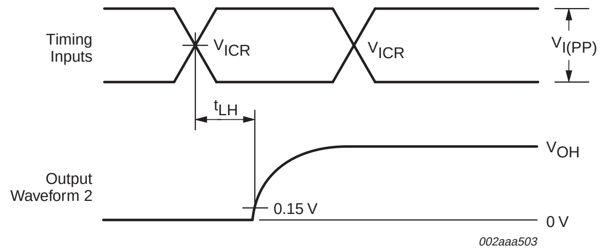
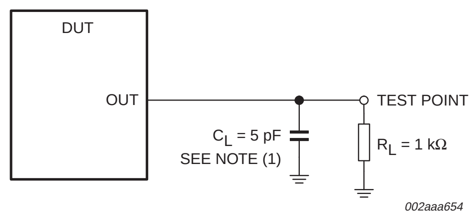


Fig 19. Voltage waveforms, open-drain output LOW-to-HIGH transition time with respect to clock inputs.

11.4 Partial Parity Out load circuit and voltage measurement information

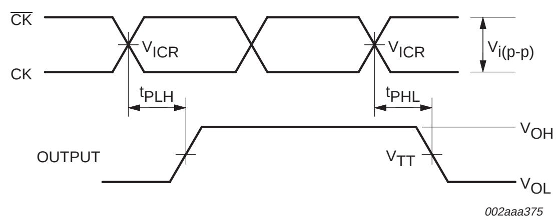
V_{DD} = 1.8 V ± 0.1 V.

All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz; Z_o = 50 Ω; input slew rate = 1 V/ns ± 20%, unless otherwise specified.



(1) C_L includes probe and jig capacitance.

Fig 20. Partial Parity Out load circuit.

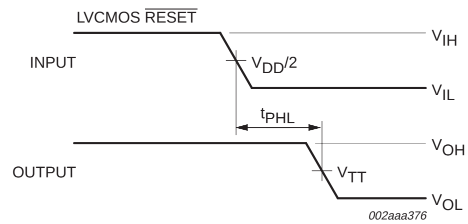


$V_{TT} = V_{DD}/2$

t_{PLH} and t_{PHL} are the same as t_{PD}.

$V_{i(p-p)}$ = 600 mV

Fig 21. Partial Parity Out voltage waveforms; propagation delay times with respect to clock inputs.



$V_{TT} = V_{DD}/2$

t_{PLH} and t_{PHL} are the same as t_{PD}.

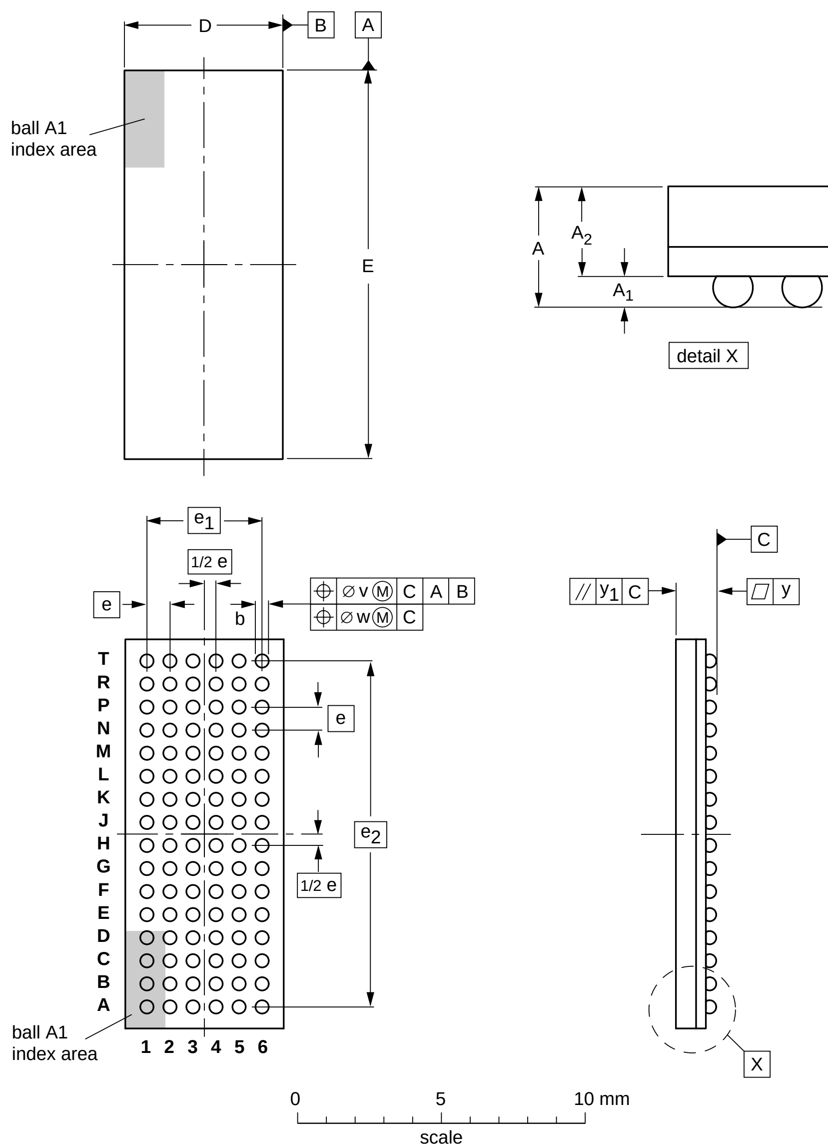
$V_{IH} = V_{REF}$ + 250 mV (AC voltage levels) for differential inputs. $V_{IH} = V_{DD}$ for LVCMOS inputs.

$V_{IL} = V_{REF}$ – 250 mV (AC voltage levels) for differential inputs. $V_{IL} = V_{DD}$ for LVCMOS inputs.

Fig 22. Partial Parity Out voltage waveforms; propagation delay times with respect to $\overline{\text{RESET}}$ input.

12. Package outline

LFBGA96: plastic low profile fine-pitch ball grid array package; 96 balls; body 13.5 x 5.5 x 1.05 mm SOT536-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	b	D	E	e	e_1	e_2	v	w	y	y_1
mm	1.5	0.41 0.31	1.2 0.9	0.51 0.41	5.6 5.4	13.6 13.4	0.8	4	12	0.15	0.1	0.1	0.2

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT536-1						~~00-03-04~~ 03-02-05

Fig 23. LFBGA96 package outline (SOT536-1).

13. Soldering

13.1 Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *Data Handbook IC26; Integrated Circuit Packages* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended. In these situations reflow soldering is recommended.

13.2 Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement. Driven by legislation and environmental forces the worldwide use of lead-free solder pastes is increasing.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 270 °C depending on solder paste material. The top-surface temperature of the packages should preferably be kept:

- below 225 °C (SnPb process) or below 245 °C (Pb-free process)
  - for all BGA, HTSSON..T and SSOP..T packages
  - for packages with a thickness ≥ 2.5 mm
  - for packages with a thickness < 2.5 mm and a volume ≥ 350 mm^3 so called thick/large packages.
- below 240 °C (SnPb process) or below 260 °C (Pb-free process) for packages with a thickness < 2.5 mm and a volume < 350 mm^3 so called small/thin packages.

Moisture sensitivity precautions, as indicated on packing, must be respected at all times.

13.3 Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.

- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time of the leads in the wave ranges from 3 to 4 seconds at 250 °C or 265 °C, depending on solder material applied, SnPb or Pb-free respectively.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

13.4 Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

13.5 Package related soldering information

Table 14: Suitability of surface mount IC packages for wave and reflow soldering methods

Package[1]	Soldering method	
	Wave	Reflow[2]
BGA, HTSSON..T[3], LBGA, LFBGA, SQFP, SSOP..T[3], TFBGA, USON, VFBGA	not suitable	suitable
DHVQFN, HBCC, HBGA, HLQFP, HSO, HSOP, HSQFP, HSSON, HTQFP, HTSSOP, HVQFN, HVSON, SMS	not suitable[4]	suitable
PLCC[5], SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended[5][6]	suitable
SSOP, TSSOP, VSO, VSSOP	not recommended[7]	suitable
CWQCCN..L[8], PMFP[9], WQCCN..L[8]	not suitable	not suitable

[1] For more detailed information on the BGA packages refer to the *(LF)BGA Application Note* (AN01026); order a copy from your Philips Semiconductors sales office.

[2] All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods*.

[3] These transparent plastic packages are extremely sensitive to reflow soldering conditions and must on no account be processed through more than one soldering cycle or subjected to infrared reflow soldering with peak temperature exceeding 217 °C ± 10 °C measured in the atmosphere of the reflow oven. The package body peak temperature must be kept as low as possible.

[4] These packages are not suitable for wave soldering. On versions with the heatsink on the bottom side, the solder cannot penetrate between the printed-circuit board and the heatsink. On versions with the heatsink on the top side, the solder might be deposited on the heatsink surface.

[5] If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.

[6] Wave soldering is suitable for LQFP, QFP and TQFP packages with a pitch (e) larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.

[7] Wave soldering is suitable for SSOP, TSSOP, VSO and VSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

[8] Image sensor packages in principle should not be soldered. They are mounted in sockets or delivered pre-mounted on flex foil. However, the image sensor package can be mounted by the client on a flex foil by using a hot bar soldering process. The appropriate soldering profile can be provided on request.

[9] Hot bar soldering or manual soldering is suitable for PMFP packages.

14. Revision history

Table 15: Revision history

Rev	Date	CPCN	Description
01	20040709	-	Objective data (9397 750 12145).

15. Data sheet status

Level	Data sheet status[1]	Product status[2][3]	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
III	Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

16. Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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