32 Mbit (4M x 8/2M x 16)
3V Only CMOS Flash Memory

1. FEATURES

- Single supply voltage 2.7V-3.6V
- Fast access time: 70/90 ns
- 4,194,304x8 / 2,097,152x16 switchable by $\overline{BYTE}$ pin
  Compatible with JEDEC standard
  - Pin-out, packages and software commands compatible with single-power supply Flash
- Low power consumption
  - 20mA typical active current
  - 25uA typical standby current
- 100,000 program/erase cycles typically
- 20 Years Data Retention
- Command register architecture
  - Byte Word Programming (9 μs/11 μs typical)
  - Byte Mode : eight 8KB, sixty three 64KB sectors.
  - Word Mode : eight 4K word, sixty-three 32 K word sectors.
- Auto Erase (chip & sector) and Auto Program
  - Any combination of sectors can be erased concurrently; Chip erase also provided.
  - Automatically program and verify data at specified address
- Erase Suspend/Erase Resume
  - Suspend or Resume erasing sectors to allow the read/program in another sector
- Secured Silicon Sector
  - 128word sector for permanent, secure identification through an 8- word random Electronic Serial Number
  - May be programmed and locked at the factory or by the customer
  - Accessible through a command sequence.

- Ready/Busy (RY/$\overline{BY}$)
  - RY/$\overline{BY}$ output pin for detection of program or erase operation completion
- End of program or erase detection
  - Data polling
  - Toggle bits
- Hardware reset
  - Hardware pin ($\overline{RESET}$) resets the internal state machine to the read mode
- Sector Protection /Unprotection
  - Hardware Protect/Unprotect any combination of sectors from a program or erase operation.
- Low V_{CC} Write inhibit is equal to or less than 2.0V
- Boot Sector Architecture
  - U = Upper Boot Block
  - B = Bottom Boot Block
- Packages available:
  - 48-pin TSOPI
  - All Pb-free products are RoHS-Compliant
- CFI (Common Flash Interface) complaint
  - Provides device-specific information to the system, allowing host software to easily reconfigure to different Flash devices.

2. ORDERING INFORMATION

Part No	Boot	Speed	Package	Comments	Part No	Boot	Speed	Package	Comments
F49L320UA-70TG	Upper	70 ns	TSOPI	Pb-free	F49L320UA-90TG	Upper	90 ns	TSOPI	Pb-free
F49L320BA-70TG	Bottom	70 ns	TSOPI	Pb-free	F49L320BA-90TG	Bottom	90 ns	TSOPI	Pb-free

3. GENERAL DESCRIPTION

The F49L320UA/F49L320BA is a 32 Megabit, 3V only CMOS Flash memory device organized as 4M bytes of 8 bits or 2M words of 16bits. This device is packaged in standard 48-pin TSOP. It is designed to be programmed and erased both in system and can in standard EPROM programmers.

With access times of 70 ns and 90 ns, the F49L320UA/F49L320BA allows the operation of high-speed microprocessors. The device has separate chip enable $\overline{CE}$, write enable $\overline{WE}$, and output enable $\overline{OE}$ controls. ESMT's memory devices reliably store memory data even after 100,000 program and erase cycles.

The F49L320UA/F49L320BA is entirely pin and command set compatible with the JEDEC standard for 32 Megabit Flash memory devices. Commands are written to

The F49L320UA/F49L320BA features a sector erase architecture. The device array is divided into eight 8KB, sixty-three 64KB for

byte mode. The device memory array is divided into eight 4K word, sixty-three 32K word sectors for word mode. Sectors can be erased individually or in groups without affecting the data in other sectors. Multiple-sector erase and whole chip erase capabilities provide the flexibility to revise the data in the device.

The sector protect/unprotect feature disables both program and erase operations in any combination of the sectors of the memory. This can be achieved in-system or via programming equipment.

A low V_{CC} detector inhibits write operations on loss of power. End of program or erase is detected by the Ready/Busy status pin, Data Polling of DQ7, or by the Toggle Bit I feature on DQ6. Once the program or erase cycle has been successfully completed, the device internally resets to the Read mode. The command register using standard microprocessor write timings.

4. PIN CONFIGURATIONS

4.1 48-pin TSOP
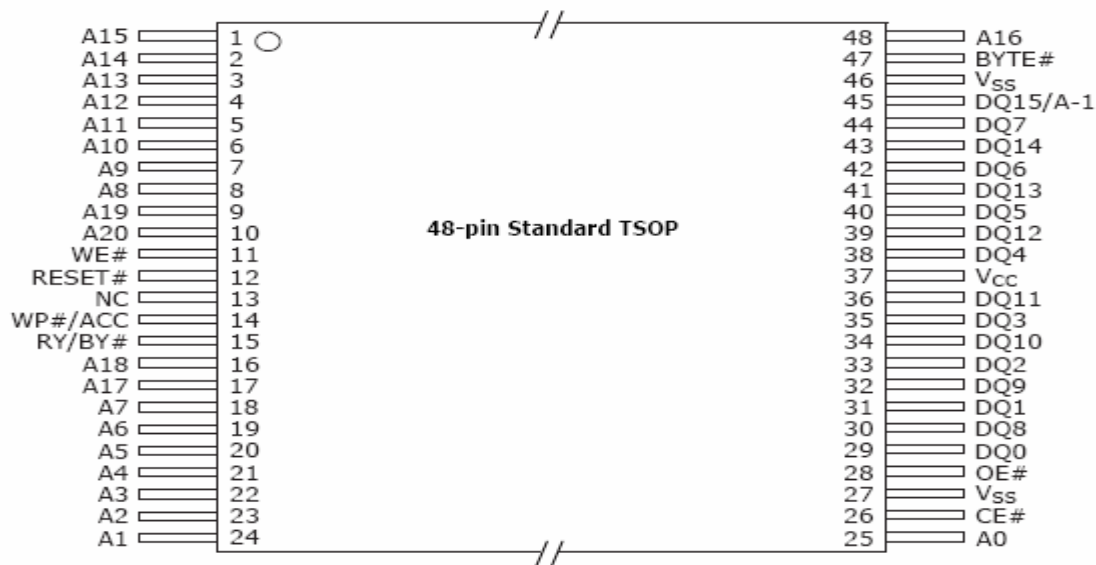
4.2 Pin Description

Symbol	Pin Name	Functions
A0~A20	Address Input	To provide memory addresses.
DQ0~DQ14	Data Input/Output	To output data when Read and receive data when Write. The outputs are in tri-state when $\overline{OE}$ or $\overline{CE}$ is high.
DQ15/A-1	Q15 (Word mode) / LSB addr (Byte Mode)	To bi-direction date I/O when $\overline{BYTE}$ is High. To input address when $\overline{BYTE}$ is Low
$\overline{CE}$	Chip Enable	To activate the device when $\overline{CE}$ is low.
$\overline{OE}$	Output Enable	To gate the data output buffers.
$\overline{WE}$	Write Enable	To control the Write operations.
$\overline{RESET}$	Reset	Hardware Reset Pin/Sector Protect Unprotect
$\overline{BYTE}$	Word/Byte selection input	To select word mode or byte mode
RY/$\overline{BY}$	Ready/Busy	To check device operation status
V_{CC}	Power Supply	To provide power
GND	Ground	
NC	No connection	

5. SECTOR STRUCTURE

Table 1: F49L320UA Sector Address Table

Sector	Sector Size		Address range			Sector Address								
	Byte Mode	Word Mode	Byte Mode(x8)	Word Mode(x16)	A20	A19	A18	A17	A16	A15	A14	A13	A12
SA0	64Kbytes	32Kwords	000000-00FFFF	00000-07FFF	0	0	0	0	0	0	X	X	X
SA1	64Kbytes	32Kwords	010000-01FFFF	08000-0FFFF	0	0	0	0	0	1	X	X	X
SA2	64Kbytes	32Kwords	020000-02FFFF	10000-17FFF	0	0	0	0	1	0	X	X	X
SA3	64Kbytes	32Kwords	030000-03FFFF	18000-1FFFF	0	0	0	0	1	1	X	X	X
SA4	64Kbytes	32Kwords	040000-04FFFF	20000-27FFF	0	0	0	1	0	0	X	X	X
SA5	64Kbytes	32Kwords	050000-05FFFF	28000-2FFFF	0	0	0	1	0	1	X	X	X
SA6	64Kbytes	32Kwords	060000-06FFFF	30000-37FFF	0	0	0	1	1	0	X	X	X
SA7	64Kbytes	32Kwords	070000-07FFFF	38000-3FFFF	0	0	0	1	1	1	X	X	X
SA8	64Kbytes	32Kwords	080000-08FFFF	40000-47FFF	0	0	1	0	0	0	X	X	X
SA9	64Kbytes	32Kwords	090000-09FFFF	48000-4FFFF	0	0	1	0	0	1	X	X	X
SA10	64Kbytes	32Kwords	0A0000-0AFFFF	50000-57FFF	0	0	1	0	1	0	X	X	X
SA11	64Kbytes	32Kwords	0B0000-0BFFFF	58000-5FFFF	0	0	1	0	1	1	X	X	X
SA12	64Kbytes	32Kwords	0C0000-0CFFFF	60000-67FFF	0	0	1	1	0	0	X	X	X
SA13	64Kbytes	32Kwords	0D0000-0DFFFF	68000-6FFFF	0	0	1	1	0	1	X	X	X
SA14	64Kbytes	32Kwords	0E0000-0EFFFF	70000-77FFF	0	0	1	1	1	0	X	X	X
SA15	64Kbytes	32Kwords	0F0000-0FFFFF	78000-7FFFF	0	0	1	1	1	1	X	X	X
SA16	64Kbytes	32Kwords	100000-10FFFF	80000-87FFF	0	1	0	0	0	0	X	X	X
SA17	64Kbytes	32Kwords	110000-11FFFF	88000-8FFFF	0	1	0	0	0	1	X	X	X
SA18	64Kbytes	32Kwords	120000-12FFFF	90000-97FFF	0	1	0	0	1	0	X	X	X
SA19	64Kbytes	32Kwords	130000-13FFFF	98000-9FFFF	0	1	0	0	1	1	X	X	X
SA20	64Kbytes	32Kwords	140000-14FFFF	A0000-A7FFF	0	1	0	1	0	0	X	X	X
SA21	64Kbytes	32Kwords	150000-15FFFF	A8000-AFFFF	0	1	0	1	0	1	X	X	X
SA22	64Kbytes	32Kwords	160000-16FFFF	B0000-B7FFF	0	1	0	1	1	0	X	X	X
SA23	64Kbytes	32Kwords	170000-17FFFF	B8000-BFFF	0	1	0	1	1	1	X	X	X
SA24	64Kbytes	32Kwords	180000-18FFFF	C0000-C7FFF	A20	1	1	0	0	0	X	X	X
SA25	64Kbytes	32Kwords	190000-19FFFF	C8000-CFFFF	0	1	1	0	0	1	X	X	X
SA26	64Kbytes	32Kwords	1A0000-1AFFFF	D0000-D7FFF	0	1	1	0	1	0	X	X	X
SA27	64Kbytes	32Kwords	1B0000-1BFFFF	D8000-DFFFF	0	1	1	0	1	1	X	X	X
SA28	64Kbytes	32Kwords	1C0000-1CFFFF	E0000-E7FFF	0	1	1	1	0	0	X	X	X
SA29	64Kbytes	32Kwords	1D0000-1DFFFF	E8000-EFFFF	0	1	1	1	0	1	X	X	X
SA30	64Kbytes	32Kwords	1E0000-1EFFFF	F0000-F7FFF	0	1	1	1	1	0	X	X	X
SA31	64Kbytes	32Kwords	1F0000-1FFFFF	F8000-FFFFF	0	1	1	1	1	1	X	X	X
SA32	64Kbytes	32Kwords	200000-20FFFF	100000-107FFF	1	0	0	0	0	0	X	X	X
SA33	64Kbytes	32Kwords	210000-21FFFF	108000-10FFFF	1	0	0	0	0	1	X	X	X
SA34	64Kbytes	32Kwords	220000-22FFFF	110000-117FFF	1	0	0	0	1	0	X	X	X

SA35	64Kbytes	32Kwords	230000-23FFFF	118000-11FFFF	1	0	0	0	1	1	X	X	X
SA36	64Kbytes	32Kwords	240000-24FFFF	120000-127FFF	1	0	0	1	0	0	X	X	X
SA37	64Kbytes	32Kwords	250000-25FFFF	128000-12FFFF	1	0	0	1	0	1	X	X	X
SA38	64Kbytes	32Kwords	260000-26FFFF	130000-137FFF	1	0	0	1	1	0	X	X	X
SA39	64Kbytes	32Kwords	270000-27FFFF	138000-13FFFF	1	0	0	1	1	1	X	X	X
SA40	64Kbytes	32Kwords	280000-28FFFF	140000-147FFF	1	0	1	0	0	0	X	X	X
SA41	64Kbytes	32Kwords	290000-29FFFF	148000-14FFFF	1	0	1	0	0	1	X	X	X
SA42	64Kbytes	32Kwords	2A0000-2AFFFF	150000-157FFF	1	0	1	0	1	0	X	X	X
SA43	64Kbytes	32Kwords	2B0000-2BFFFF	158000-15FFFF	1	0	1	0	1	1	X	X	X
SA44	64Kbytes	32Kwords	2C0000-2CFFFF	160000-167FFF	1	0	1	1	0	0	X	X	X
SA45	64Kbytes	32Kwords	2D0000-2DFFFF	168000-16FFFF	1	0	1	1	0	1	X	X	X
SA46	64Kbytes	32Kwords	2E0000-2EFFFF	170000-177FFF	1	0	1	1	1	0	X	X	X
SA47	64Kbytes	32Kwords	2F0000-2FFFFF	178000-17FFFF	1	0	1	1	1	1	X	X	X
SA48	64Kbytes	32Kwords	300000-30FFFF	180000-187FFF	1	1	0	0	0	0	X	X	X
SA49	64Kbytes	32Kwords	310000-31FFFF	188000-18FFFF	1	1	0	0	0	1	X	X	X
SA50	64Kbytes	32Kwords	320000-32FFFF	190000-197FFF	1	1	0	0	1	0	X	X	X
SA51	64Kbytes	32Kwords	330000-33FFFF	198000-19FFFF	1	1	0	0	1	1	X	X	X
SA52	64Kbytes	32Kwords	340000-34FFFF	1A0000-1A7FFF	1	1	0	1	0	0	X	X	X
SA53	64Kbytes	32Kwords	350000-35FFFF	1A8000-1AFFFF	1	1	0	1	0	1	X	X	X
SA54	64Kbytes	32Kwords	360000-36FFFF	1B0000-1B7FFF	1	1	0	1	1	0	X	X	X
SA55	64Kbytes	32Kwords	370000-37FFFF	1B8000-1BFFFF	1	1	0	1	1	1	X	X	X
SA56	64Kbytes	32Kwords	380000-38FFFF	1C0000-1C7FFF	1	1	1	0	0	0	X	X	X
SA57	64Kbytes	32Kwords	390000-39FFFF	1C8000-1CFFFF	1	1	1	0	0	1	X	X	X
SA58	64Kbytes	32Kwords	3A0000-3AFFFF	1D0000-1D7FFF	1	1	1	0	1	0	X	X	X
SA59	64Kbytes	32Kwords	3B0000-3BFFFF	1D8000-1DFFFF	1	1	1	0	1	1	X	X	X
SA60	64Kbytes	32Kwords	3C0000-3CFFFF	1E0000-1E7FFF	1	1	1	1	0	0	X	X	X
SA61	64Kbytes	32Kwords	3D0000-3DFFFF	1E8000-1EFFFF	1	1	1	1	0	1	X	X	X
SA62	64Kbytes	32Kwords	3E0000-3EFFFF	1F0000-1F7FFF	1	1	1	1	1	0	X	X	X
SA63	8Kbytes	4Kwords	3F0000-3F1FFF	1F8000-1F8FFF	1	1	1	1	1	1	0	0	0
SA64	8Kbytes	4Kwords	3F2000-3F3FFF	1F9000-1F9FFF	1	1	1	1	1	1	0	0	1
SA65	8Kbytes	4Kwords	3F4000-3F5FFF	1FA000-1FAFFF	1	1	1	1	1	1	0	1	0
SA66	8Kbytes	4Kwords	3F6000-3F7FFF	1FB000-1FBFFF	1	1	1	1	1	1	0	1	1
SA67	8Kbytes	4Kwords	3F8000-3F9FFF	1FC000-1FCFFF	1	1	1	1	1	1	1	0	0
SA68	8Kbytes	4Kwords	3FA000-3FBFFF	1FD000-1FDFFF	1	1	1	1	1	1	1	0	1
SA69	8Kbytes	4Kwords	3FC000-3FDFFF	1FE000-1FEFFF	1	1	1	1	1	1	1	1	0
SA70	8Kbytes	4Kwords	3FE000-3FFFFF	1FF000-1FFFFF	1	1	1	1	1	1	1	1	1

Note: Byte Mode: address range A20 : A-1, Word mode : address range A20 : A0

Table 2: F49L320BA Sector Address Table

Sector	Sector Size		Address range			Sector Address								
	Byte Mode	Word Mode	Byte Mode(x8)	Word Mode(x16)	A20	A19	A18	A17	A16	A15	A14	A13	A12
SA0	8Kbytes	4Kwords	000000-001FFF	00000-00FFF	0	0	0	0	0	0	0	0	0
SA1	8Kbytes	4Kwords	002000-003FFF	01000-01FFF	0	0	0	0	0	0	0	0	1
SA2	8Kbytes	4Kwords	004000-005FFF	02000-02FFF	0	0	0	0	0	0	0	1	0
SA3	8Kbytes	4Kwords	006000-007FFF	03000-03FFF	0	0	0	0	0	0	0	1	1
SA4	8Kbytes	4Kwords	008000-009FFF	04000-04FFF	0	0	0	0	0	0	1	0	0
SA5	8Kbytes	4Kwords	00A000-00BFFF	05000-05FFF	0	0	0	0	0	0	1	0	1
SA6	8Kbytes	4Kwords	00C000-00DFFF	06000-06FFF	0	0	0	0	0	0	1	1	0
SA7	8Kbytes	4Kwords	00E000-00FFFF	07000-07FFF	0	0	0	0	0	0	1	1	1
SA8	64Kbytes	32Kwords	010000-01FFFF	08000-0FFFF	0	0	0	0	0	1	X	X	X
SA9	64Kbytes	32Kwords	020000-02FFFF	010000-017FFF	0	0	0	0	1	0	X	X	X
SA10	64Kbytes	32Kwords	030000-03FFFF	018000-01FFFF	0	0	0	0	1	1	X	X	X
SA11	64Kbytes	32Kwords	040000-04FFFF	020000-027FFF	0	0	0	1	0	0	X	X	X
SA12	64Kbytes	32Kwords	050000-05FFFF	028000-02FFFF	0	0	0	1	0	1	X	X	X
SA13	64Kbytes	32Kwords	060000-06FFFF	030000-037FFF	0	0	0	1	1	0	X	X	X
SA14	64Kbytes	32Kwords	070000-07FFFF	038000-03FFFF	0	0	0	1	1	1	X	X	X
SA15	64Kbytes	32Kwords	080000-08FFFF	040000-047FFF	0	0	1	0	0	0	X	X	X
SA16	64Kbytes	32Kwords	090000-09FFFF	048000-04FFFF	0	0	1	0	0	1	X	X	X
SA17	64Kbytes	32Kwords	0A0000-0AFFFF	050000-057FFF	0	0	1	0	1	0	X	X	X
SA18	64Kbytes	32Kwords	0B0000-0BFFFF	058000-05FFFF	0	0	1	0	1	1	X	X	X
SA19	64Kbytes	32Kwords	0C0000-0CFFFF	060000-067FFF	0	0	1	1	0	0	X	X	X
SA20	64Kbytes	32Kwords	0D0000-0DFFFF	068000-06FFFF	0	0	1	1	0	1	X	X	X
SA21	64Kbytes	32Kwords	0E0000-0EFFFF	070000-077FFF	0	0	1	1	1	0	X	X	X
SA22	64Kbytes	32Kwords	0F0000-0FFFFF	078000-07FFFF	0	0	1	1	1	1	X	X	X
SA23	64Kbytes	32Kwords	100000-10FFFF	080000-087FFF	0	1	0	0	0	0	X	X	X
SA24	64Kbytes	32Kwords	110000-11FFFF	088000-08FFFF	0	1	0	0	0	1	X	X	X
SA25	64Kbytes	32Kwords	120000-12FFFF	090000-097FFF	0	1	0	0	1	0	X	X	X
SA26	64Kbytes	32Kwords	130000-13FFFF	098000-09FFFF	0	1	0	0	1	1	X	X	X
SA27	64Kbytes	32Kwords	140000-14FFFF	0A0000-0A7FFF	0	1	0	1	0	0	X	X	X
SA28	64Kbytes	32Kwords	150000-15FFFF	0A8000-0AFFFF	0	1	0	1	0	1	X	X	X
SA29	64Kbytes	32Kwords	160000-16FFFF	0B0000-0B7FFF	0	1	0	1	1	0	X	X	X
SA30	64Kbytes	32Kwords	170000-17FFFF	0B8000-0BFFFF	0	1	0	1	1	1	X	X	X
SA31	64Kbytes	32Kwords	180000-18FFFF	0C0000-0C7FFF	0	1	1	0	0	0	X	X	X
SA32	64Kbytes	32Kwords	190000-19FFFF	0C8000-0CFFFF	0	1	1	0	0	1	X	X	X
SA33	64Kbytes	32Kwords	1A0000-1AFFFF	0D0000-0D7FFF	0	1	1	0	1	0	X	X	X
SA34	64Kbytes	32Kwords	1B0000-1BFFFF	0D8000-0DFFFF	0	1	1	0	1	1	X	X	X
SA35	64Kbytes	32Kwords	1C0000-1CFFFF	0E0000-0E7FFF	0	1	1	1	0	0	X	X	X

SA36	64Kbytes	32Kwords	1D0000-1DFFFF	0E8000-0EFFFF	0	1	1	1	0	1	X	X	X
SA37	64Kbytes	32Kwords	1E0000-1EFFFF	0F0000-0F7FFF	0	1	1	1	1	0	X	X	X
SA38	64Kbytes	32Kwords	1F0000-1FFFFF	0F8000-0FFFFF	0	1	1	1	1	1	X	X	X
SA39	64Kbytes	32Kwords	200000-20FFFF	100000-107FFF	1	0	0	0	0	0	X	X	X
SA40	64Kbytes	32Kwords	210000-21FFFF	108000-10FFFF	1	0	0	0	0	1	X	X	X
SA41	64Kbytes	32Kwords	220000-22FFFF	110000-117FFF	1	0	0	0	1	0	X	X	X
SA42	64Kbytes	32Kwords	230000-23FFFF	118000-11FFFF	1	0	0	0	1	1	X	X	X
SA43	64Kbytes	32Kwords	240000-24FFFF	120000-127FFF	1	0	0	1	0	0	X	X	X
SA44	64Kbytes	32Kwords	250000-25FFFF	128000-12FFFF	1	0	0	1	0	1	X	X	X
SA45	64Kbytes	32Kwords	260000-26FFFF	130000-137FFF	1	0	0	1	1	0	X	X	X
SA46	64Kbytes	32Kwords	270000-27FFFF	138000-13FFFF	1	0	0	1	1	1	X	X	X
SA47	64Kbytes	32Kwords	280000-28FFFF	140000-147FFF	1	0	1	0	0	0	X	X	X
SA48	64Kbytes	32Kwords	290000-29FFFF	148000-14FFFF	1	0	1	0	0	1	X	X	X
SA49	64Kbytes	32Kwords	2A0000-2AFFFF	150000-157FFF	1	0	1	0	1	0	X	X	X
SA50	64Kbytes	32Kwords	2B0000-2BFFFF	158000-15FFFF	1	0	1	0	1	1	X	X	X
SA51	64Kbytes	32Kwords	2C0000-2CFFFF	160000-167FFF	1	0	1	1	0	0	X	X	X
SA52	64Kbytes	32Kwords	2D0000-2DFFFF	168000-16FFFF	1	0	1	1	0	1	X	X	X
SA53	64Kbytes	32Kwords	2E0000-2EFFFF	170000-177FFF	1	0	1	1	1	0	X	X	X
SA54	64Kbytes	32Kwords	2F0000-2FFFFF	178000-17FFFF	1	0	1	1	1	1	X	X	X
SA55	64Kbytes	32Kwords	300000-30FFFF	180000-187FFF	1	1	0	0	0	0	X	X	X
SA56	64Kbytes	32Kwords	310000-31FFFF	188000-18FFFF	1	1	0	0	0	1	X	X	X
SA57	64Kbytes	32Kwords	320000-32FFFF	190000-197FFF	1	1	0	0	1	0	X	X	X
SA58	64Kbytes	32Kwords	330000-33FFFF	198000-19FFFF	1	1	0	0	1	1	X	X	X
SA59	64Kbytes	32Kwords	340000-34FFFF	1A0000-1A7FFF	1	1	0	1	0	0	X	X	X
SA60	64Kbytes	32Kwords	350000-35FFFF	1A8000-1AFFFF	1	1	0	1	0	1	X	X	X
SA61	64Kbytes	32Kwords	360000-36FFFF	1B0000-1B7FFF	1	1	0	1	1	0	X	X	X
SA62	64Kbytes	32Kwords	370000-37FFFF	1B8000-1BFFFF	1	1	0	1	1	1	X	X	X
SA63	64Kbytes	32Kwords	380000-38FFFF	1C0000-1C7FFF	1	1	1	0	0	0	X	X	X
SA64	64Kbytes	32Kwords	390000-39FFFF	1C8000-1CFFFF	1	1	1	0	0	1	X	X	X
SA65	64Kbytes	32Kwords	3A0000-3AFFFF	1D0000-1D7FFF	1	1	1	0	1	0	X	X	X
SA66	64Kbytes	32Kwords	3B0000-3BFFFF	1D8000-1DFFFF	1	1	1	0	1	1	X	X	X
SA67	64Kbytes	32Kwords	3C0000-3CFFFF	1E0000-1E7FFF	1	1	1	1	0	0	X	X	X
SA68	64Kbytes	32Kwords	3D0000-3DFFFF	1E8000-1EFFFF	1	1	1	1	0	1	X	X	X
SA69	64Kbytes	32Kwords	3E0000-3EFFFF	1F0000-1F7FFF	1	1	1	1	1	0	X	X	X
SA70	64Kbytes	32Kwords	3F0000-3FFFFF	1F8000-1FFFFF	1	1	1	1	1	1	X	X	X

Note: Byte Mode: address range A20 : A-1, Word mode : address range A20 : A0

6. FUNCTIONAL BLOCK DIAGRAM
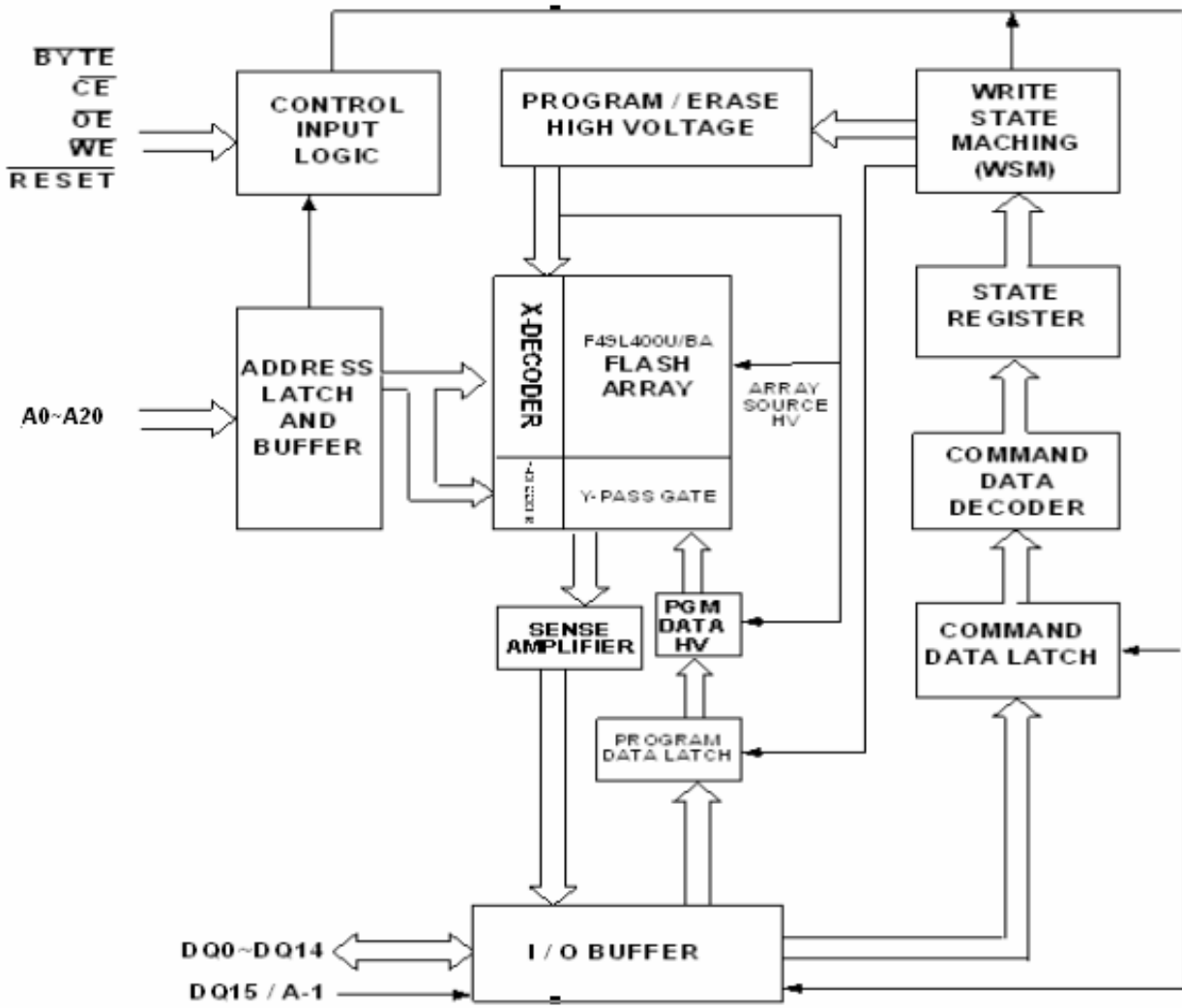
7. FUNCTIONAL DESCRIPTION

7.1 Device operation

This section describes the requirements and use of the device bus operations, which are initiated through the internal command register. The register is composed of latches that store the command, address and data information needed to execute the command. The contents of the register serve as inputs to the internal state machine. The state machine outputs dictate the function of the device. The F49L320UA /F49L320BA features various bus operations as Table 3.

Table 3. F49L320UA/F49L320BA Operation Modes Selection

Operation	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$\overline{RESET}$	$\overline{WP}$ /ACC	Addresses (Note 3)	DQ0-DQ7	DQ8-DQ15	
								$\overline{BYTE}$ =V_{IH}	$\overline{BYTE}$ =V_{IL}
Read	L	L	H	H	L/H	A_{IN}	D_{OUT}	D_{OUT}	DQ8-DQ14 = High-X, DQ15 = A-1
Write(Note1)	L	H	L	H	(Note 4)	A_{IN}	(Note 5)	(Note 5)	
Accelerated Program	L	H	L	H	V_{HH}	A_{IN}	(Note 5)	(Note 5)	
Standby	V_{CC} ± 0.3	X	X	V_{CC} ± 0.3	H	X	High-Z	High-Z	High-Z
Output Disable	L	H	H	H	L/H	X	High-Z	High-Z	High-Z
Reset	X	X	X	L	L/H	X	High-Z	High-Z	High-Z
Sector Protect (Note 3)	L	H	L	V_{ID}	L/H	SA, A6 = L, A1 = H, A0 =L	(Note 5)	X	X
Sector Unprotect (Note 3)	L	H	L	V_{ID}	(Note 4)	SA, A6 = H, A1 = H, A0 = L	(Note 5)	X	X
Temporary Sector Unprotect	X	X	X	V_{ID}	(Note 4)	A_{IN}	(Note 5)	(Note 5)	High-Z

Notes:
1. When the ACC pin is at VHH, the device enters the accelerated program mode. See
2. Addresses are A20:A0 in word mode (BYTE# = VIH), A20:A-1 in byte mode (BYTE# = VIL).
3. The sector protect and sector unprotect functions may also be implemented via programming equipment.
4. If WP#/ACC = VIL, the two outermost boot sectors remain protected. If WP#/ACC = VIH, the two outermost boot sector protection depends on whether they were last protected or unprotected. If WP#/ACC = VHH, all sectors are unprotected.
5. DIN or DOUT as required by command sequence, data polling, or sector protection algorithm.

Write Protect(WP#)

The write protect function provides a hardware method of protecting certain boot sectors without using VID. This function is one of two provided by WP#/ACC pin. If the system asserts VIL On the WP#/ACC pin, the device disables program and erase functions in the two outermost 8-Kbyte boot sectors independently of whether those sectors were protected or unprotected using the method. The two outermost 8-Kbyte boot sectors are the two sectors containing the lowest addresses in a bottom-boot configured device, or the two sectors containing the highest addresses in a top-boot configured device.

If the system asserted VIH on the WP#/ACC pin, the device reverts to whether the two outermost 8-Kbyte boot sectors were last set to be protected or unprotected. That is, sector protection or unprotection for these two sectors depends on whether they were last protected or unprotected using the method.

Table 4. F49L320UA/F49L320BA Auto-Select Mode (High Voltage Method)

Description	Mode	CE#	OE#	WE#	A20 to A12	A11 to A10	A9	A8 to A7	A6	A5 to A4	A3	A2	A1	A0	DQ8 to DQ15	DQ7 to DQ0
Manufacturer ID: ESMT		L	L	H	X	X	V_{ID}	X	L	X	L	L	L	L	X	8Ch
											L	H				7Fh
											H	L				7Fh
											H	H				7Fh
Device ID: F49L320UA	Word	L	L	H	X	X	V_{ID}	X	L	X	L	L	L	H	22h	F6h
	Byte	L	L	H											X	F6h
Device ID: F49L320BA	Word	L	L	H	X	X	V_{ID}	X	L	X	L	L	L	H	22h	F9h
	Byte	L	L	H											X	F9h
Sector Protection Verification		L	L	H	SA	X	V_{ID}	X	L	X	L	L	H	L	X	01h (protected)
															X	00h (unprotected)
Sector Silicon Sector Indicator Bit (DQ7) F49L320UA		L	L	H	X	X	V_{ID}	X	L	X	L	L	H	H	X	8D (factory locked)
															X	0D (not factory locked)
Sector Silicon Sector Indicator Bit (DQ7) F49L320BA		L	L	H	X	X	V_{ID}	X	L	X	L	L	H	H	X	9D (factory locked)
															X	1D (not factory locked)

Notes :

L = Logic Low = VIL, H = Logic High = VIH, SA = Sector Address, X = Don't care.

1.Manufacturer and device codes may also be accessed via the software command sequence in Table 5.

Reset Mode :
Hardware Reset

When the $\overline{RESET}$ pin is driven low for at least a period of t_{RP}, the device immediately terminates any operation in progress, tri-states all output pins, and ignores all read/write commands for the duration of the $\overline{RESET}$ pulse. The device also resets the internal state machine to reading array data. The operation that was interrupted should be reinitiated later once the device is ready to accept another command sequence, to ensure the data integrity.

The current is reduced for the duration of the $\overline{RESET}$ pulse. When $\overline{RESET}$ is held at V_{SS} ±0. 3V, the device draws CMOS standby current (I_{CC4}). If $\overline{RESET}$ is held at V_{IL} but not within V_{SS}±0. 3V, the standby current will be greater.

The $\overline{RESET}$ pin may be tied to system reset circuitry. A system reset would thus reset the Flash memory, enabling the system to read the boot-up firm-ware from the Flash memory.

If $\overline{RESET}$ is asserted during a program or erase embedded algorithm operation, the RY/$\overline{BY}$ pin remains a "0" (busy) until the internal reset operation is complete, which requires a time of t_{READY} (during Embedded Algorithms). The system can thus monitor RY/$\overline{BY}$ to determine whether the reset operation is complete.

If $\overline{RESET}$ is asserted when a program or erase operation is not executing, i.e. the RY/$\overline{BY}$ is "1", the reset operation is completed within a time of t_{READY} (not during Embedded Algorithms). The system can read data after t_{RH} when the $\overline{RESET}$ pin returns to V_{IH}. Refer to the AC Characteristics tables 17 for Hardware Reset section & Figure 23 for the timing diagram.

Read Mode

To read array data from the outputs, the system must drive the $\overline{CE}$ and $\overline{OE}$ pins to V_{IL}. $\overline{CE}$ is the power control and selects the device. $\overline{OE}$ is the output control and gates array data to the output pins. $\overline{WE}$ should remain at V_{IH}. The internal state machine is set for reading array data upon device power-up, or after a hardware reset. This ensures that no spurious alteration of the memory content occurs during the power transition.

No command is necessary in this mode to obtain array data. Standard microprocessor's read cycles that assert valid addresses on the device address inputs produce valid data on the device data outputs. The device remains enabled for read access until the command register contents are altered.

See "Read Command" section for more information. Refer to the AC Read Operations table 14 for timing specifications and to Figure 5 for the timing diagram. I_{CC1} in the DC Characteristics table represents the active current specification for reading array data.

Write Mode

To write a command or command sequence (which includes programming data to the device and erasing sectors of memory), the system must drive $\overline{WE}$ and $\overline{CE}$ to V_{IL}, and $\overline{OE}$ to V_{IH}. The "Program Command" section has details on programming data to the device using standard command sequences.

An erase operation can erase one sector, multiple sectors, or the entire device. Tables 1 and 2 indicate the address space that each sector occupies. A "sector address" consists of the address bits required to uniquely select a sector. The "Software Command Definitions" section has details on erasing a sector or t he entire chip, or suspending/resuming the erase operation.

When the system writes the auto-select command sequence, the device enters the auto-select mode. The system can then read auto-select codes from the internal register (which is separate from the memory array) on DQ7–DQ0. Standard read cycle timings apply in this mode. Refer to the Auto-select Mode and Auto-select Command sections for more information. I_{CC2} in the DC Characteristics table represents the active current specification for the write mode. The "AC Characteristics" section contains timing specification tables and timing diagrams for write operations.

Automatic Sleep Mode

The automatic sleep mode minimizes Flash device energy consumption. The device automatically enables this mode when addresses remain unchanged for over 250ns. The automatic sleep mode is independent of the $\overline{CE}$, $\overline{WE}$, and $\overline{OE}$ control signals. Standard address access timings provide new data when addresses are changed. While in sleep mode, output data is latched and always available to the system. I_{CC4} in the DC Characteristics table represents the automatic sleep mode current specification.

Word / Byte Mode

This pin controls the I/O configuration of device. When $\overline{BYTE}$ = V_{IH} or Vcc ± 0. 3V. The I/O configuration is x16 and t he pin of D15/A-1 is bi-direction Data I/O. However, $\overline{BYTE}$ = V_{IL} or V_{SS} ± 0.3V. The I/O configuration would be x8 and The pin of DQ15/A-1 only address input pin. You must define the function of this pin before enable this device.

Temporary Sector Unprotect Mode

This feature allows temporary unprotection of previously protected sector to change data in-system. This mode is activated by setting the $\overline{RESET}$ pin to V_{ID}(10V-10.5V). During this mode, all formerly protected sectors are un-protected and can be programmed or erased by selecting the sector addresses. Once V_{ID} is removed from the $\overline{RESET}$ pin, all the previously protected sectors are protected again.

```
                    ┌─────────────────┐
                    │      Start      │
                    └─────────────────┘
                             │
                             ▼
                    ┌─────────────────────┐
                    │ RESET = VID (Note 1) │
                    └─────────────────────┘
                             │
                             ▼
                    ┌─────────────────┐
                    │ Perform Erase or │
                    │ Program Operation│
                    └─────────────────┘
                             │
                             ▼
                    ┌─────────────────┐
                    │Operation Completed│
                    └─────────────────┘
                             │
                             ▼
                    ┌─────────────────┐
                    │   RESET = VIH   │
                    └─────────────────┘
                             │
                             ▼
                    ┌─────────────────┐
                    │Temporary Sector │
                    │Unprotect Completed│
                    │    (Note 2)     │
                    └─────────────────┘
```
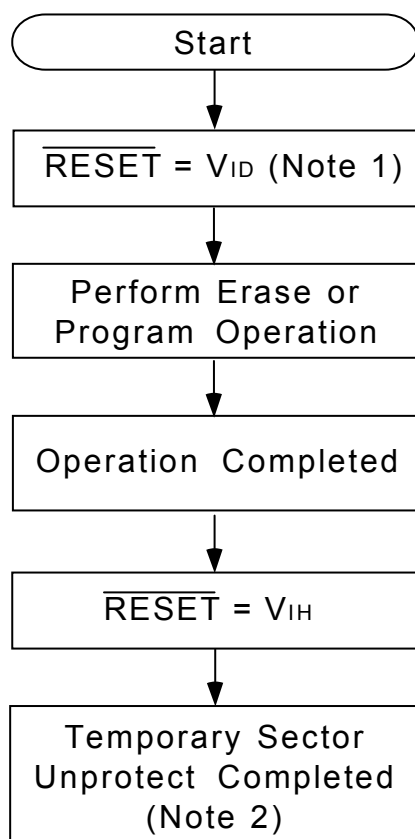
Notes:
 1. All protected sectors unprotected.
 2. All previously protected sectors are protected once again.

Output Disable Mode

With the $\overline{OE}$ is at a logic high level (V_{IH}), outputs from the devices are disabled. This will cause the output pins in a high impedance state

Standby Mode

When $\overline{CE}$ and $\overline{RESET}$ are both held at $V_{CC} \pm 0.3V$, the device enter CMOS Standby mode. If $\overline{CE}$ and $\overline{RESET}$ are held at V_{IH}, but not within the range of $V_{CC} \pm 03V$, t he device will still be in the standby mode, but the standby current will be larger.

If the device is deselected during auto algorithm of erasure or programming, the device draws active current I_{CC2} until the operation is completed. I_{CC3} in the DC Characteristics table represents the standby current specification.

The device requires standard access time (t_{CE}) for read access from either of these standby modes, before it is ready to read data.

Sector Protect / Un-protect Mode

The hardware sector protect feature disables both program and erase operations in any sector. The hardware sector unprotect feature re-enables both the program and erase operations in previously protected sectors. Sector protect/unprotect can be implemented via two methods.

The primary method requires V_{ID} on the $\overline{RESET}$ pin only, and can be implemented either in-system or via programming equipment.

Figure 16 shows the algorithms and Figure 15 shows the timing diagram. This method uses standard microprocessor bus cycle timing. For sector unprotect, all unprotected sectors must first be protected prior to the first sector unprotect write cycle.

The alternate method intended only for programming equipment requires V_{ID} on address pin A9, $\overline{OE}$, and $\overline{RESET}$.

Auto-select Mode

The auto-select mode provides manufacturer and device identification and sector protection verification, through outputs on DQ7–DQ0. This mode is primarily intended for programming equipment to automatically match a device to be programmed with its corresponding programming algorithm. However, the auto-select codes can also be accessed in-system through the command register.

When using programming equipment, this mode requires V_{ID} (10 V to 10.5 V) on address pin A9. While address pins A3, A2, A1, and A0 must be as shown in Table 4.

To verify sector protection, all necessary pins have to be set as required in Table 4, the programming equipment may then read the corresponding identifier code on DQ7-DQ0.

To access the auto-select codes in-system, the host system can issue the auto-select command via the command register, as shown in Table 5. This method does not require V_{ID}. See "Software Command Definitions" for details on using the auto-select mode.

7.2 Software Command Definitions

Writing specific address and data commands or sequences into the command register initiates the device operations. Table 5 defines the valid register command sequences. Writing incorrect address and data values or writing them in the improper sequence resets the device to reading array data.

All addresses are latched on the falling edge of $\overline{WE}$ or $\overline{CE}$, whichever happens later. All data is latched on the rising edge of $\overline{WE}$ or $\overline{CE}$, whichever happens first. Refer to the corresponding timing diagrams in the AC Characteristics section.

Table 5. F49L320UA/F49L320BA Software Command Definitions

Command Sequence		Cycles	Bus Cycle Note1~4											
			1st		2nd		3rd		4th		5th		6th	
			Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Read **Note** 5		1	RA	RD										
Reset **Note** 6		1	XXX	F0										
Autoselect **Note** 7 Manufacturer ID	Word	4	555	AA	2AA	55	555	90	X00	XX8C				
									X04	XX7F				
									X08	XX7F				
									X0C	XX7F				
	Byte		AAA		555		AAA		X00	8C				
									X04	7F				
									X08	7F				
									X0C	7F				
Device ID, F49L320UA	Word	4	555	AA	2AA	55	555	90	X01	22F6				
	Byte		AAA		555		AAA		X02	F6				
Device ID, F49L320BA	Word	4	555	AA	2AA	55	555	90	X01	22F9				
	Byte		AAA		555		AAA		X02	F9				
Secured Silicon Sector Factory Protect F49L320UA **Note** 8	Word	4	555	AA	2AA	55	555	90	X03	8D/0D				
	Byte		AAA		555		AAA		X06					
Secured Silicon Sector Factory Protect F49L320BA **Note** 8	Word	4	555	AA	2AA	55	555	90	X03	9D/1D				
	Byte		AAA		555		AAA		X06					
Sector Protect Verify **Note** 9	Word	4	555	AA	2AA	55	555	90	(SA) X02	XX00				
										XX01				
	Byte		AAA		555		AAA		(SA) X04	00				
										01				
Enter Secured Silicon Sector Region	Word	3	555	AA	2AA	55	555	88						
	Byte		AAA		555		AAA							
Exit Secured Silicon Sector Region	Word	4	555	AA	2AA	55	555	90	XXX	00				
	Byte		AAA		555		AAA							
CFI Query **Note** 10	Word	1	55	98										
	Byte		AA											
Program	Word	4	555	AA	2AA	55	555	A0	PA	PD				
	Byte		AAA		555		AAA							
Chip Erase	Word	6	555	AA	2AA	55	555	80	555	AA	2AA	55	555	10
	Byte		AAA		555		AAA		AAA		555		AAA	
Sector Erase	Word	6	555	AA	2AA	55	555	80	555	AA	2AA	55	SA	30
	Byte		AAA		555		AAA		AAA		555			
Erase Suspend **Note** 11		1	XXX	B0										
Erase Resume **Note** 12		1	XXX	30										

Legend:

X = Don't care

RA = Address of the memory location to be read.

RD = Data read from location RA during read operation.

PA = Address of the memory location to be programmed. Addresses latch on the falling edge of the WE# or CE# pulse, whichever happens later.

PD = Data to be programmed at location PA. Data latches on the rising edge of WE# or CE# pulse, whichever happens first. SA = Address of the sector to be verified (in autoselect mode) or erased. Address bits A20–A12 uniquely select any sector.

Notes:

1. All values are in hexadecimal.
2. Except for the read cycle and the fourth cycle of the autoselect command sequence, all bus cycles are write cycles.
3. Data bits DQ15–DQ8 are don't cares for unlock and command cycles.
4. Address bits A20–A11 are don't cares for unlock and command cycles, unless SA or PA required.
5. No unlock or command cycles required when reading array data.
6. The Reset command is required to return to reading array data when device is in the autoselect mode, or if DQ5 goes high (while the device is providing status data).
7. The fourth cycle of the autoselect command sequence is a read cycle.
8. For word mode data is 8Dh for factory locked and 0Dh for not factory locked. For byte mode data is 9Dh for factory locked and 1Dh for not factory locked.
9. The data is 00h for an unprotected sector and 01h for a protected sector. See " Autoselect Command Sequence" for more information.
10. Command is valid when device is ready to read array data or when device is in autoselect mode.
11. The system may read and program in non-erasing sectors, or enter the autoselect mode, when in the Erase Suspend mode. The Erase Suspend command is valid only during a sector erase operation.
12. The Erase Resume command is valid only during the Erase Suspend mode.

Reset Command

Writing the reset command to the device resets the device to reading array data. Address bits are all don't cares for this command.

The reset command may be written between the sequence cycles in an erase command sequence before erasing begins. This resets the device to reading array data. Once erasure begins, however, the device ignores reset commands until the operation is complete.

The reset command may be written between the sequence cycles in a program command sequence before programming begins. This resets the device to reading array data (also applies to programming in Erase Suspend mode). Once programming begins, however, the device ignores reset commands until the operation is complete.

The reset command may be written between the sequence cycles in an auto-select command sequence. Once in the auto-select mode, the reset command must be written to return to reading array data (also applies to auto-select during Erase Suspend).

If DQ5 goes high (see "DQ5: Exceeded Timing Limits" section) during a program or erase operation, writing the reset command returns the device to reading array data (also applies during Erase Suspend).

Read Command

The device is automatically set to reading array data after device power-up. No commands are required to retrieve data. The device is also ready to read array data after completing an Embedded Program or Embedded Erase algorithm.

When the device accepts an Erase Suspend command, the device enters the Erase Suspend mode. The system can read array data using the standard read timings, except that if it reads an address within erase-suspended sectors, the device outputs status data. After completing a programming operation in the Erase Suspend mode, the system may once again read array data with the same exception. See "Erase Suspend/Erase Resume Commands" for more information on this mode.

The system must issue the reset command to re-enable the device for reading array data if DQ5 goes high, or while in the auto-select mode. See the "Reset Command" section. See also the "Read Mode" in the "Device Operations section for more information. Refer to Figure 5 for the timing diagram.

Program Command

The program command sequence programs one byte into the device. Programming is a four-bus-cycle operation. The program command sequence is initiated by writing two unlock write cycles, followed by the program set-up command. The program address and data are written next, which in turn initiate the Embedded Program algorithm. The system is not required to provide further controls or timings. The device automatically provides internally generated program pulses and verifies the programmed cell margin.

When the Embedded Program algorithm is complete, the device then returns to reading array data and addresses are no longer latched. The system can determine the status of the program operation by using DQ7, DQ6, or RY/$\overline{BY}$. See "Write Operation Status" section for more information on these status bits.

Any commands written to the device during the Embedded Program Algorithm are ignored. Note that a hardware reset immediately terminates the programming operation. The Program command sequence should be reinitiated once the device has reset to reading array data, to ensure data integrity.

Programming is allowed in any sequence and across sector boundaries. A bit cannot be programmed from a "0" back to a "1". Attempting to do so may halt the operation and set DQ5 to "1", or cause the Data Polling algorithm to indicate the operation was successful. However, a succeeding read will show that the data is still "0". Only erase operations can convert a "0" to a "1".

Chip Erase Command

Chip erase is a six-bus cycle operation. The chip erase command sequence is initiated by writing two unlock cycles, followed by a set-up command. Two additional unlock write cycles are then followed by the chip erase command, which in turn invokes the Embedded Erase algorithm.

The device does not require the system to preprogram prior to erase. The Embedded Erase algorithm automatically preprograms and verifies the entire memory for an all zero data pattern prior to electrical erase.

Any commands written to the chip during the Embedded Erase algorithm are ignored. Note that a hardware reset during the chip erase operation immediately terminates the operation. The Chip Erase command sequence should be reinitiated once the device has returned to reading array data, to ensure the data integrity.

The system can determine the status of the erase operation by using DQ7, DQ6, DQ2, or RY/$\overline{BY}$. See "Write Operation Status" section for more Information on these status bits.

When the Embedded Erase algorithm is complete, the device returns to reading array data and addresses are no longer latched. See the Erase/Program Operations tables in "AC Characteristics" for parameters.

Sector Erase Command

Sector erase is a six-bus cycle operation. The sector erase command sequence is initiated by writing two unlock cycles, followed by a set-up command. Two additional unlock write cycles are then followed by the address of the sector to be erased, and the sector erase command.

The device does not require the system to preprogram the memory prior to erase. The Embedded Erase algorithm automatically programs and verifies the sector for an all zero data pattern prior to electrical erase. The system is not required to provide any controls or timings during these operations.

After the command sequence is written, a sector erase time-out of 50μ s begins. Driving the time-out period, additional sector addresses and sector erase commands may be written. Loading the sector erase buffer may be done in any sequence, and the number of sectors may be from one sector to all sectors. The time between these additional cycles must be less than 50　 s, otherwise the last address and command might not be accepted, and erasure may begin.

It is recommended that processor interrupts be disabled during this time to ensure all commands are accepted. The interrupts can be re-enabled after the last Sector Erase command is written. If the time between additional sector erase commands can be assumed to be less than 50 μ s, the system need not monitor DQ3.

Any command other than Sector Erase or Erase Suspend during the time-out period resets the device to reading array data. The system must rewrite the command sequence and any additional sector addresses and commands.

The system can monitor DQ3 to determine if the sector erase timer has timed out. (See the "DQ3: Sector Erase Timer" section.) The time-out begins from the rising edge of the final $\overline{WE}$ pulse in the command sequence.

Once the sector erase operation has begun, only the Erase Suspend command is valid. All other commands are ignored. Note that a hardware reset during the sector erase operation immediately terminates the operation. The Sector Erase command sequence should be reinitiated once the device has returned to reading array data, to ensure the data integrity.

When the Embedded Erase algorithm is complete, the device returns to reading array data and addresses are no longer latched. The system can determine the status of the erase operation by using DQ7, DQ6, DQ2, or RY/$\overline{BY}$. (Refer to "Write Operation Status" section for more information on these status bits.)

Refer to the Erase/Program Operations tables in the "AC Characteristics" section for parameters.

Sector Erase Suspend/Resume Command

The Erase Suspend command allows the system to interrupt a sector erase operation and then read data from, or program data to, any sector not selected for erasure (The device " erase suspends" all sect or selected for erasure.). This command is valid only during the sector erase operation, including the 50 μs time-out period during the sector erase command sequence. The Erase Suspend command is ignored if written during the chip erase operation or Embedded Program algorithm. Addresses are "don't -cares" when writing the Erase Suspend command as shown in Table 5.

When the Erase Suspend command is written during a sector erase operation, the device requires a maximum of 20μs to suspend the erase operation. However, when the Erase Suspend command is written during the sector erase time-out, the device immediately terminates the time-out period and suspends the erase operation.

Reading at any address within erase-suspended sectors produces status data on DQ7–DQ0. The system can use DQ7, or DQ6 and DQ2 together, to determine if a sector is actively erasing or is erase-suspended. See "Write Operation Status" section for more information on these status bits.

After an erase-suspended program operation is complete, the system can once again read array data within non-suspended sectors. The system can determine the status of the program operation using the DQ7 or DQ6

status bits, just as in the standard program operation. See "Write Operation Status" f or more information.

The system may also write the auto-select command sequence when the device is in the Erase Suspend mode. The device allows reading auto-select codes even at addresses within erasing sectors, since the codes are not stored in the memory array. When the device exits the auto-select mode, the device reverts to the Erase Suspend mode, and is ready for another valid operation.

After an erase-suspended program operation is complete, the system can once again read array data within non-suspended sectors. The system can determine the status of the program operation using the DQ7 or DQ6 status bits, just as in the standard program operation. See "Write Operation Status" f or more information.

The system may also write the auto-select command sequence when the device is in the Erase Suspend mode. The device allows reading auto-select codes even at addresses within erasing sectors, since the codes are not stored in the memory array. When the device exits the auto-select mode, the device reverts to the Erase Suspend mode, and is ready for another valid operation.

The system must write the Erase Resume command (address bits are "don't care" as shown in Table 5) to exit the erase suspend mode and continue the sector erase

operation. Further writes of the Resume command are ignored. Another Erase Suspend command can be written after the device has resumed erasing.

Auto-select Command

The auto-select command sequence allows the host system to access the manufacturer and devices codes, and determine whether or not a sector is protected. Table 6 shows the address and data requirements. This method is an alternative to that shown in Table 4, which is intended for PROM programmers and requires V_{ID} on address bit A9.

The auto-select command sequence is initiated by writing two unlock cycles, followed by the auto-select command. The device then enters the auto-select mode, and the system may read at any address any number of times, without initiating another command sequence. The read cycles at address 04H, 08H, 0CH, and 00H retrieves the ESMT manufacturer ID. A read cycle at address 01H retrieves the device ID. A read cycle containing a sector address(SA) and the address 02H returns 01H if that sector is protected, or 00H if it is unprotected. Refer to Tables 1 and 2 for valid sector addresses.

The system must write the reset command to exit the auto-select mode and return to reading array data.

7.3 Write Operation Status

The device provides several bits to determine the status of a write operation: RY/$\overline{BY}$, DQ7, DQ6, DQ5, DQ3, DQ2, and. Table 7 and the following subsections describe the functions of these bits.

RY/$\overline{BY}$, DQ7, and DQ6 each offer a method for determining whether a program or erase operation is complete or in progress.

Table 7. Write Operation Status

			DQ7 (Note1)	DQ6	DQ5 (Note2)	DQ3	DQ2	RY/$\overline{BY}$
In Progress	Embedded Program Algorithm		$\overline{DQ7}$	Toggle	0	N/A	No Toggle	0
	Embedded Erase Algorithm		0	Toggle	0	1	Toggle	0
	Erase Suspended Mode	Reading Erase Suspended Sector	1	No Toggle	0	N/A	Toggle	1
		Reading Non-Erase Suspended Sector	Data	Data	Data	Data	Data	1
		Erase Suspend Program	$\overline{DQ7}$	Toggle	0	N/A	N/A	0
Exceeded Time Limits	Embedded Program Algorithm		$\overline{DQ7}$	Toggle	1	N/A	No Toggle	0
	Embedded Erase Algorithm		0	Toggle	1	1	Toggle	0
	Erase Suspend Program		$\overline{DQ7}$	Toggle	1	N/A	N/A	0

Notes:
1. DQ7 and DQ2 require a valid address when reading status information. Refer to the appropriate subsection for further details.
2. DQ5 switches to '1' when an Embedded Program or Embedded Erase operation has exceeded the maximum timing limits. See "DQ5: Exceeded Timing Limits" for more information.

RY/$\overline{BY}$:
Ready/Busy

The RY/$\overline{BY}$ is a dedicated, open-drain output pin that indicates whether an Embedded Algorithm is in progress or complete. The RY/$\overline{BY}$ status is valid after the rising edge of the final $\overline{WE}$ pulse in the command sequence. Since RY/$\overline{BY}$ is an open-drain output, several RY/$\overline{BY}$ pins can be tied together in parallel with a pull-up resistor to V$_{CC}$.

If the output is low (Busy), the device is actively erasing or programming. (This includes programming in the Erase Suspend mode.) If the output is high (Ready), the device is ready to read array data (including during the Erase Suspend mode), or is in the standby mode. Table 7 shows the outputs for RY/$\overline{BY}$.

DQ7: Data Polling

The DQ7 indicates to the host system whether an Embedded Algorithm is in progress or completed, or whether the device is in Erase Suspend mode. The Data Polling is valid after the rising edge of the final $\overline{WE}$ pulse in the program or erase command sequence.

During the Embedded Program algorithm, the device outputs on DQ7 the complement of the datum programmed to DQ7. This DQ7 status also applies to programming during Erase Suspend. When the Embedded Program algorithm is complete, the device outputs the true data on DQ7. The system must provide the program address to read valid status information on DQ7. If a program address falls within a protected sector, Data Polling on DQ7 is active for approximately 1 µs, then the device returns to reading array data.

During the Embedded Erase algorithm, Data Polling produces a "0" on DQ7. When the Embedded Erase algorithm is complete, or if the device enters the Erase Suspend mode, Data Polling produces a "1" on DQ7. The system must provide an address within any of the sectors selected for erasure to read valid status information on DQ7.

After an erase command sequence is written, if all sectors selected for erasing are protected, Data Polling on DQ7 is active for approximately 100 µs, then the device returns to reading array data. If not all selected sectors are protected, the Embedded Erase algorithm erases the unprotected sectors, and ignores the selected sectors that are protected.

When the system detects DQ7 has changed from the complement to true data, it can read valid data at DQ7~ DQ0 on the following read cycles. This is because DQ7 may change asynchronously with DQ0–DQ6 while

Output Enable ($\overline{OE}$) is asserted low. Refer to Figure 21, Data Polling Timings (During Embedded Algorithms), Figure 19 shows the Data Polling algorithm.

DQ6:Toggle BIT I

Toggle Bit I on DQ6 indicates whether an Embedded Program or Erase algorithm is in progress or complete, or whether the device has entered the Erase Suspend mode. Toggle Bit I may be read at any address, and is valid after the rising edge of the final $\overline{WE}$ pulse in the command sequence (prior to the program or erase operation), and during the sector erase time-out.

During an Embedded Program or Erase algorithm operation, successive read cycles to any address cause DQ6 to toggle. The system may use either $\overline{OE}$ or $\overline{CE}$ to control the read cycles. When the operation is complete, DQ6 stops toggling.

When an erase command sequence is written, if all sectors selected for erasing are protected, DQ6 toggles for approximately 100 µs, then returns to reading array data. If not all selected sectors are protected, the Embedded Erase algorithm erases the unprotected sectors, and ignores the selected sectors that are protected.

The system can use DQ6 and DQ2 together to determine whether a sector is actively erasing or is erase-suspended. When the device is actively erasing (i.e. the Embedded Erase algorithm is in progress), DQ6 toggles. When the device enters the Erase Suspend mode, DQ6 stops toggling. However, the system must also use DQ2 to determine which sectors are erasing or erase-suspended. Alternatively, the system can use DQ7.

If a program address falls within a protected sector, DQ6 toggles for approximately 2µs after the program command sequence is written, then returns to reading array data.

DQ6 also toggles during the erase-suspend-program mode, and stops toggling once the Embedded Program algorithm is complete. Table 7 shows the outputs for Toggle Bit I on DQ6. Figure 20 shows the toggle bit algorithm. Figure 22 shows the toggle bit timing diagrams. Figure 25 shows the differences between DQ2 and DQ6 in graphical form. Refer to the subsection on DQ2: Toggle Bit II.

DQ2: Toggle Bit II

The "Toggle Bit II" on DQ2, when used with DQ6, indicates whether a particular sector is actively erasing (that is, the Embedded Erase algorithm is in progress), or whether that sector is erase-suspended. Toggle Bit II is valid after the rising edge of the final or $\overline{CE}$, whichever happens first, in the command sequence.

DQ2 toggles when the system reads at addresses within those sectors that have been selected for erasure. (The system may use either $\overline{OE}$ or $\overline{CE}$ to control the read cycles.) But DQ2 cannot distinguish whether the sector is actively erasing or is erase-suspended.

DQ6, by comparison, indicates whether the device is actively erasing, or whether is in erase-suspended, but cannot distinguish which sectors are selected for erasure. Thus, both status bits are required for sector and mode information. Refer to Table 7 to compare outputs for DQ2 and DQ6.

Figure 20 shows the toggle bit algorithm in flowchart form. See also the DQ6: Toggle Bit I subsection. Figure 22 shows the toggle bit timing diagram. Figure 25 shows the differences between DQ2 and DQ6 in graphical form.

Reading Toggle Bits DQ6/ DQ2

Refer to Figure 20 for the following discussion. Whenever the system initially begins reading toggle bit status, it must read DQ7–DQ0 at least twice in a row to determine whether a toggle bit is toggling. Typically, the system would note and store the value of the toggle bit after the first read. After the second read, the system would compare the new value of the toggle bit with the first. If the toggle bit is not toggling, the device has completed the program or erase operation. The system can read array data on DQ7–DQ0 on the following read cycle.

However, if after the initial two read cycles, the system determines that the toggle bit is still toggling, the system should note whether the value of DQ5 is high (see the section on DQ5). If it is, the system should then determine again whether the toggle bit is toggling, since the toggle bit may have stopped toggling just as DQ5 went high. If the toggle bit is no longer toggling, the device has successfully completed the program or erase operation. If it is still toggling, the device did not completed the operation successfully, and the system must write the reset command to return to reading array data.

The remaining scenario is that the system initially determines that the toggle bit is toggling and DQ5 has not gone high. The system may continue to monitor the toggle bit and DQ5 through successive read cycles, determining the status as described earlier. Alternatively, it may choose to perform other system tasks. In this case, the system must start at the beginning of the algorithm when it returns to determine the status of the operation.

DQ5: Exceeded Timing Limits

DQ5 indicates whether the program or erase time has

exceeded the specified limits(internal pulse count). Under these conditions DQ5 will produce a "1". This time-out condition indicates that the program or erase cycle was not successfully completed. Data Polling and Toggle Bit are the only operating functions of the device under this condition.
If this time-out condition occurs during sector erase operation, it specifies that a particular sector is bad and it may not be reused. However, other sectors are still functional and may be used for the program or erase operation. The device must be reset to use other sectors. Write the Reset command sequence to the device, and then execute program or erase command sequence. This allows the system to continue to use the other active sectors in the device.

If this time-out condition occurs during the chip erase operation, it specifies that the entire chip is bad or combination of sectors are bad.

If this time-out condition occurs during the programming operation, it specifies that the sector containing that byte is bad and this sector may not be reused, however other sectors are still functional and can be reused.

The time-out condition will not appear if a user tries to program a non blank location without erasing. Please note that this is not a device failure condition since the device was incorrectly used.

DQ3:Sector Erase Timer

After writing a sector erase command sequence, the system may read DQ3 to determine whether or not an erase operation has begun. (The sector erase timer does not apply to the chip erase command.) If additional sectors are selected for erasure, the entire timeout also applies after each additional sector erase command.
When the time-out is complete, DQ3 switches from " 0" to " 1." If the time between additional sector erase commands from the system can be assumed to be less than 50 μ s, the system need not monitor DQ3.

When the sector erase command sequence is written, the system should read the status on DQ7 (Data Polling) or DQ6 (Toggle Bit I) to ensure the device has accepted the command sequence, and then read DQ3. If DQ3 is " 1", the internally controlled erase cycle has begun; all further commands (except Erase Suspend) are ignored until the erase operation is complete.

If DQ3 is " 0", the device will accept additional sector erase commands. To ensure the command has been accepted, the system software should check the status of DQ3 prior to and following each subsequent sector erase command. If DQ3 is high on the second status check, the last command might not have been accepted. Table 7 shows the outputs for DQ3.
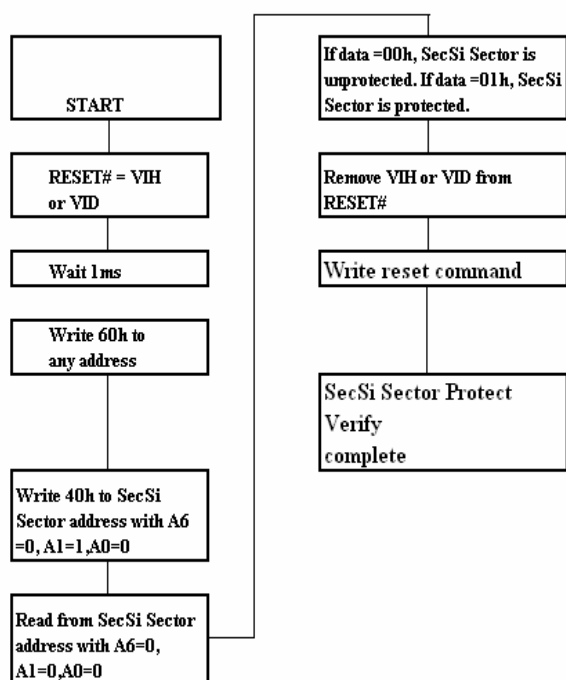
Customer Lockable : Secured Silicon Sector NOT Programmed or Protected at the Factory

The customer lockable version allows the Secured Silicon Sector to be programmed once, and then permanently locked after it ships. Note that the accelerated programming (ACC) is not available when programming the Secured Silicon Sector.

The Secured Silicon Sector area can be protected using the following procedures:

■ Write the three-cycle Enter Secured silicon Region command sequence, and then follow the in-system sector protect algorithm as shown in Figure 16. of page41, except that RESET# may be either VIH or VID. This allows in system protection of the Secured Silicon Sector without raising any device pin to a high voltage. Note that this method is only applicable to the Secured silicon Sector.

■ To verify the protect/unprotect status of the Secured Silicon Sector, follow the algorithm shown in below table.

Once the Secured Silicon Sector protection must be used with caution since, once protected, there is no procedure available for unprotecting the Secured silicon Sector area, and none of the bits in the Secured Silicon Sector memory space can be modified in any way.

Factory Locked : Secured Silicon Sector Programmed and Protected at the Factory

The Secured Silicon Sector feature provides a 256 –byte Flash memory region that enables permanent part identification through an Electronic Serial Number (ESN). The Secured Silicon Sector uses a Secured Silicon Sector Indicator Bit (DQ7) to indicate whether or not the Secured Silicon Sector is locked when shipped from the factory. Factory Locked version the Bit(DQ7) set to 1, Customer Lockable version the Bit (DQ7) set to 0.

In a factory locked device, the Secured Silicon Sector cannot be modified in any way. The device is available pre-programmed with one of the following:

1. A random, secure ESN only.
2. Customer code through the Express Flash service.
3. Both a random, secure ESN and customer code through the Express Flash device.

In device that have an ESN, a Bottom Boot device has the 16-byte (8-word) ESN in sector 0 at address 00000H-0000FH in byte mode(or 00000H~00007H in word mode).In the Top Boot device, the ECN is in sector 70 at addresses 3FFF00h-3FFF0Fh in byte mode (or 1FFF80h-1FFF87h in word mode). In the uniform device, the ESN is in sector 63 at addresses 3FFF00h-3FFF0Fh in byte mode (or 1FFF80h-1FFF87h in word mode).

Customers may opt to have their code programmed by ESMT through the Express-Flash service. ESMT programs the customer's code, with or without the random ESN. The devices are then shipped from the ESMT factory with the Secured Silicon Sector locked.

Note:

1. After entering Secured Silicon Sector mode, user can program Secured Silicon Sector (means to write ESN code) and do Secured Silicon Sector protection once when device is customer lockable version.

2. Enter Secured Silicon Sector mode, the under functions are not allowed except for CFI.
   a. Sector Erase/Erase Suspend/Resume.
   b. Chip Erase.

3. Secured Silicon Sector mode doesn't have "Erase" and "Unprotect" function.

Word mode Secured Silicon Sector Addresses

Sector Address A20~12	Sector Size (bytes/words)	(x8) Address Range	(x16) Address Range
111111111	256/128	3FFF00h-3FFFFFh	1FFF80h-1FFFFFh

Byte mode Secured Silicon Sector Addresses

Sector Address A20~12	Sector Size (bytes/words)	(x8) Address Range	(x16) Address Range
000000000	256/128	000000h-0000FFh	000000h-00007Fh

7.4 More Device Operations

Hardware Data Protection

The command sequence requirement of unlock cycles for programming or erasing provides data protection against inadvertent writes. In addition, the following hardware data protection measures prevent accidental erasure or programming, which might otherwise be caused by spurious system level signals during V_{CC} power-up and power-down transitions, or from system noise.

Low V_{CC} Write Inhibit

When V_{CC} is less than V_{LKO}, the device does not accept any write cycles. This protects data during V_{CC} power-up and power-down. The command register and all internal program/erase circuits are disabled, and the device resets. Subsequent writes are ignored until V_{CC} is greater than V_{LKO}. The system must provide the proper signals to the control pins to prevent unintentional writes when V_{CC} is greater than V_{LKO}.

Write Pulse "Glitch" Protection

Noise pulses of less than 5 ns (typical) on $\overline{CE}$ or $\overline{WE}$ do not initiate a write cycle.

Logical Inhibit

Write cycles are inhibited by holding any one of $\overline{OE}$ = V_{IL}, $\overline{CE}$ = V_{IH} or $\overline{WE}$ = V_{IH}. To initiate a write cycle, $\overline{CE}$ and $\overline{WE}$ must be a logical zero while $\overline{OE}$ is a logical one.

Power Supply Decoupling

In order to reduce power switching effect, each device should have a 0.1uF ceramic capacitor connected between its V_{CC} and GND.

Power-Up Sequence

The device powers up in the Read Mode. In addition, the memory contents may only be altered after successful completion of the predefined command sequences.

Power-Up Write Inhibit

If $\overline{WE}$ = $\overline{CE}$ = V_{IL} and $\overline{OE}$ = V_{IH} during power up, the device does not accept commands on the rising edge of $\overline{WE}$. The internal state machine is automatically reset to reading array data on power-up.

COMMON FLASH MEMORY INTERFACE (CFI)

The Common Flash Interface (CFI) specification outlines device and host system software interrogation handshake, which allows specific vendor-specified software algorithms to be used for entire families of devices. Software support can then be device-independent, JEDEC ID-independent, and forward- and backward- compatible for the specified flash device families. Flash vendors can standardize their existing interfaces for long-term compatibility.

This device enters the CFI Query mode when the system writes the CFI Query command, 98h, to address 55h in word mode (or address AAh in byte mode), any time the device is ready to array data. The system can read CFI information at the address given in Tables 8-10 in word mode, the upper address bits (A7-MSB) must be all zeros. To terminate reading CFI data, the system must write the reset command.

The system can also write the CFI query command when the device is in the autoselect mode. The device enters the CFI query mode, and the system can read CFI data at the addresses given in Tables 8-10. The system must write the reset command to return the device to the autoselect mode.

Table 8 CFI Query Identification String

Addresses (Word Mode)	Address (Byte Mode)	Data	Description
10h 11h 12h	20h 22h 24h	0051h 0052h 0059h	Query Unique ASCII string "QRY"
13h 14h	26h 28h	0002h 0000h	Primary OEM Command Set
15h 16h	2Ah 2Ch	0040h 0000h	Address for Primary Extended Table
17h 18h	2Eh 30h	0000h 0000h	Alternate OEM Command Set (00h = none exists)
19h 1Ah	32h 34h	0000h 0000h	Address for Alternate OEM Extended Table (00h = none exists)

Table 9 System Interface String

Addresses (Word Mode)	Address (Byte Mode)	Data	Description
1Bh	36h	0027h	V_{CC} Min. (write/erase) D7~D4 : volt, D3~D0 : 100 millivolt
1Ch	38h	0036h	V_{CC} Max. (write/erase) D7~D4 : volt, D3~D0 : 100 millivolt
1Dh	3Ah	0000h	V_{PP} Min. voltage (00h = no V_{PP} pin present)
1Eh	3Ch	0000h	V_{PP} Max. voltage (00h = no V_{PP} pin present)
1Fh	3Eh	0004h	Typical timeout per single byte/word write 2^N μs
20h	40h	0000h	Typical timeout for Min. size buffer write 2^N μs (00h = not supported)
21h	42h	000Ah	Typical timeout per individual block erase 2^N ms
22h	44h	0000h	Typical timeout for full chip erase 2^N ms (00h = not supported)
23h	46h	0005h	Max. timeout for byte/word write 2^N word times typical
24h	48h	0000h	Max. timeout for buffer write 2^N word times typical
25h	4Ah	0004h	Max. timeout per individual block erase 2^N word times typical
26h	4Ch	0000h	Max. timeout per full chip erase 2^N word times typical (00h = not supported)

Table 10 Device Geometry Definition

Addresses (Word Mode)	Address (Byte Mode)	Data	Description
27h	4Eh	0016h	Device Size = 2^N byte
28h 29h	50h 52h	0002h 0000h	Flash Device Interface description (refer to CFI publication 100)
2Ah 2Bh	54h 56h	0000h 0000h	Max. number of byte in multi-byte write = 2^N (00h = not supported)
2Ch	58h	0002h	Number of Erase Block Regions within device
2Dh 2Eh 2Fh 30h	5Ah 5Ch 5Eh 60h	0007h 0000h 0020h 0000h	Erase Block Region 1 Information (refer to the CFI specification or CFI publication 100)
31h 32h 33h 34h	62h 64h 66h 68h	003Eh 0000h 0000h 0001h	Erase Block Region 2 Information
35h 36h 37h 38h	6Ah 6Ch 6Eh 70h	0000h 0000h 0000h 0000h	Erase Block Region 3 Information
39h 3Ah 3Bh 3Ch	72h 74h 76h 78h	0000h 0000h 0000h 0000h	Erase Block Region 4 Information

Table 11 Primary Vendor-Specific Extended Query

Addresses (Word Mode)	Address (Byte Mode)	Data	Description
40h 41h 42h	80h 82h 84h	0050h 0052h 0049h	Query-unique ASCII string " PRI"
43h	86h	0031h	Major version number, ASCII
44h	88h	0031h	Minor version number, ASCII
45h	8Ah	0000h	Address Sensitive Unlock 0 = Required, 1 = Not Required
46h	8Ch	0002h	Erase Suspend 0 = Not Supported, 1 = To Read Only, 2 = To Read & Write
47h	8Eh	0001h	Erase Protect 0 = Not Supported, X = Number of sectors in per group
48h	90h	0001h	Sector Temporary Unprotect 00 = Not Supported, 01 = Supported
49h	92h	0004h	Sector Protect/Group Unprotect scheme
4Ah	94h	0000h	Simultaneous Operation 00 = Not Supported, 01 = Supported
4Bh	96h	0000h	Burst Mode Type 00 = Not Supported, 01 = Supported
4Ch	98h	0000h	Page Mode Type 00 = Not Supported, 01 = 4 Word Page, 02 = 8 Word Page
4Dh	9Ah	00B5h	ACC (Acceleration) Supply Minimum 00h = Not Supported, D7-D4 : Volt, D3-D0 : 100mV
4Eh	9Ch	00C5h	ACC (Acceleration) Supply Maximum 00h = Not Supported, D7-D4 : Volt, D3-D0 : 100mV
4Fh	9Eh	000Xh	Top / Bottom Boot Sector Flag (02h = Bottom Boot device, 03h = Top Boot Device)

8. ABSOLUTE MAXIMUM RATINGS

Storage Temperature

Plastic Packages . . . . –65°C to +150°C

Ambient Temperature

with Power Applied. . . . . –65°C to +125°C

Voltage with Respect to Ground

V_{CC} (Note 1) . . . . –0.5 V to +4.0 V

A9, $\overline{OE}$, and $\overline{RESET}$ (Note 2) . . . –0.5 V to +10.5V

All other pins (Note 1). . . . . –0.5 V to V_{CC} +0.5 V

Output Short Circuit Current (Note 3) .. . .. 200 mA

Notes:

1. Minimum DC voltage on input or I/O pins is –0.5 V. During voltage transitions, input or I/O pins may overshoot V_{SS} to –2.0 V for periods of up to 20 ns. See Figure 1. Maximum DC voltage on input or I/O pins is V_{CC} +0.5 V. During voltage transitions, input or I/O pins may overshoot to V_{CC} +2.0 V for periods up to 20 ns. See Figure 2.

2. Minimum DC input voltage on pins A9, $\overline{OE}$, and $\overline{RESET}$ is -0.5 V. During voltage transitions, A9, $\overline{OE}$, and $\overline{RESET}$ may overshoot V_{SS} to –2.0 V for periods of up to 20 ns. See Figure 1. Maximum DC input voltage on pin A9 is +10.5V which may overshoot to 14V periods up to 20 ns.

3. No more than one output may be shorted to ground at a time. Duration of the short circuit should not be greater than one second.

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this data sheet is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.

Figure 1. Maximum Negative Overshoot Waveform
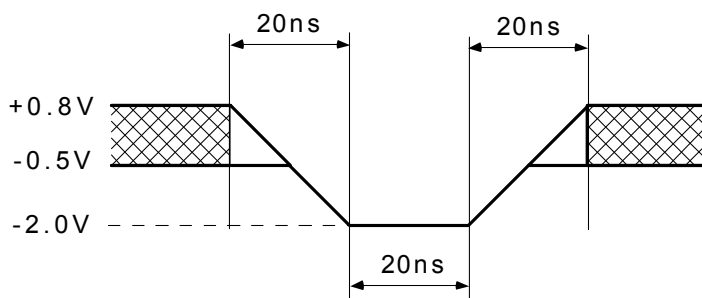
Figure 2. Maximum Positive Overshoot Waveform
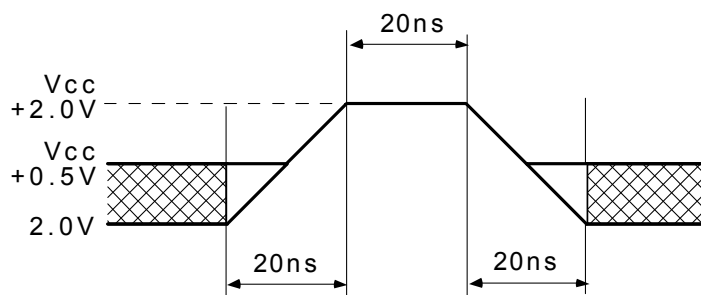
OPERATING RANGES

Commercial (C) Devices Ambient Temperature (TA) . . . . 0 °C to +70°C

V_CC Supply Voltages V_{CC} for all devices . . . . .2.7 V to 3.6 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

Table 12. Capacitance T_A = 25°C , f = 1.0 MHz

Symbol	Description	Conditions	Min.	Typ.	Max.	Unit
C_{IN1}	Input Capacitance	V_{IN} = 0V			8	pF
C_{IN2}	Control Pin Capacitance	V_{IN} = 0V			12	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V			12	pF

9. DC CHARACTERISTICS

Table 13. DC Characteristics T_A = 0°C to 70°C, V_{CC} = 2.7V to 3.6V

Symbol	Description	Conditions		Min.	Typ.	Max.	Unit
I_{LI}	Input Leakage Current	V_{IN} = V_{SS} or V_{CC}, V_{CC} = V_{CC} max.				± 1	uA
I_{LIT}	A9 Input Leakage Current	V_{CC} = V_{CC} max; A9=10.5V				35	uA
I_{LO}	Output Leakage Current	V_{OUT} = V_{SS} or V_{CC}, V_{CC} = V_{CC} max				± 1	uA
I_{CC1}	V_{CC} Active Read Current	$\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IH} (Byte Mode)	@5MHz		9	25	mA
			@1MHz		2	5	mA
		$\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IH} (Word Mode)	@5MHz		9	40	mA
			@1MHz		2	5	mA
I_{CC2}	V_{CC} Active write Current	$\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IH}			20	50	mA
I_{CC3}	V_{CC} Standby Current	$\overline{CE}$; $\overline{RESET}$ = $V_{CC} \pm$ 0.3V			25	100	uA
I_{CC4}	V_{CC} Standby Current During Reset	$\overline{RESET}$ = $V_{SS} \pm$ 0.3V			25	100	uA
I_{CC5}	Automatic sleep mode	V_{IH} = $V_{CC} \pm$ 0.3V; V_{IL} = $V_{SS} \pm$ 0.3V			25	100	uA
V_{IL}	Input Low Voltage(Note 1)			-0.5		0.8	V
V_{IH}	Input High Voltage			0.7x V_{CC}		V_{CC} + 0.3	V
V_{ID}	Voltage for Auto-Select and Temporary Sector Unprotect	V_{CC} =3.3V		10		10.5	V
V_{OL}	Output Low Voltage	I_{OL} = 4.0mA, V_{CC} = V_{CC} min				0.45	V
V_{OH1}	Output High Voltage(TTL)	I_{OH} = -2mA, V_{CC} = V_{CC} min		0.7x V_{CC}			
V_{OH2}	Output High Voltage	I_{OH} = -100uA, V_{CC} min		V_{CC} -0.4			
V_{LKO}	Low V_{CC} Lock-out Voltage			2.3		2.5	V

Notes :

    1. V_{IL} min. = -1.0V for pulse width is equal to or less than 50 ns.

       V_{IL} min. = -2.0V for pulse width is equal to or less than 20 ns.

    2. V_{IH} max. = V_{CC} + 1.5V for pulse width is equal to or less than 20 ns

       If V_{IH} is over the specified maximum value, read operation cannot be guaranteed.

    3. Automatic sleep mode enable the low power mode when addresses remain stable for t_{ACC} + 30 ns

10. AC CHARACTERISTICS
TEST CONDITIONS
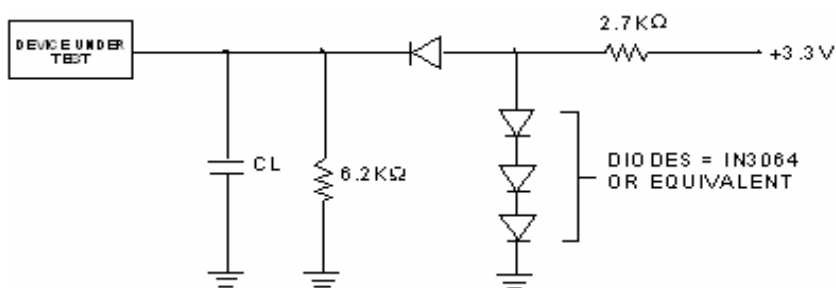
CL = 100pF Including jig capacitance

Figure 3. Test Setup

Figure 4. Input Waveforms and Measurement Levels
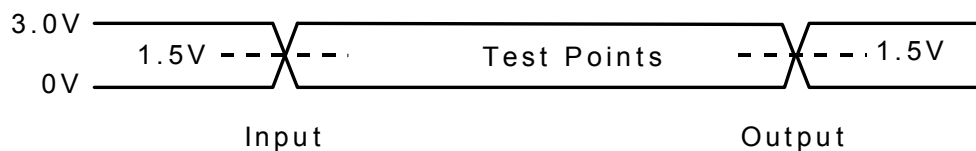
AC TESTING : Inputs are driven at 3.0V for a logic "1" and 0V for a logic "0"
Input pulse rise and fall times are < 5ns.

10.1 Read Operation
TA = 0°C to 70°C, V_{CC} = 2.7V~3.6V

Table 14. Read Operations

Symbol	Description		Conditions	-70		-90		Unit
				Min.	Max.	Min.	Max.	
t_{RC}	Read Cycle Time (Note 1)			70		90		ns
t_{ACC}	Address to Output Delay		$\overline{CE} = \overline{OE} = V_{IL}$		70		90	ns
t_{CE}	$\overline{CE}$ to Output Delay		$\overline{OE} = V_{IL}$		70		90	ns
t_{OE}	$\overline{OE}$ to Output Delay		$\overline{CE} = V_{IL}$		30		35	ns
t_{DF}	$\overline{OE}$ High to Output Float (Note1)		$\overline{CE} = V_{IL}$		25		30	ns
t_{OEH}	Output Enable	Read		0		0		ns
	Hold Time	Toggle and Data Polling		10		10		ns
t_{OH}	Address to Output hold		$\overline{CE} = \overline{OE} = V_{IL}$	0		0		ns

Notes :
1. Not 100% tested.
2. t_{DF} is defined as the time at which the output achieves the open circuit condition and data is no longer driven.

Figure 5. Read Timing Waveform
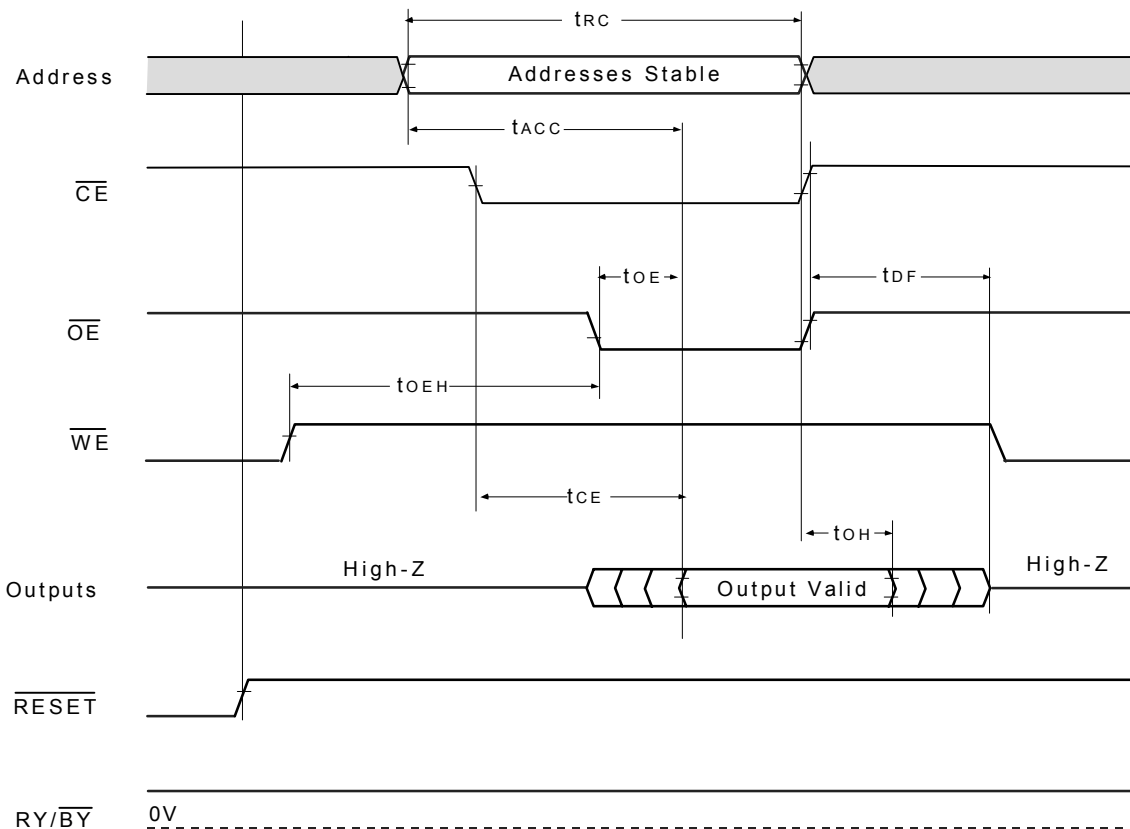
10.2 Program/Erase Operation

Table 15. $\overline{WE}$ Controlled Program/Erase Operations($T_A = 0°C$ to $70°C$, $V_{CC} = 2.7V\sim3.6V$)

Symbol	Description		-70 Min.	-70 Max.	-90 Min.	-90 Max.	Unit
t_{WC}	Write Cycle Time (Note 1)		**70**		**90**		ns
t_{AS}	Address Setup Time		0		0		ns
t_{AH}	Address Hold Time		45		45		ns
t_{DS}	Data Setup Time		35		45		ns
t_{DH}	Data Hold Time		0		0		ns
t_{OES}	Output Enable Setup Time		0		0		ns
t_{GHWL}	Read Recovery Time Before Write ($\overline{OE}$ High to $\overline{WE}$ low)		0		0		ns
t_{CS}	$\overline{CE}$ Setup Time		0		0		ns
t_{CH}	$\overline{CE}$ Hold Time		0		0		ns
t_{WP}	Write Pulse Width		35		35		ns
t_{WPH}	Write Pulse Width High		30		30		ns
t_{WHWH1}	Programming Operation (Note 2)	Byte	9(typ.)		9(typ.)		us
		Word	11(typ.)		11(typ.)		
t_{WHWH2}	Sector Erase Operation (Note 2)		0.7(typ.)		0.7(typ.)		sec
t_{VCS}	V_{CC} Setup Time (Note 1)		50		50		us
t_{RB}	Recovery Time from RY/$\overline{BY}$		0		0		ns
t_{busy}	Program/Erase Valid to RY/$\overline{BY}$ Delay		90		90		ns

Notes :
1. Not 100% tested.
2. See the "Erase and Programming Performance" section for more information.

Table 16. $\overline{CE}$ Controlled Program/Erase Operations(T_A = 0°C to 70°C, V_{CC} = 2.7V~3.6V)

Symbol	Description		-70 Min.	-70 Max.	-90 Min.	-90 Max.	Unit
t_{WC}	Write Cycle Time (Note 1)		70		90		ns
t_{AS}	Address Setup Time		0		0		ns
t_{AH}	Address Hold Time		45		45		ns
t_{DS}	Data Setup Time		35		45		ns
t_{DH}	Data Hold Time		0		0		ns
t_{OES}	Output Enable Setup Time		0		0		ns
t_{GHEL}	Read Recovery Time Before Write		0		0		ns
t_{WS}	$\overline{WE}$ Setup Time		0		0		ns
t_{WH}	$\overline{WE}$ Hold Time		0		0		ns
t_{CP}	$\overline{CE}$ Pulse Width		35		35		ns
t_{CPH}	$\overline{CE}$ Pulse Width High		30		30		ns
t_{WHWH1}	Programming Operation(note2)	Byte	9(typ.)		9(typ.)		us
		Word	11(typ.)		11(typ.)		us
t_{WHWH2}	Sector Erase Operation (note2)		0.7(typ.)		0.7(typ.)		sec

Notes :

1. Not 100% tested.
2. See the "Erase and Programming Performance" section for more information.

Figure 6. Write Command Timing Waveform
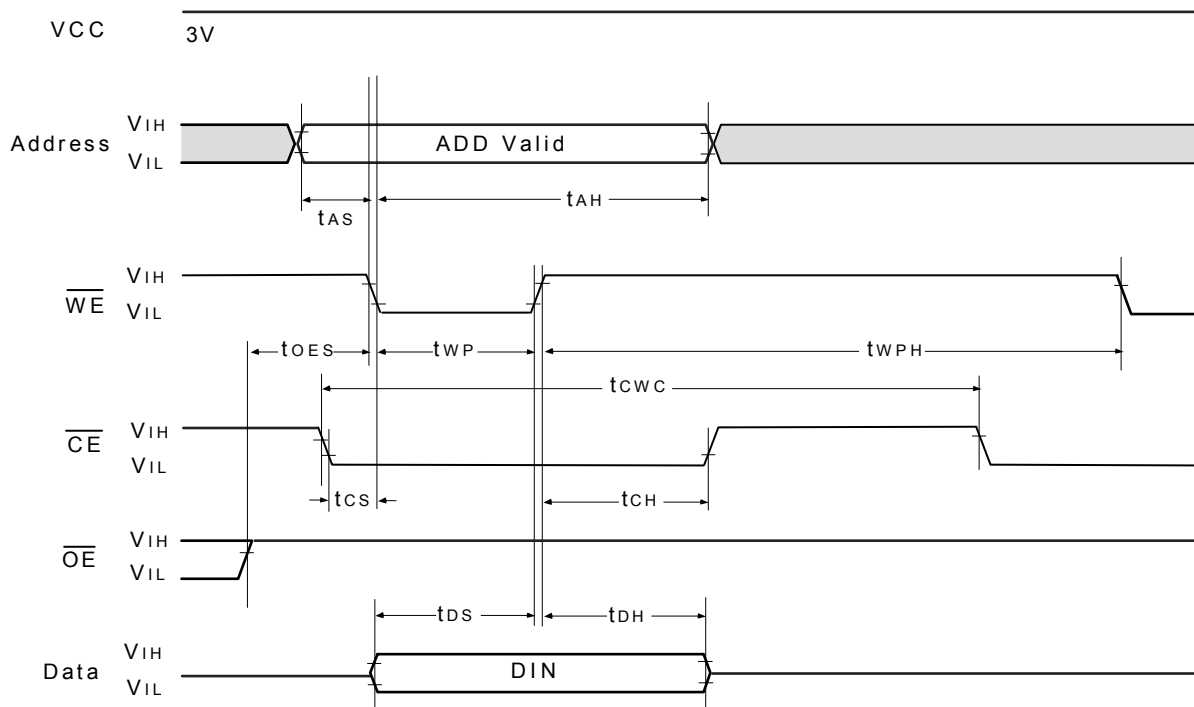
Figure 7. Embedded Programming Timing Waveform

Program Command Sequence (last two cycle)   Read Status Data (last two cycle)
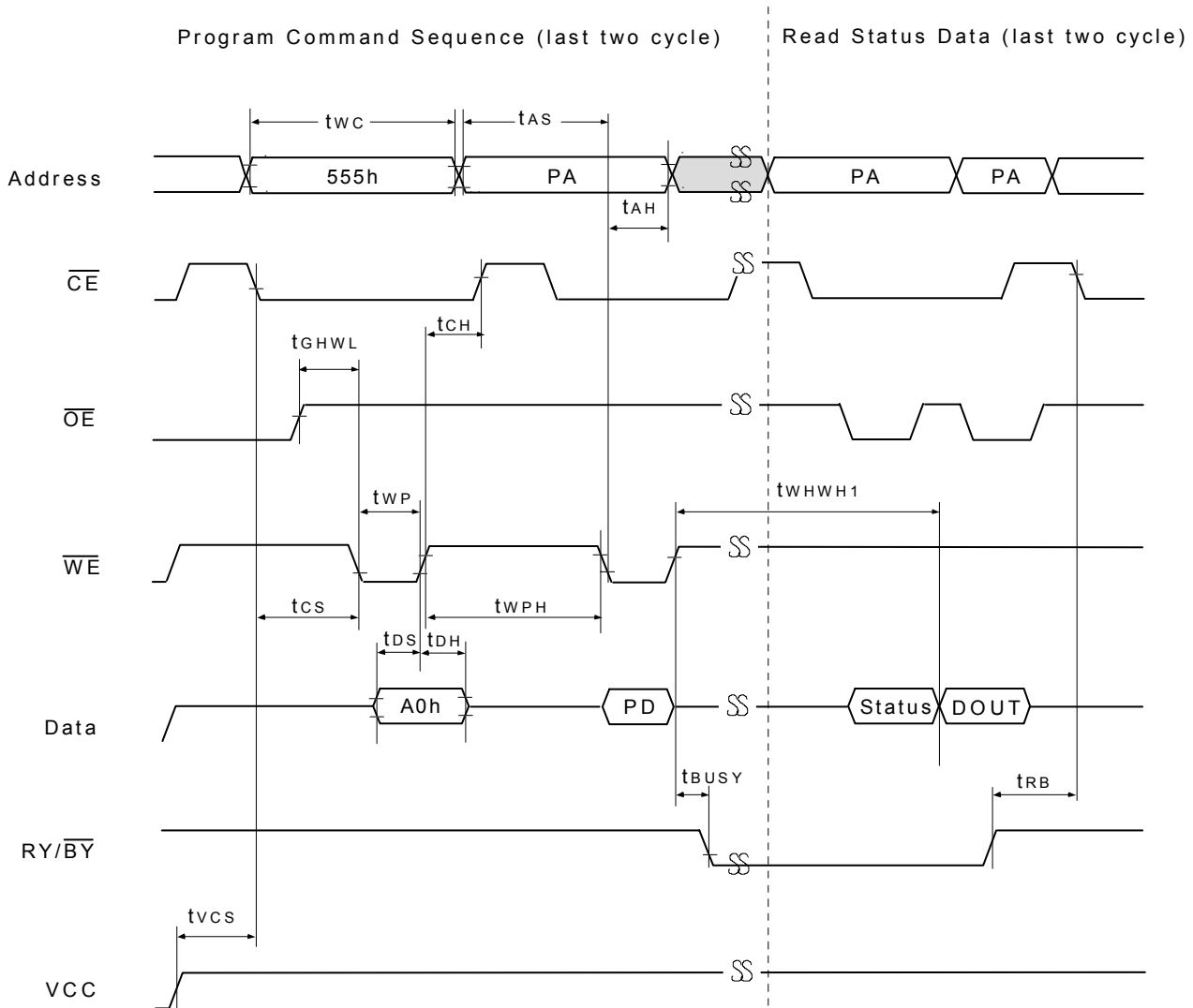
Notes :
1. PA = Program Address, PD = Program Data, DOUT is the true data the program address.

Figure 8. Embedded Programming Algorithm Flowchart

Start

Write Data AAH Address 555H

Write Data 55H Address 2AAH

Write Data A0H Address 555H

Write Program Data/Address

Data Poll from system

Verify Work OK? — No

Yes

Last address? — No → Increment address

Yes

Embedded Program Completed
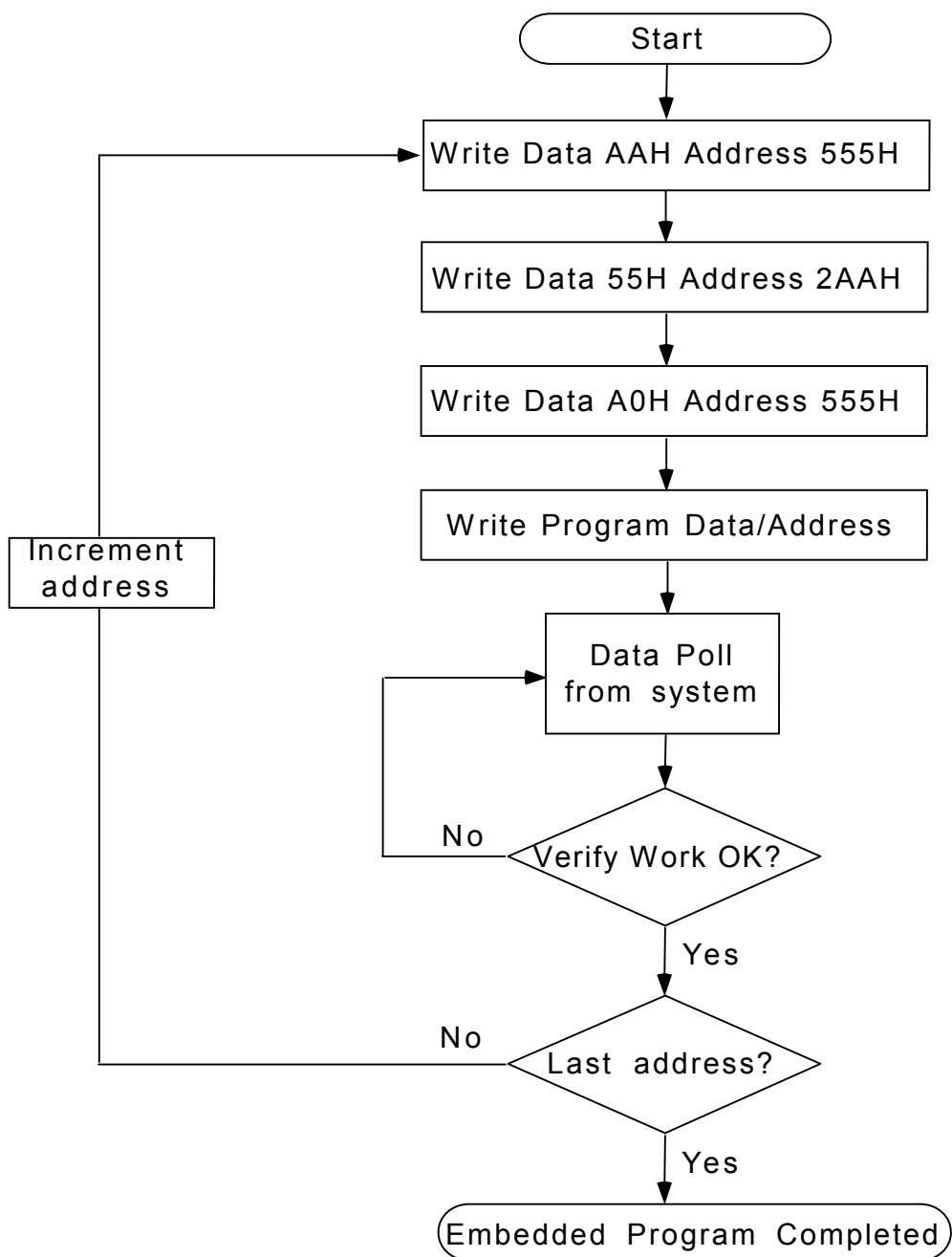
Figure 9. CE Controlled Program Timing Waveform
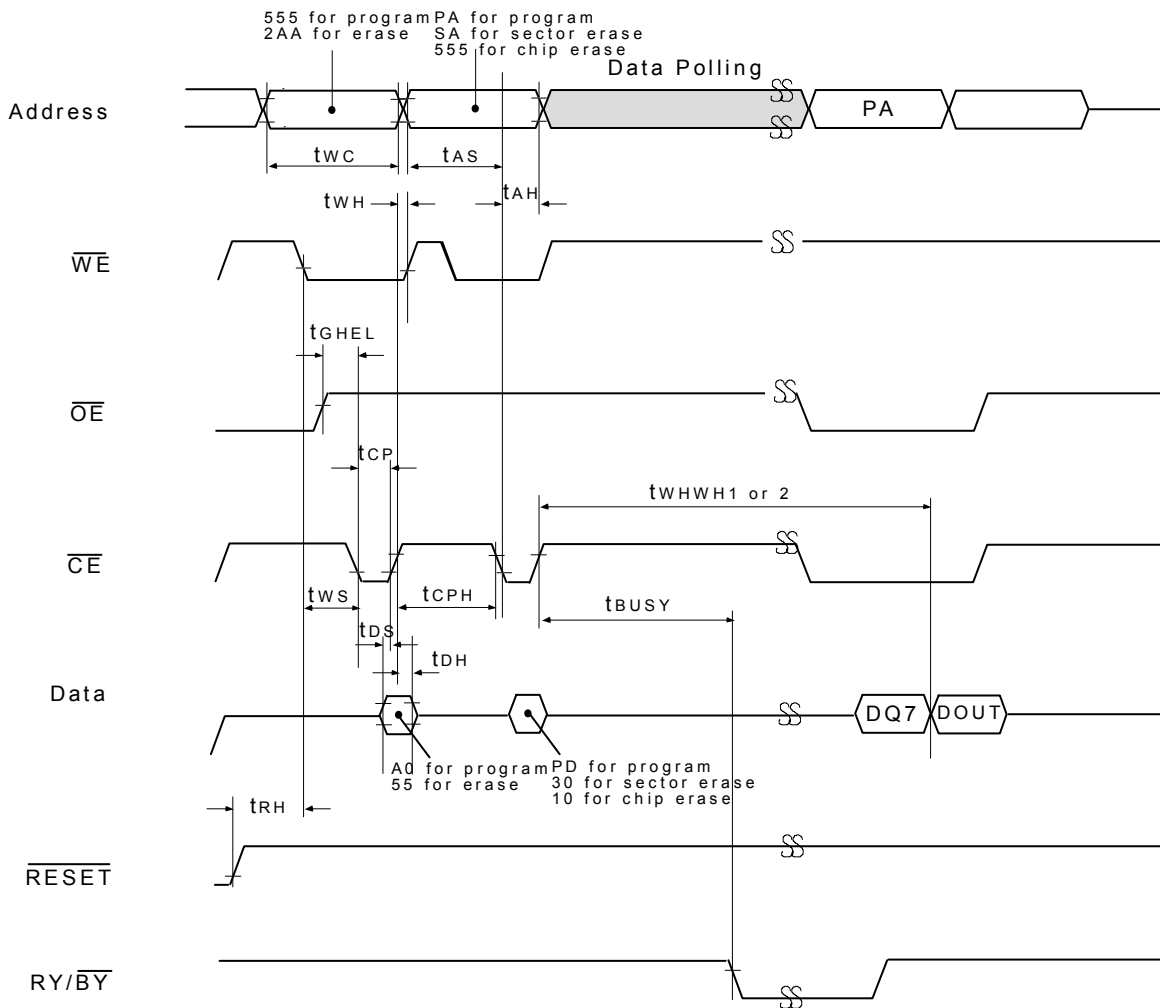
Notes :

1. PA = Program Address, PD = Program Data, DOUT = Data Out , DQ7 = complement of data written to device
2. Figure indicates the last two bus cycles of the command sequence..

Figure 10. Embedded Chip Erase Timing Waveform
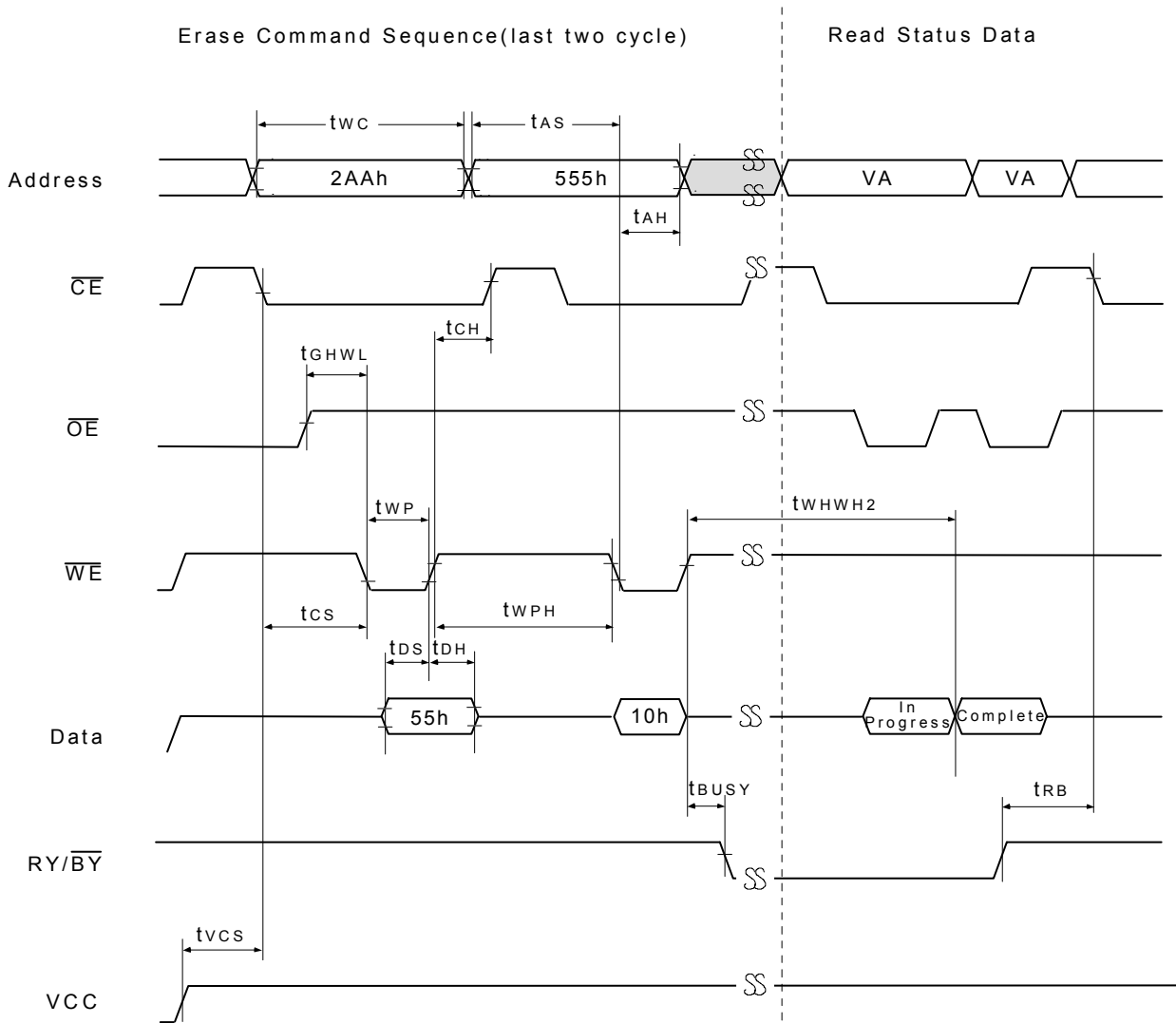
Notes :

SA = Sector Address (for Sector Erase, VA = Valid Address for reading status data
(see "Write Operation Status")

Figure 11. Embedded Chip Erase Algorithm Flowchart

```
                        ┌─────────────┐
                        (    Start    )
                        └──────┬──────┘
                               │
                               ▼
              ┌────────────────────────────────────┐
              │   Write Data AAH Address 555H       │
              └────────────────┬───────────────────┘
                               │
                               ▼
              ┌────────────────────────────────────┐
              │   Write Data 55H Address 2AAH       │
              └────────────────┬───────────────────┘
                               │
                               ▼
              ┌────────────────────────────────────┐
              │   Write Data 80H Address 555H       │
              └────────────────┬───────────────────┘
                               │
                               ▼
              ┌────────────────────────────────────┐
              │   Write Data AAH Address 555H       │
              └────────────────┬───────────────────┘
                               │
                               ▼
              ┌────────────────────────────────────┐
              │   Write Data 55H Address 2AAH       │
              └────────────────┬───────────────────┘
                               │
                               ▼
              ┌────────────────────────────────────┐
              │   Write Data 10H Address 555H       │
              └────────────────┬───────────────────┘
                               │
                               ▼
      ┌──────►┌────────────────────────────────────┐
      │       │      Data Poll from System          │
      │       └────────────────┬───────────────────┘
      │                        │
      │                        ▼
      │            No       ◇ Data = FFh? ◇
      └─────────────────────
                               │ Yes
                               ▼
                ┌──────────────────────────────────┐
                ( Embedded Chip Erease Completed    )
                └──────────────────────────────────┘
```
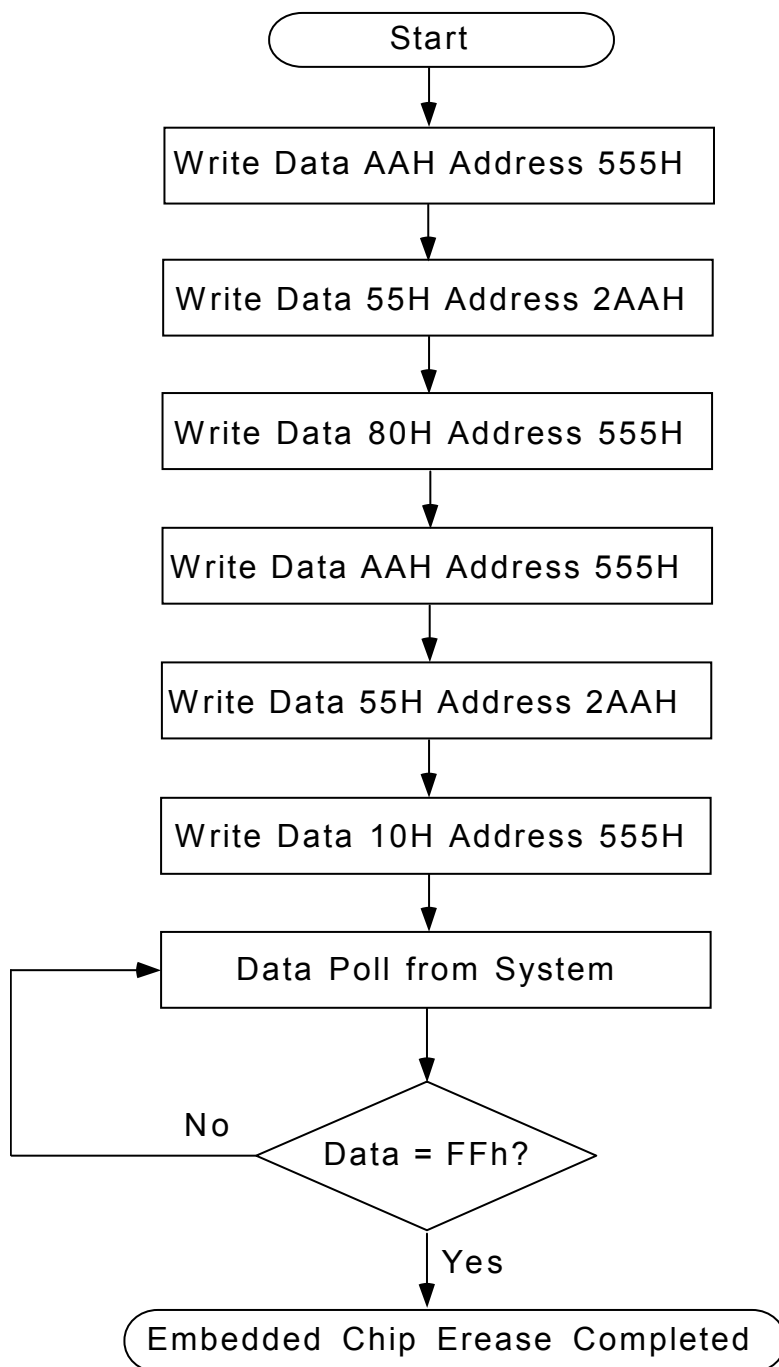
Figure 12. Embedded Sector Erase Timing Waveform

Notes :

Erase Command Sequence(last two cycle)   Read Status Data

SA = Sector Address (for Sector Erase, VA = Valid Address for reading status data
(see "Write Operation Status")
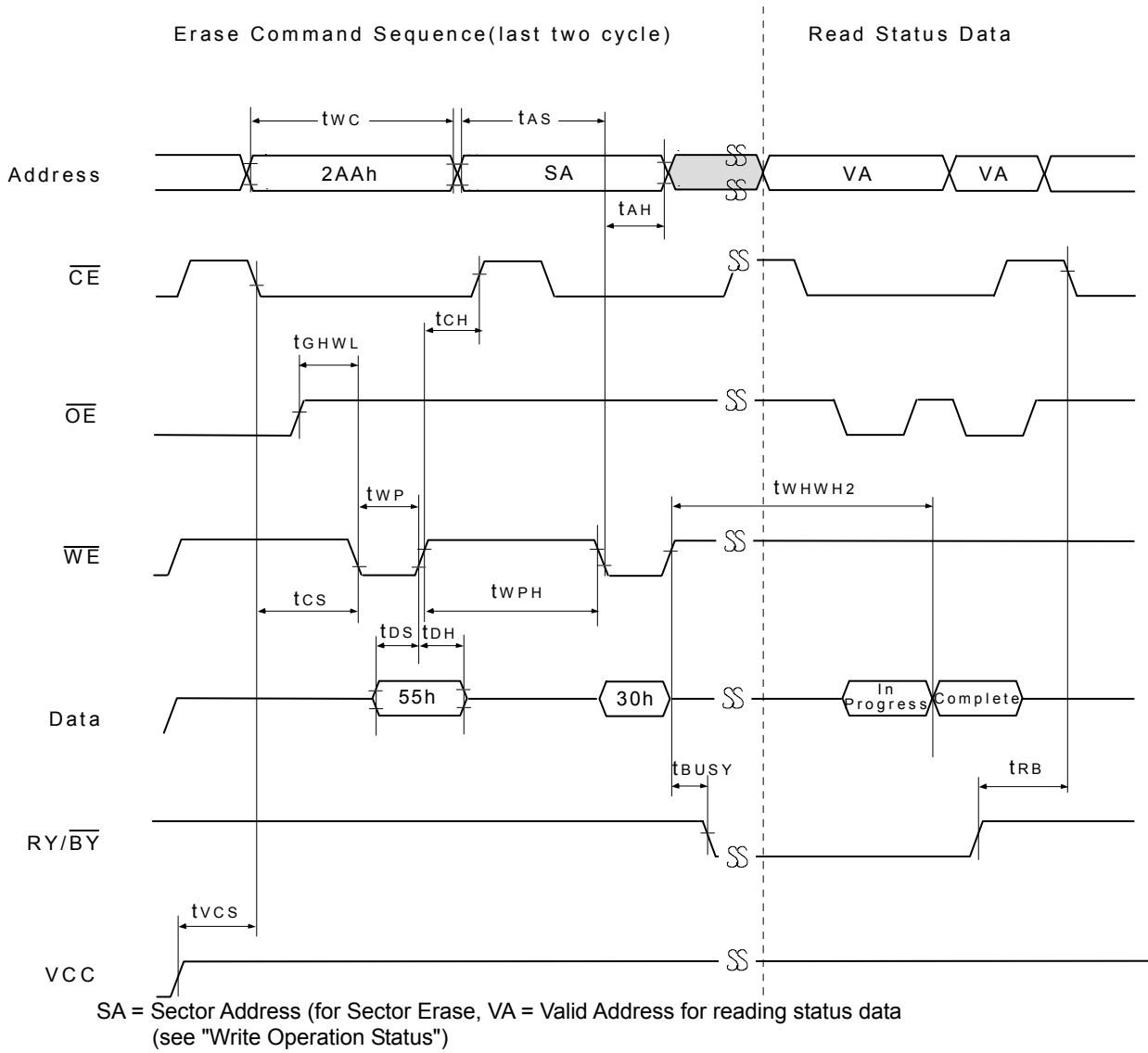
Figure 13. Embedded Sector Erase Algorithm Flowchart

```
                        ┌──────────────┐
                        │    Start     │
                        └──────────────┘
                               │
                               ▼
              ┌────────────────────────────────┐
              │  Write Data AAH Address 555H    │
              └────────────────────────────────┘
                               │
                               ▼
              ┌────────────────────────────────┐
              │  Write Data 55H Address 2AAH    │
              └────────────────────────────────┘
                               │
                               ▼
              ┌────────────────────────────────┐
              │  Write Data 80H Address 555H    │
              └────────────────────────────────┘
                               │
                               ▼
              ┌────────────────────────────────┐
              │  Write Data AAH Address 555H    │
              └────────────────────────────────┘
                               │
                               ▼
              ┌────────────────────────────────┐
              │  Write Data 55H Address 2AAH    │
              └────────────────────────────────┘
                               │
                               ▼
              ┌────────────────────────────────┐◄──────┐
              │  Write Data 30H Address SA      │       │
              └────────────────────────────────┘       │
                               │                        │
                               ▼                        │
                         ╱ Last Sector ╲     No         │
                        ╱   to Erase     ╲──────────────┘
                         ╲              ╱
                               │ Yes
                               ▼
              ┌────────────────────────────────┐◄──────┐
              │     Data Poll from System       │       │
              └────────────────────────────────┘       │
                               │                        │
                               ▼                        │
                         ╱ Data = FFH? ╲      No         │
                        ╱                ╲──────────────┘
                         ╲              ╱
                               │
                               ▼
                ┌──────────────────────────────────┐
                │ Embedded Sector Erease Completed  │
                └──────────────────────────────────┘
```
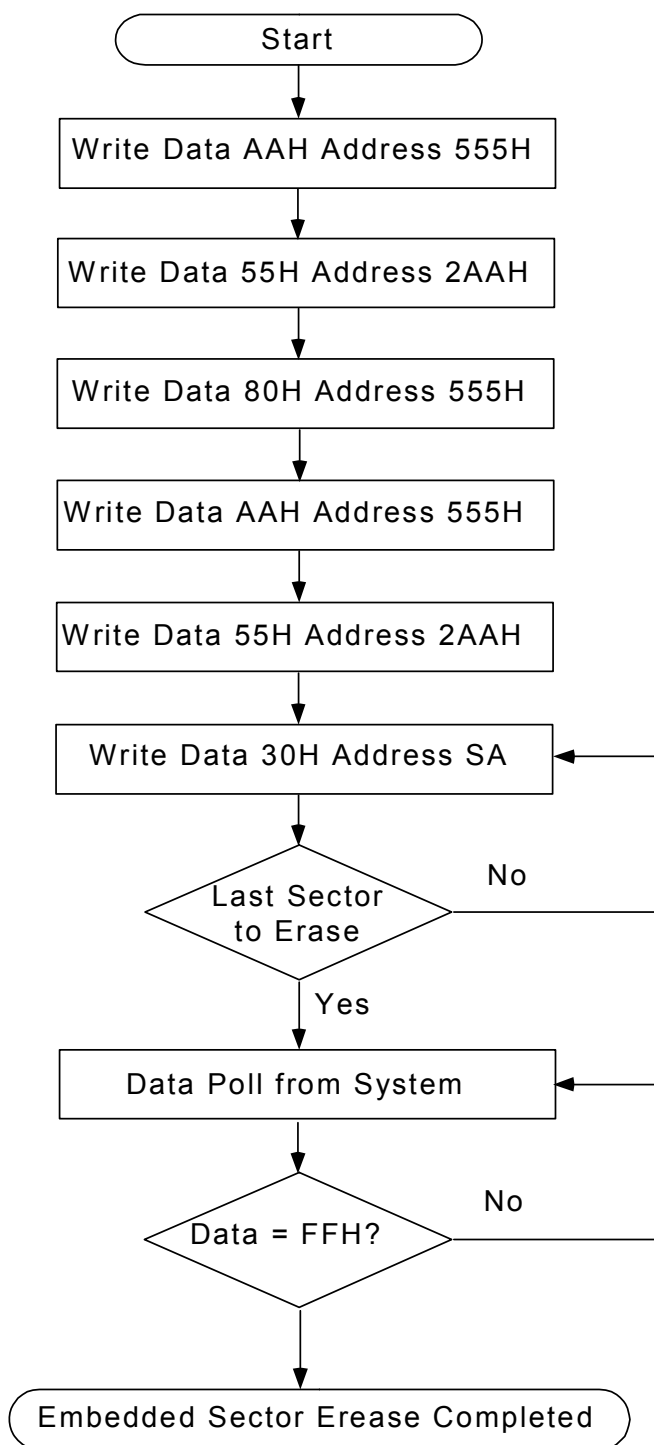
Figure 14. Erase Suspend/Erase Resume Flowchart

```
                    ┌─────────┐
                    │  Start  │
                    └────┬────┘
                         │
              ┌──────────────────────┐
              │   Write Data B0H      │ ────┐
              └──────────┬───────────┘      │
                         │                  │   ERASE SUSPEND
                    ◇ Toggle Bit      No     │
                      checking Q6 ──────────┘
                      not toggled
                         │ Yes
              ┌──────────────────────┐
              │  Read Array or        │ ◄──┐
              │  Program              │    │
              └──────────┬───────────┘    │
                    ◇ Reading or     No    │
                      Programming End ─────┘
                         │ Yes
              ┌──────────────────────┐
              │   Write Data 30H      │ ────┐
              └──────────┬───────────┘      │   ERASE RESUME
              ┌──────────────────────┐      │
              │  Continue Erase       │ ◄──┐ │
              └──────────┬───────────┘    │
                    ◇ Another       No    │
                      Erase Suspend? ─────┘
                         │ Yes
```

Figure 15. In-System Sector Protect/Unprotect Timing Waveform ($\overline{\text{RESET}}$ Control)

Notes :
When sector protect, A6=0, A1=1, A0=0.
When sector unprotect, A6=1, A1=1, A0=0.

Figure 16. In-System Sector Protect/Unprotect Algorithm ($\overline{RESET}$ = V$_{ID}$)
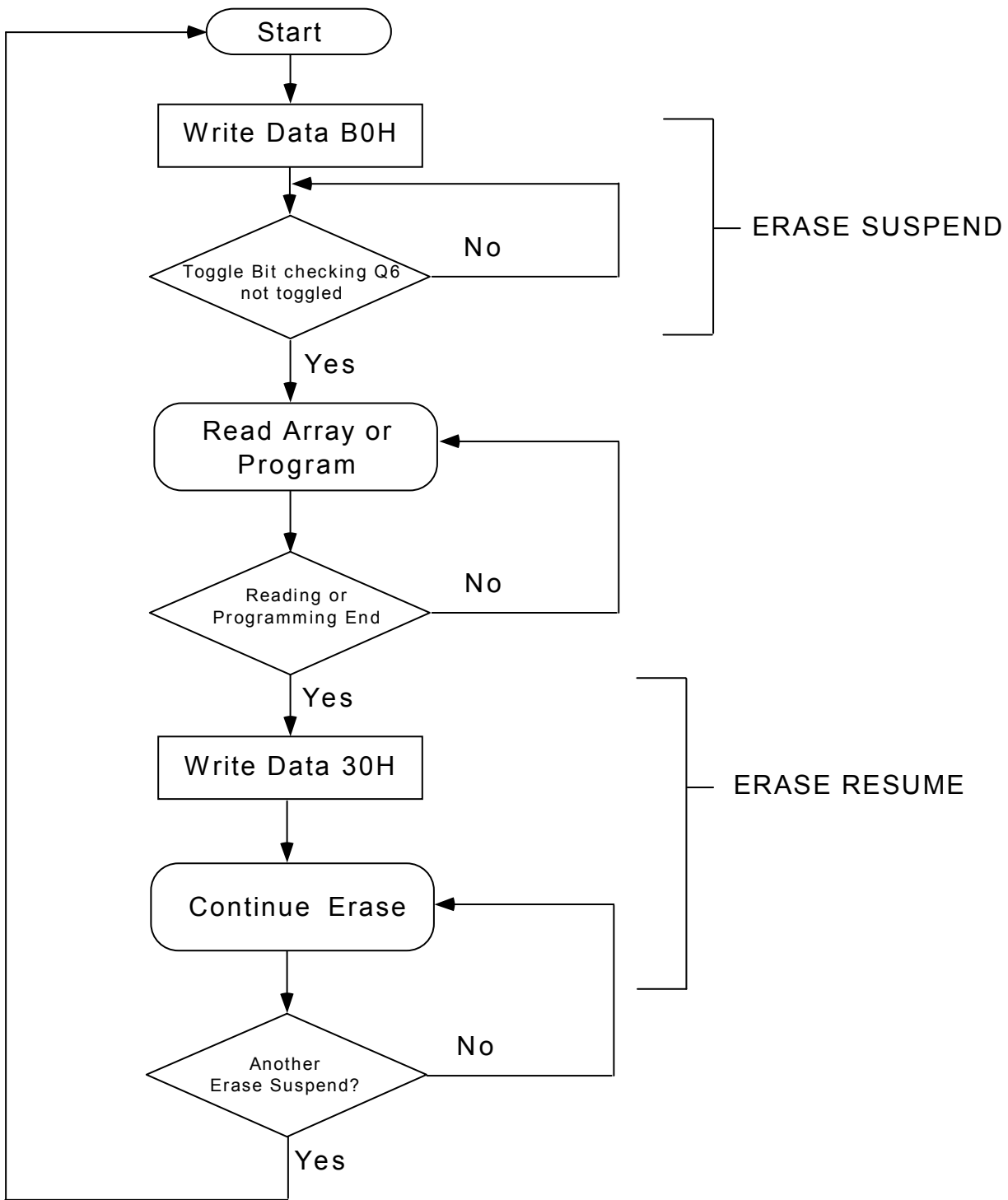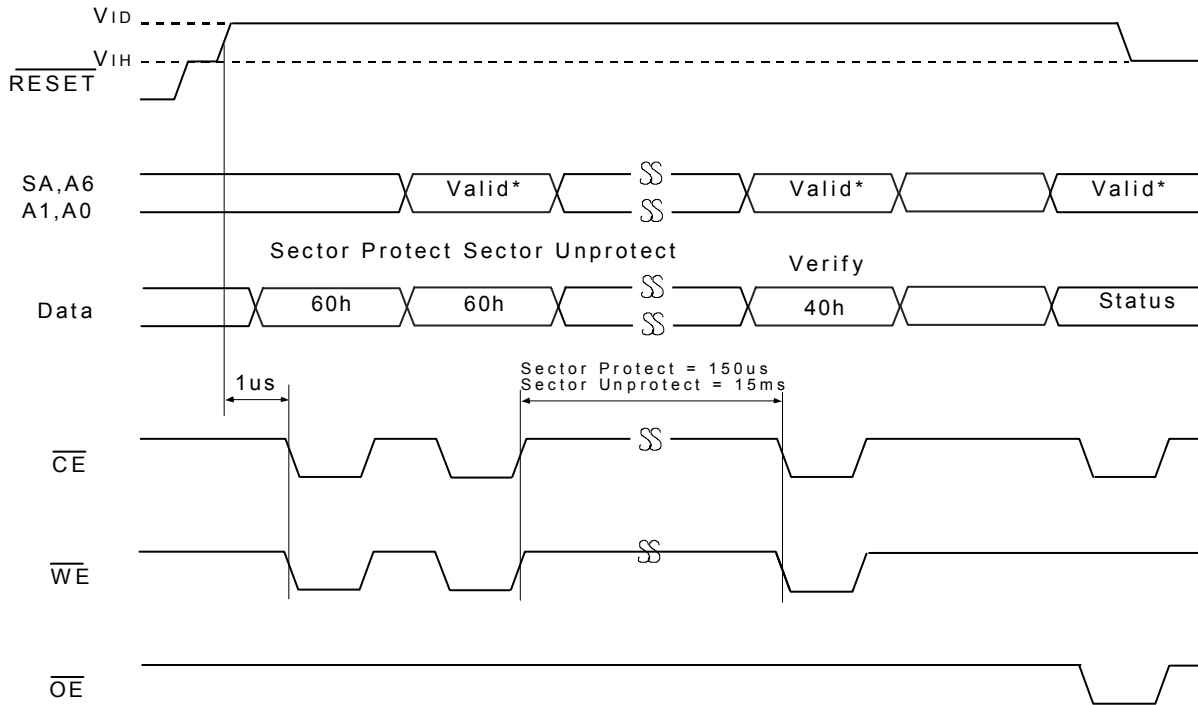
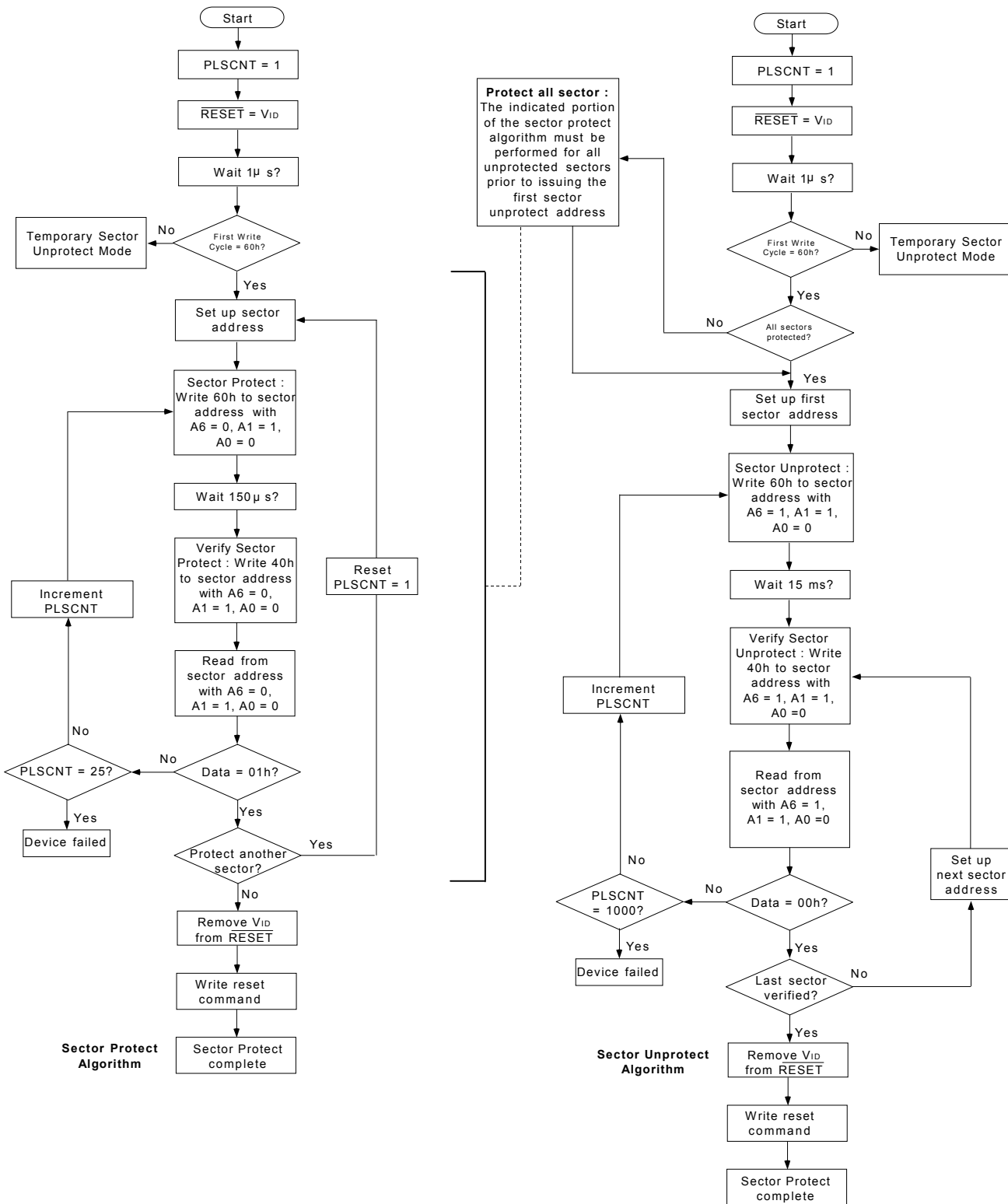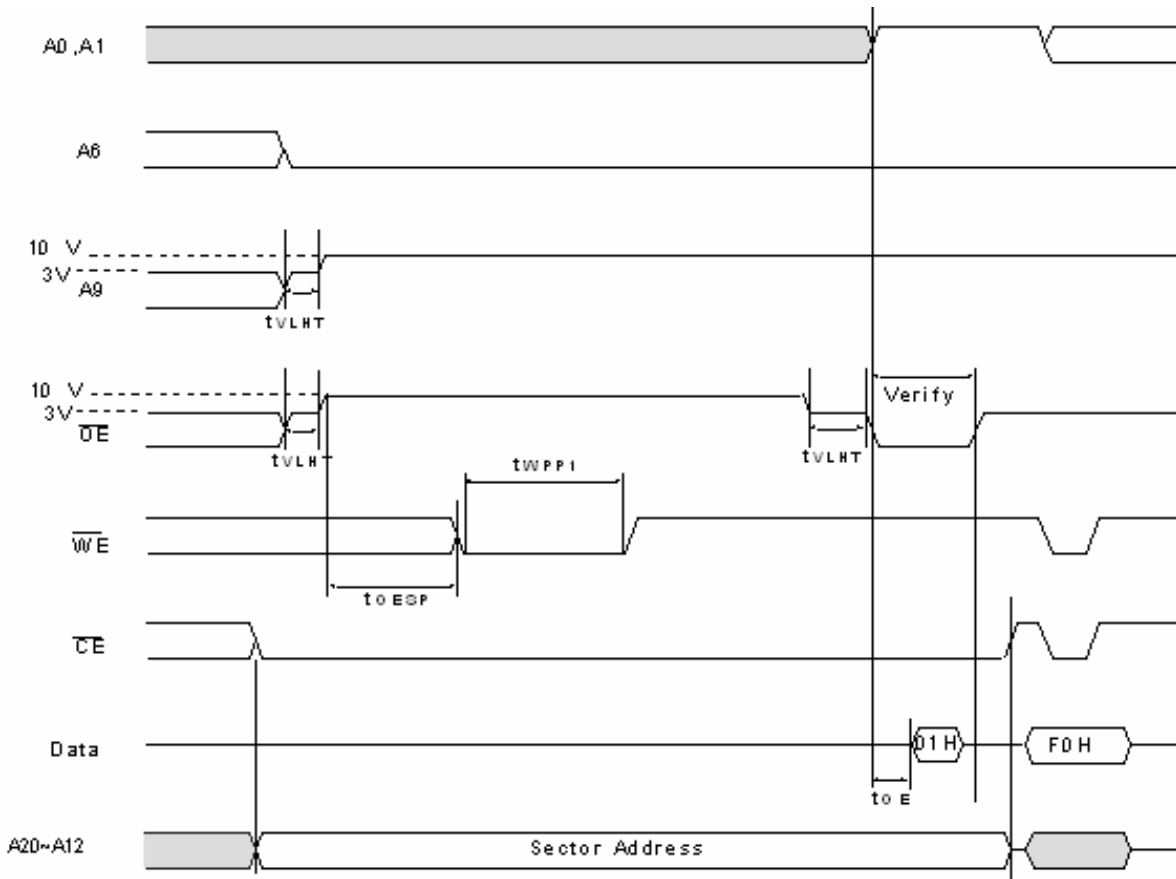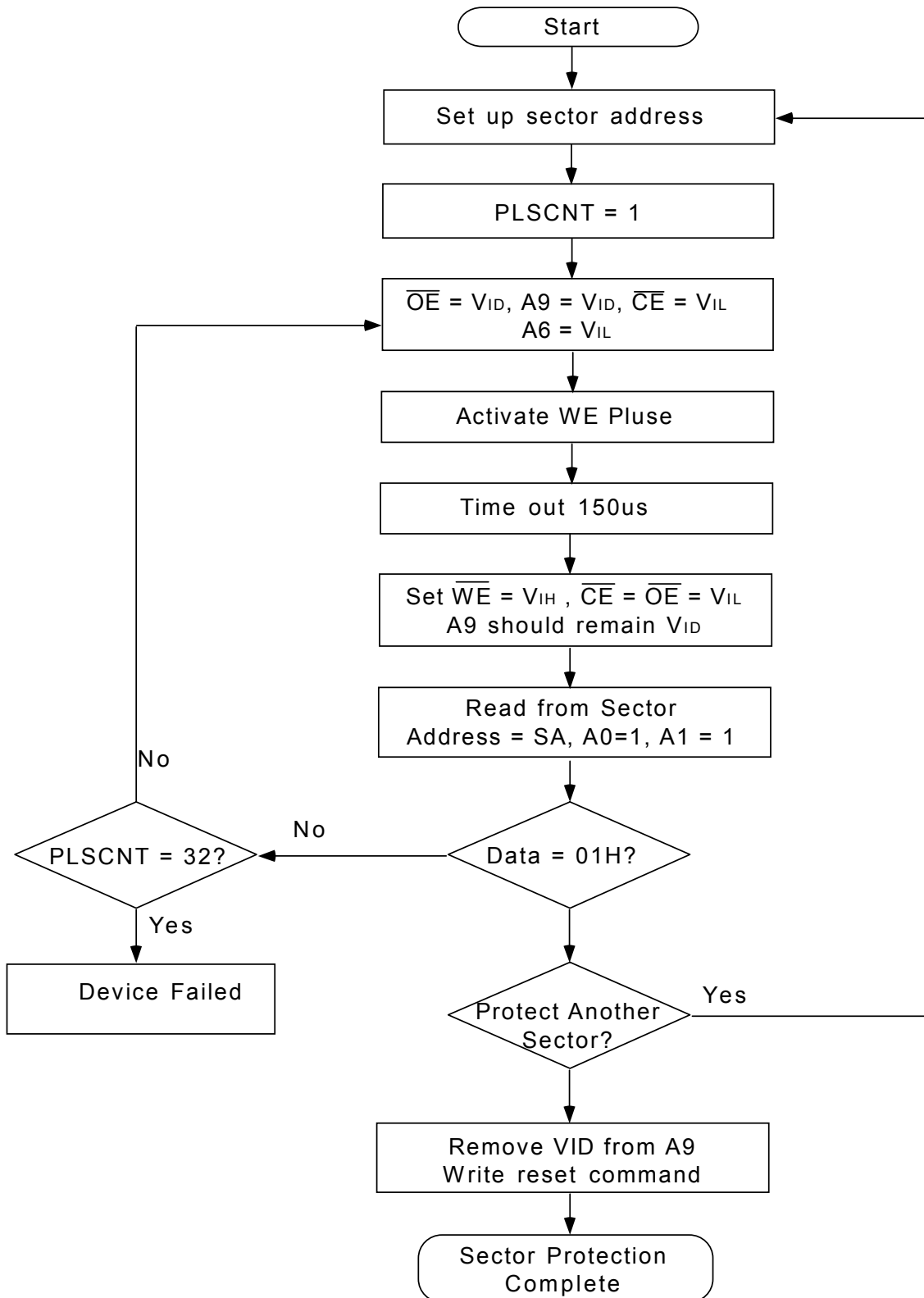## Figure 17. Sector Protect Timing Waveform (A9, $\overline{OE}$ Control)

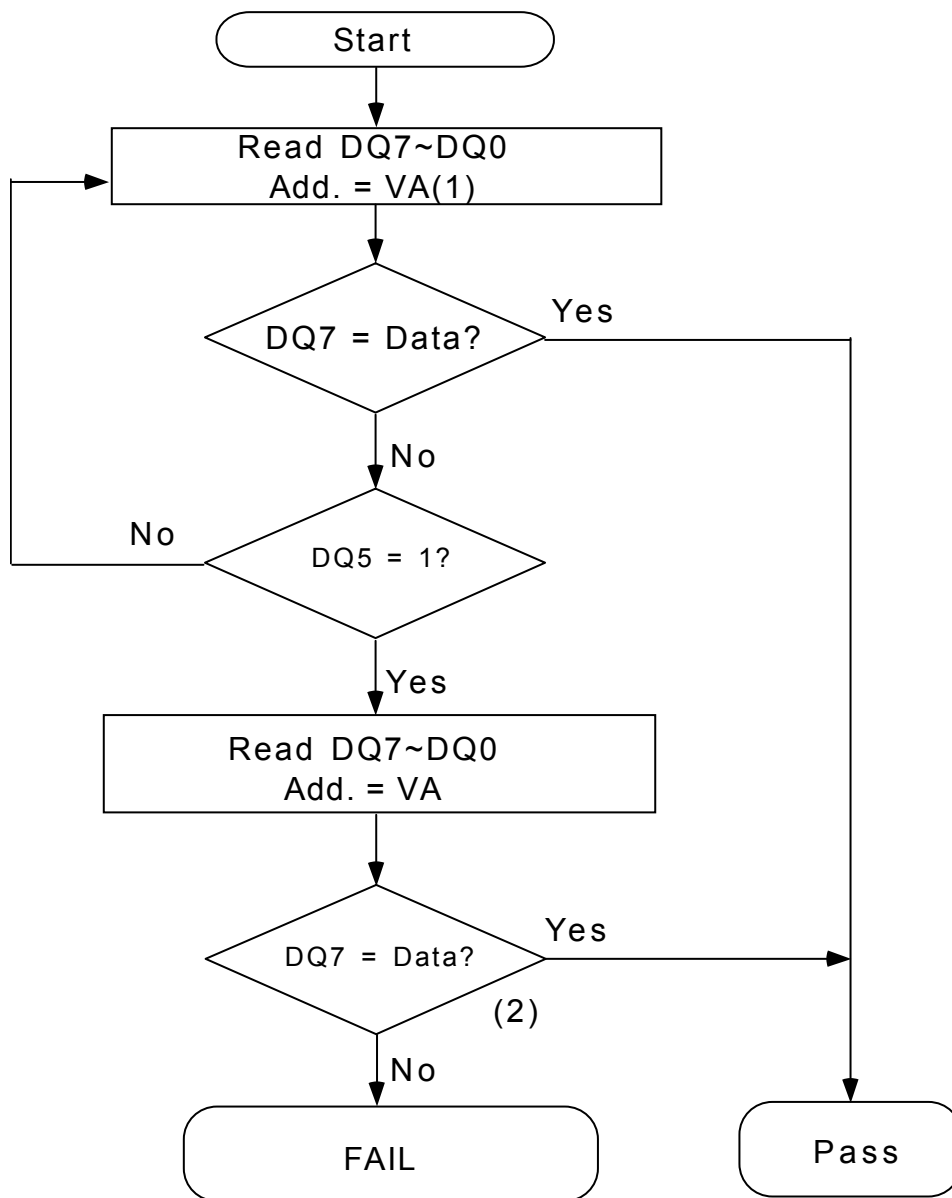**Figure 18. Sector Protection Algorithm (A9, $\overline{OE}$ Control)**

```
                    ┌──────────┐
                    │  Start   │
                    └────┬─────┘
                         ▼
              ┌──────────────────────┐
              │ Set up sector address │◄─────────────┐
              └──────────┬───────────┘               │
                         ▼                            │
              ┌──────────────────────┐               │
              │      PLSCNT = 1       │               │
              └──────────┬───────────┘               │
                         ▼                            │
   ┌─────────►┌──────────────────────┐               │
   │          │ OE = VID, A9 = VID,   │               │
   │          │ CE = VIL   A6 = VIL   │               │
   │          └──────────┬───────────┘               │
   │                     ▼                            │
   │          ┌──────────────────────┐               │
   │          │  Activate WE Pluse    │               │
   │          └──────────┬───────────┘               │
   │                     ▼                            │
   │          ┌──────────────────────┐               │
   │          │    Time out 150us     │               │
   │          └──────────┬───────────┘               │
   │                     ▼                            │
   │          ┌──────────────────────┐               │
   │          │ Set WE = VIH,         │               │
   │          │ CE = OE = VIL         │               │
   │          │ A9 should remain VID  │               │
   │          └──────────┬───────────┘               │
   │                     ▼                            │
   │          ┌──────────────────────┐               │
   │          │   Read from Sector    │               │
   │          │ Address = SA, A0=1,   │               │
   │          │          A1 = 1       │               │
   │          └──────────┬───────────┘               │
   │                     ▼                            │
   │ No                ◇◇◇◇                            │
   ◇◇◇◇◇◇◇◇  ◄── No ──  Data = 01H?                    │
   PLSCNT = 32?          ◇◇◇◇                          │
   ◇◇◇◇◇◇◇◇                │ Yes                       │
      │ Yes                ▼                           │
      ▼                  ◇◇◇◇◇                         │
 ┌─────────────┐         Protect Another ── Yes ───────┘
 │Device Failed│         Sector?
 └─────────────┘          ◇◇◇◇◇
                            │ No
                            ▼
                 ┌──────────────────────┐
                 │ Remove VID from A9    │
                 │ Write reset command   │
                 └──────────┬───────────┘
                            ▼
                    ┌──────────────┐
                    │Sector Protection│
                    │   Complete    │
                    └──────────────┘
```

WRITE OPERATION STATUS

Figure 19. Data Polling Algorithm

```
                        ┌──────────┐
                        │  Start   │
                        └──────────┘
                             │
                             ▼
              ┌──────────────────────────┐
        ┌────▶│     Read DQ7~DQ0         │
        │     │     Add. = VA(1)         │
        │     └──────────────────────────┘
        │                  │
        │                  ▼
        │           ╱────────────╲        Yes
        │          ╱  DQ7 = Data? ╲──────────────┐
        │          ╲              ╱               │
        │           ╲────────────╱                │
        │                  │ No                    │
        │                  ▼                       │
        │    No     ╱────────────╲                │
        └──────────╱   DQ5 = 1?   ╲               │
                   ╲              ╱                │
                    ╲────────────╱                │
                          │ Yes                   │
                          ▼                       │
              ┌──────────────────────┐            │
              │    Read DQ7~DQ0      │            │
              │    Add. = VA         │            │
              └──────────────────────┘            │
                          │                       │
                          ▼                       │
                   ╱────────────╲      Yes        │
                  ╱  DQ7 = Data? ╲────────────────┤
                  ╲              ╱                 │
                   ╲────────────╱  (2)            │
                          │ No                     │
                          ▼                       ▼
                   ┌──────────┐            ┌──────────┐
                   │   FAIL   │            │   Pass   │
                   └──────────┘            └──────────┘
```

Notes :
1. VA =Valid address for programming.
2. DQ7 should be re-checked even DQ5 = "1" because
   DQ7 may change simultaneously with DQ5.

Figure 20. Toggle Bit Algorithm
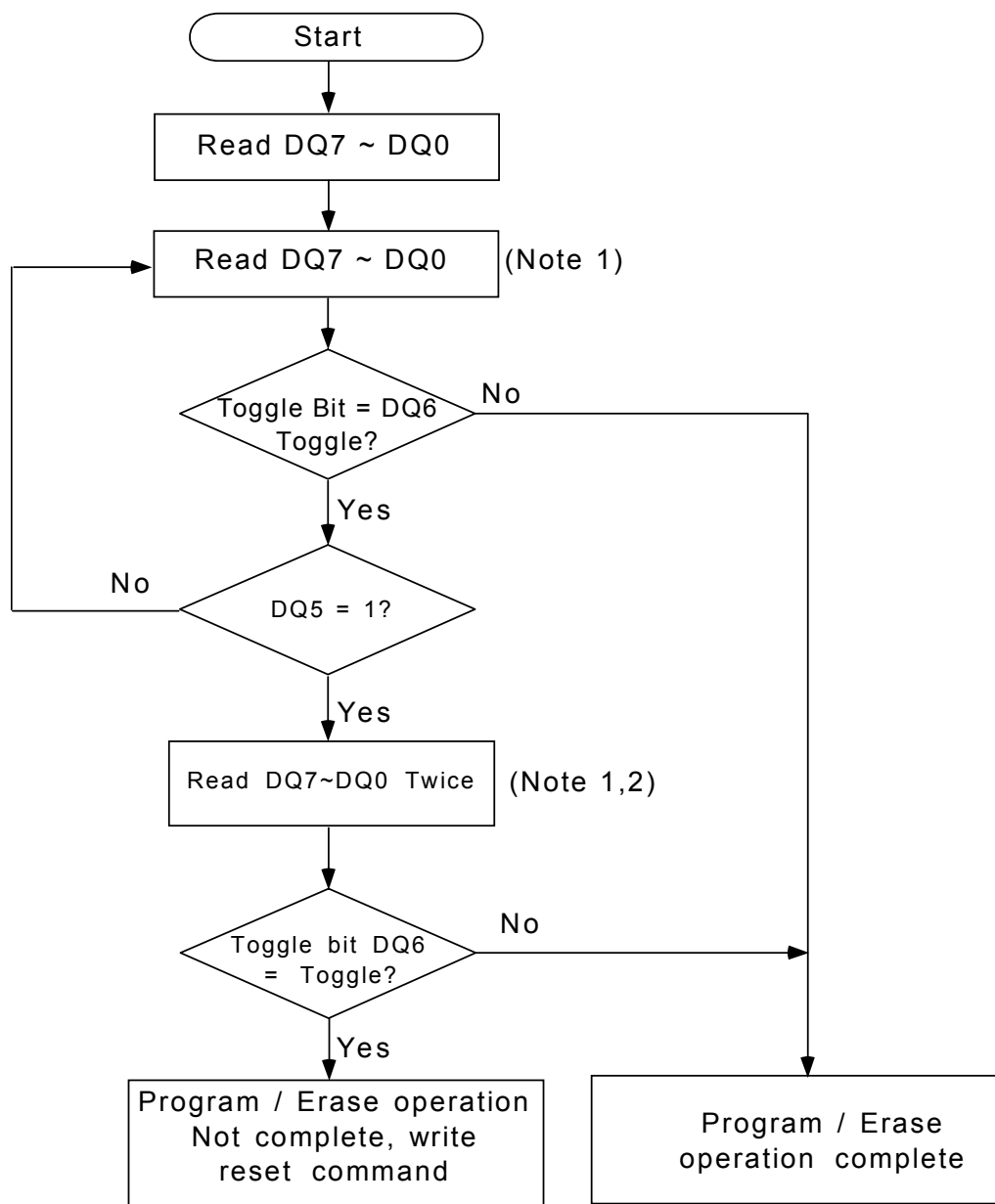
Note :
   1. Read toggle bit twice to determine whether or not it is toggle.
   2. Recheck toggle bit because it may stop toggling as DQ5 change to "1".

Figure 21. Data Polling Timings (During Embedded Algorithms)
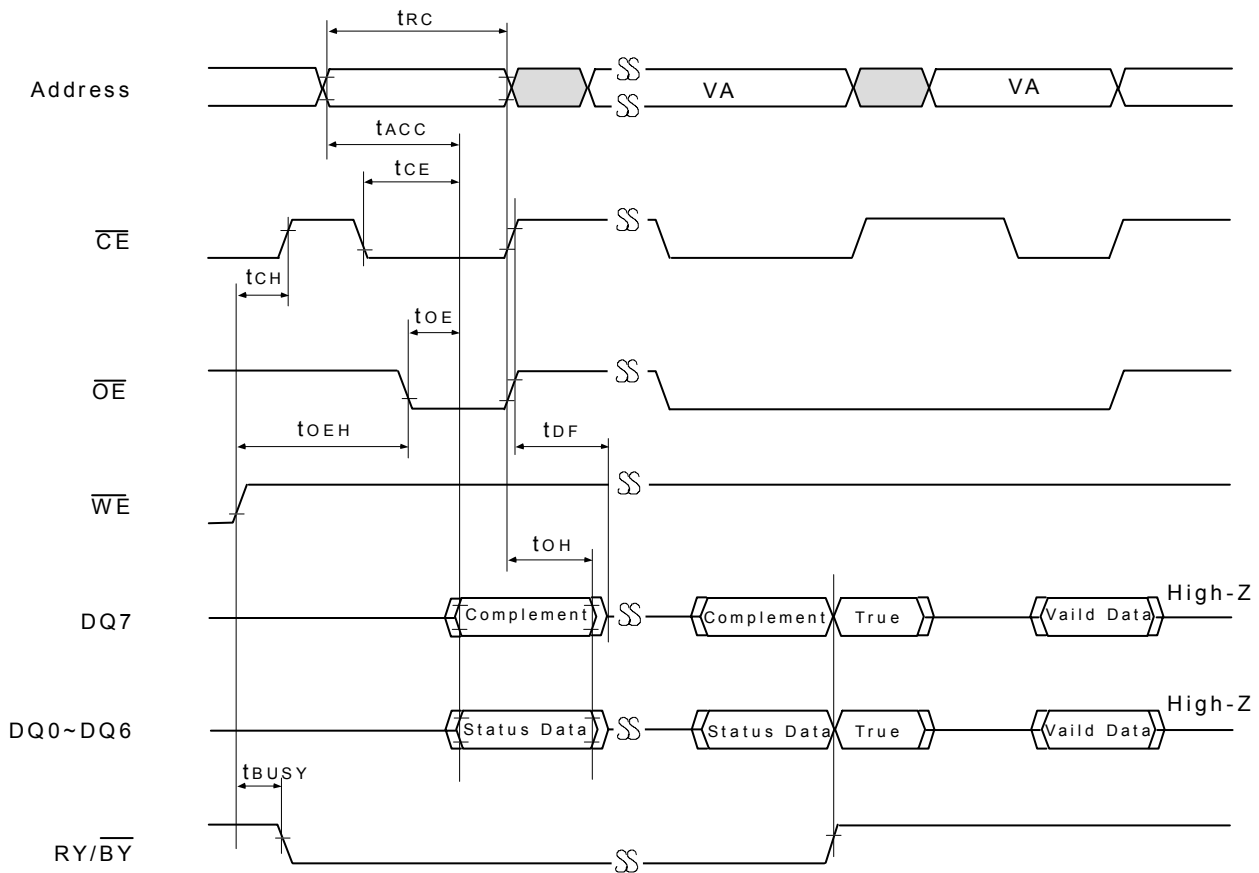
Notes :

VA = Valid Address. Figure shows first status cycle after command sequence, last status read cycle, and array data read cycle.

Figure 22. Toggle Bit Timing Waveforms (During Embedded Algorithms)
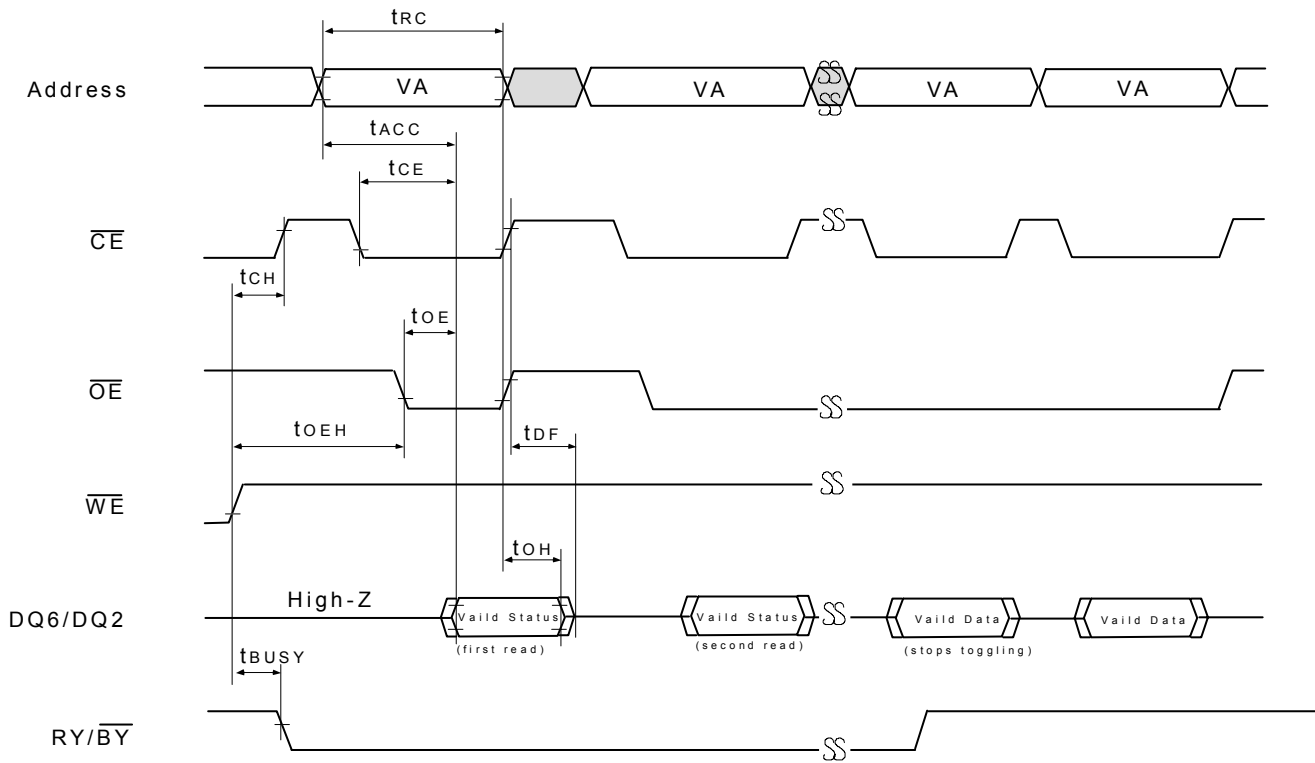
Notes :

    VA = Valid Address; not required for DQ6. Figure shows first status cycle after command sequence, last status read cycle, and array data read cycle.

10.3 Hardware Reset Operation

Table 17. AC CHARACTERISTICS

Symbol	Description		All Speed Options	Unit
T$_{READY1}$	$\overline{RESET}$ Pin Low (During Embedded Algorithms) to Read or Write (See Note)	Max	20	us
T$_{READY2}$	$\overline{RESET}$ Pin Low (NOT During Embedded Algorithms) to Read or Write (See Note)	Max	500	ns
T$_{RP}$	$\overline{RESET}$ Pulse Width (During Embedded Algorithms)	Min	500	ns
T$_{RH}$	$\overline{RESET}$ High Time Before Read(See Note)	Min	50	ns
T$_{RB}$	RY/$\overline{BY}$ Recovery Time(to $\overline{CE}$, $\overline{OE}$ go low)	Min	0	ns

Notes :

Not 100% tested

Figure 23. $\overline{RESET}$ Timing Waveform
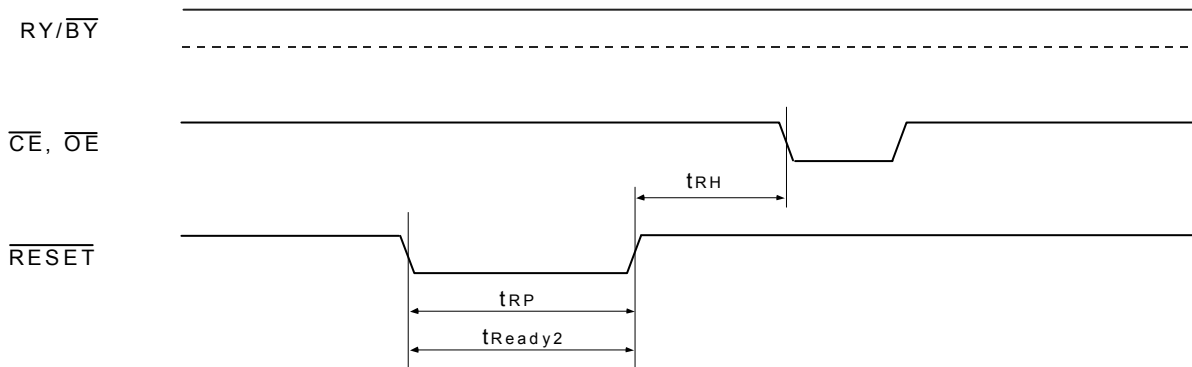
Reset Timing NOT during Automatic Algorithms
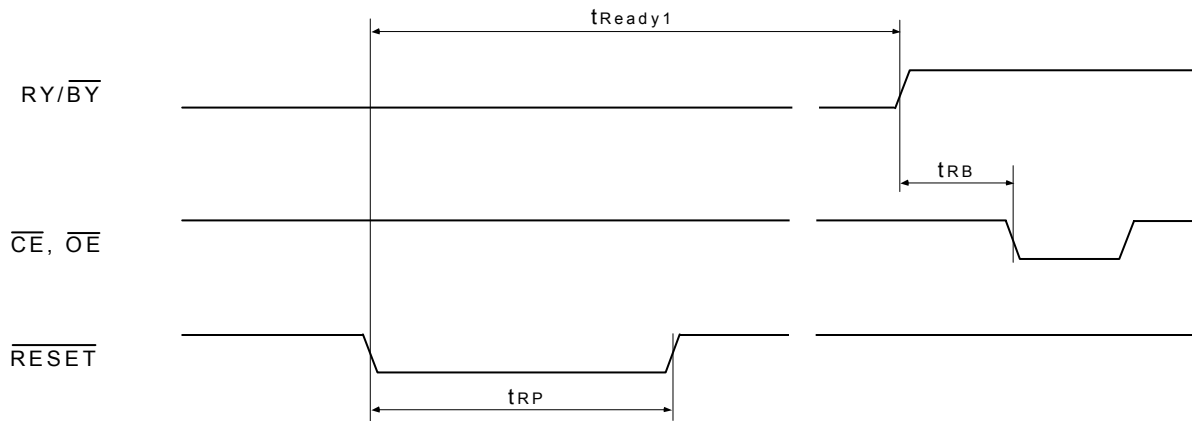
Reset Timing during Automatic Algorithms

10.4 TEMPORARY SECTOR UNPROTECT Operation

Table 18. Temporary Sector Unprotect

Symbol	Description		All Speed Options	Unit
T_{VIDR}	V_{ID} Rise and Fall Time (See Note)	Min	500	ns
T_{RSP}	$\overline{RESET}$ Setup Time for Temporary Sector Unprotect	Min	4	us

Notes:

Not 100% tested
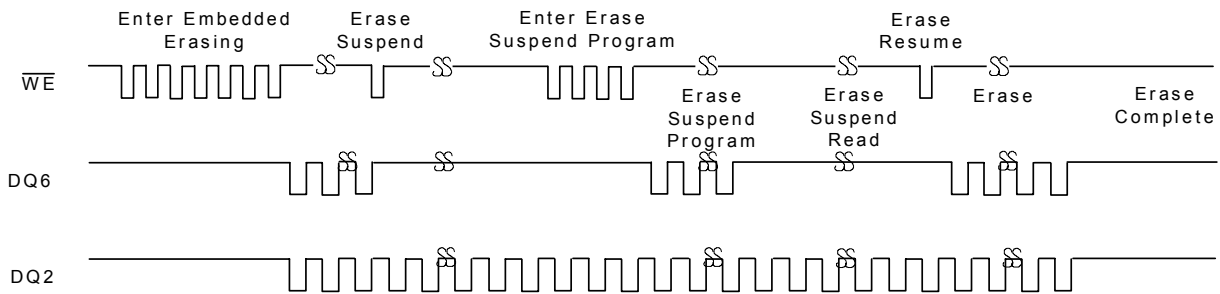
Figure 24. Temporary Sector Unprotect Timing Diagram
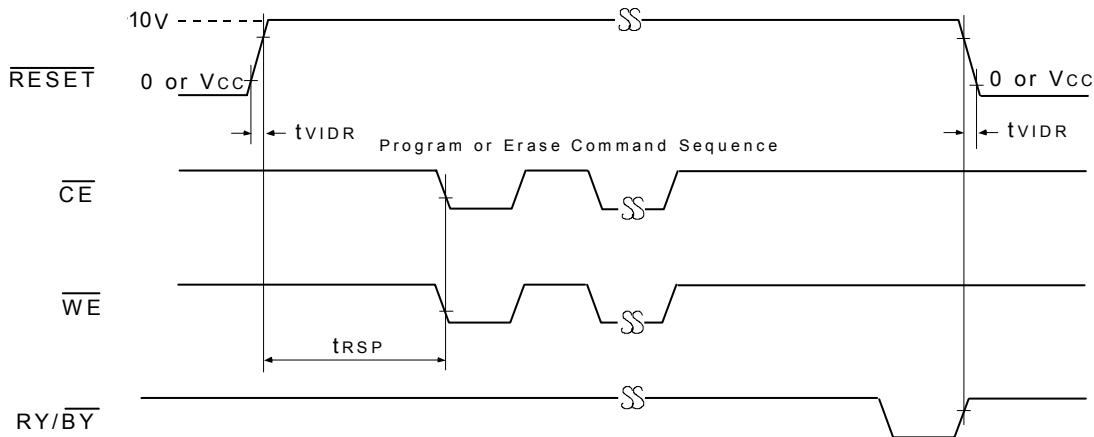

Figure 25. DQ6 vs DQ2 for Erase and Erase Suspend Operations

Notes :

The system can use OE or CE to toggle DQ2 / DQ6, DQ2 toggles only when read at an address within an erase-suspended.

Figure 26. Temporary Sector Unprotect Algorithm

```
                    ┌──────────────────┐
                    │      Start       │
                    └──────────────────┘
                             │
                             ▼
        ┌────────────────────────────────────────────┐
        │         RESET = V_ID (Note 1)               │
        └────────────────────────────────────────────┘
                             │
                             ▼
        ┌────────────────────────────────────────────┐
        │     Program Erase or Program Operation      │
        └────────────────────────────────────────────┘
                             │
                             ▼
        ┌────────────────────────────────────────────┐
        │         Operation  Completed                │
        └────────────────────────────────────────────┘
                             │
                             ▼
        ┌────────────────────────────────────────────┐
        │            RESET = V_IH                      │
        └────────────────────────────────────────────┘
                             │
                             ▼
        ┌────────────────────────────────────────────┐
        │ Temporary Sector Unprotect Completed (Note 2) │
        └────────────────────────────────────────────┘
```
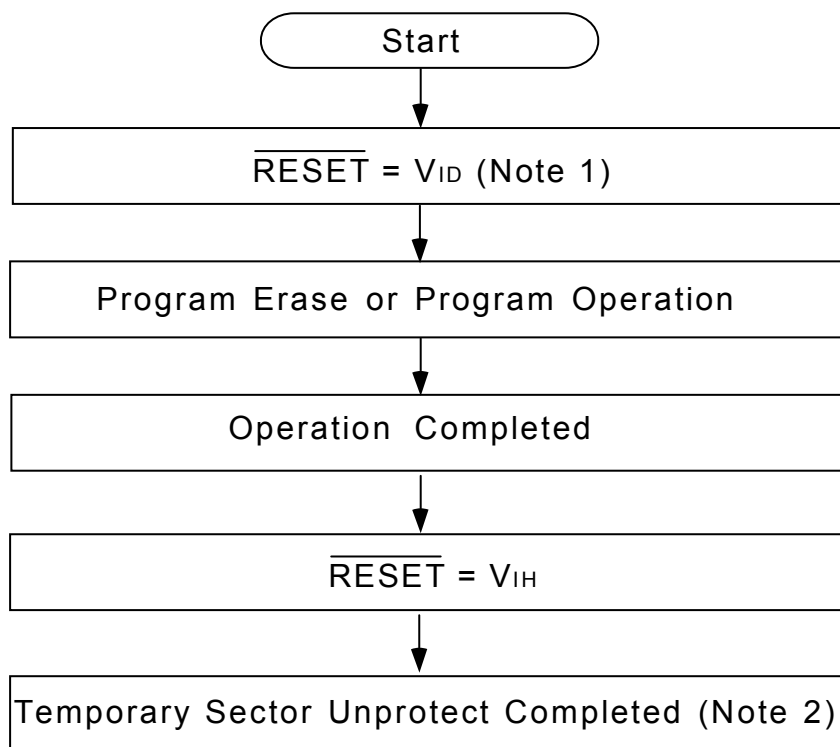
Notes :

1. All protected status are temporary unprotect.
   V_{ID} = 10V~10.5V
2. All previously protected sectors are protected again.

Figure 27. ID Code Read Timing Waveform
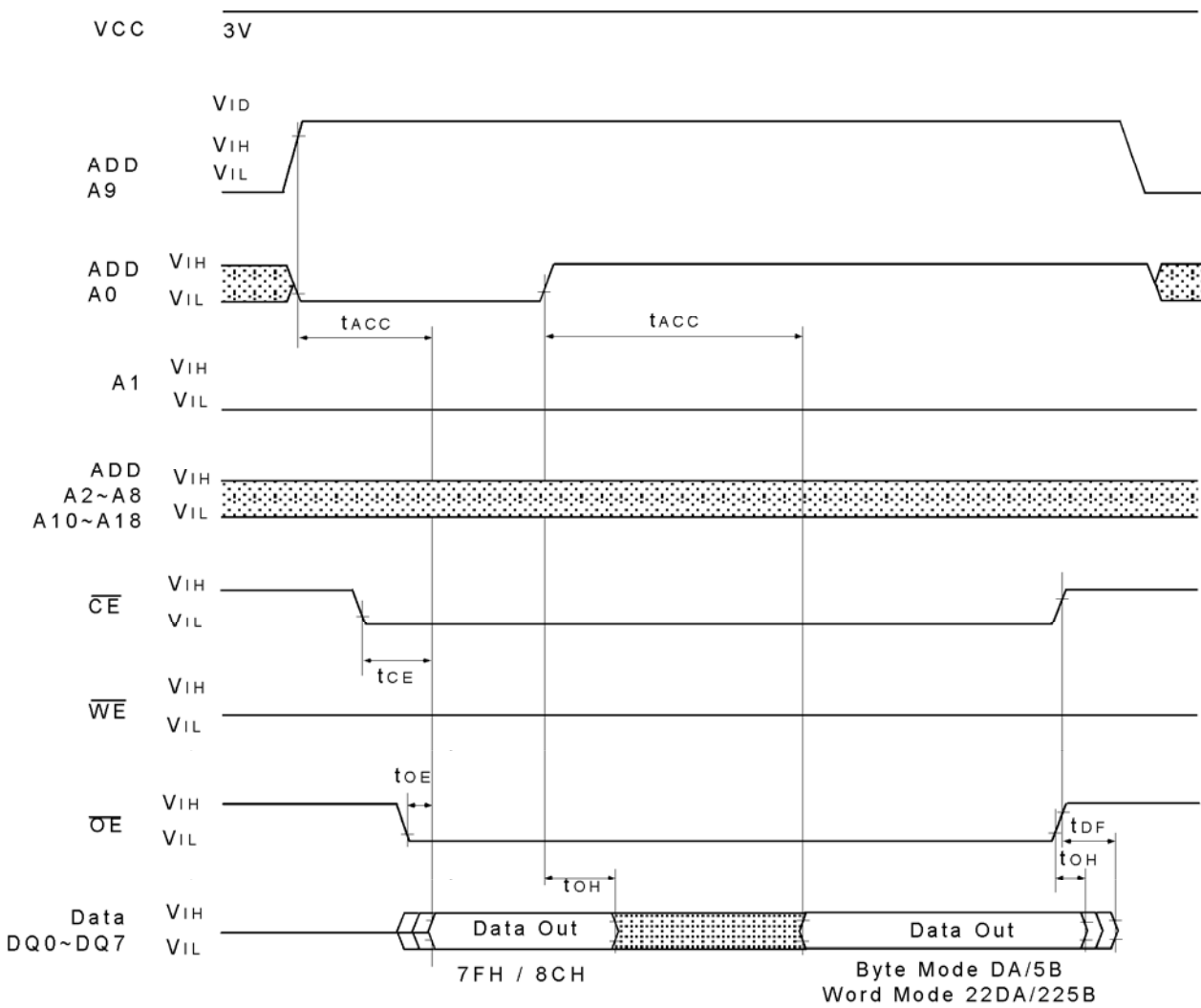
11. ERASE AND PROGRAMMING PERFORMANCE

Table 19. Erase And Programming Performance (Note.1)

Parameter		Limits		Unit
		Typ.(2)	Max.(3)	
Sector Erase Time		0.7	15	Sec
Chip Erase Time		25	50	Sec
Byte Programming Time		9	300	Us
Word Programming Time		11	360	Us
Chip Programming Time	Byte Mode	36	108	Sec
	Word Mode	24	72	Sec
Erase/Program Cycles (1)		100,000		Cycles
Data Retention		20		Years

Notes:

1. Not 100% Tested, Excludes external system level over head.
2. Typical values measured at 25 ° C, 3.3V.
3. Maximum values measured at 85° C, 2.7V.

12. PACKAGE DIMENSION

48-LEAD   TSOP(I) (12x20 mm)

DETAIL F

SECTION B-B

See Detail F
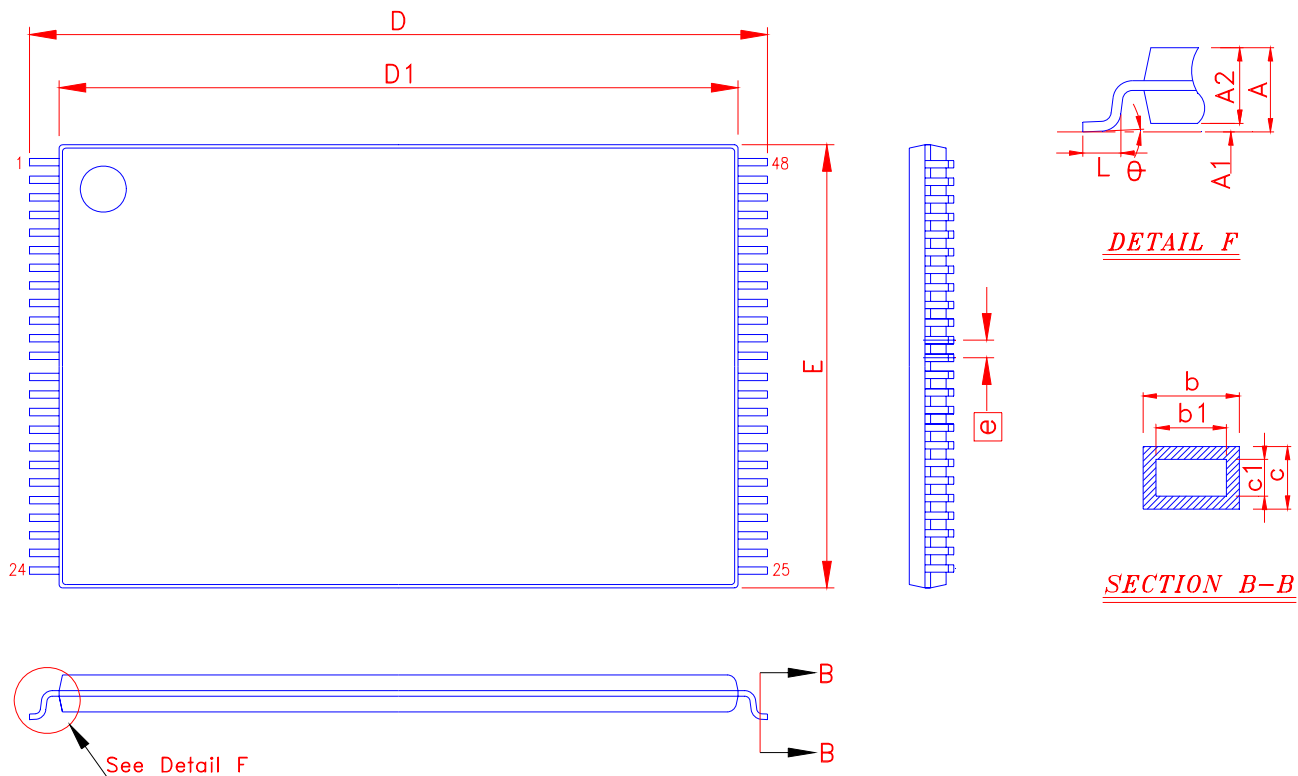
Symbol	Dimension in mm			Dimension in inch			Symbol	Dimension in mm			Dimension in inch		
	Min	Norm	Max	Min	Norm	Max		Min	Norm	Max	Min	Norm	Max
A	-------	-------	1.20	-------	-------	0.047	D	20.00 BSC			0.787 BSC		
A 1	0.05	-------	0.15	0.006	-------	0.002	D 1	18.40 BSC			0.724 BSC		
A 2	0.95	1.00	1.05	0.037	0.039	0.041	E	12.00 BSC			0.472 BSC		
b	0.17	0.22	0.27	0.007	0.009	0.011	e	0.50 BSC			0.020 BSC		
b1	0.17	0.20	0.23	0.007	0.008	0.009	L	0.50	0.60	0.70	0.020	0.024	0.028
c	0.10	-------	0.21	0.004	-------	0.008	θ	0°	-------	8°	0°	-------	8°
c1	0.10	-------	0.16	0.004	-------	0.006							

Revision History

Revision	Date	Description
0.1	2007.05.31	Original
0.2	2007.10.01	Modify Manufacturer ID command
0.3	2007.11.28	Add Unlock Bypass Program description
0.4	2008.01.14	1.Remove Unlock Bypass Program description 2.Add "All Pb-free products are RoHS – Compliant" to FEATURES 3.Modify Icc spec and V_{IH} , V_{IOH1}
1.0	2008.08.20	1. Delete Preliminary 2. Add Revision History 3. Add CFI address (4Dh-4Fh)
1.1	2008.09.30	Modify Chip Erase Time