SR176

13.56MHz Short Range Contactless Memory Chip
176 bit USER EEPROM and 64 bits Unique ID

FEATURES SUMMARY

- ISO 14443 - 2 Type B Air Interface Compliant
- ISO 14443 - 3 Type B Frame Format Compliant
- 13.56MHz Carrier Frequency
- 847.5kHz Subcarrier Frequency
- 106kbit/s Data Transfer
- Data Transfer
    - ASK Modulation from Reader to Tag
    - BPSK Coding from Tag to Reader
- 176-bit EEPROM with Write Protect Feature
- 64-bit Unique Identifier
- READ BLOCK and WRITE BLOCK (16 Bits)
- Internal Tuning Capacitor
- Self-Timed Programming Cycle
- 5ms Programming Time (typical)
- More than 100,000 Erase/Write Cycles
- More than 40 Years Data Retention
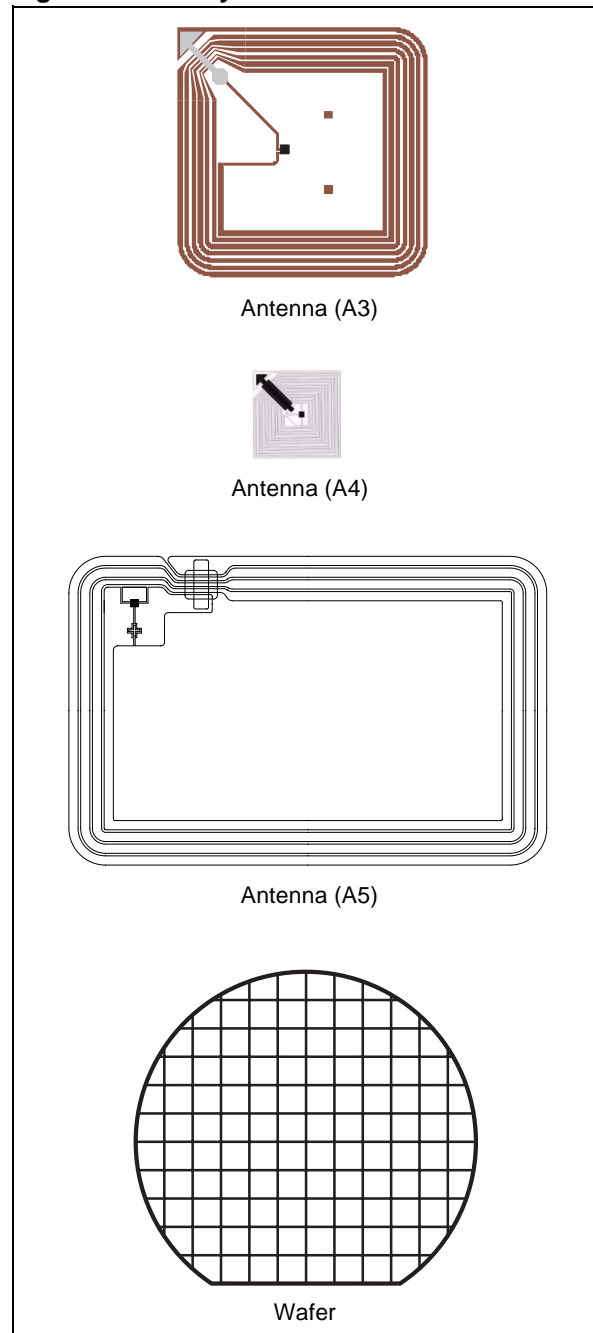
Figure 1. Delivery Forms

Antenna (A3)

Antenna (A4)

Antenna (A5)

Wafer

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SUMMARY DESCRIPTION

The SR176 is a contactless memory, powered by an externally transmitted radio wave. It contains 176 bits of user EEPROM, fabricated with STMicroelectronics CMOS technology. The memory is organized as 16 blocks of 16 bits, of which 11 blocks are user accessible.

The SR176 is accessed via the 13.56MHz carrier. Incoming data are demodulated and decoded from the received Amplitude Shift Keying modulation signal (ASK). The modulation index of this signal is 10%. Outgoing data are generated by load variation using Bit Phase Shift Keying (BPSK) of a 847.5kHz sub-carrier. The Data transfer rate between the SR176 and the reader is 106kbit/s in both reception and emission modes.

The SR176 follows the ISO 14443 part 2 type B recommendation for radio frequency power and signal interfacing.

Figure 2. Pad Connections
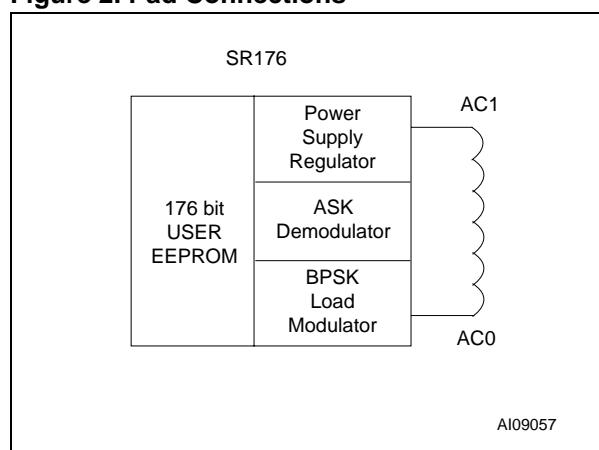
The SR176 is principally designed for short range applications, such as object identification, that need a low cost and non-reusable tag. The SR176 does not include any anti-collision mechanism. It provides an "addressed" selection mechanism to cope with cases where more than one tag is present within the range of the reader.

Table 1. Signal Names

AC1	Antenna Coil
AC0	Antenna Coil

The SR176 contactless EEPROM offers read and write random access in block mode. One block is composed by 16 bits. The device has an instruction set containing seven commands:

■ READ_BLOCK
■ WRITE_BLOCK
■ INITIATE
■ SELECT
■ COMPLETION
■ PROTECT_BLOCK
■ GET_PROTECTION.

The memory array of the SR176 is divided into two main areas: the unique identifier (UID) and the User EEPROM. The UID is a 64-bit unique identifier, written by ST during product manufacture. The User EEPROM is divided into areas which can be write-protected so that they behave as ROM. The write protection is activated using an OTP lock bits register. It is possible to program the SR176 4-bit chip_ID used by the SELECT command. Its default value is fixed at the value 0 (0000_b) by ST. When correctly set, up to sixteen SR176 devices can be selected individually.

Figure 3. Die Floor Plan
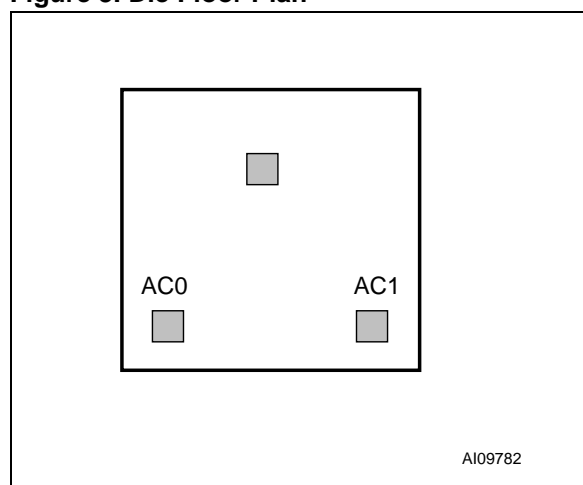
SIGNAL DESCRIPTION

AC1, AC0. AC1 and AC0 pads must be directly bonded to the antenna.

DATA TRANSFER

Input Data Transfer from the Reader to the SR176 (Request Frame)

The reader that accesses the SR176 must generate a 13.56MHz sinusoidal carrier wave on its antenna, with enough energy to "tele-power" the SR176 device. The energy received on the SR176 antenna is transformed to a power supply voltage by a regulator, and to data bits through the ASK demodulator. To decode correctly the information sent to the SR176, the reader must use a 10% amplitude modulation of the 13.56MHz wave, as represented (though not to scale) in Figure 4.. The data transfer rate is 106 kbit/second.

Figure 4. Received Wave Using ASK Modulation

Data Bit Transmit to the SR176

13.5MHz 10% ASK Modulation Generated by the Reader

One bit time is 1/106kHz

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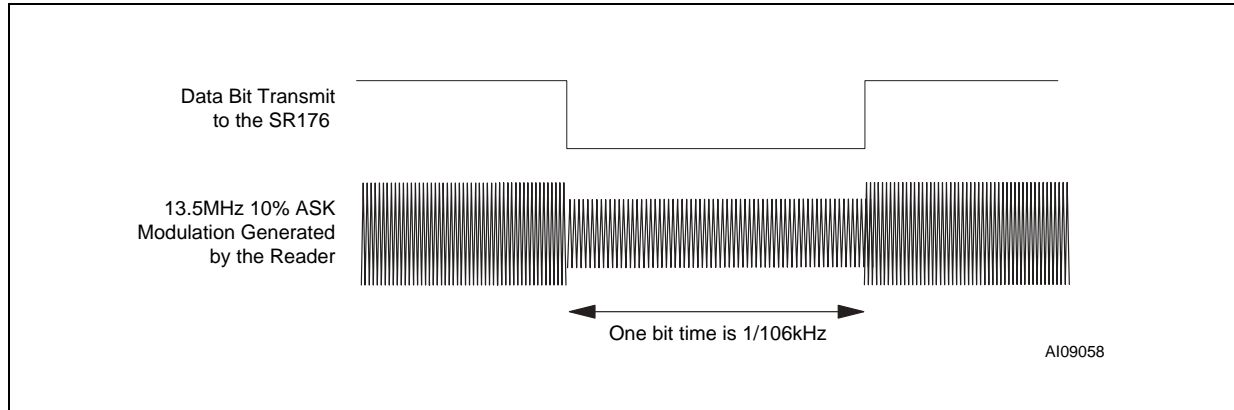
Character Transmission Format for Request Frame

Data Bytes are transmitted and received by the SR176 as 10-bit characters, as shown in Figure 5., with the least significant bit (b_0) transmitted first. These characters, with the addition of the Start Of Frame (SOF) and the End Of Frame (EOF), are grouped to form a Command Frame as shown in Figure 11.. The frame includes an SOF, instructions, addresses, data, a CRC and an EOF as defined by ISO14443-3 type B. If an error is detected during the data transfer, no error frame is generated by the SR176, and the instruction is not executed.

Each bit duration is referred to as an ETU (Elementary Time Unit). One ETU is equal to 9.44µs (1/106kHz).

Request Start Of Frame

The SOF, as shown in Figure 6., consists of:
– one falling edge
– followed by 10 ETUs at logic 0
– followed by one single rising edge
– followed by at least 2 ETUs (but no more than 3 ETUs) at logic 1.

Request End Of Frame

The EOF, as shown in Figure 7., consists of:
– one falling edge
– followed by 10 ETUs set to logic 0
– followed by one single rising edge

Figure 5. SR176 Request Frame Character Format
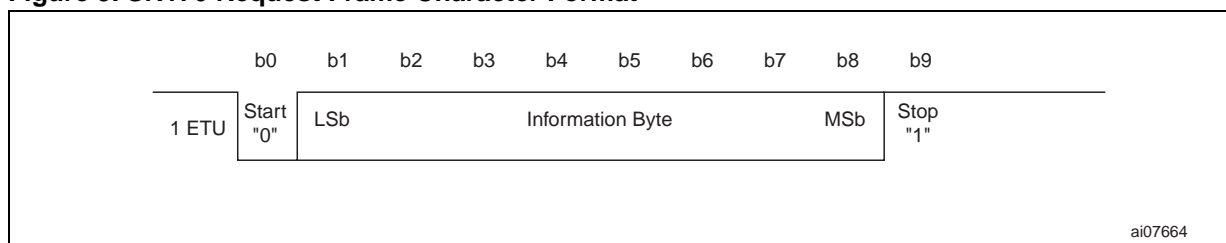
Table 2. Bit Description

Bit	Description	Value
b_0	Start bit used to synchronize the transmission	$b_0 = 0$
b_1 to b_8	Information Byte (command, address or data or CRC)	Information Byte sent, least significant bit first
b_9	Stop bit used to indicate the end of a character	$b_9 = 1$

Figure 6. Request Start Of Frame
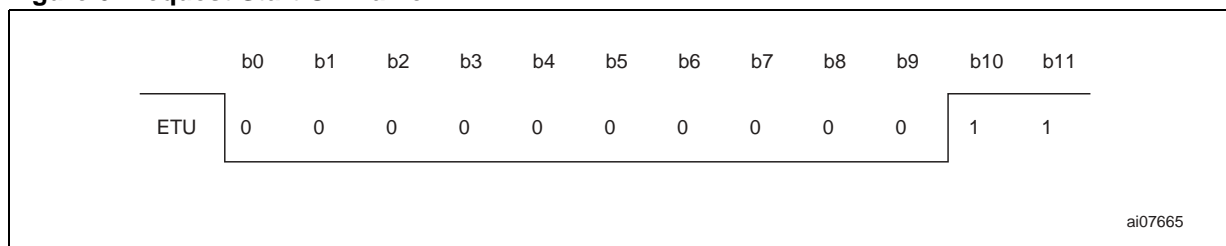
Figure 7. Request End Of Frame
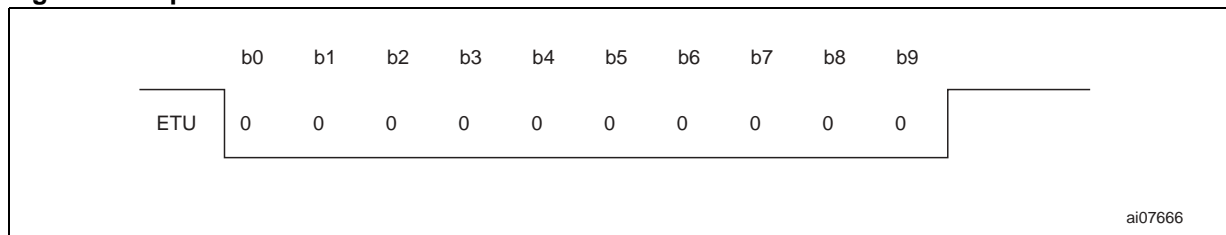
Output Data Transfer from the SR176 to the Reader (Answer Frame)

The SR176 uses load modulation to return data to the reader. This modulation is achieved by modifying the SR176 current flow in its antenna. With appropriate detector circuitry, the reader is able to decode the information from the SR176. The data is transmitted using a BPSK coding of a 847.5kHz sub-carrier frequency, f_S, as specified in ISO14443-2 type B, and as shown in Figure 8..

Character Transmission Format for Answer Frame

The character format is the same as for the input data transfer (Figure 5.). The transmitted frames include an SOF, data, a CRC and an EOF (as shown in Figure 11.). Like the input data transfer, in case of error, the reader does not emit any error code to the SR176, but must be able to detect and manage this situation. The data transfer rate is 106 kbit/second.

Answer Start Of Frame

The SOF, as shown in Figure 9., consists of:

– 10 ETUs at logic 0
– 2 ETUs at logic 1

Answer End Of Frame

The EOF, as shown in Figure 10., consists of:

– 10 ETUs at logic 0
– 2 ETUs at logic 1

Figure 8. Emitted Wave Using BPSK Sub-carrier Modulation
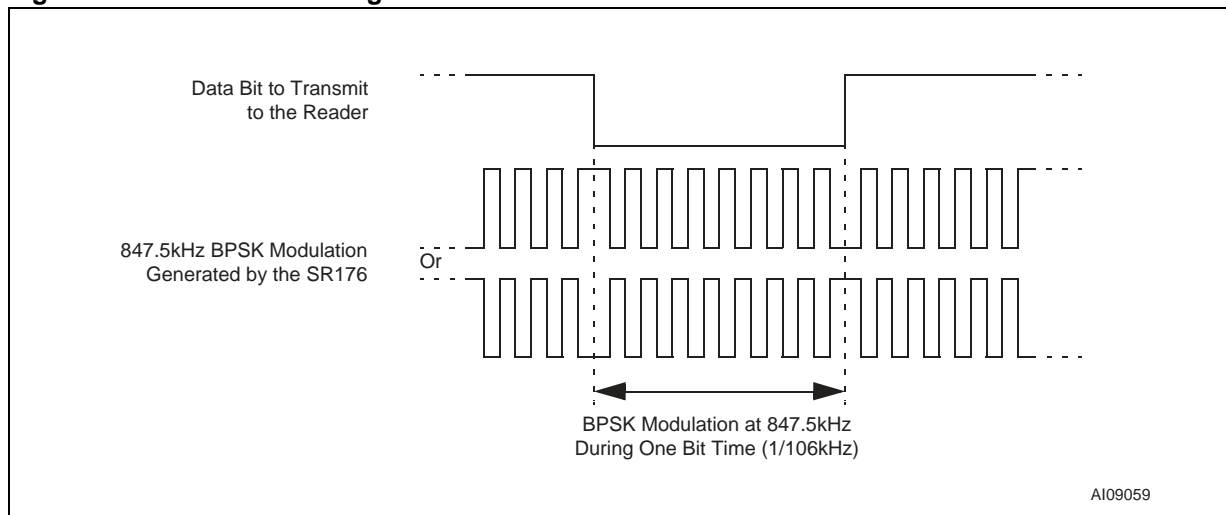
Figure 9. Answer Start Of Frame
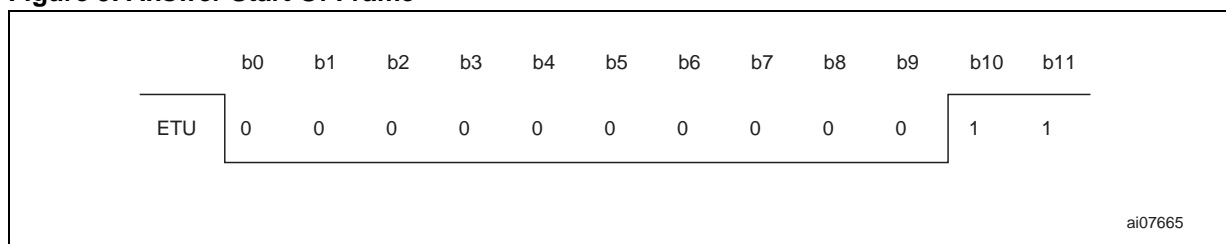
Figure 10. Answer End Of Frame
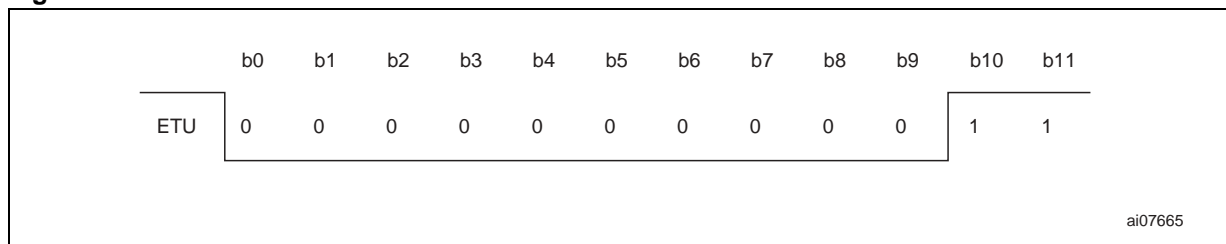
Transmission Frame

Between the Request and the Answer data transfer, there is a guard time without ASK and BPSK modulation, for a minimum period of $t_0 = 128/f_S$. This delay allows the reader to switch from transmission to reception mode, and is applied after each frame. After t_0, the 13.56MHz carrier frequency is modulated by the SR176 at 847.5kHz for a period of $t_1 = 128/f_S$, to allow the reader to synchronize. After t_1, the first phase transition generated by the SR176 represent the start bit ('0') of the Answer SOF. After the falling edge of the Answer EOF, the reader has to wait for the minimum delay, t_2, before sending a new Request Frame to the SR176.

Figure 11. Example of a Complete Transmission Frame
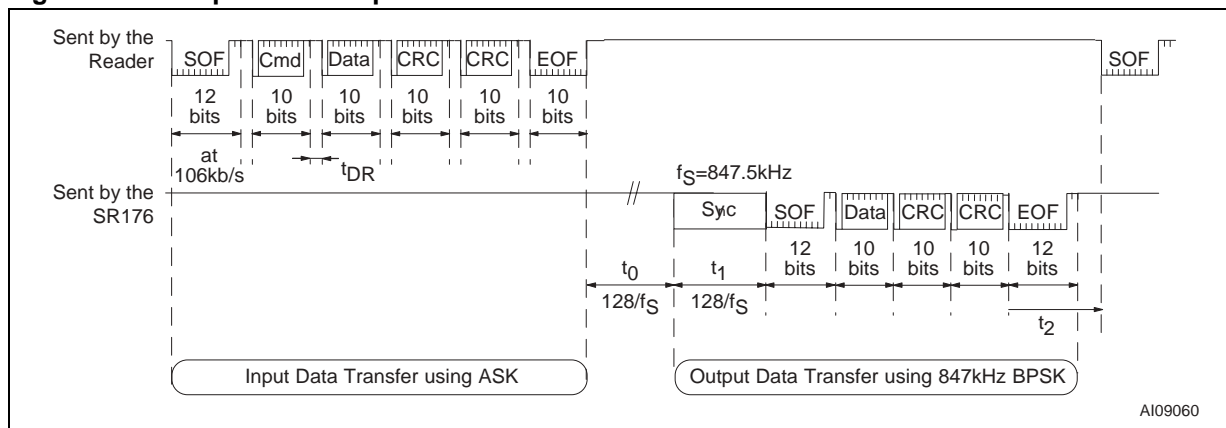
CRC

The 16-bit CRC that is used by the SR176 follows the ISO14443 type B recommendation. For further information, see APPENDIX A.. The initial register content is all ones: FFFFh.

A two-byte CRC is appended to each Request and each Answer, within each frame, before the EOF. The CRC is calculated on all the Bytes after the SOF, up to the CRC field.

On reception of a Request from a reader, the SR176 verifies that the CRC value is valid. If it is invalid, it discards the frame and does not answer the reader.

On reception of an Answer from the SR176, it is recommended that the reader verify that the CRC value is valid. If it is invalid, that choice of actions that are to be performed are the responsibility of the reader designer.

The CRC is transmitted least significant byte first. Each byte is transmitted least significant bit first.

Figure 12. CRC Transmission Rules
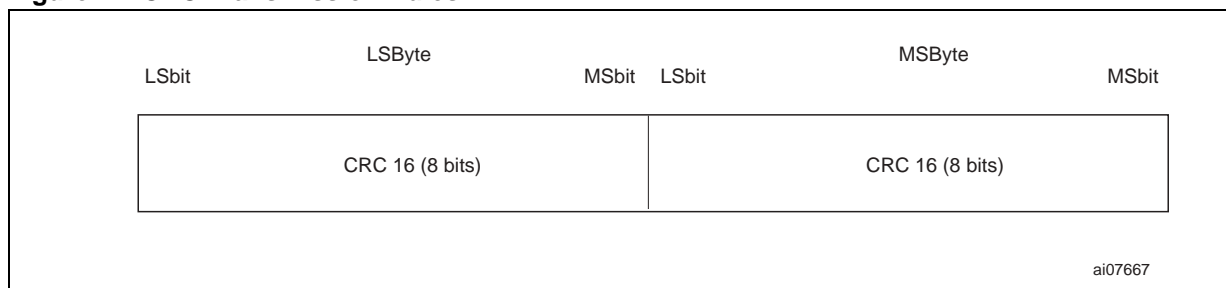
MEMORY MAPPING

The SR176 is organized as 16 blocks of 16 bits, as shown in Figure 13..

The first four blocks, from location 0 to 3, are used to store read-only data. They store the 64-bit UID. This value cannot be modified.

Blocks from locations 4 to 14 offer a 176-bit EE-PROM user area in which the application can store its data values. Block 15 contains the OTP LOCK_REG and the programmed Chip_ID.

The PROTECT_BLOCK command is used to lock write access to blocks 4 to 15 in groups of two blocks.

The GET_PROTECTION command gives the status of the protection of blocks 4 to 15.

Figure 13. SR176 Memory Mapping

Block Address	MSb b15	16-bit block b8 b7	LSb b0	Description
0		UID0		64-bit UID ROM
1		UID1		
2		UID2		
3		UID3		
4		User Area		Lockable EEPROM
5		User Area		
6		User Area		Lockable EEPROM
7		User Area		
8		User Area		Lockable EEPROM
9		User Area		
10		User Area		Lockable EEPROM
11		User Area		
12		User Area		Lockable EEPROM
13		User Area		
14		User Area		Lockable EEPROM
15	OTP LOCK_REG	Reserved	Chip_ID	

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Device Identification

The SR176 has a 64-bit Unique Identifier (UID) which is written by STMicroelectronics during the manufacturing process. The UID is unique for each tag and cannot be altered. It is stored in a Read Only Memory area (ROM). In the SR176, the UID is stored in the first four blocks of the memory in blocks 0 to 3.

Device Selection

After introducing the device in the reader's electromagnetic field, the SR176 has to be activated by a INITIATE command. After this command, the SR176 is in the ACTIVE state and waits for a SE-LECT command, as shown in Figure 14.. The SE-LECT command specifies a 4-bit Chip_ID as a parameter. If the Chip-ID of the SR176 matches this parameter, the SR176 goes in the SELECTED state, and memory blocks become available for READ_BLOCK and WRITE_BLOCK commands up to the reception of a COMPLETION command. If the Chip_ID does not match, the SR176 returns to, or stays in, the DESELECTED state. Write access rights are activated by the SELECT command.

After the Power On of the SR176, if the INITIATE command is not send or is not correctly generated, memory blocks will not be activated, and the SR176 will not respond to any command.

DEVICE OPERATIONS (INSTRUCTIONS)

All instructions, data and the CRC are transmitted to the SR176 in 10-bit character format using ASK modulation. The start bit (b_0 of the 10 bits) is sent first. The command frame received by the SR176 on the antenna is demodulated by the 10% ASK demodulator, and is decoded by internal logic. Prior to any operation, the SR176 must have been previously activated by an INITIATE command (as shown in Figure 14.). Each frame transmitted to the SR176 must start with a Start Of Frame, followed by one or more data characters, and is end-ed by two CRC bytes and the End Of Frame. When an invalid frame is decoded by the SR176 (because of a wrong instruction or CRC error), the memory does not send any error code.

When a valid frame is received, the SR176 may have to send back data to the reader. For this, it sends 10-bit characters back, with SOF, CRC and EOF, using the BPSK coding. The transfer is end-ed by the SR176 sending the EOF.

Figure 14. State Transition Diagram
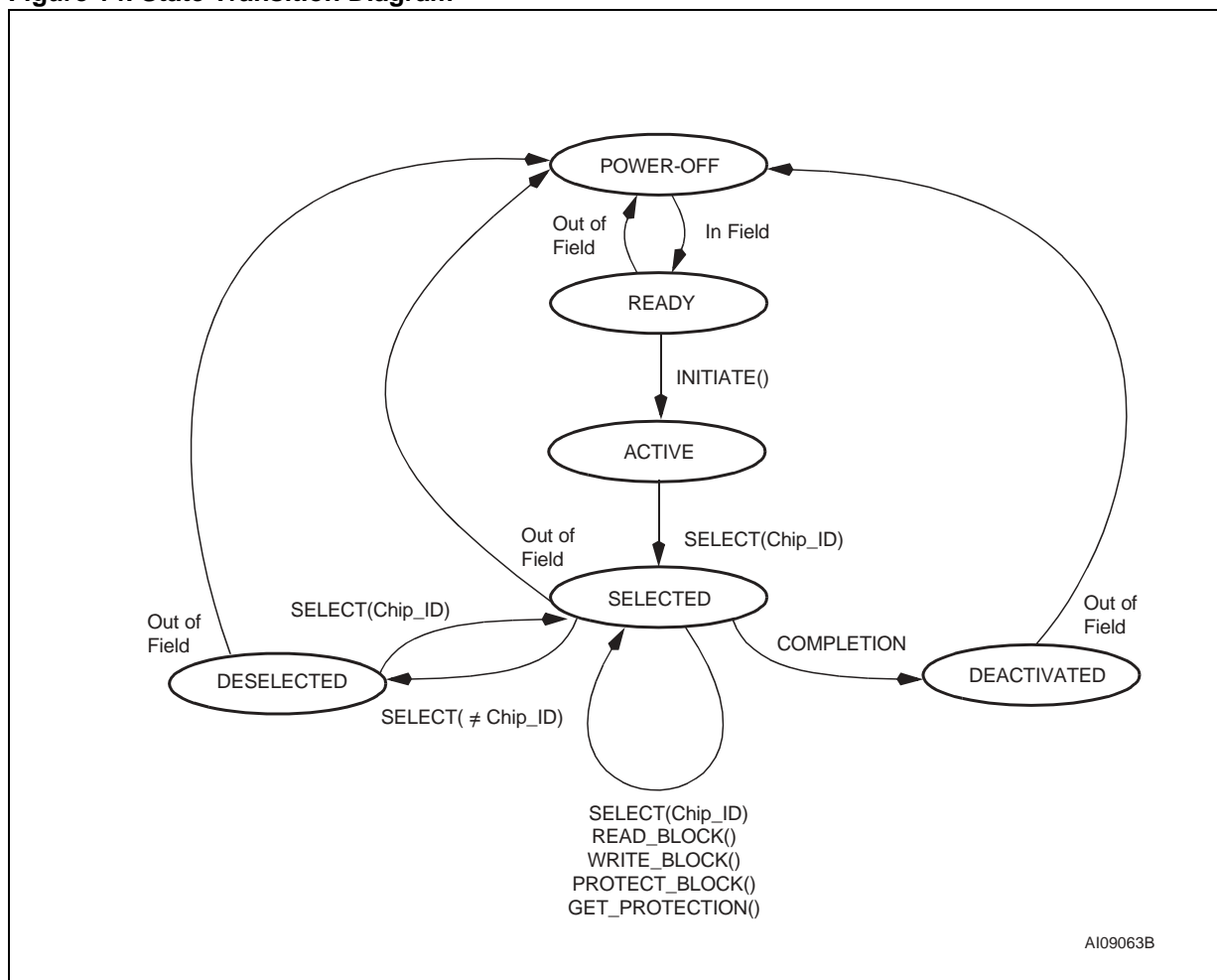
INITIATE()

Command Code = 06h,00h

Prior to any other command, the SR176 must be activated by an INITIATE command. All other commands sent to the SR176 before the INITIATE are ignored. In response to receiving the INITIATE command, the SR176 sends back its Chip_ID, using an 8-bit format (Figure 18.).

Upon receiving a valid INITIATE command, the SR176 switches to the ACTIVE state, where it will not answer to any new INITIATE command. Once In the ACTIVE state, the SR176 will remain in this state until it receives a valid SELECT command.

Request parameters (Figure 15.):

– none

Response parameters (Figure 16.):

– Chip_ID (formatted as shown in Figure 17.)

Figure 15. INITIATE Request Format

SOF	INITIATE	CRC$_L$	CRC$_H$	EOF
	06h 00h	8 bits	8 bits	

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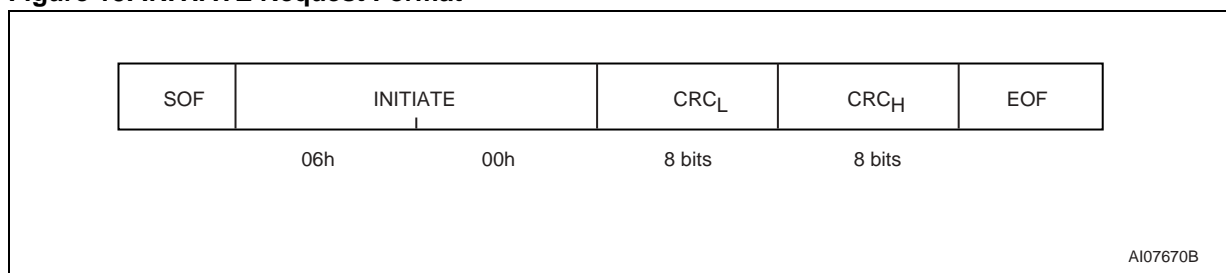
Figure 16. INITIATE Response Format

SOF	Chip_ID	CRC$_L$	CRC$_H$	EOF
	4 reserved bits + 4-bit ID	8 bits	8 bits	

AI07701B
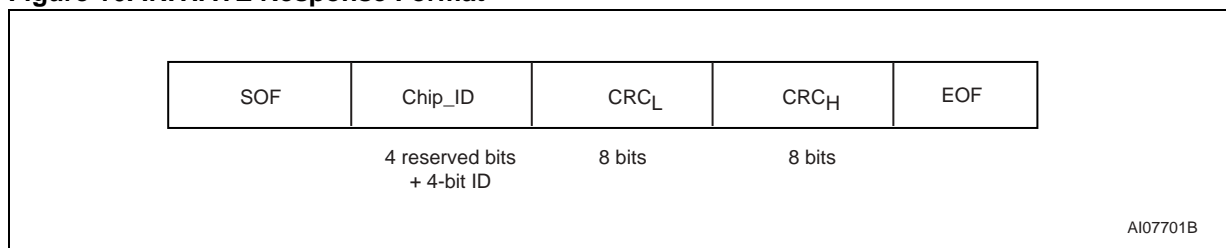
Figure 17. 8-bit Chip_ID Format

b7	b6	b5	b4	b3	b2	b1	b0
Reserved bits (block 15)				b3 Block 15 b0			
				4-bit Chip_ID of the SR176			

AI07700B
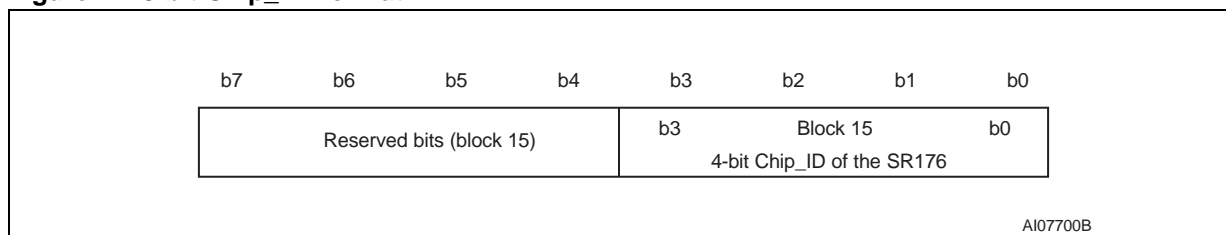
Figure 18. INITIATE Frame Exchange between Reader and SR176

Reader | SOF | 06h | 00h | CRC$_L$ | CRC$_H$ | EOF |

SR176 | t_0 | t_1 | SOF | Chip_ID | CRC$_L$ | CRC$_H$ | EOF |

AI09783
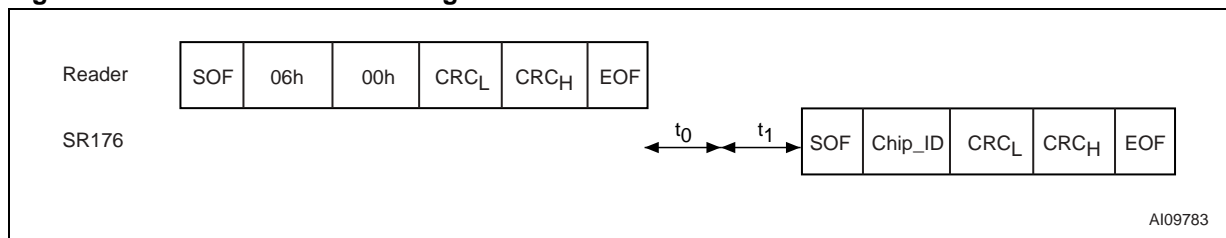
SELECT(Chip_ID)

Command Code = 0Eh,(X.ID)h

Prior to any memory access, the SR176 must have been set in the SELECTED state by a SELECT() command. All other commands sent to the SR176 before the SELECT(), except INITIATE(), are ignored. In response to receiving the SELECT() command, the SR176 sends back its Chip_ID, using an 8-bit format (Figure 22.).

Any SR176 that is already in the SELECTED state, and which receives a SELECT() command that does not match its Chip_ID, is automatically put in the DESELECTED state. The SR176 stays in the SELECTED state up to the reception of a COMPLETION or a SELECT with a non-matching Chip_ID.

After a PROTECT_BLOCK command, it is necessary to send a new SELECT command in order to load enable the write access again in the internal logic. If a SELECT is not send, the SR176 keeps the previous write access rights.

Request parameters (Figure 19.):

– Chip_ID (formatted as shown in Figure 21.)

Response parameters (Figure 20.):

– Chip_ID (formatted as shown in Figure 21.)

Figure 19. SELECT Request Format

SOF	SELECT	Chip_ID	CRC$_L$	CRC$_H$	EOF
	0Eh	4 reserved bits + 4-bit ID	8 bits	8 bits	

AI07702B
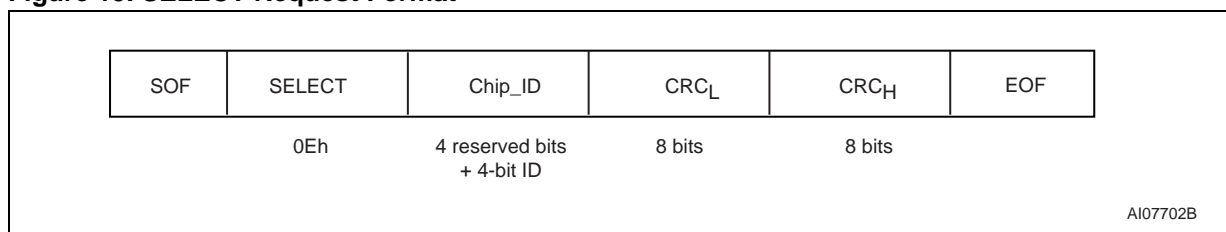
Figure 20. SELECT Response Format

SOF	Chip_ID	CRC$_L$	CRC$_H$	EOF
	4 reserved bit + 4-bit ID	8 bits	8 bits	

AI07703B
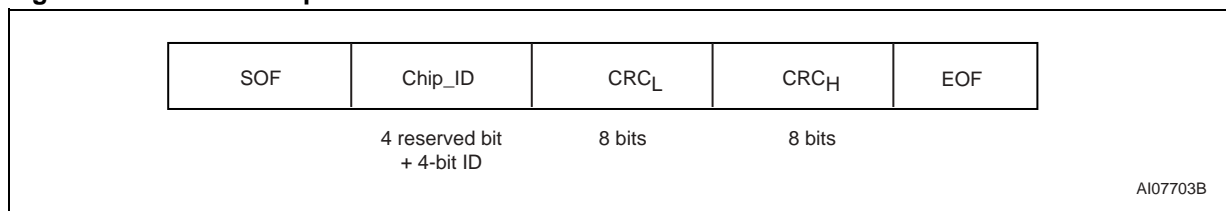
Figure 21. 8-bit Chip_ID Format

b7	b6	b5	b4	b3	b2	b1	b0
Test bits (block 15)				b3 Block 15 b0			
				4-bit Chip_ID of the SR176			

AI07704B
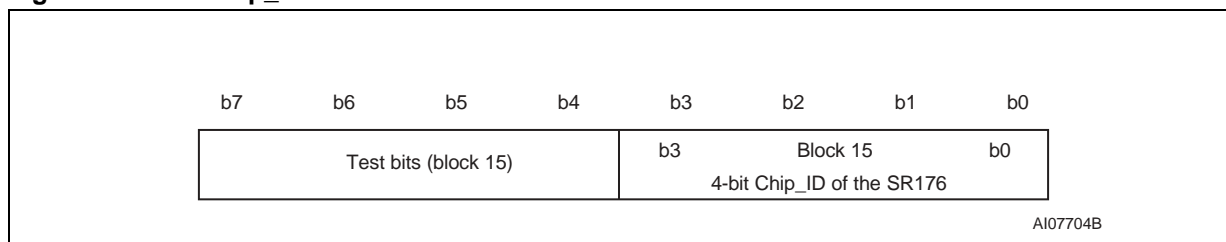
Figure 22. SELECT Frame Exchange between Reader and SR176

Reader	SOF	0Eh	Chip_ID	CRC$_L$	CRC$_H$	EOF

SR176 t_0 t_1 | SOF | Chip_ID | CRC$_L$ | CRC$_H$ | EOF |

AI09784
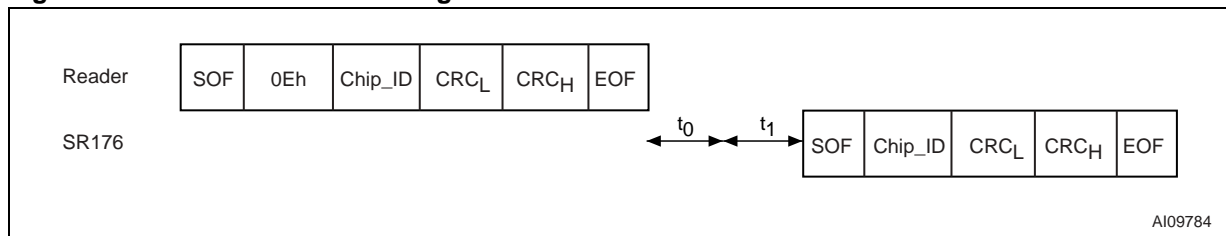
COMPLETION

Command Code = 0Fh

When the COMPLETION command is received, the SR176 is put in the DEACTIVED state, and does not decode any new commands up to a Power-Off, and a new Power-On has occurred. This allows a new SR176 to be activated by an INITIATE command, without needing to remove the previous ones. The SR176 does not generate any response when it executes a COMPLETION command (Figure 24.).

Prior to any COMPLETION command, the SR176 must have been put in the SELECTED mode by a SELECT command. A SR176 which was not selected does not interpret this command.

Request parameters (Figure 23.):

– none

Figure 23. COMPLETION Request Format

SOF	COMPLETION	CRC$_L$	CRC$_H$	EOF
	0Fh	8 bits	8 bits	

AI07679B
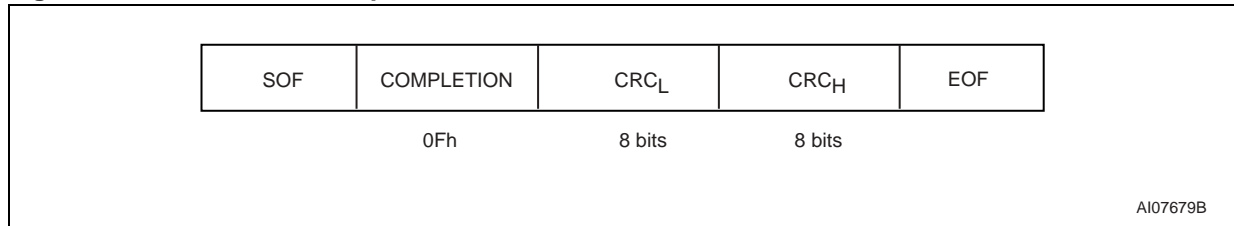
Figure 24. COMPLETION Frame Exchange between Reader and SR176

Reader	SOF	0Fh	CRC$_L$	CRC$_H$	EOF

SR176		No Response

AI09785
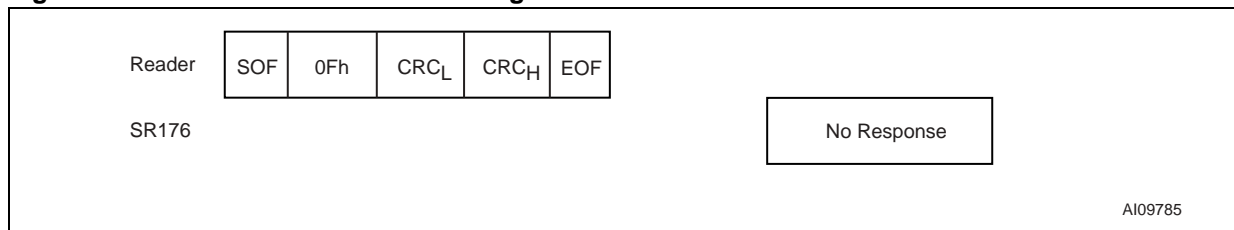
READ_BLOCK

Command Code = 08h,(X.AD)

When receiving the READ_BLOCK command, the SR176 reads the requested block and sends back its 16-bit value in response (Figure 27.). The AD value of the four least significant bits of the address code, (X.AD) (b_3 to b_0) represents the block address to be read. For example, address 06h sends back the value of block 6.

Prior to any READ_BLOCK command, the SR176 must have been set into the SELECTED state.

Request parameters (Figure 25.):

– ADDRESS: to specify an address block from 00h to 0Eh

Response parameters (Figure 26.):

– DATA$_L$: least significant Byte

– DATA$_H$: most significant Byte

Read the 64-bit UID

To read the complete 64-bit UID value from the SR176, the reader must provide a sequence of four READ_BLOCK commands, in the following order (Figure 28.):

– READ_BLOCK @ 0 to get UID0

– READ_BLOCK @ 1 to get UID1

– READ_BLOCK @ 2 to get UID2

– READ_BLOCK @ 3 to get UID3

Figure 25. READ_BLOCK Request Format

SOF	READ_BLOCK	ADDRESS	CRC$_L$	CRC$_H$	EOF
	08h	4 zero-bits + 4-bit address	8 bits	8 bits	

AI07705B
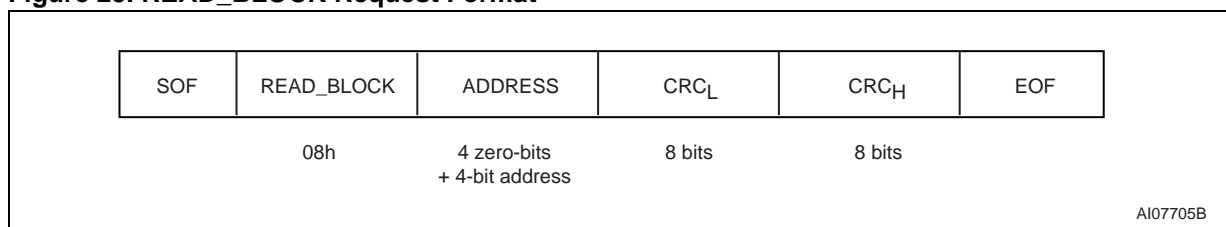
Figure 26. READ_BLOCK Response Format

SOF	DATA$_L$	DATA$_H$	CRC$_L$	CRC$_H$	EOF
	8 bits	8 bits	8 bits	8 bits	

AI07706B
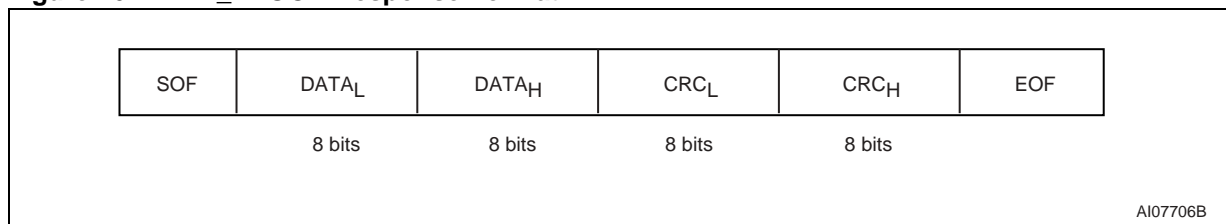
Figure 27. READ_BLOCK Frame Exchange between Reader and SR176

AI07707B
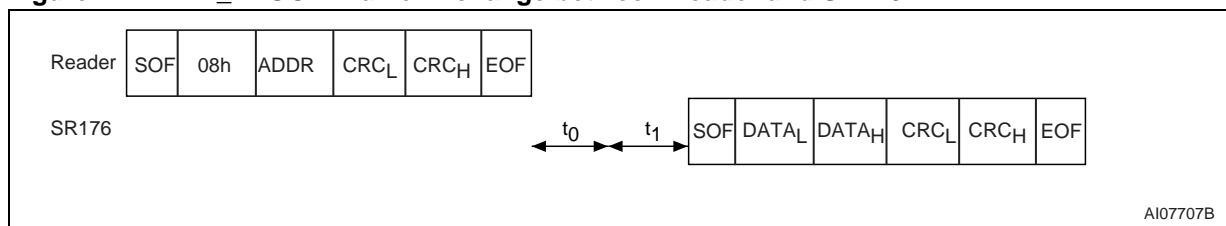
Figure 28. 64-bit UID Storage Format

AI07708B
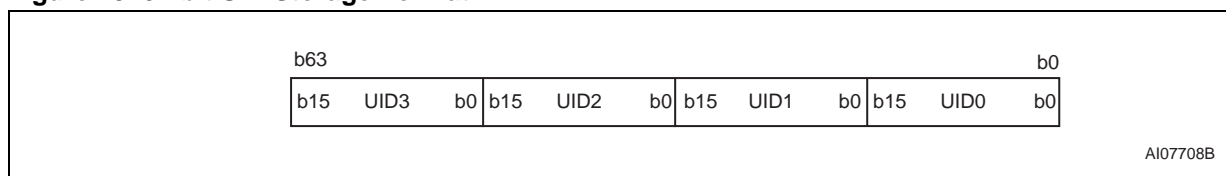
WRITE_BLOCK

Command Code = 09h,(X.AD)

Prior to any WRITE_BLOCK command, the SR176 must have been set into the SELECTED state.

When executing the WRITE_BLOCK command, the SR176 overwrites the contents of the addressed block with the 16-bit value that was sent in the command, provided that the block is available and not write protected. The AD value of the four least significant bits of the address code (X.AD) (b_3 to b_0) represents the block address. For example, address 06h specifies that the data should be written in block 6. The SR176 does not generate any response when it executes a WRITE_BLOCK command (Figure 30.). The reader must check after the programming time, t_W, that the data bits were correctly programmed.

Block addresses between 0 to 3 cannot be accessed using the WRITE_BLOCK command (the command has no effect on these blocks). Write access to block 15 is described in the section on the PROTECT_BLOCK command.

Request parameters (Figure 29.):

– ADDRESS: address block from 4 to 14
– DATA$_L$: least significant Byte
– DATA$_H$: most significant Byte

Figure 29. WRITE_BLOCK Request Format

SOF	WRITE_BLOCK	ADDRESS	DATA$_L$	DATA$_H$	CRC$_L$	CRC$_H$	EOF
	09h	4 zero-bits + 4-bit address	8 blts	8 blts	8 blts	8 blts	

AI07709B
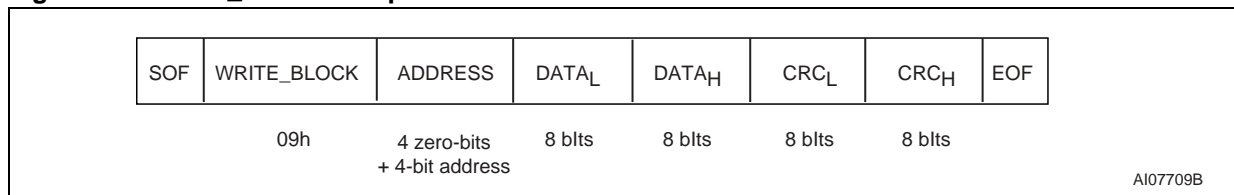
Figure 30. WRITE_BLOCK Frame Exchange between Reader and SR176

Reader	SOF	09h	ADDR	DATA$_L$	DATA$_H$	CRC$_L$	CRC$_H$	EOF		
SR176										No Response

AI07710B
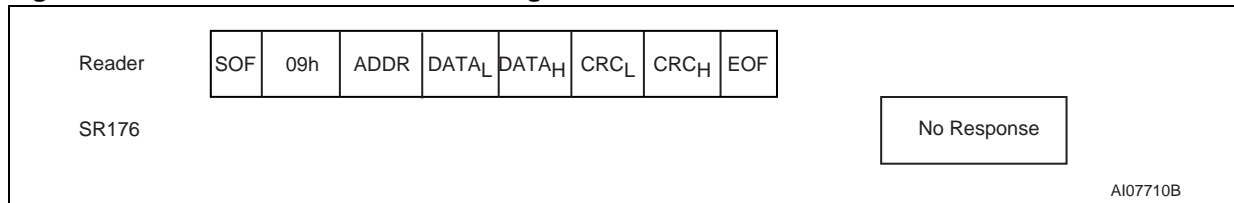
PROTECT_BLOCK

Command Code = 09h,0Fh,00h,LOCK_REG

Prior to any PROTECT_BLOCK command, the SR176 must have been set into the SELECTED state.

The PROTECT_BLOCK command allows the write access to be blocked to memory blocks 4 to 15. It must be followed by a SELECT() command. This re-initializes the write protection conditions to blocks 4 to 15. Until then, the new protection setting is not taken into account by the SR176 logic. The SR176 does not generate any response when it executes a PROTECT_BLOCK command (Figure 32.). The reader must use the

GET_PROTECTION command to get the information on the protection status.

The OTP LOCK_REG controls the write-protection on blocks 4 to 15, and is, itself, One-Time Programmable. Each '1' in the LOCK_REG parameter indicates that the corresponding bit in the OTP LOCK_REG should be set. Each '0' indicates that the corresponding bit should be left unchanged. Once a bit in the OTP LOCK_REG has been set to '1', it is not possible to reset it to '0' and the corresponding memory blocks are forever write protected (and behaves like ROM).

Request parameters (Figure 31.):

– LOCK_REG (Table 3.)

Figure 31. PROTECT_BLOCK Request Format

SOF	PROTECT_BLOCK	LOCK_REG	CRC$_L$	CRC$_H$	EOF
	09h 0Fh 00h	8 blts	8 blts	8 blts	

AI07711B
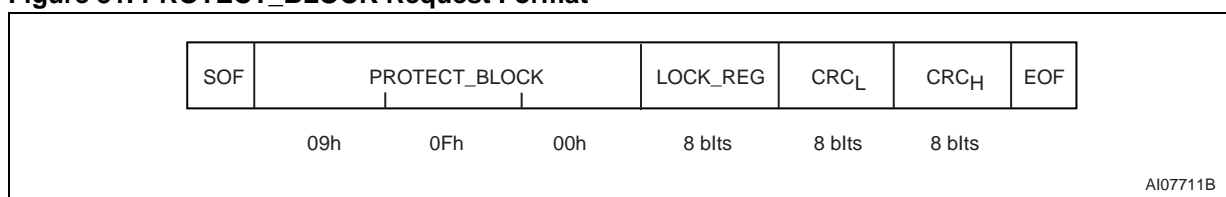
Table 3. Bits in the LOCK_REG Parameter, and in the OTP LOCK_REG Register

Lock Reg Parameter Bit	Meaning	Block 15 Bit	Meaning
b_7	1: set b_{15} of Block 15 to '1' 0: leave it unchanged	b_{15}	1: Write-Protect Blocks 14 and 15 0: Allow write access
b_6	1: set b_{14} of Block 15 to '1' 0: leave it unchanged	b_{14}	1: Write-Protect Blocks 12 and 13 0: Allow write access
b_5	1: set b_{13} of Block 15 to '1' 0: leave it unchanged	b_{13}	1: Write-Protect Blocks 10 and 11 0: Allow write access
b_4	1: set b_{12} of Block 15 to '1' 0: leave it unchanged	b_{12}	1: Write-Protect Blocks 8 and 9 0: Allow write access
b_3	1: set b_{11} of Block 15 to '1' 0: leave it unchanged	b_{11}	1: Write-Protect Blocks 6 and 7 0: Allow write access
b_2	1: set b_{10} of Block 15 to '1' 0: leave it unchanged	b_{10}	1: Write-Protect Blocks 4 and 5 0: Allow write access
b_1	1: set b_9 of Block 15 to '1' 0: leave it unchanged	b_9	1: Write-Protect Blocks 2 and 3 0: Allow write access
b_0	1: set b_8 of Block 15 to '1' 0: leave it unchanged	b_8	1: Write-Protect Blocks 0 and 1 0: Allow write access

Figure 32. PROTECT_BLOCK Frame Exchange between Reader and SR176

| Reader | SOF | 09h | 0Fh | 00h | LOCK_REG | CRC$_L$ | CRC$_H$ | EOF |

SR176   No Response

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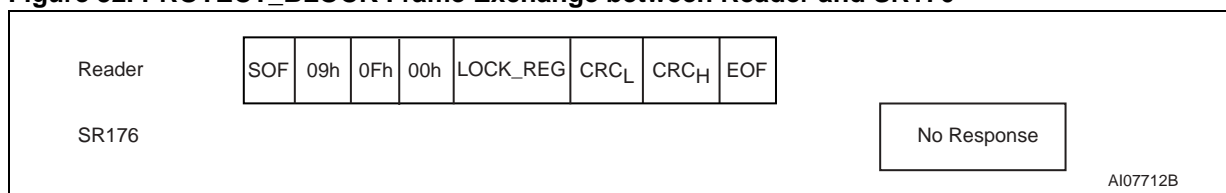
GET_PROTECTION

Command Code = 08h,0Fh

Prior to any GET_PROTECTION, the SR176 must have been set into the SELECTED state.

GET_PROTECTION allows the protection status of memory blocks 4 to 15 to be read. When receiving the GET_PROTECTION command, the SR176 responds with the 16-bit value of block 15

(Figure 35.). It gives the status of the LOCK_REG and the Chip_ID of the SR176.

Request parameters (Figure 33.):
–   none

Response parameters (Figure 34.):
–   Chip_ID: least significant Byte
–   LOCK_REG: most significant Byte
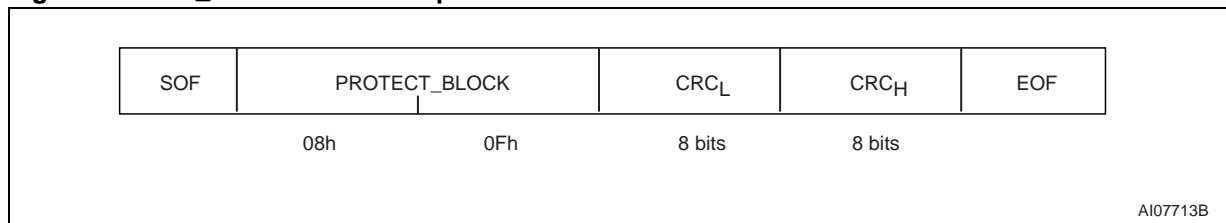
Figure 33. GET_PROTECTION Request Format

SOF	PROTECT_BLOCK		CRC$_L$	CRC$_H$	EOF
	08h	0Fh	8 bits	8 bits	

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Figure 34. GET_PROTECTION Response Format

SOF	Chip_ID	LOCK_REG	CRC$_L$	CRC$_H$	EOF
	8 bits	8 bits	8 bits	8 bits	

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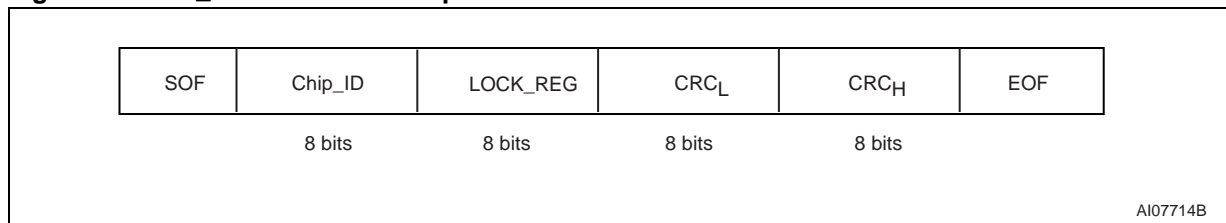
Table 4. Chip_ID and LOCK_REG

Block 15 Bits	Response Parameter Bits	Meaning
b_{15}	LOCK_REG b_7	1: Blocks 14 and 15 are write-protected (0: indicates that write-access is allowed)
b_{14}	LOCK_REG b_6	1: Blocks 12 and 13 are write-protected (0: indicates that write-access is allowed)
b_{13}	LOCK_REG b_5	1: Blocks 10 and 11 are write-protected (0: indicates that write-access is allowed)
b_{12}	LOCK_REG b_4	1: Blocks 8 and 9 are write-protected (0: indicates that write-access is allowed)
b_{11}	LOCK_REG b_3	1: Blocks 6 and 7 are write-protected (0: indicates that write-access is allowed)
b_{10}	LOCK_REG b_2	1: Blocks 4 and 5 are write-protected (0: indicates that write-access is allowed)
b_9	LOCK_REG b_1	1: Blocks 2 and 3 are write-protected (0: indicates that write-access is allowed)
b_8	LOCK_REG b_0	1: Blocks 0 and 1 are write-protected (0: indicates that write-access is allowed)
b_4 to b_7	Chip_ID b_4 to b_7	Reserved
b_0 to b_3	Chip_ID b_0 to b_3	Chip_ID (Value from 0h to Fh)

Figure 35. GET_PROTECTION Frame Exchange between Reader and SR176

| Reader | SOF | 08h | 0Fh | CRC_L | CRC_H | EOF |

| SR176 | | t_0 | t_1 | SOF | Chip_ID | LOCK_REG | CRC_L | CRC_H | EOF |

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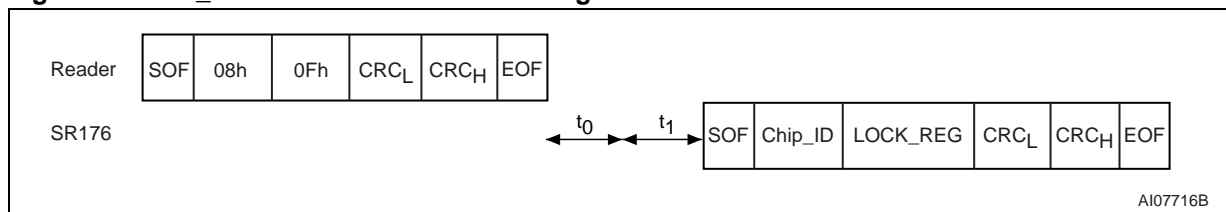
Power On State

After Power On, the SR176 is in the following state:

– The device is in the low power mode.

– The device is deselected.

– The device presents its highest impedance to the reader antenna field.

– It will not answer to any command except INITIATE.

SR176 COMMAND SUMMARY

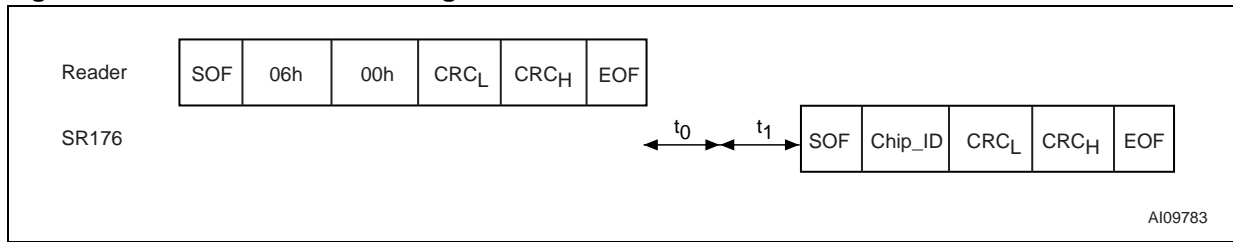### Figure 36. INITIATE Frame Exchange between Reader and SR176

Reader	SOF	06h	00h	CRC_L	CRC_H	EOF

SR176 t_0 t_1 | SOF | Chip_ID | CRC_L | CRC_H | EOF |

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Figure 37. SELECT Frame Exchange between Reader and SR176

Reader	SOF	0Eh	Chip_ID	CRC_L	CRC_H	EOF

SR176 t_0 t_1 | SOF | Chip_ID | CRC_L | CRC_H | EOF |

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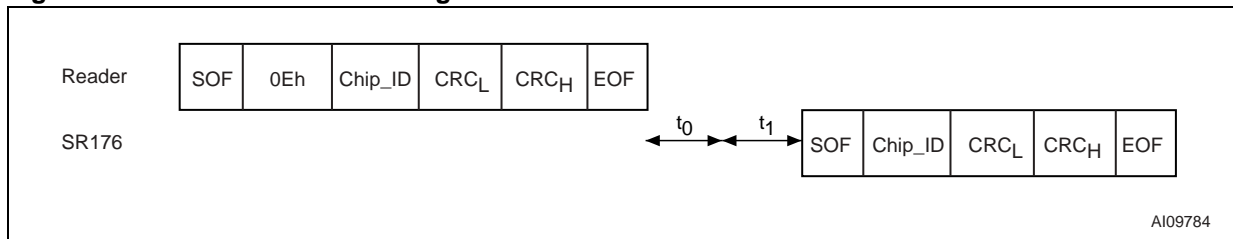
Figure 38. COMPLETION Frame Exchange between Reader and SR176

Reader	SOF	0Fh	CRC_L	CRC_H	EOF

SR176   No Response

AI09785
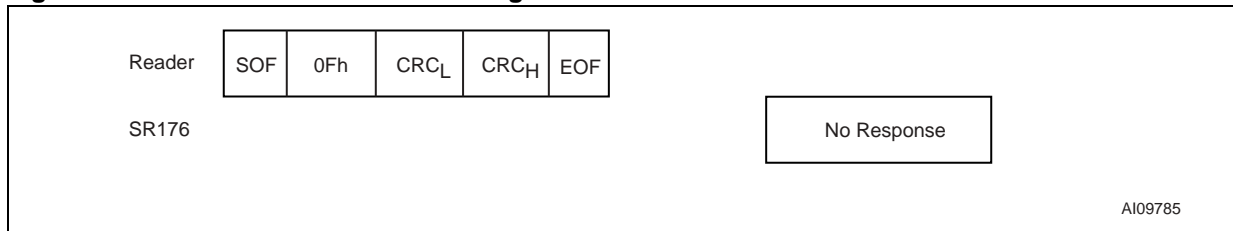
Figure 39. READ_BLOCK Frame Exchange between Reader and SR176

Reader	SOF	08h	ADDR	CRC_L	CRC_H	EOF

SR176 t_0 t_1 | SOF | $DATA_L$ | $DATA_H$ | CRC_L | CRC_H | EOF |

AI07707B
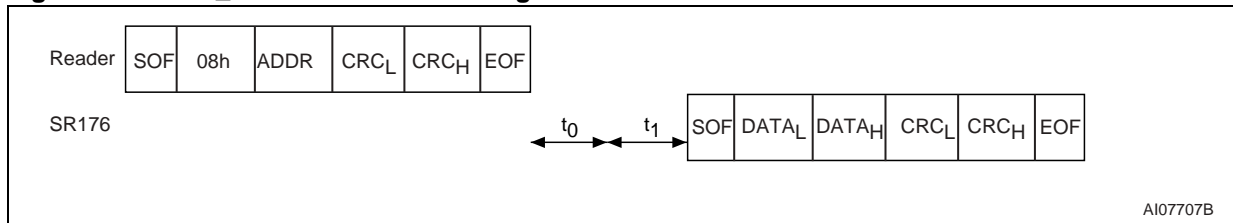
Figure 40. WRITE_BLOCK Frame Exchange between Reader and SR176

Reader	SOF	09h	ADDR	$DATA_L$	$DATA_H$	CRC_L	CRC_H	EOF

SR176   No Response

AI07710B
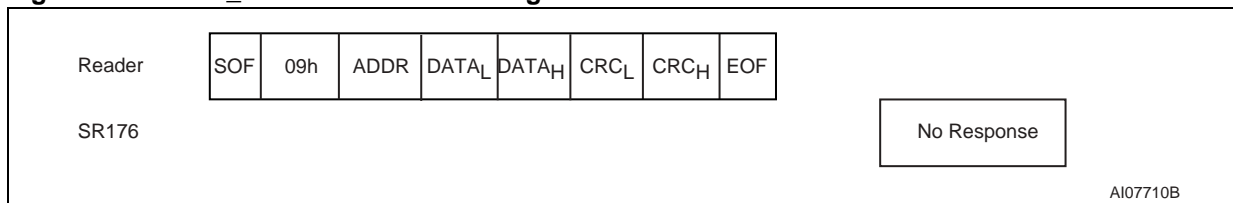
Figure 41. PROTECT_BLOCK Frame Exchange between Reader and SR176

Reader	SOF	09h	0Fh	00h	LOCK_REG	CRC$_L$	CRC$_H$	EOF		

| SR176 | | | | | | | | No Response | |

AI07712B
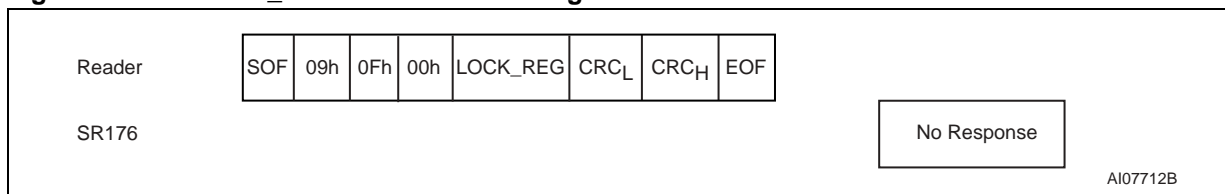
Figure 42. GET_PROTECTION Frame Exchange between Reader and SR176

Reader	SOF	08h	0Fh	CRC$_L$	CRC$_H$	EOF

SR176 t_0 t_1 | SOF | Chip_ID | LOCK_REG | CRC$_L$ | CRC$_H$ | EOF |

AI07716B
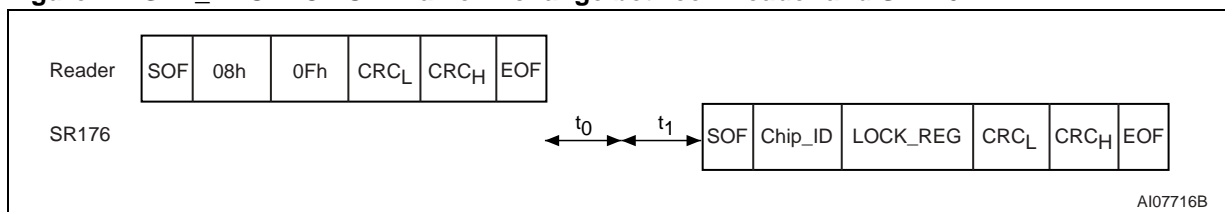
MAXIMUM RATING

Stressing the device above the rating listed in the Absolute Maximum Ratings" table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not im-

plied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

Table 5. Absolute Maximum Ratings

Symbol	Parameter		Min.	Max.	Unit
T_{STG}, h_{STG}, t_{STG}	Storage Conditions	Wafer	15	25	°C
				23	months
			kept in its antistatic bag		
		A3, A4, A5	15	25	°C
			40%	60%	RH
				2	years
I_{CC}	Supply Current on AC0 / AC1		−20	20	mA
V_{MAX}	Input Voltage on AC0 / AC1		−7	7	V
V_{ESD}	Electrostatic Discharge Voltage	Machine model [1]	−100	100	V
		Human Body model [1]	−1000	1000	V
		Human Body model [2]	−4000	4000	V

Note: 1. Mil. Std. 883 - Method 3015
      2. ESD test: ISO10373-6 for proximity cards

DC AND AC PARAMETERS

This section summarizes the operating and measurement conditions, and the DC and AC characteristics of the device. The parameters in the DC and AC Characteristic tables that follow are derived from tests performed under the Measurement Conditions summarized in the relevant tables. Designers should check that the operating conditions in their circuit match the measurement conditions when relying on the quoted parameters.

Table 6. Operating Conditions

Symbol	Parameter		Min.	Max.	Unit
T_A	Ambient Operating Temperature	Wafer	−20	85	°C
		A3, A4, A5	−20	85	°C

Table 7. DC Characteristics

Symbol	Parameter	Condition	Min	Max	Unit
V_{CC}	Regulated Voltage		2.5	3.5	V
V_{RET}	Retromodulation Induced Voltage	ISO10373-6	20		mV
C_{TUN}	Internal Tuning Capacitor	70pF at 13.56MHz	64	78	pF

Table 8. AC Characteristics

Symbol	Parameter	Condition	Min	Max	Unit
f_{CC}	External RF Signal Frequency		13.553	13.567	MHz
$MI_{CARRIER}$	Carrier Modulation Index	MI=(A-B)/(A+B)	10	14	%
t_{RFR}, t_{RFF}	10% Rise and Fall time	10% to 90%	0.5	1.5	µs
t_{RFSBL}	10% Modulation Pulse Width	ETU = 128/f_{CC}	9.44		µs
t_{JIT}	ASK modulation Data Jitter	Coupler to SR176	- 2	+ 2	µs
$t_{MIN CD}$	Minimum Time from Carrier Generation to First Data	From H-field Min	40		µs
f_S	Subcarrier Frequency	f_{CC}/16	847.5		kHz
t_0	Antenna Reversal delay	128/f_S	151		µs
t_1	Synchronization delay	128/f_S	151		µs
t_2	Answer to New Request delay	14 etu	132		µs
t_{DR}	Time Between Request Characters	Coupler to SR176	0	57	µs
t_{DA}	Time Between Answer characters	SR176 to Coupler	0		µs
t_W	Programming Time for WRITE			5	ms

Note: 1. All timing measurements were performed on a reference antenna with the following characteristics:
External size: 75mm x 48mm
Number of turns: 3
Width of conductor: 1mm
Space between 2 conductors: 0.4mm
Value of the coil: 1.4µH
Tuning Frequency: 14.4MHz.

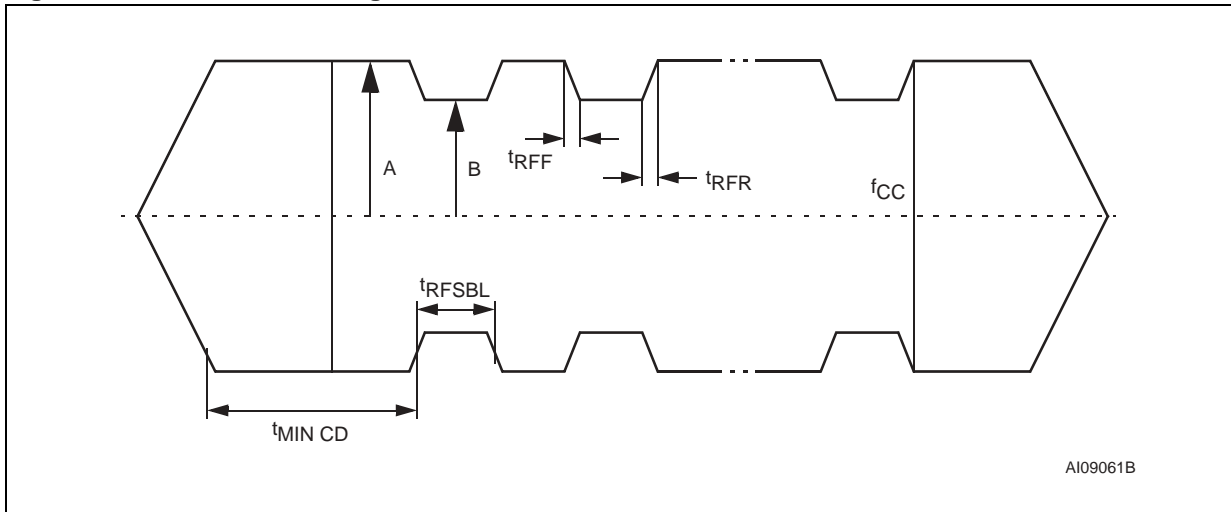**Figure 43. ASK Modulated Signal from the Reader to the Contactless Device**

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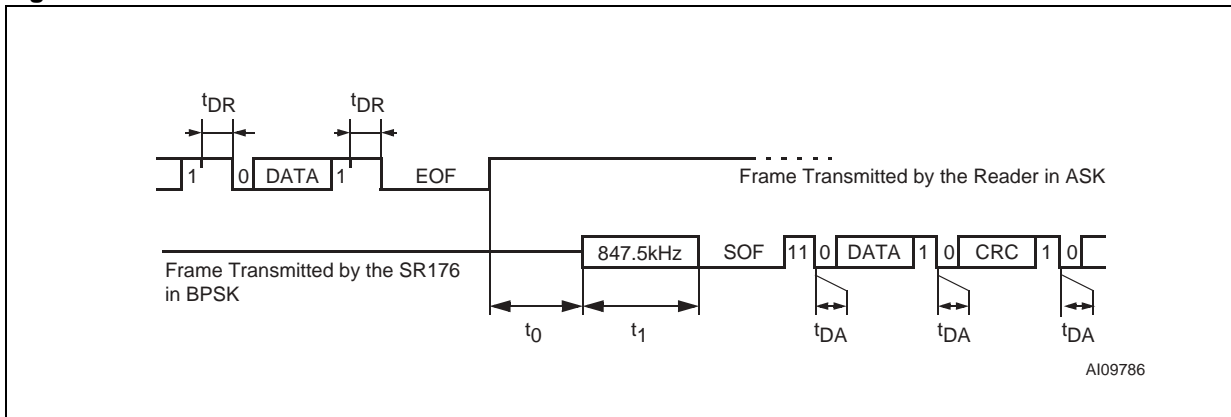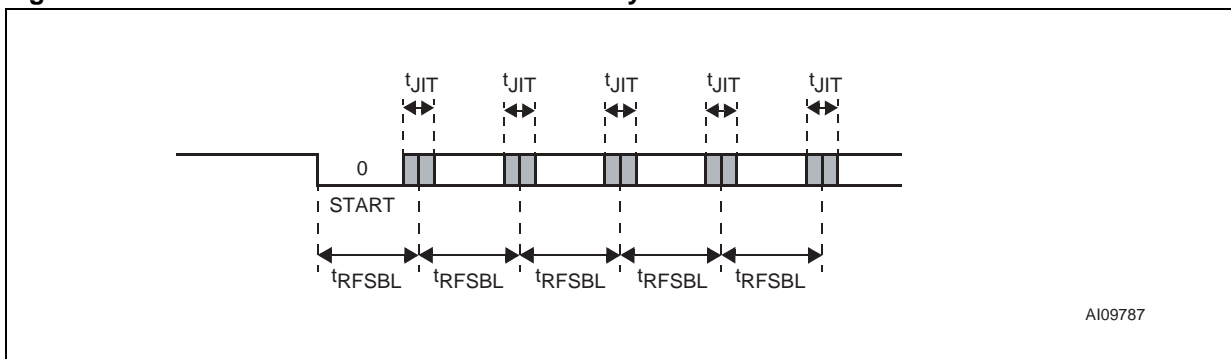**Figure 44. Frame Transmission between the Reader and the Contactless Device**

AI09786

Figure 45. Data Jitter on the Frame Transmitted by the Reader in ASK

AI09787

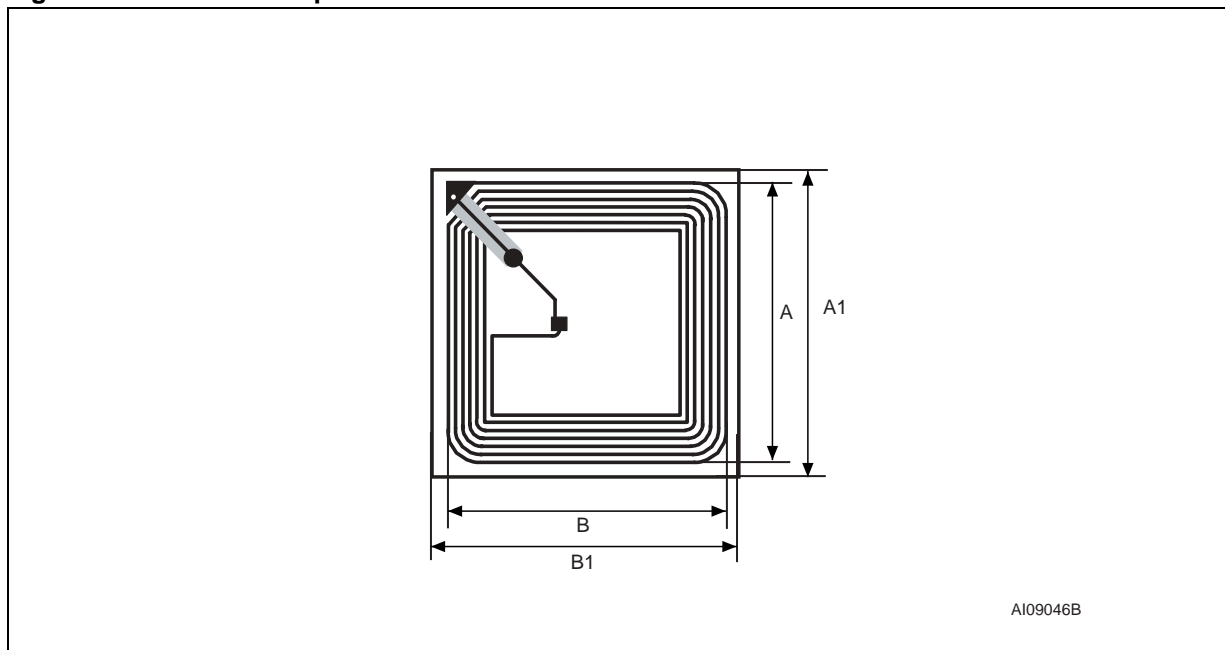## PACKAGE MECHANICAL

Figure 46. A3 Antenna Specification

AI09046B

Table 9. A3 Antenna Specification

Symbol	Parameter	Type	Min	Max	Unit
A	Coil Width	38	37.5	38.5	mm
B	Coil Length	38	37.5	38.5	mm
A1	Inlay Width	43	42.5	43.5	mm
B1	Inlay Length	43	42.5	43.5	mm
	Overall Thickness of Copper Antenna Coil	110	90	130	µm
	Silicon Thickness	180	165	195	µm
Q	Unloaded Q Value	40			
F_{NOM}	Unloaded Free-air Resonance	15.1			MHz
P_A	H-field Energy for Device Operation		0.5 114		A/m dbµA/m

Figure 47. A4 Antenna Specification

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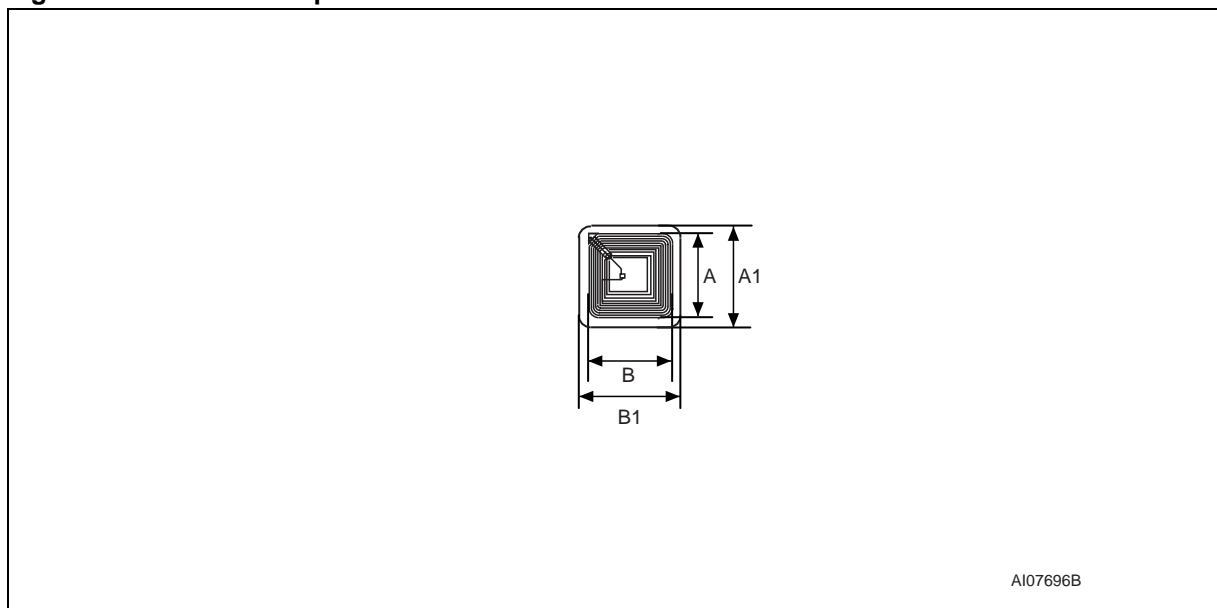
Table 10. A4 Antenna Specification

Symbol	Parameter	Type	Min	Max	Unit
A	Coil Width	15	14.5	15.5	mm
B	Coil Length	15	14.5	15.5	mm
A1	Inlay Width	19	18.5	19.5	mm
B1	Inlay Length	19	18.5	19.5	mm
	Overall Thickness of Copper Antenna Coil	110	90	130	µm
	Silicon Thickness	180	165	195	µm
Q	Unloaded Q Value	30			
F_{NOM}	Unloaded Free-air Resonance	14.5			MHz
P_A	H-field Energy for Device Operation		1.5 123.5		A/m dbµA/m

Figure 48. A5 Antenna Specification

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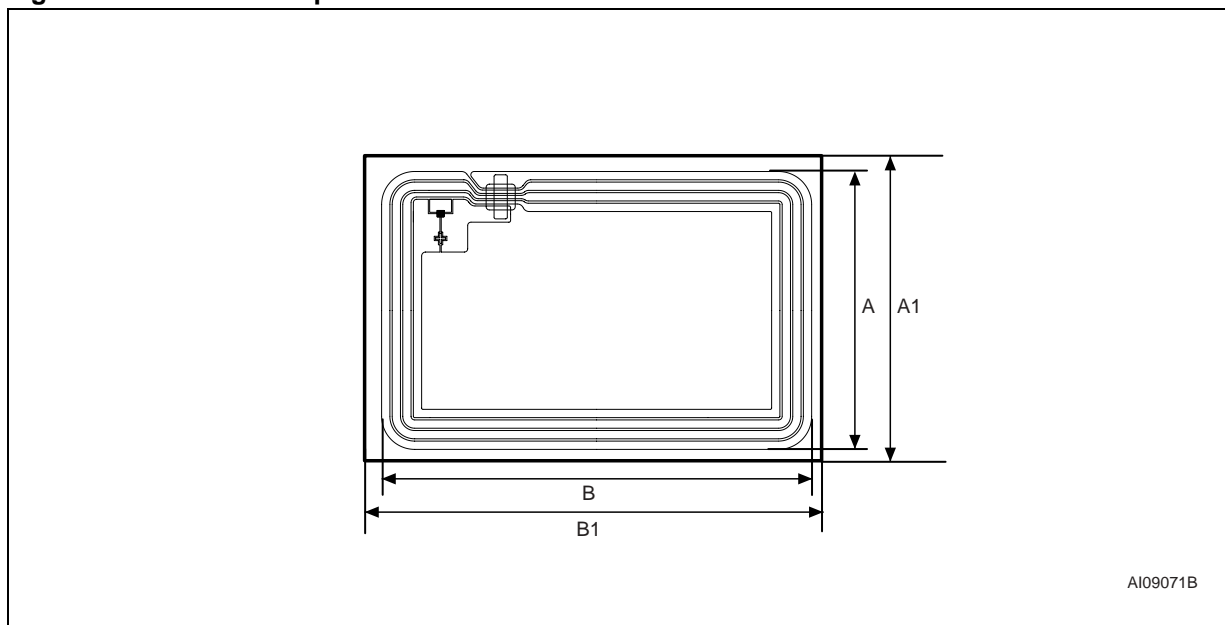
Table 11. A5 Antenna Specification

Symbol	Parameter	Type	Min	Max	Unit
A	Coil Width	42	41.5	42.5	mm
B	Coil Length	65	64.5	65.5	mm
A1	Inlay Width	46	45.5	46.5	mm
B1	Inlay Length	70	69.5	70.5	mm
	Overall Thickness of Copper Antenna Coil	140	130	150	µm
	Silicon Thickness	180	165	195	µm
Q	Unloaded Q Value	30			
F_{NOM}	Unloaded Free-air Resonance	14.8			MHz
P_A	H-field Energy for Device Operation		0.25 108		A/m dbµA/m

PART NUMBERING

Table 12. Ordering Information Scheme

Example:SR176   –   W4   / XXX

Device Type

SR176

Package

W4 =180 µm ± 15 µm Unsawn Wafer

SBN18= 180µm ± 15 µm Bumped and Sawn Wafer on 8-inch Frame

A3T= 38mm x 38mm Copper Antenna on Continuous Tape

A3S= 38mm x 38mm Copper Singulated Adhesive Antenna on Tape

A4T= 15mm x 15mm Copper Antenna on Continuous Tape

A4S= 15mm x 15mm Copper Singulated Adhesive Antenna on Tape

A5T= 42mm x 65mm Copper Antenna on Continuous Tape

A5S= 42mm x 65mm Copper Singulated Adhesive Antenna on Tape

Customer Code

XXX = Given by STMicroelectronics

Note: Devices are shipped from the factory with the memory content bits erased to 1.

For a list of available options (Speed, Package, etc.) or for further information on any aspect of this device, please contact your nearest ST Sales Office.

APPENDIX A. ISO14443 TYPE B CRC CALCULATION

```c
#include <stdio.h>
#include <stdlib.h>
#include <string.h>
#include <ctype.h>
#define BYTEunsigned char
#define USHORTunsigned short

unsigned short UpdateCrc(BYTE ch, USHORT *lpwCrc)
{
    ch = (ch^(BYTE)((*lpwCrc) & 0x00FF));
    ch = (ch^(ch<<4));
    *lpwCrc = (*lpwCrc >> 8)^((USHORT)ch << 8)^((USHORT)ch<<3)^((USHORT)ch>>4);
    return(*lpwCrc);
}

void ComputeCrc(char *Data, int Length, BYTE *TransmitFirst, BYTE *TransmitSecond)
{
BYTE chBlock; USHORTt wCrc;
    wCrc = 0xFFFF; // ISO 3309
    do
        {
        chBlock = *Data++;
        UpdateCrc(chBlock, &wCrc);
        } while (--Length);
    wCrc = ~wCrc; // ISO 3309
    *TransmitFirst = (BYTE) (wCrc & 0xFF);
    *TransmitSecond = (BYTE) ((wCrc >> 8) & 0xFF);
    return;
}

int main(void)
{
BYTE BuffCRC_B[10] = {0x0A, 0x12, 0x34, 0x56}, First, Second, i;
    printf("Crc-16 G(x) = x^16 + x^12 + x^5 + 1");
    printf("CRC_B of [ ");
    for(i=0; i<4; i++)
        printf("%02X ",BuffCRC_B[i]);
    ComputeCrc(BuffCRC_B, 4, &First, &Second);
    printf("] Transmitted: %02X then %02X.", First, Second);
    return(0);
```

REVISION HISTORY

Table 13. Document Revision History

Date	Rev.	Description of Revision
23-Sep-2002	1.0	Document written
04-Oct-2004	2.0	First public release of full datasheet
29-Nov-2004	3.0	INITIATE() command specified.

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