4-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTER

GENERAL DESCRIPTION

The MMC 40104 is a monolithic i.c., available in 16-lead dual in-line plastic or ceramic package The MMC 40104 is a universal shift register featuring parallel inputs, parallel outputs, SHIFT RIGHT and SHIFT LEFT serial inputs, and a high-impedance third output state allowing the device to be used in bus-organized systems. In the parallel-load mode (S0 and S1 are high), data is loaded into the associated flip-flop and appears at the output after the positive transition of the CLOCK input. During loading, serial data flow is inhibited. Shift-right and shift-left are accomplished synchronously on the positive clock edge with serial data entered at the SHIFT RIGHT and SHIFT LEFT serial inputs, respectively. Clearing the register is accomplished by setting both mode controls low and clocking the register When the output enable input is low, all outputs assume the high impedance state.

FEATURES

- Medium-speed operation: f_{CL} = 9 MHz, V_{DD} = 10 V
- Fully static operation
- Synchronous parallel or serial operation
- Three-state outputs

APPLICATIONS

Control circuitry

ABSOLUTE MAXIMUM RATINGS

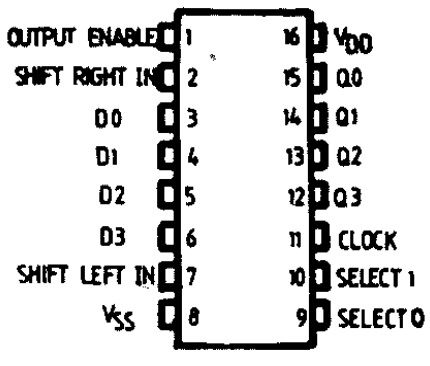
V_{DD}*	Supply voltage:	G and H types	-0.5 to	20	V
		E and F types	-0.5 to	18	V
V_I	Input voltage		-0.5 to	V_{DD}+0.5	V
I_I	DC input current (any one input)			±10	mA
P_{tot}	Total power dissipation (per package)			200	mW
	Dissipation per output transistor for T_A = full package-temperature range			100	mW
T_A	Operating temperature :	G and H types	-55 to	125	°C
		E and F types	-40 to	85	°C
T_{stg}	Storage temperature		-65 to	150	°C

* All voltage values are referred to V_{SS} pin voltage

RECOMMENDED OPERATING CONDITIONS

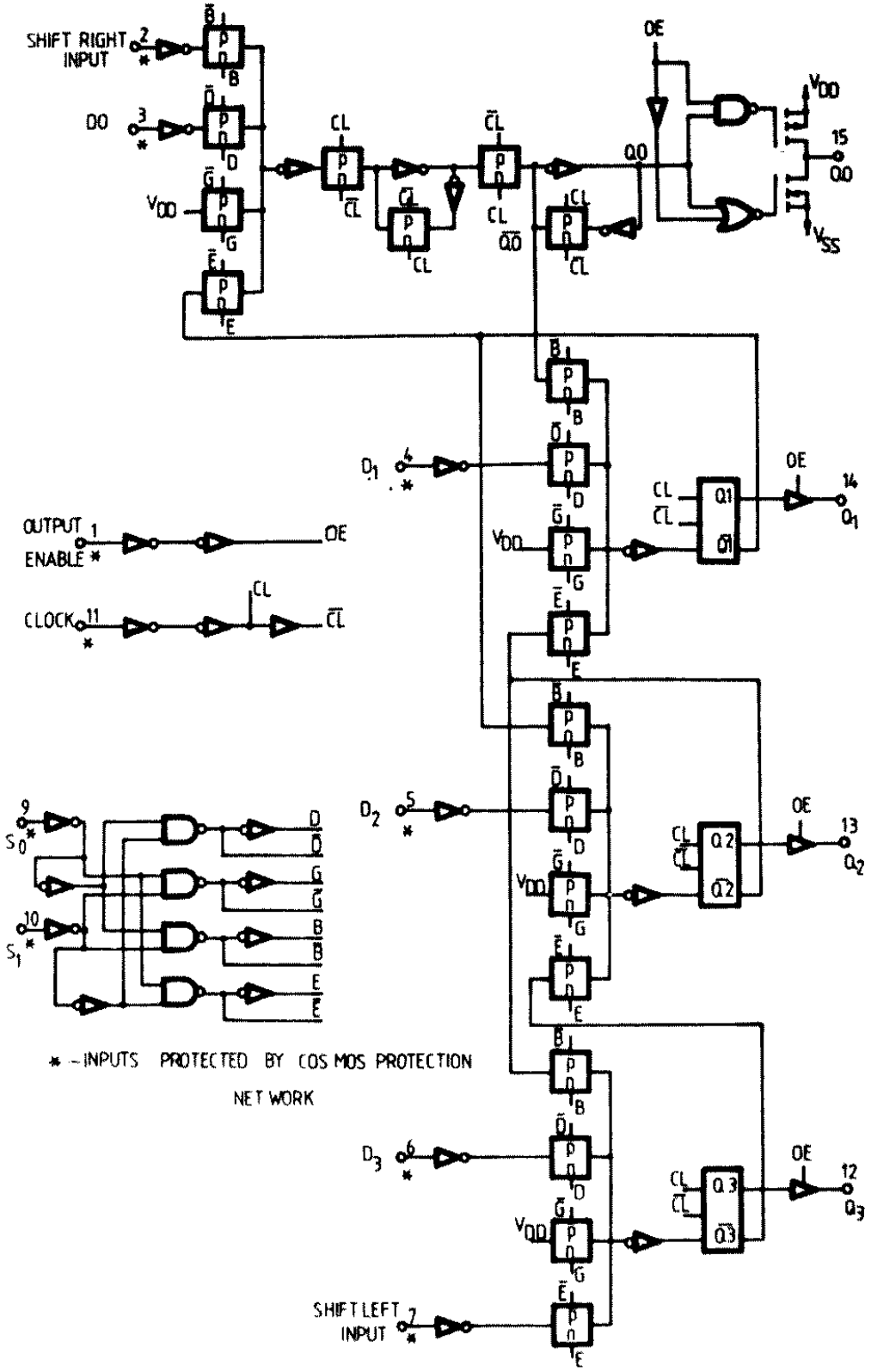
V_{DD}*	Supply voltage:	G and H types	3 to	18	V
		E and F types	3 to	15	V
V_I	Input voltage		0 to	V_{DD}	V
T_A	Operating temperature :	G and H types	-55 to	125	°C
		E and F types	-40 to	85	°C

CONNECTION DIAGRAM



TOP VIEW

LOGIC DIAGRAM



STATIC ELECTRICAL CHARACTERISTICS

(over recommended operating conditions)

PARAMETER			TEST CONDITIONS				VALUES							UNIT
			V_I (V)	V_O (V)	$\|I_O\|$ (μA)	V_{DD} (V)	T^*_{LOW} min.	T^*_{LOW} max.	25°C min.	25°C typ	25°C max.	T^*_{HIGH} min.	T^*_{HIGH} max.	
I_L	Quiescent current	G, H types	0/ 5			5		5		0.04	5		150	μA
			0/10			10		10		0.04	10		300	
			0/15			15		20		0.04	20		600	
			0/20			20		100		0.08	100		3000	
		E, F types	0/ 5			5		20		0.04	20		150	
			0/10			10		40		0.04	40		300	
			0/15			15		80		0.04	80		600	
V_{OH}	Output high voltage		0/ 5		< 1	5	4.95		4.95			4.95		V
			0/10		< 1	10	9.95		9.95			9.95		
			0/15		< 1	15	14.95		14.95			14.95		
V_{OL}	Output low voltage		5 /0		< 1	5		0.05			0.05		0.05	V
			10/0		< 1	10		0.05			0.05		0.05	
			15/0		< 1	15		0.05			0.05		0.05	
V_{IH}	Input high voltage			0.5/4.5	< 1	5	3.5		3.5			3.5		V
				1/9	< 1	10	7		7			7		
				1.5/13.5	< 1	15	11		11			11		
V_{IL}	Input low voltage			4.5/0.5	< 1	5		1.5			1.5		1.5	V
				9/1	< 1	10		3			3		3	
				13.5/1.5	< 1	15		4			4		4	
I_{OH}	Output drive current	G, H types	0/ 5	2.5		5	−2		−1.6	−3.2		−1.15		mA
			0/ 5	4.6		5	−0.64		−0.51	−1		−0.36		
			0/10	9.5		10	−1.6		−1.3	−2.6		−0.9		
			0/15	13.5		15	−4.2		−3.4	−6.8		−2.4		
		E, F types	0/ 5	2.5		5	−1.53		−1.36	−3.2		−1.1		
			0/ 5	4.6		5	−0.52		−0.44	−1		−0.36		
			0/10	9.5		10	−1.3		−1.1	−2.6		−0.9		
			0/15	13.5		15	−3.6		3.0	6.8		2.4		
I_{OL}	Output sink current	G, H types	0/ 5	0.4		5	0.64		0.51	1		0.36		mA
			0/10	0.5		10	1.6		1.3	2.6		0.9		
			0/15	1.5		15	4.2		3.4	6.8		2.4		
		E, F types	0/ 5	0.4		5	0.52		0.44	1		0.36		
			0/10	0.5		10	1.3		1.1	2.6		0.9		
			0/15	1.5		15	3.6		3.0	6.8		2.4		
I_{IH}, I_{IL}	Input leakage current	G, H types	0/18	Any input		18		±0.1		±10 $^{-5}$	±0.1		±1	μA
		E, F types	0/15			15		±0.3		±10 $^{-5}$	±0.3		±1	
C_I	Input capacitance			Any input						5	7.5			pF

* $T_{LOW} = -55°C$ for G, H devices; $-40°C$ for E, F devices.

* $T_{HIGH} = +125°C$ for G, H devices; $+85°C$ for E, F devices.

The Noise Margin for both "1" and "0" level is:

1 V min. with V_{DD} = 5 V

2 V min. with V_{DD} = 10 V

2.5 V min. with V_{DD} = 15 V

DYNAMIC ELECTRICAL CHARACTERISTICS

(T_A = 25°C, C_L = 50 pF, R_L = 200 kohm, typical temperature coefficient for all V_{DD} values is 0.3%/°C, all input rise and fall time = 20 ns).

PARAMETER		TEST CONDITIONS	VALUES			UNIT
		V_{DD}(V)	min.	typ.	max.	
t_{PLH}, t_{PHL}	Propagation delay time Clock to Q	5		220	440	ns
		10		100	200	
		15		70	140	
t_{PZH}, t_{PZL}, t_{PLZ}	3—state outputs High impedance	5		80	160	ns
		10		35	70	
		15		25	50	
t_{PHZ}		5		45	90	ns
		10		25	50	
		15		20	40	
t_{THL}, t_{TLH}	Transition time	5		100	200	ns
		10		50	100	
		15		40	80	
t_{setup}	Setup time D0, D3, SR, SL to Clock	5		80	100	ns
		10		35	70	
		15		20	50	
	S0, S1 to Clock	5		200	400	ns
		10		110	220	
		15		65	130	
t_{hold}	Hold time D0, D3, SR, SL	5		−65	0	ns
		10		−25	0	
		15		−15	0	
	S0, S1 to Clock	5		−170	0	ns
		10		−95	0	
		15		−55	0	
t_w	Clock pulse width	5		90	180	ns
		10		40	180	
		15		25	50	
f_{CL}	Clock input frequency	5	3	6		MHz
		10	6	12		
		15	8	15		
t_r, t_f	Clock input rise or fall time	5			1000	μs
		10			100	
		15			100	

TRUTH TABLE

CLOCK	MODE SELECT S0	MODE SELECT S1	OUTPUT ENABLE	ACTION
⌐	0	0	1	Reset
⌐	1	0	1	Shift right (Q0 toward Q3)
⌐	0	1	1	Shift left (Q3 toward Q0)
⌐	1	1	1	Parallel load
x	x	x	0	Operations occur as shown above, but outputs assume high impedance