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128K x 32 EEPROM Module

PUMA67E4007/A-15/17/20/25

Issue 4.1 : June 1996

Description

The PUMA67E4007/A is a 4Mbit CMOS EEPROM in a JEDEC J-leaded Ceramic Surface Mount Substrate. The output width is user configurable as 8,16 or 32 bits wide using $\overline{CS1\text{-}4}$ and is available with two pinout options, single $\overline{WE}$ or $\overline{WE1\text{-}4}$ (version A). Access times available are 150, 170, 200, and 250ns. Page write (256 bytes) is performed in 10ms with Toggle bit and $\overline{DATA}$ polling indication of cycle completion. The device also features both hardware and software data protection and a low power standby of 66mW maximum. Write cycle endurance is 10,000 Erase/Write cycles with a data retention time of 100 years.

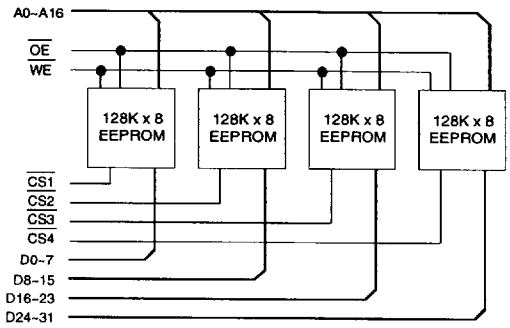
May be screened in accordance with MIL-STD-883.

Features

- Access Times of 150/170/200/250 ns.
- User Configurable as 8 / 16 / 32 bit wide output.
- Operating Power 325/583/1100 mW (max).
- Low Power Standby 66mW (max).
- JEDEC 68 'J' Ceramic Surface Mount Substrate, available in two pinouts : Single $\overline{WE}$, $\overline{WE1\sim4}$ is version A.
- Byte and Page Write (256 Bytes) in 10ms maximum with $\overline{DATA}$ Polling and Toggle bit indication of end of Write.
- Hardware and Software Data Protection.
- Endurance of 10^4 Erase/Write Cycles and Data Retention Time of 100 years.

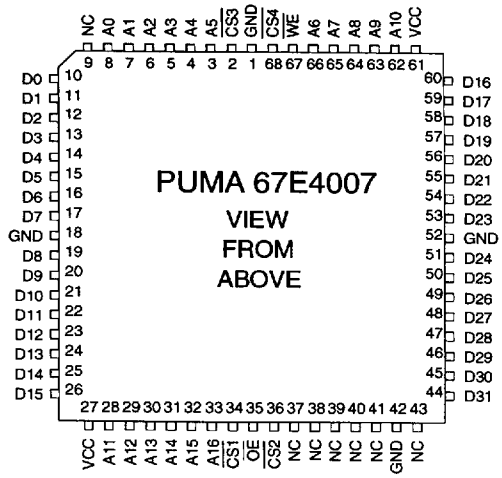
Block Diagram

(see page 11 for Block Diagram of A version)



Pin Definition

(see page 11 for A version Pinout)



Pin Functions

A0~16	Address Inputs	**D0~31**	Data Inputs/Outputs
$\overline{CS1\sim4}$	Chip Select	**$\overline{OE}$**	Output Enable
WE	Write Enable (**$\overline{WE1\sim4}$** on version A)	**NC**	No Connect
V_{cc}	Power (+5V)	**GND**	Ground

DC OPERATING CONDITIONS

Voltage on any pin relative to GND	V_T	-1.0 to +7.0	V
Storage Temperature	T_{STG}	-65 to +150	°C
Temperature Under Bias	T_{BIAS}	-65 to +135	°C

Notes : (1) Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

(2) V_T can be -3.5V pulse of less than 20ns.

Recommended Operating Conditions

Parameter	*Symbol*	*min*	*typ*	*max*	
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.0	-	V_{CC}+1	V
Input Low Voltage	V_{IL}	-0.1	-	0.8	V
Operating Temperature	T_A	0	-	70	°C
	T_{AL}	-40	-	85	°C (Suffix **I**)
	T_{AM}	-55	-	125	°C (Suffix **M, MB**)

DC Electrical Characteristics (T_A=-55°C to +125°C, V_{CC}=5V ± 10%)

Parameter		*Symbol*	*Test Condition*	*min*	*max*	*Unit*
Input Leakage Current	Address, $\overline{OE}$, $\overline{WE}$	I_{LI1}	V_{IN} = GND to V_{CC}	-	40	µA
	$\overline{CS1\text{-}4}$[1], $\overline{WE1\text{-}4}$[2]	I_{LI2}	V_{IN} = GND to V_{CC}	-	10	µA
Output Leakage Current		I_{LO}	$V_{I/O}$ = GND to V_{CC}, $\overline{CS}$ = V_{IH}	-	40	µA
Operating Supply Current		I_{CC32}	$\overline{CS}$=$\overline{OE}$=V_{IL}, $\overline{WE}$=V_{IH}, $I_{I/O}$=0mA, *f*=5MHz	-	200	mA
		I_{CC16}	As above.	-	106	mA
		I_{CC8}	As above.	-	59	mA
Standby Supply Current	(TTL levels)	I_{SB1}	$\overline{CS}$=V_{IH}, $I_{I/O}$=0mA, Other Inputs=V_{IH}, $\overline{OE}$=V_{IL}	-	12	mA
	(CMOS levels)	I_{SB2}	$\overline{CS}$=V_{CC}-0.3V, $I_{I/O}$=0mA, Other Inputs=V_{CC}, $\overline{OE}$=V_{IL}	-	2	mA
Output Low Voltage		V_{OL}	I_{OL}=2.1mA.	-	0.4	V
Output High Voltage		V_{OH}	I_{OH}=-400µA.	2.4	-	V

Notes (1) $\overline{CS}$ above are accessed through $\overline{CS1\text{-}4}$. These inputs must be operated simultaneously for 32 bit operation, in pairs in 16 bit mode and singly for 8 bit mode.

(2) $\overline{WE1\sim4}$ on the PUMA 67E4007A version, which are accessed as in note (1) above.

Capacitance (V_{CC}=5V±10%, T_A=25°C, f=1MHz)

Parameter		*Symbol*	*Test Condition*	*typ*	*max*	*Unit*
Input Capacitance	Address, $\overline{OE}$	C_{IN1}	V_{IN}=0V	-	50	pF
	$\overline{CS1\text{-}4}$, $\overline{WE1\text{-}4}$[1]	C_{IN2}	V_{IN}=0V	-	20	pF
I/O Capacitance		$C_{I/O}$	$V_{I/O}$=0V	-	50	pF

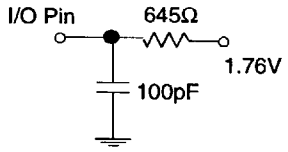
Notes: (1) On the PUMA 67E4007A version only.

This parameter is periodically sampled and not 100% tested.

AC Test Conditions

* Input pulse levels: 0V to 3.0V
* Input rise and fall times: 10ns
* Input and Output timing reference levels: 1.5V
* Output load: See Diagram
* V_{CC}=5V±10%

Output Test Load



AC OPERATING CONDITIONS

Read Cycle

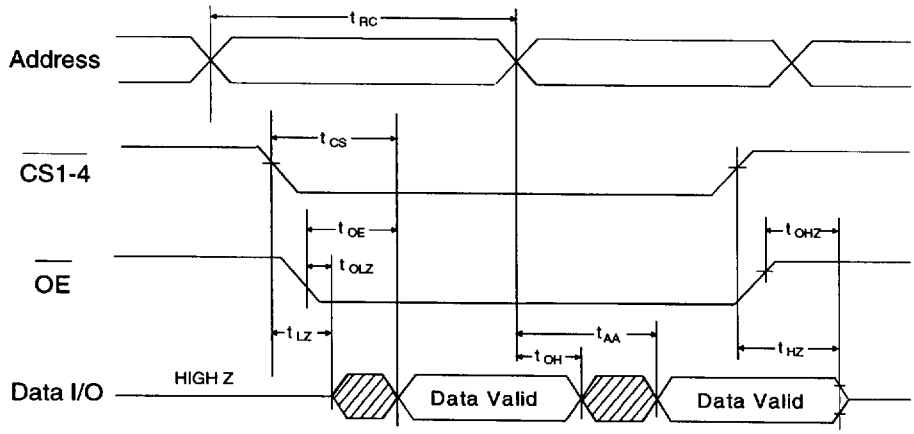
Parameter	Symbol	-15 min	-15 max	-17 min	-17 max	-20 min	-20 max	-25 min	-25 max	Unit
Read Cycle Time	t_{RC}	150	-	170	-	200	-	250	-	ns
Address Access Time	t_{AA}	-	150	-	170	-	200	-	250	ns
Chip Select Access Time	t_{CS}	-	150	-	170	-	200	-	250	ns
Output Enable Access Time	t_{OE}	0	50	0	50	0	50	0	50	ns
Chip Select High to High Z Output(1)	t_{HZ}	0	60	0	60	0	60	0	60	ns
Output Enable High to High Z Output(1)	t_{OHZ}	0	50	0	50	0	50	0	50	ns
Chip Select Low to Active Output(1)	t_{LZ}	0	-	0	-	0	-	0	-	ns
Output Enable Low to Active Output(1)	t_{OLZ}	0	-	0	-	0	-	0	-	ns
Output Hold from Address Change	t_{OH}	0	-	0	-	0	-	0	-	ns

Notes: (1) t_{LZ} min, t_{HZ}, t_{OLZ} min, and t_{OHZ} are periodically sampled and not 100% tested. t_{HZ} max. and t_{OHZ} max. are measured with C_L = 5pF, from the point when Chip Select or Output Enable return high (whichever occurs first) to the time when the outputs are no longer driven.

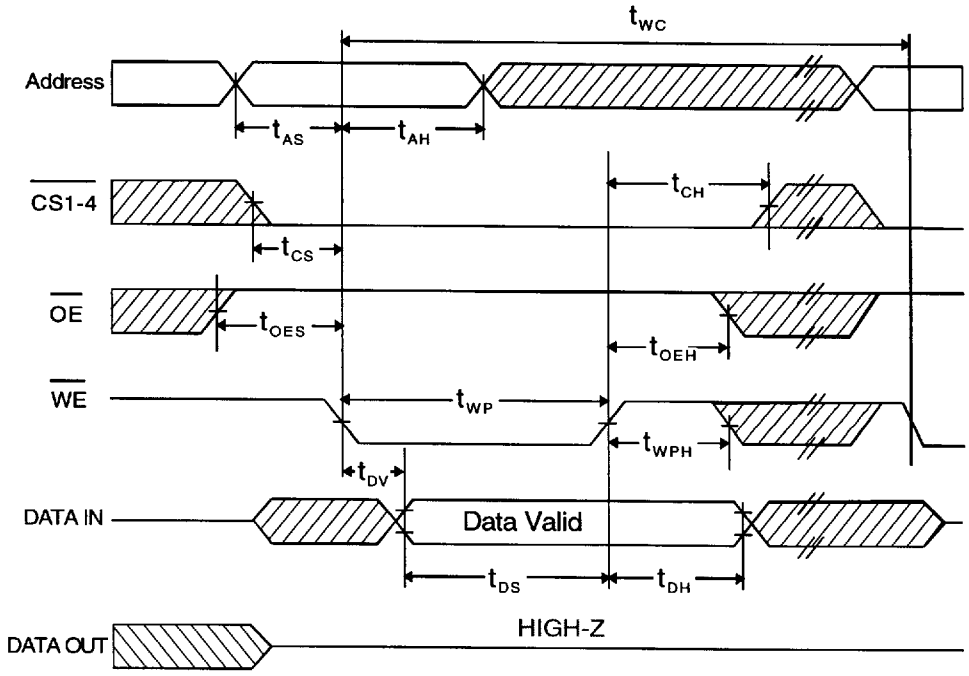
Write Cycle

Parameter	Symbol	min	typ	max	Unit
Write Cycle Time	t_{WC}	-	-	10	ms
Address Set-up Time	t_{AS}	0	-	-	ns
Address Hold Time	t_{AH}	50	-	-	ns
Output Enable Set-up Time	t_{OES}	10	-	-	ns
Output Enable Hold Time	t_{OEH}	10	-	-	ns
Chip Select Set-up Time	t_{CS}	0	-	-	ns
Write Hold Time	t_{CH}	0	-	-	ns
Chip Select Pulse Width	t_{CW}	100	-	-	ns
Write Pulse Width	t_{WP}	100	-	-	ns
Write Enable High Recovery	t_{WPH}	100	-	-	ns
Data Set-up Time	t_{DS}	50	-	-	ns
Data Hold Time	t_{DH}	10	-	-	ns
Data Valid	t_{DV}	-	-	1	µs
Delay to Next Write	t_{DW}	10	-	-	µs
Byte Load Cycle	t_{BLC}	0.2	-	100	µs

Read Cycle Timing Waveform ($\overline{WE}$ = V_{IH})

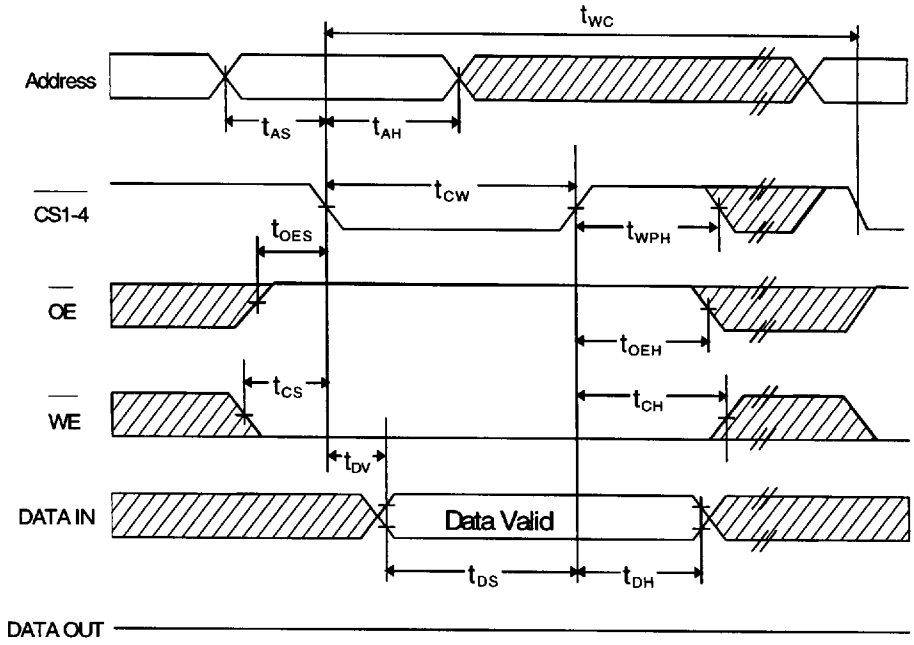


AC Write Waveform - $\overline{WE}$ Controlled

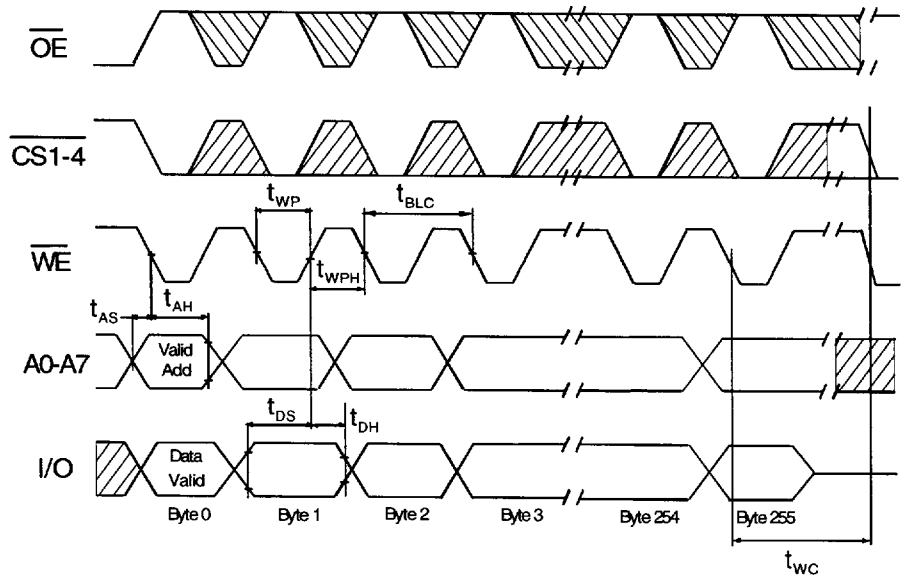


Notes $\overline{WE}$ above refers to $\overline{WE1\text{-}4}$ on the PUMA67E4007/A

AC Write Waveform - $\overline{CS}$ Controlled



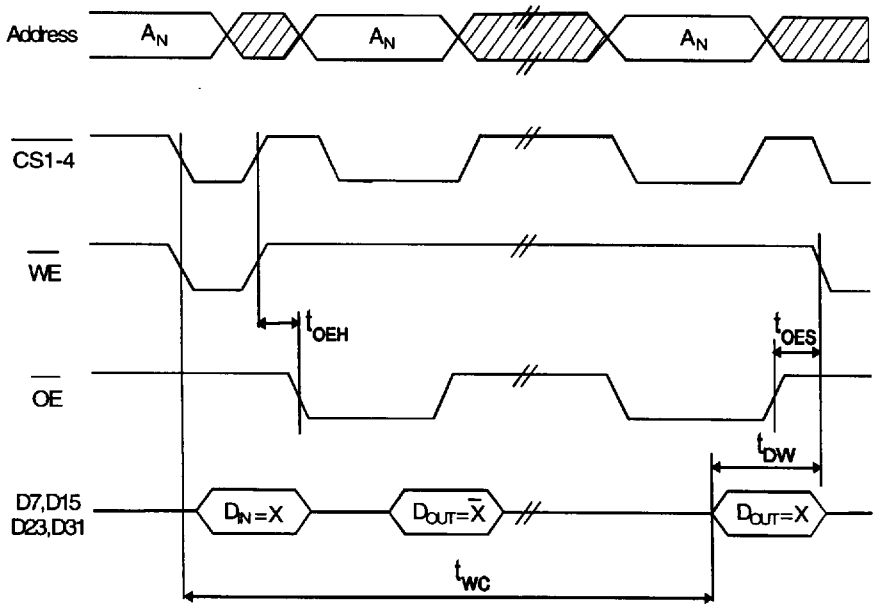
Page Mode Write Waveform



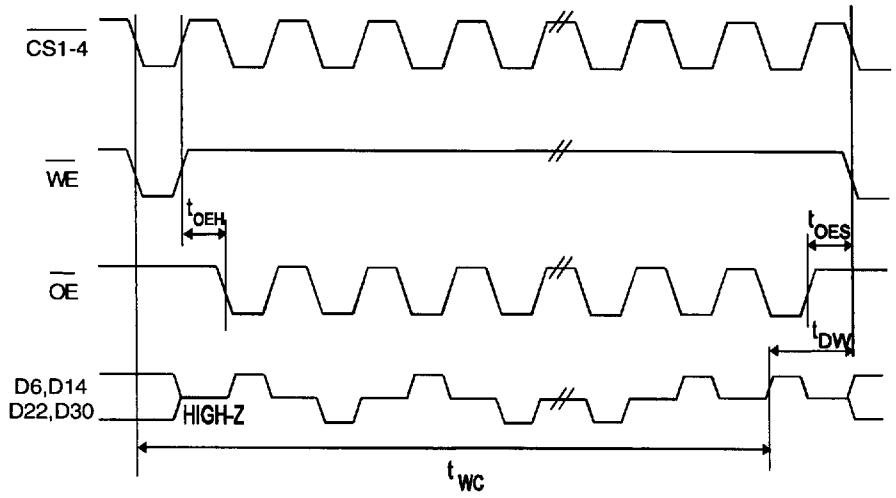
Note: A8 through A14 must specify the page address during each high to low transition of Write Enable (or Chip select).
Output Enable must be high only when Write Enable and Chip Select are both low.

$\overline{WE}$ above refers to $\overline{WE1\text{-}4}$ on the PUMA 67E4007A

DATA Polling Waveform

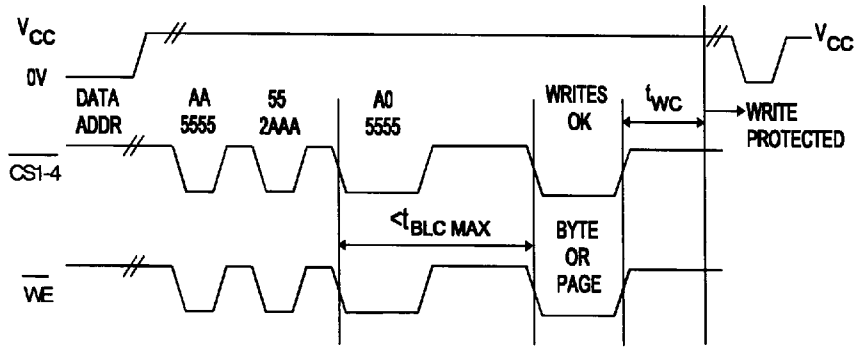


Toggle Bit Waveform

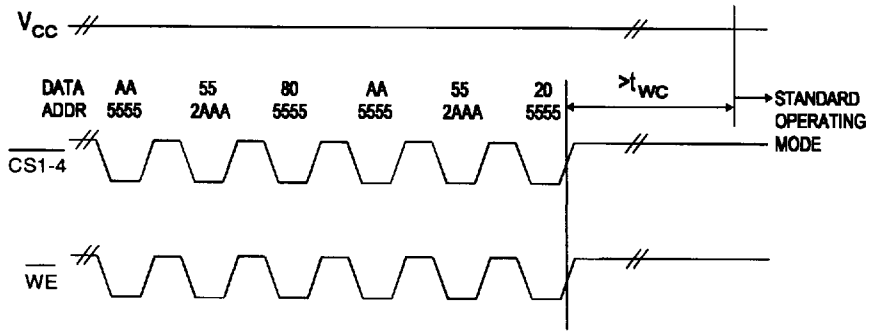


$\overline{WE}$ above refers to $\overline{WE1\text{-}4}$ on the PUMA 67E4007A

Software Data Protection Enable Waveform



Software Data Protection Disable Waveform



DEVICE OPERATION

Where references are made to byte/word operations, the user will control the memory configuration of 8, 16, 32 bits wide using $\overline{CS1\text{-}4}$. $\overline{WE}$ refers to $\overline{WE1\text{-}4}$ on the PUMA 67E4007A.

Read

The PUMA 67E4007/A read operations are initiated by both Output Enable and Chip Select(s) LOW. The read operation is terminated by either Chip Select(s) or Output Enable returning HIGH. This 2-line control architecture elimanates bus connection in a system environment. The data bus will be in a high impendence state when either Output Enable or Chip Select(s) is HIGH.

Write

Write operations are initated when both Chip Select(s) and Write Enable(s) are LOW and Output Enable is HIGH. The PUMA 67E40007/A supports both a Chip Select(s) and Write Enable(s) controlled write cycle. That is, the address is latched by the falling edge of either Chip Select(s) or Write Enable(s), whichever occurs last. Similarly, the data is latched internally by the rising edge of either Chip Select(s) or Write Enable(s), whichever occurs first. A byte/word write operation, once initiated, will automatically continue to completion, within 10 ms maximum.

Page Mode Write

The page write feature of the PUMA 67E4007/A allows the entire memory to be written in 5 seconds. Page Write allows 256 bytes/words of data to be written prior to the internal programming cycle. The host can fetch data from another location within the system during a page write operation (change the source address), but the page address (A8 through A16) for each subsequent valid write cycle to the part during this operation must be the same as the initial page address.

The page write mode can be initiated during any write operation. Following the initial byte/word write cycle, the host can write up to 256 bytes/words in the same manner as the first byte/word written. Each successive byte/word load cycle, started by the Write Enable(s) HIGH to LOW transition, must begin within 100 µs of the falling edge of the preceding Write Enable(s). If a subsequent Write Enable HIGH to LOW transition is not detected within 100 µs, the internal automatic programming cycle will commence.

$\overline{DATA}$ Polling

The PUMA 67E4007/A features $\overline{DATA}$ Polling to indicate if the write cycle is completed. $\overline{DATA}$ polling allows a simple bit test operation to determine the status of the device, eliminating additional interrupt inputs or external hardware. During the internal programming cycle, any attempt to read the last byte written will produce the compliment of that data on D7. Once the programming is complete, D7 will refect the true data. Note: If the the PUMA 67E4007/A is in a protected state and an illegal write operation is attempted $\overline{DATA}$ Polling will not operate. Above refers to 8 bit mode, for 16 bit mode use D7, D15 and 32 bit mode uses D7, D15, D23, D31.

TOGGLE bit

In addition to $\overline{DATA}$ polling, another method is provided to determine the end of a Write Cycle. During a write operation successive attempts to read data will result in D6 toggling between 1 and 0. Once a write is complete, this toggling will stop and valid data will be read. Above refers to 8 bit mode, for 16 bit mode use D6, D14 and 32 bit mode uses D6, D14, D22, D30.

Hardware Data Protection

The PUMA67E4007/A provides three harware features to protect nonvololitile data from inadvertent writes.

- Noise Protection - A Write Enable(s) pulse less than 10 ns will not initiate a write cycle.
- Default V_{CC} Sence - All functions are inhabited when V_{CC} is < 3.6 V.
- Write Inhibit - Holding either Output Enable LOW, Write Enable(s) HIGH or Chip Select(s) HIGH will prevent an inadvertent write cycle during power on or power off, maintaining data integrity.

Software Data Protection (SDP)

The PUMA67E4007/A offers a software controlled data protection feature, and is shipped with the software data protection disabled (device in standard operating mode). In this mode external circuitry should be used to protect the device during power-up/down operations. The host would then have open read & write access of the device once Vcc was stable.

The PUMA67E40007/A can be automatically protected during power-up and power-down without the need for external circuits by employing the software data protect feature. The internal software data protection circuit is enabled after the first write operation utilizing the software algorithm. This circuit is nonvolatile and will remain set for the life of the device unless the reset command is issued.

Once the software protection is enabled, the PUMA67E4007/A is also protected against inadvertent and accidental writes in that, the software algorithm must be issued prior to writing additional data to the device.

Operating Modes

The table below shows the logic inputs required to control the operation of the PUMA67E4007/A.

MODE	$\overline{CS1\text{-}4}$	$\overline{OE}$	$\overline{WE}$	OUTPUTS
Read	0	0	1	Data Out
Write	0	I	0	Data in
Standby	1	X	X	High-Z
Write Inhibit	X	X	1	
	X	0	X	

$0 = V_{IL}$: $1 = V_{IH}$: $X = V_{IH}$ or V_{IL}

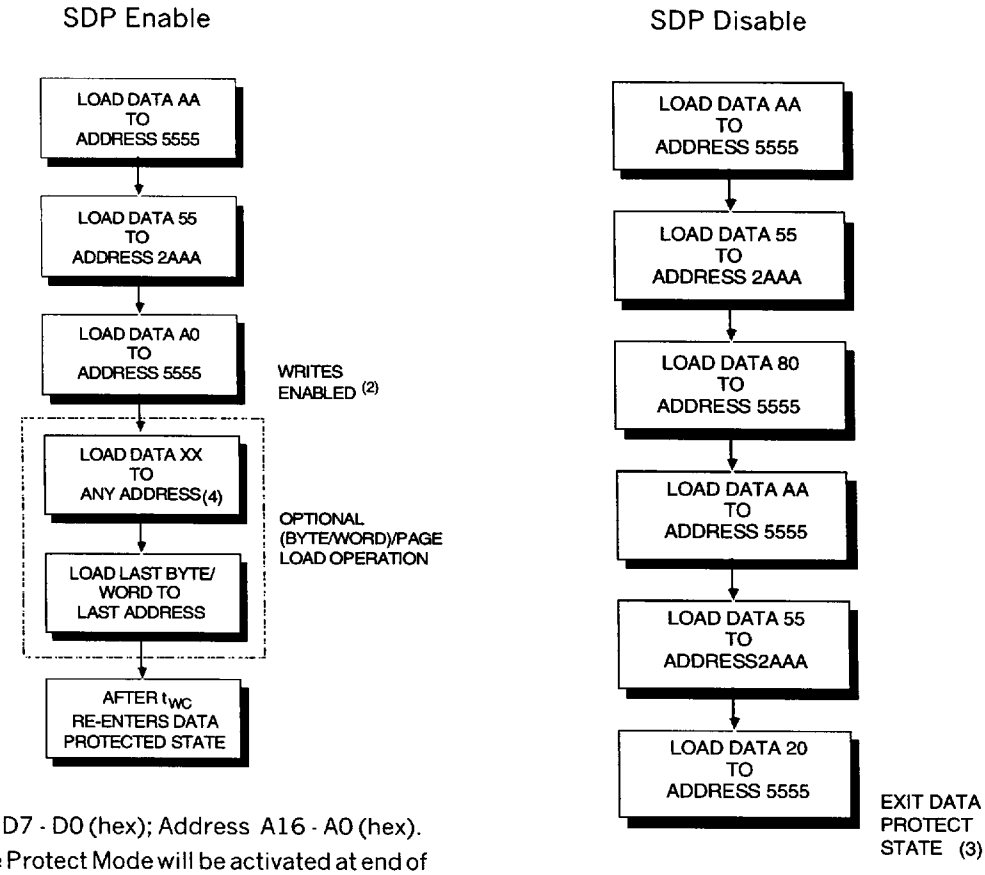
$\overline{WE}$ above refers to $\overline{WE1\text{-}4}$ on the PUMA67E4007/A.

Software Data Protection[1]

Software controlled data protection, requires the use of a software algorithm before any Write can be performed. To enable this feature a special sequence of 3 Writes to 3 specific addresses must be performed. The three byte/words sequence opens the page write window enabling the host to write from 1 to 256 bytes/words of data. Once set the data protection remains operational until it is disabled by using a second algorithm; power transitions will not reset this feature.

Note that the PUMA67E4007/A is supplied with the Software data Protection feature **disabled**.

The algorithms to enable and disable the protection are shown below:



Notes: (1) Data D7 - D0 (hex); Address A16 - A0 (hex).

(2) Write Protect Mode will be activated at end of Write even if no other data is loaded.

(3) Write protect state will be disabled at end of write period even if no other data is loaded.

(4) 1 to 256 bytes/words of data can be loaded.

Once initiated, the enable/Disable sequence of write operations should not be interrupted

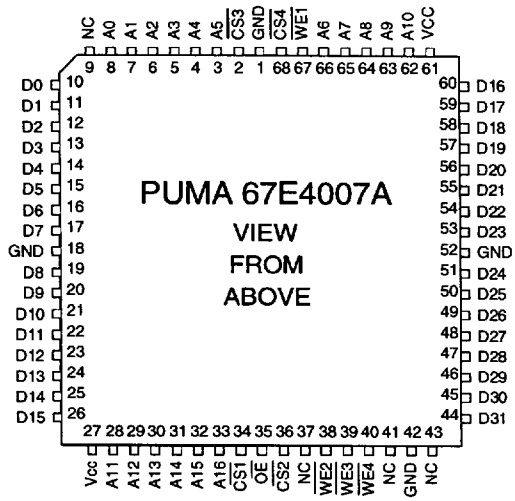
Note : Load data above represents 8 bit mode. For 16 or 32 bit mode, place the load data in the 2 bytes or all 4 bytes on the data lines respectively. Eg/ 8 bit load data = 55_{HEX}, 16 bit load data = $FFFFECEC_{HEX}$

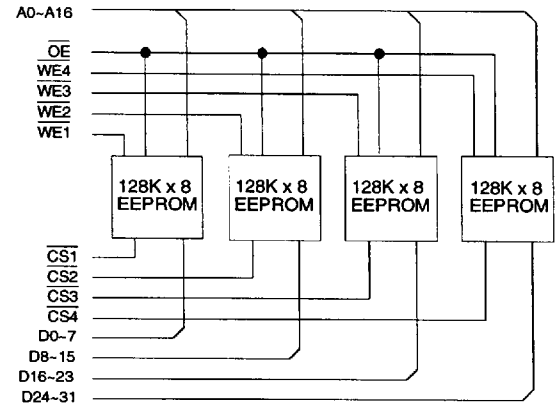
All software write commands must obey the Page Write timing specifications.

The process of disabling the Data Protection mode is very similar to that described for enable, except 6 bytes/words must be loaded to specific locations in the EEPROM as shown. After t_{WC}, the PUMA67E4007/A will be in standard operating mode.

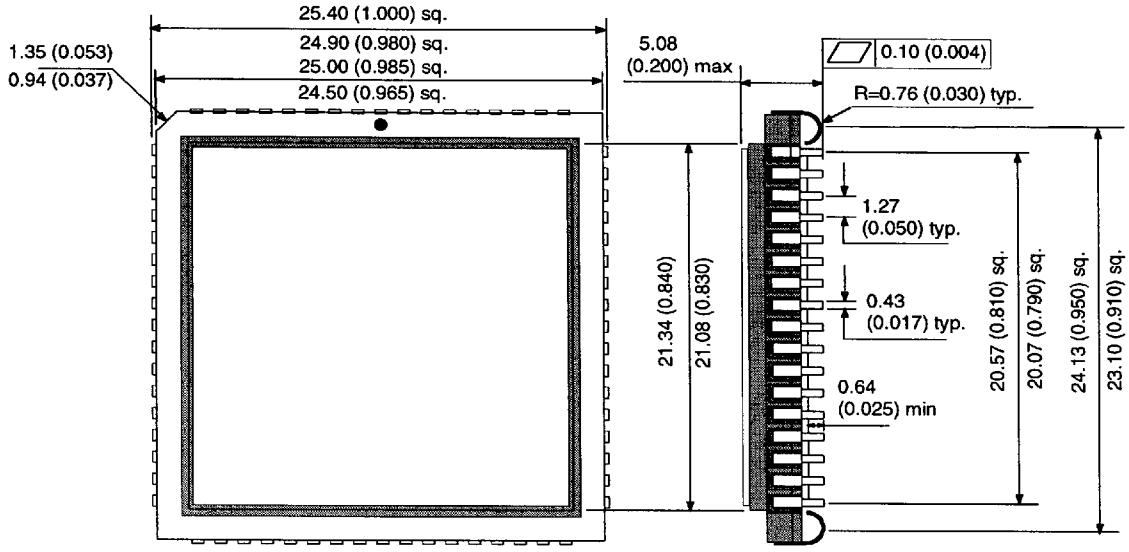
Note here the use of the word 'load' to describe enabling and disabling the protection modes in preference to 'write'. Although it may seem that if the Write command sequence is performed to enable protection then the three bytes/words at those addresses will be overwritten with AA,55,A0, this is not the case.

Pin Definition version A' / Block Diagram version A





Package Details **Dimensions in inches. Lead finish gold.**



Military Screening Procedure

MultiChip Screening Flow for high reliability product is in accordance with Mil-883 method 5004 .

MB MULTICHIP MODULE SCREENING FLOW

SCREEN	*TEST METHOD*	*LEVEL*
Visual and Mechanical		
Internal visual	2010 Condition B or manufacturers equivalent	100%
Temperature cycle	1010 Condition C (10 Cycles, -65°C to +150°C)	100%
Constant acceleration	2001 Condition B (Y1 & Y2) (10,000g)	100%
Endurance		
Write Cycle endurance and Data Retention performance	As Per Internal Specification	
Burn-In		
Pre-Burn-in electrical	Per applicable device specifications at T_A=+25°C	100%
Burn-in	T_A=+125°C, 160hrs min	100%
Final Electrical Tests	Per applicable Device Specification	
Static (DC)	a) @ T_A=+25°C and power supply extremes	100%
	b) @ temperature and power supply extremes	100%
Functional	a) @ T_A=+25°C and power supply extremes	100%
	b) @ temperature and power supply extremes	100%
Switching (AC)	a) @ T_A=+25°C and power supply extremes	100%
	b) @ temperature and power supply extremes	100%
Percent Defective allowable (PDA)	Calculated at post-burn-in at T_A=+25°C	10%
Hermeticity	1014	
Fine	Condition A	100%
Gross	Condition C	100%
Quality Conformance	Per Applicable Device Specification	Sample
External Visual	2009 Per vendor or customer specification	100%

Ordering Information

PUMA 67E4007AMB-15 E

Endurance	Blank	= 10k Cycles
	E	= 100k Cycles
Speed	15	= 150 n
	17	= 170 ns
	20	= 200 ns
	25	= 250 ns
Temp. range/screening	Blank	= Commercial Temperature
	I	= Industrial Temperature
	M	= Military Temperature
	MB	= Screened in accordance with MIL-STD-883
Special Features	Blank	= $\overline{WE1}$
	A	= $\overline{WE1 \sim 4}$.
Organisation	4007	= 128K x 32, user configurable as 256K x 16 and 512K x 8
Memory Type	E	= EEPROM
Package	PUMA67	= 68 pin "J" Leaded Ceramic Surface Mount Module.