IS63LV1024
IS63LV1024L

128K x 8 HIGH-SPEED CMOS STATIC RAM
3.3V REVOLUTIONARY PINOUT

JULY 2010

FEATURES

- High-speed access times:
  8, 10, 12 ns
- High-performance, low-power CMOS process
- Multiple center power and ground pins for greater noise immunity
- Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ options
- $\overline{CE}$ power-down
- Fully static operation: no clock or refresh required
- TTL compatible inputs and outputs
- Single 3.3V power supply
- Packages available:
  – 32-pin 300-mil SOJ
  – 32-pin 400-mil SOJ
  – 32-pin TSOP (Type II)
  – 32-pin STSOP (Type I)
  – 36-pin BGA (8mmx10mm)
- Lead-free Available

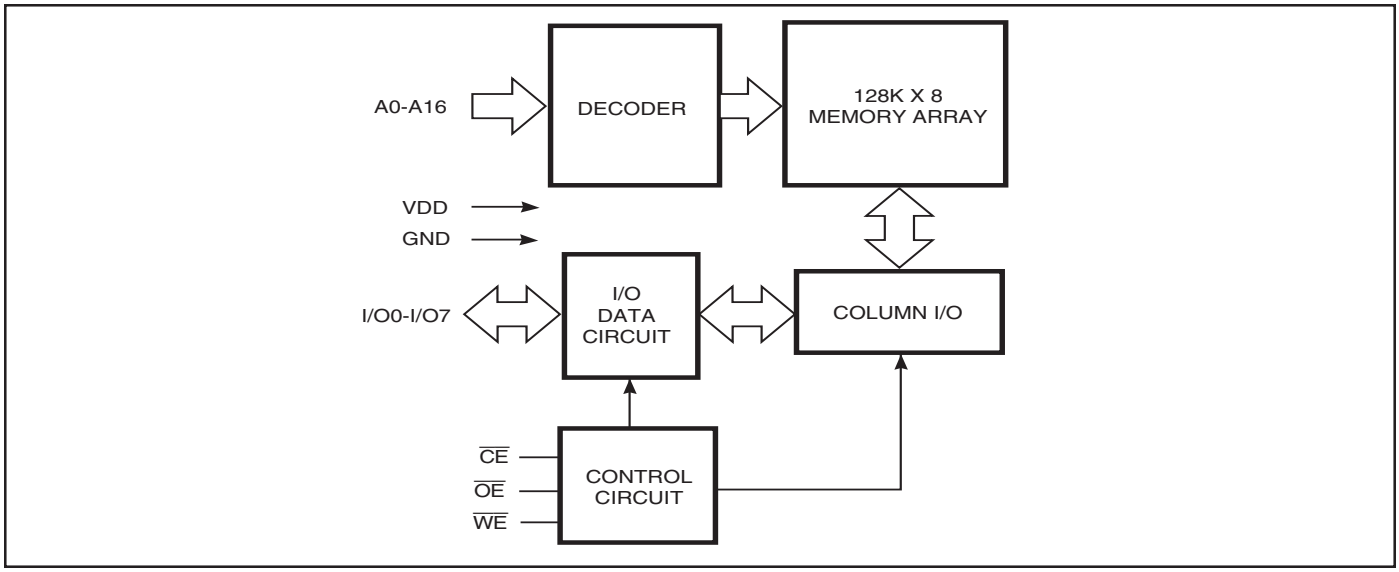
DESCRIPTION

The *ISSI* IS63LV1024/IS63LV1024L is a very high-speed, low power, 131,072-word by 8-bit CMOS static RAM in revolutionary pinout. The IS63LV1024/IS63LV1024L is fabricated using *ISSI*'s high-performance CMOS technology. This highly reliable process coupled with innovative circuit design techniques, yields higher performance and low power consumption devices.

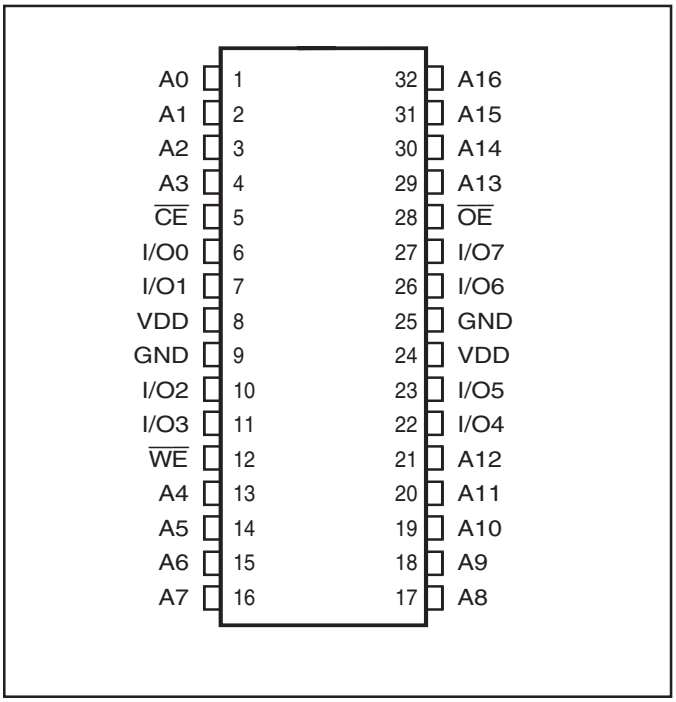
When $\overline{CE}$ is HIGH (deselected), the device assumes a standby mode at which the power dissipation can be reduced down to 250 µW (typical) with CMOS input levels.

The IS63LV1024/IS63LV1024L operates from a single 3.3V power supply and all inputs are TTL-compatible.

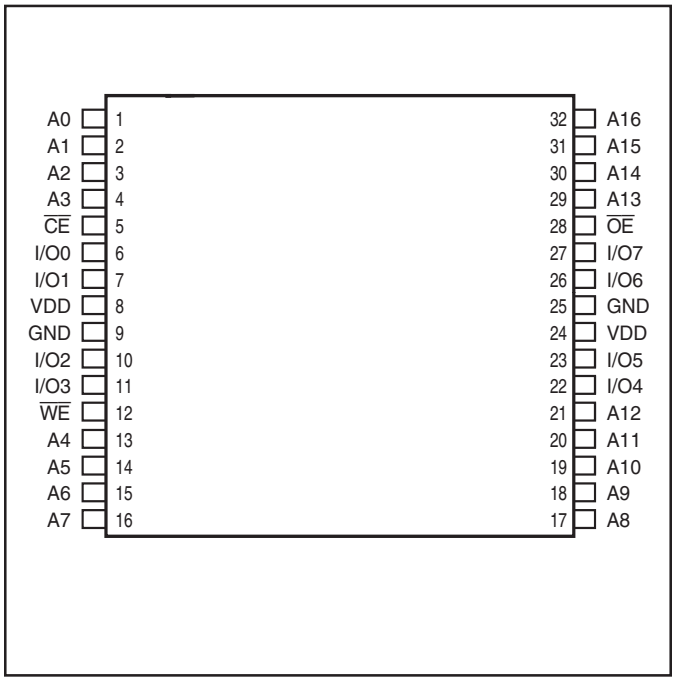
FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION
32-Pin SOJ



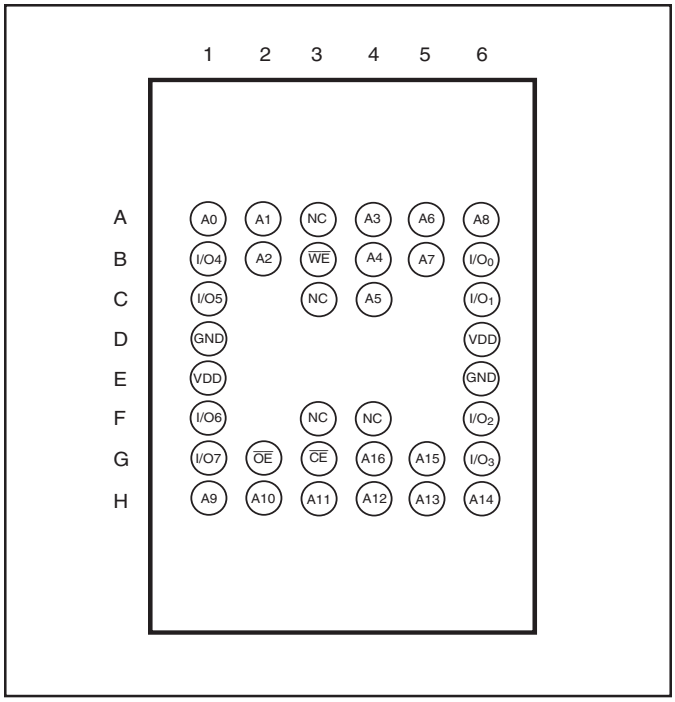
PIN CONFIGURATION
32-Pin TSOP (Type II) (T)
32-Pin STSOP (Type I) (H)



PIN DESCRIPTIONS

A0-A16	Address Inputs
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
$\overline{WE}$	Write Enable Input
I/O0-I/O7	Data Inputs/Outputs
V_{DD}	Power
GND	Ground

PIN CONFIGURATION
36-mini BGA (B) (8 mm x 10 mm)



TRUTH TABLE

Mode	$\overline{WE}$	$\overline{CE}$	$\overline{OE}$	I/O Operation	V_{DD} Current
Not Selected (Power-down)	X	H	X	High-Z	I_{SB1}, I_{SB2}
Output Disabled	H	L	H	High-Z	I_{CC1}, I_{CC2}
Read	H	L	L	D_{OUT}	I_{CC1}, I_{CC2}
Write	L	L	X	D_{IN}	I_{CC1}, I_{CC2}

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Parameter	Value	Unit
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to V_{DD} + 0.5	V
T_{STG}	Storage Temperature	–65 to +150	°C
P_T	Power Dissipation	1.0	W

Notes:
1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

OPERATING RANGE

Range	Ambient Temperature	V_{DD}
Commercial	0°C to +70°C	3.3V ± 0.3V
Industrial	–40°C to +85°C	3.3V ± 0.15V

DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

Symbol	Parameter	Test Conditions		Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{DD} = Min., I_{OH} = –4.0 mA		2.4	—	V
V_{OL}	Output LOW Voltage	V_{DD} = Min., I_{OL} = 8.0 mA		—	0.4	V
V_{IH}	Input HIGH Voltage			2.2	V_{DD} + 0.3	V
V_{IL}	Input LOW Voltage(1)			–0.3	0.8	V
I_{LI}	Input Leakage	GND ≤ V_{IN} ≤ V_{DD}	Com. Ind.	–1 –5	1 5	µA
I_{LO}	Output Leakage	GND ≤ V_{OUT} ≤ V_{DD}, Outputs Disabled	Com. Ind.	–1 –5	1 5	µA

Note:
1. V_{IL} (min.) = –0.3V DC; V_{IL} (min.) = –2.0V AC (pulse width under Vss < 5ns). Not 100% tested.
   V_{IH} (max.) = V_{DD} + 0.3V DC; V_{IH} (max.) = V_{DD} + 2.0V AC (pulse width over V_{DD} < 5ns). Not 100% tested.

IS63LV1024 POWER SUPPLY CHARACTERISTICS[1] (Over Operating Range)

Symbol	Parameter	Test Conditions		-8 ns Min.	-8 ns Max.	-10 ns Min.	-10 ns Max.	-12 ns Min.	-12 ns Max.	Unit
I_{CC1}	V_{DD} Operating Supply Current	V_{DD} = Max., $\overline{CE}$ = V_{IL}	Com.	—	160	—	150	—	130	mA
		I_{OUT} = 0 mA, f = Max.	Ind.	—	170	—	160	—	140	
			typ.[2]	—	105	—	95	—	75	
			Ind. (@15 ns)					—	90	
I_{SB}	TTL Standby Current (TTL Inputs)	V_{DD} = Max., V_{IN} = V_{IH} or V_{IL} $\overline{CE} \geq V_{IH}$, f = Max	Com.	—	55	—	45	—	40	mA
			Ind.	—	55	—	45	—	40	
I_{SB1}	TTL Standby Current (TTL Inputs)	V_{DD} = Max., V_{IN} = V_{IH} or V_{IL} $\overline{CE} \geq V_{IH}$, f = 0	Com.	—	25	—	25	—	25	mA
			Ind.	—	30	—	30	—	30	
I_{SB2}	CMOS Standby Current (CMOS Inputs)	V_{DD} = Max., $\overline{CE} \geq V_{DD}$ – 0.2V, $V_{IN} \geq V_{DD}$ – 0.2V, or $V_{IN} \leq$ 0.2V, f = 0	Com.	—	5	—	5	—	5	mA
			Ind.	—	10	—	10	—	10	
			typ.[2]	—	0.5	—	0.5	—	0.5	

Notes:
1. At f = f_{MAX}, address and data inputs are cycling at the maximum frequency, f = 0 means no input lines change.
2. Typical values are measured at V_{DD} = 3.3V, T_A = 25°C. Not 100% tested.

IS63LV1024L POWER SUPPLY CHARACTERISTICS[1] (Over Operating Range)

Symbol	Parameter	Test Conditions		-8 ns Min.	-8 ns Max.	-10 ns Min.	-10 ns Max.	-12 ns Min.	-12 ns Max.	Unit
I_{CC1}	V_{DD} Operating Supply Current	V_{DD} = Max., $\overline{CE}$ = V_{IL}	Com.	—	100	—	95	—	90	mA
		I_{OUT} = 0 mA, f = Max.	Ind.	—	110	—	105	—	100	
			typ.[2]	—	75	—	70	—	65	
I_{SB}	TTL Standby Current (TTL Inputs)	V_{DD} = Max., V_{IN} = V_{IH} or V_{IL} $\overline{CE} \geq V_{IH}$, f = Max	Com.	—	35	—	30	—	25	mA
			Ind.	—	40	—	35	—	30	
I_{SB1}	TTL Standby Current (TTL Inputs)	V_{DD} = Max., V_{IN} = V_{IH} or V_{IL} $\overline{CE} \geq V_{IH}$, f = 0	Com.	—	15	—	15	—	15	mA
			Ind.	—	20	—	20	—	20	
I_{SB2}	CMOS Standby Current (CMOS Inputs)	V_{DD} = Max., $\overline{CE} \geq V_{DD}$ – 0.2V, $V_{IN} \geq V_{DD}$ – 0.2V, or $V_{IN} \leq$ 0.2V, f = 0	Com.	—	1	—	1	—	1	mA
			Ind.	—	1.5	—	1.5	—	1.5	
			typ.[2]	—	0.05	—	0.05	—	0.05	

Notes:
1. At f = f_{MAX}, address and data inputs are cycling at the maximum frequency, f = 0 means no input lines change.
2. Typical values are measured at V_{DD} = 3.3V, T_A = 25°C. Not 100% tested.

CAPACITANCE[1,2]

Symbol	Parameter	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	pF
$C_{I/O}$	Input/Output Capacitance	V_{OUT} = 0V	8	pF

Notes:
1. Tested initially and after any design or process changes that may affect these parameters.
2. Test conditions: T_A = 25°C, f = 1 MHz, V_{DD} = 3.3V.

READ CYCLE SWITCHING CHARACTERISTICS[1] (Over Operating Range)

Symbol	Parameter	-8 ns Min.	-8 ns Max.	-10 ns Min.	-10 ns Max.	-12 ns Min.	-12 ns Max.	Unit
t_{RC}	Read Cycle Time	8	—	10	—	12	—	ns
t_{AA}	Address Access Time	—	8	—	10	—	12	ns
t_{OHA}	Output Hold Time	2	—	2	—	2	—	ns
t_{ACE}	$\overline{CE}$ Access Time	—	8	—	10	—	12	ns
t_{DOE}	$\overline{OE}$ Access Time	—	4	—	5	—	6	ns
t_{LZOE}[2]	$\overline{OE}$ to Low-Z Output	0	—	0	—	0	—	ns
t_{HZOE}[2]	$\overline{OE}$ to High-Z Output	0	4	0	5	0	6	ns
t_{LZCE}[2]	$\overline{CE}$ to Low-Z Output	3	—	3	—	3	—	ns
t_{HZCE}[2]	$\overline{CE}$ to High-Z Output	0	4	0	5	0	6	ns
t_{PU}	$\overline{CE}$ to Power Up Time	0	—	0	—	0	—	ns
t_{PD}	$\overline{CE}$ to Power Down Time	—	8	—	10	—	12	ns

Notes:
1. Test conditions assume signal transition times of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V loading specified in Figure 1.
2. Tested with the loading specified in Figure 2. Transition is measured ±500 mV from steady-state voltage. Not 100% tested.

AC TEST CONDITIONS

Parameter	Unit
Input Pulse Level	0V to 3.0V
Input Rise and Fall Times	3 ns
Input and Output Timing and Reference Levels	1.5V
Output Load	See Figures 1 and 2

AC TEST LOADS

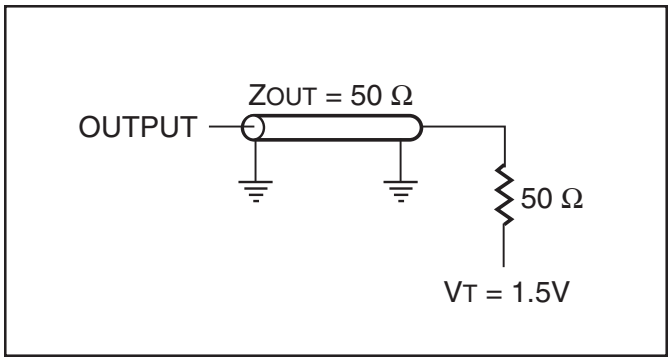


Figure 1

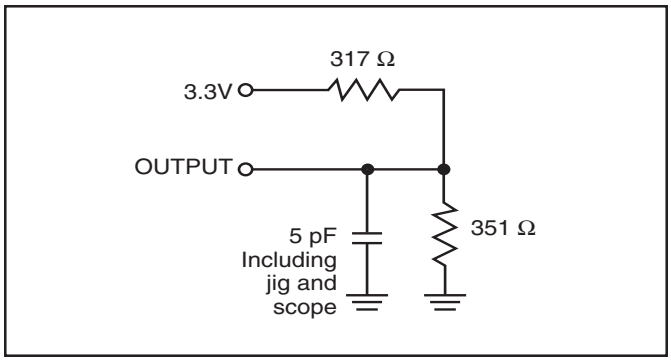
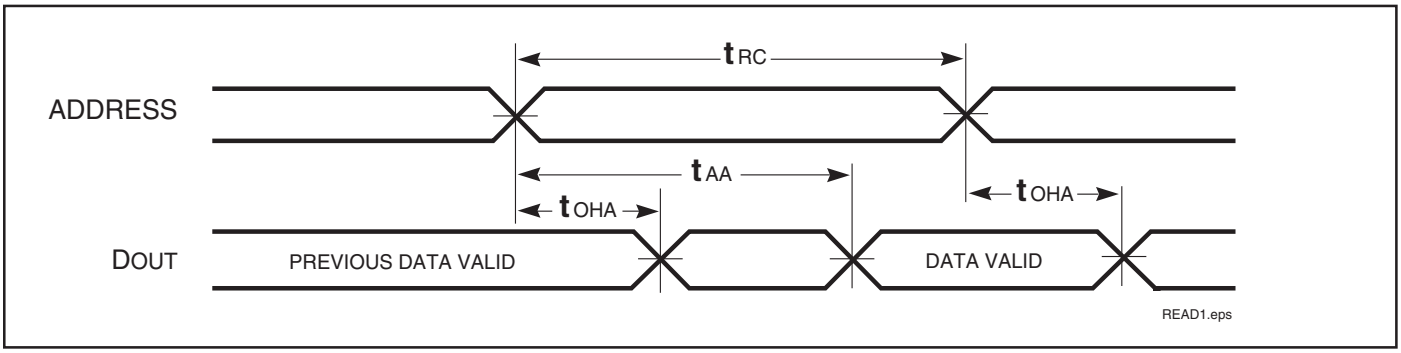


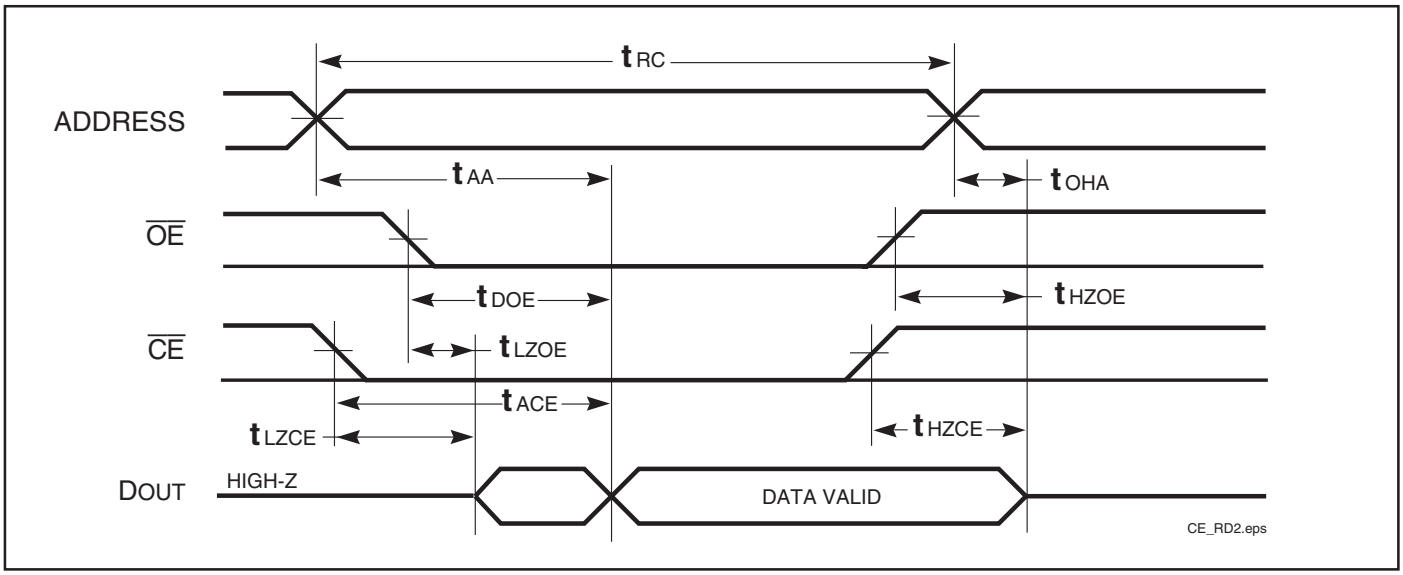
Figure 2

AC WAVEFORMS

READ CYCLE NO. 1[1,2]



READ CYCLE NO. 2[1,3]



Notes:
1. $\overline{WE}$ is HIGH for a Read Cycle.
2. The device is continuously selected. $\overline{OE}$, $\overline{CE}$ = V_{IL}.
3. Address is valid prior to or coincident with $\overline{CE}$ LOW transitions.

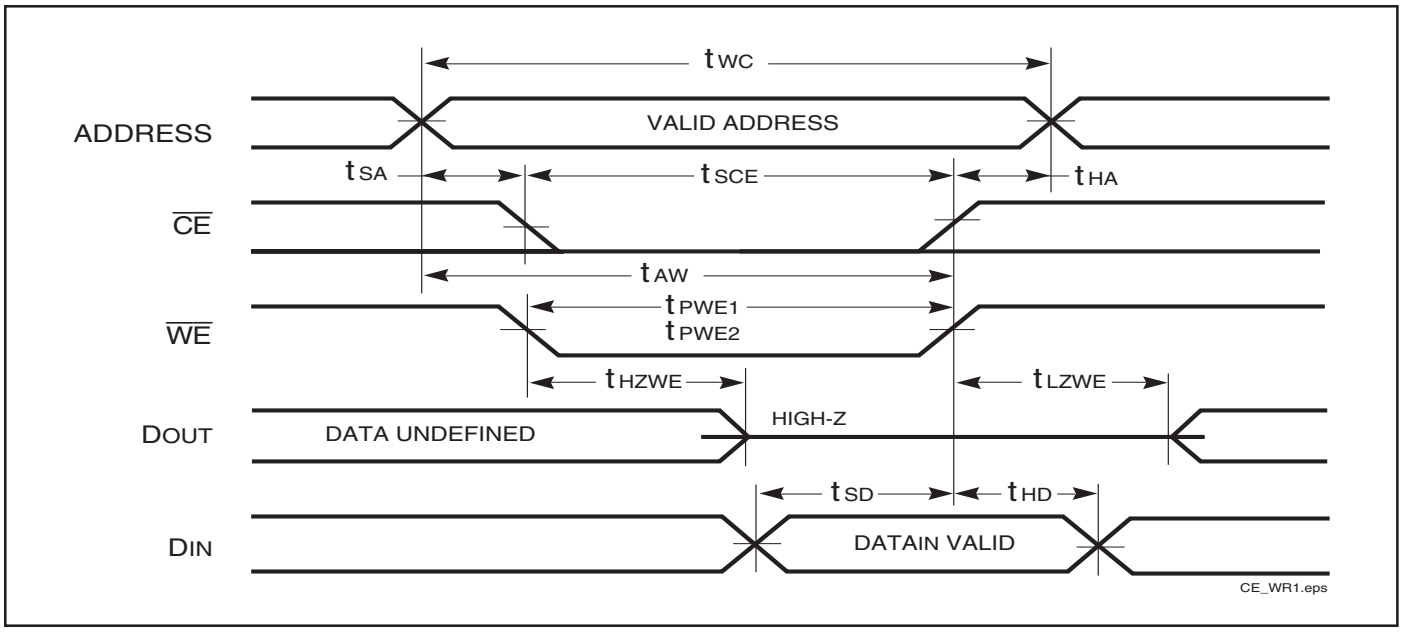
WRITE CYCLE SWITCHING CHARACTERISTICS[1,3] (Over Operating Range)

Symbol	Parameter	-8 ns Min.	-8 ns Max.	-10 ns Min.	-10 ns Max.	-12 ns Min.	-12 ns Max.	Unit
t_{WC}	Write Cycle Time	8	—	10	—	12	—	ns
t_{SCE}	$\overline{CE}$ to Write End	7	—	7	—	8	—	ns
t_{AW}	Address Setup Time to Write End	8	—	8	—	8	—	ns
t_{HA}	Address Hold from Write End	0	—	0	—	0	—	ns
t_{SA}	Address Setup Time	0	—	0	—	0	—	ns
t_{PWE_1}[1]	$\overline{WE}$ Pulse Width ($\overline{OE}$ High)	7	—	7	—	8	—	ns
t_{PWE_2}[2]	$\overline{WE}$ Pulse Width ($\overline{OE}$ Low)	8	—	10	—	12	—	ns
t_{SD}	Data Setup to Write End	5	—	5	—	6	—	ns
t_{HD}	Data Hold from Write End	0	—	0	—	0	—	ns
t_{HZWE}[2]	$\overline{WE}$ LOW to High-Z Output	—	4	—	5	—	6	ns
t_{LZWE}[2]	$\overline{WE}$ HIGH to Low-Z Output	3	—	3	—	3	—	ns

Notes:
1. Test conditions assume signal transition times of 3ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading specified in Figure 1.
2. Tested with the load in Figure 2. Transition is measured ±500 mV from steady-state voltage. Not 100% tested.
3. The internal write time is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the Write.

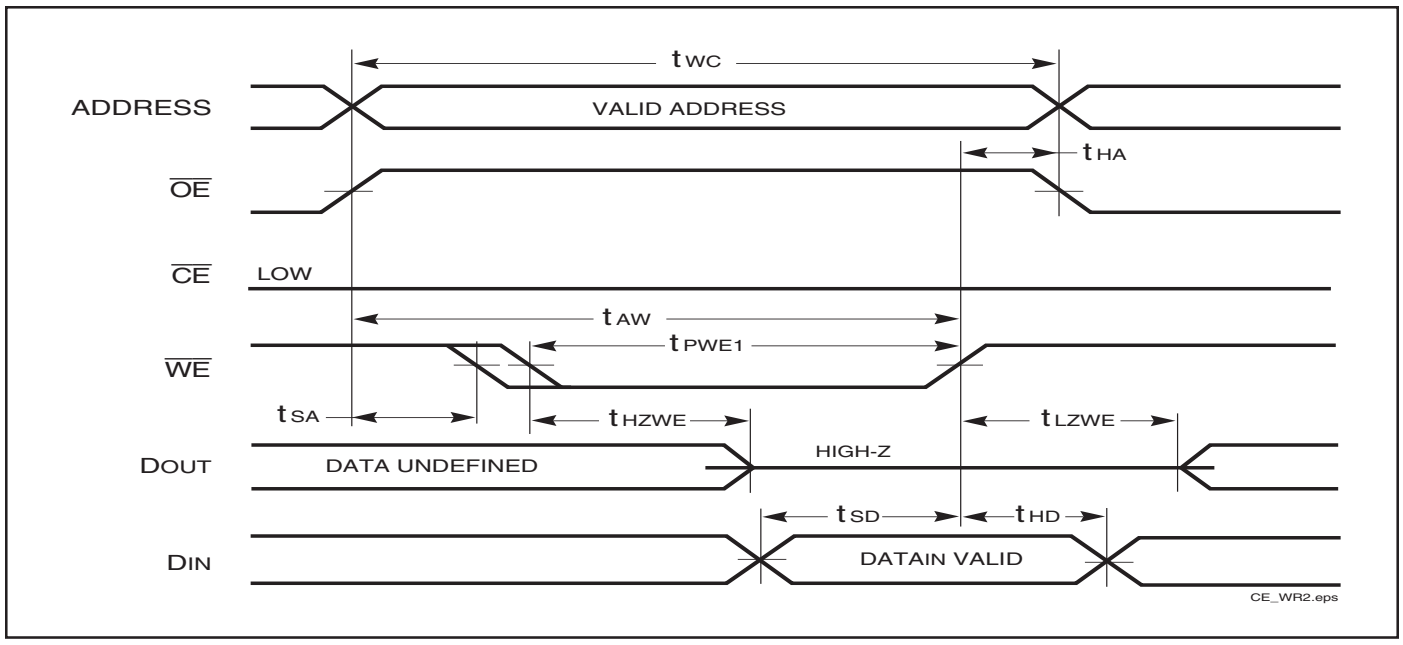
AC WAVEFORMS

WRITE CYCLE NO. 1[1,2] ($\overline{CE}$ Controlled, $\overline{OE}$ = HIGH or LOW)

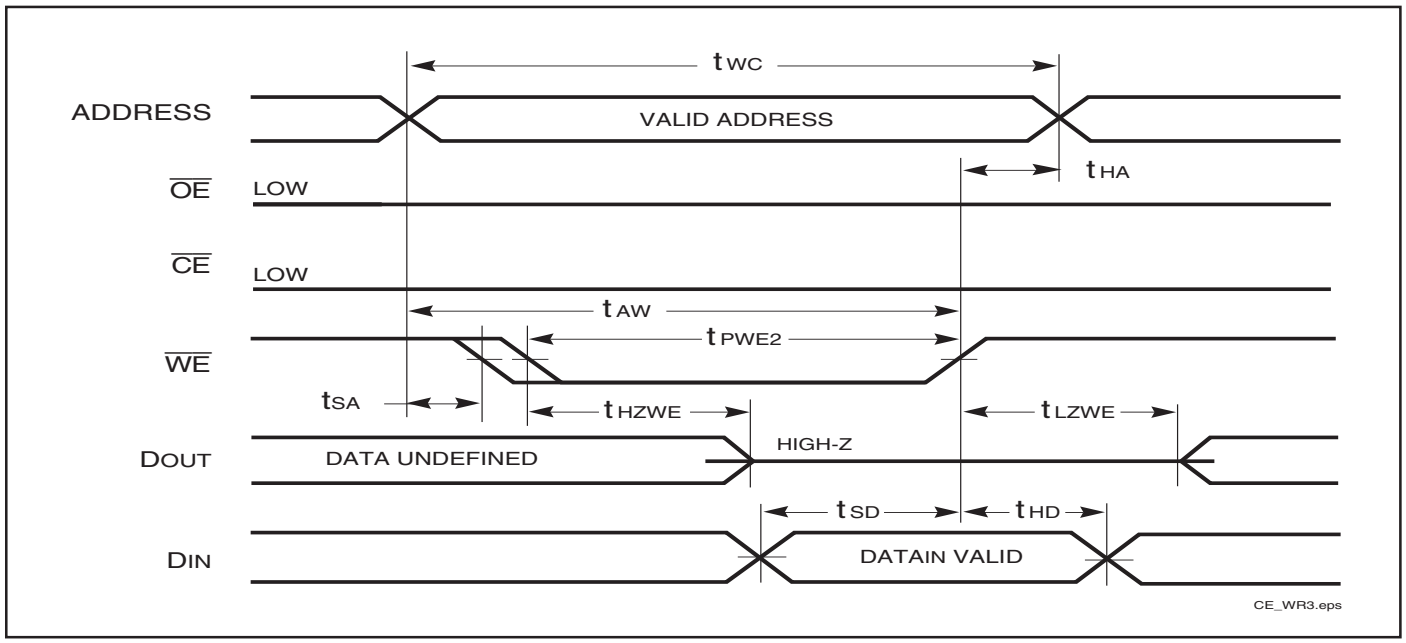


AC WAVEFORMS

WRITE CYCLE NO. 2[1] ($\overline{WE}$ Controlled, = HIGH during Write Cycle)



($\overline{WE}$ Controlled: $\overline{OE}$ is LOW During Write Cycle)

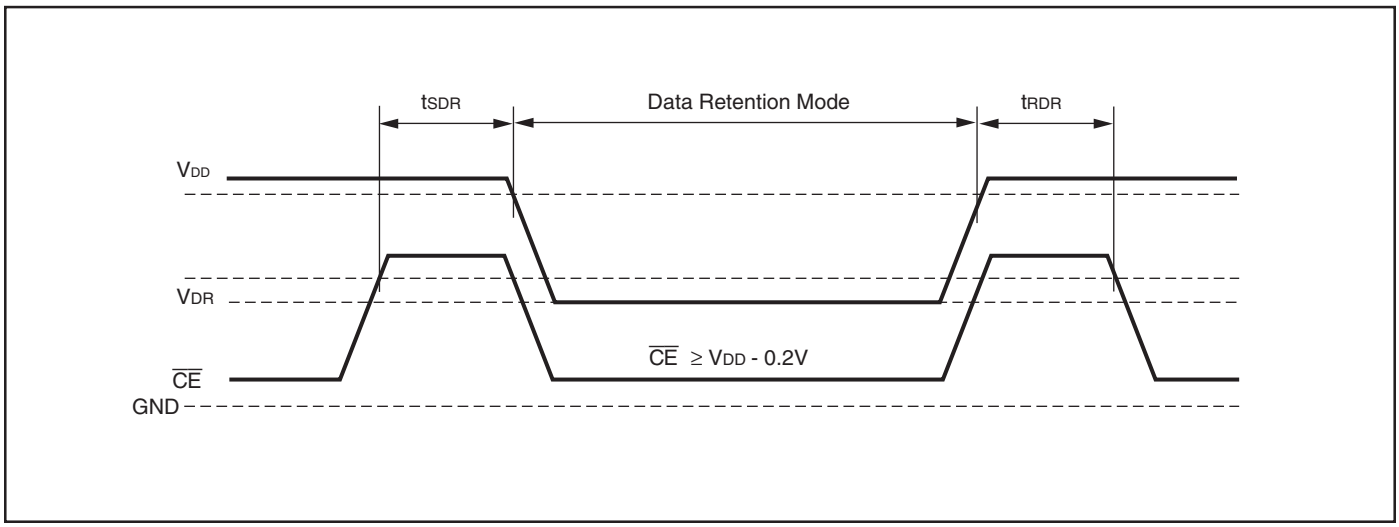


Notes:
1. The internal write time is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the Write.
2. I/O will assume the High-Z state if $\overline{OE}$ > V_{IH}.

Symbol	Parameter	Test Condition	Options	Min.	Typ.(1)	Max.	Unit
V_{DR}	V_{DD} for Data Retention	See Data Retention Waveform		2.0	—	3.6	V
I_{DR}	Data Retention Current	V_{DD} = 2.0V, $\overline{CE} \geq V_{DD} - 0.2V$	IS63LV1024	—	0.5	10	mA
			IS63LV1024L	—	0.05	1.5	
t_{SDR}	Data Retention Setup Time	See Data Retention Waveform		0	—	—	ns
t_{RDR}	Recovery Time	See Data Retention Waveform		t_{RC}	—	—	ns

Note 1: Typical values are measured at V_{DD} = 3.0V, T_A = 25°C and not 100% tested.

($\overline{CE}$ Controlled)



Speed (ns)	Order Part No.	Package
8	IS63LV1024-8K	400-mil Plastic SOJ
	IS63LV1024-8KL	400-mil Plastic SOJ, Lead-free
10	IS63LV1024-10T	TSOP (Type II)
	IS63LV1024-10J	300-mil Plastic SOJ
	IS63LV1024-10K	400-mil Plastic SOJ
12	IS63LV1024-12T	TSOP (Type II)
	IS63LV1024-12J	300-mil Plastic SOJ
	IS63LV1024-12JL	300-mil Plastic SOJ, Lead-free
	IS63LV1024-12KL	400-mil Plastic SOJ, Lead-free

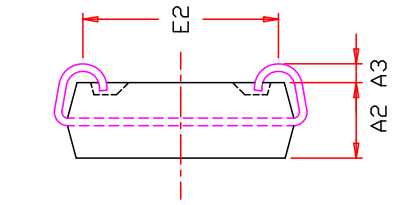
Speed (ns)	Order Part No.	Package
8	IS63LV1024-8KI	400-mil Plastic SOJ
10	IS63LV1024-10KI	400-mil Plastic SOJ
12	IS63LV1024-12TI	TSOP (Type II)

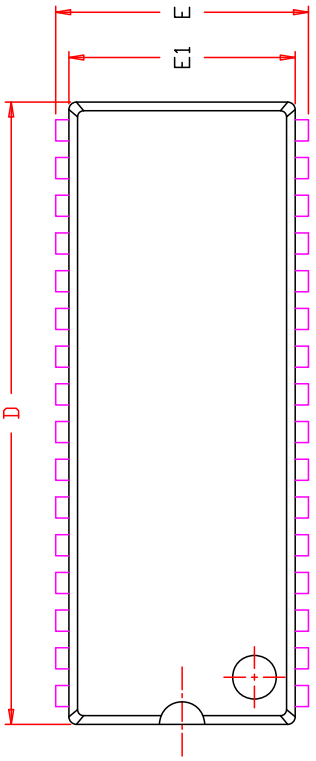
Speed (ns)	Order Part No.	Package
8	IS63LV1024L-8T	TSOP (Type II)
	IS63LV1024L-8TL	TSOP (Type II), Lead-free
	IS63LV1024L-8B	mBGA (8mmx10mm)
10	IS63LV1024L-10T	TSOP (Type II)
	IS63LV1024L-10TL	TSOP (Type II), Lead-free
	IS63LV1024L-10HL	sTSOP (Type I) (8mm x13.4mm), Lead-free
12	IS63LV1024L-12T	TSOP (Type II)
	IS63LV1024L-12TL	TSOP (Type II), Lead-free
	IS63LV1024L-12H	sTSOP (Type I) (8mm x13.4mm)
	IS63LV1024L-12J	300-mil Plastic SOJ
	IS63LV1024L-12JL	300-mil Plastic SOJ, Lead-free
	IS63LV1024L-12B	mBGA (8mmx10mm)

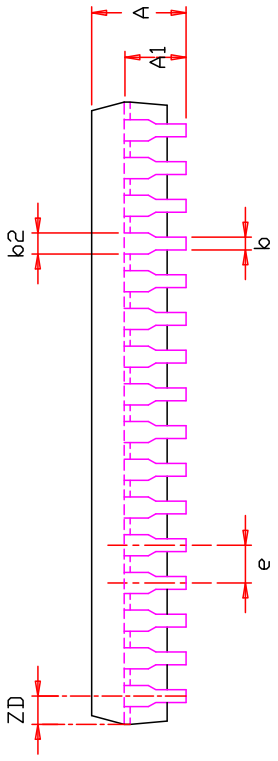
Speed (ns)	Order Part No.	Package
8	IS63LV1024L-8TI	TSOP (Type II)
	IS63LV1024L-8JI	300-mil Plastic SOJ
	IS63LV1024L-8KI	400-mil Plastic SOJ
	IS63LV1024L-8BI	mBGA (8mmx10mm)
10	IS63LV1024L-10HI	sTSOP (Type I) (8mm x13.4mm)
	IS63LV1024L-10JLI	300-mil Plastic SOJ, Lead-free
	IS63LV1024L-10KLI	400-mil Plastic SOJ, Lead-free
	IS63LV1024L-10TLI	TSOP (Type II), Lead-free
12	IS63LV1024L-12BI	mBGA (8mmx10mm)
	IS63LV1024L-12BLI	mBGA (8mmx10mm), Lead-free
	IS63LV1024L-12TI	TSOP (Type II)
	IS63LV1024L-12TLI	TSOP (Type II), Lead-free

Speed (ns)	Top Mark	Order Part No.	Package
8	IS63LV1024L-10KLI	U788B-8KLI	400-mil Plastic SOJ, Lead-free
	IS63LV1024L-10TLI	U788A-8TLI	TSOP (Type II), Lead-free

SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	3.05	—	3.76	0.120	—	0.148
A1	2.08	—	2.41	0.082	—	0.095
A2	2.41	2.54	2.67	0.095	0.100	0.105
A3	0.64	—	1.09	0.025	—	0.043
b	0.41	—	0.51	0.016	—	0.020
b2	0.66	—	0.81	0.026	—	0.032
D	20.82	—	21.09	0.820	—	0.830
E	8.38	8.51	8.64	0.330	0.335	0.340
E1	7.49	7.62	7.75	0.295	0.300	0.305
E2	6.48	—	6.99	0.255	—	0.275
e	1.27 BSC.			0.050 BSC.		
ZD	0.95 REF.			0.037 REF.		





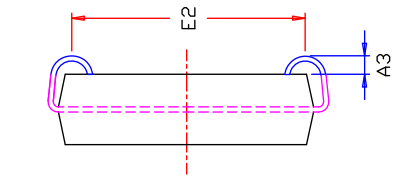


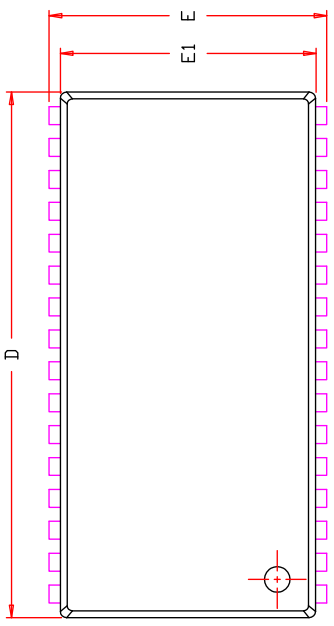
NOTE :

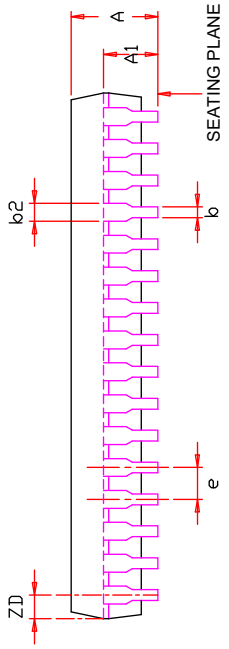
1. CONTROLLING DIMENSION : MM
2. DIMENSION D AND E1 DO NOT INCLUDE MOLD PROTRUSION.
3. DIMENSION b2 DOES NOT INCLUDE DAMBAR PROTRUSION/INTRUSION.

TITLE	32L 300mil SOJ Package Outline	REV.	C	DATE	08/14/2009

SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	3.25	—	3.76	0.128	—	0.148
A1	2.08	—	—	0.082	—	—
A3	0.635	—	—	0.025	—	—
b	0.38	—	0.51	0.015	—	0.020
b2	0.66	0.71	0.81	0.026	0.028	0.032
D	20.82	20.95	21.08	0.820	0.825	0.830
E	11.05	11.18	11.30	0.435	0.440	0.445
E1	10.03	10.16	10.29	0.395	0.400	0.405
E2	9.40 BSC			0.370 BSC		
e	1.27 BSC.			0.050 BSC.		
ZD	0.95 REF			0.037 REF		





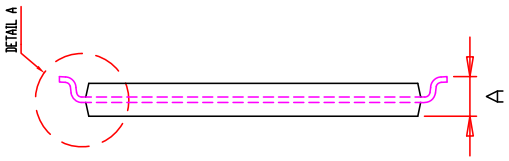


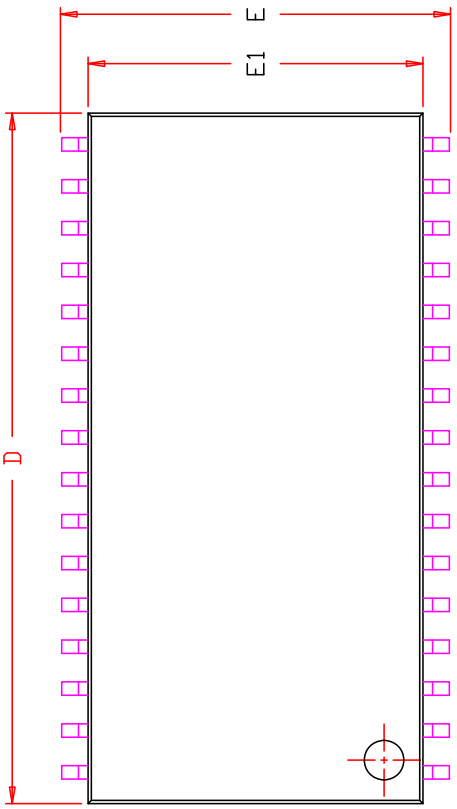
NOTE :

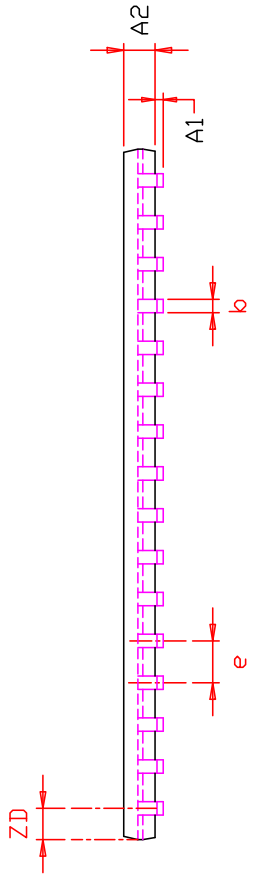
1. Controlling dimension : mm
2. Dimension D and E1 do not include mold protrusion .
3. Dimension b2 does not include dambar protrusion/intrusion.
4. Formed leads shall be planar with respect to one another within 0.1mm at the seating plane after final test.
5. Reference document : JEDEC SPEC MS-027.

	TITLE	32L 400mil SOJ Package Outline	REV.	E	DATE	12/19/2007

SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	1.00	—	1.20	0.039	—	0.047
A1	0.05	—	0.15	0.002	—	0.006
A2	0.95	1.00	1.05	0.037	0.039	0.041
b	0.30	—	0.52	0.012	—	0.020
D	20.82	20.95	21.08	0.820	0.825	0.830
E	11.56	11.76	11.96	0.455	0.463	0.471
E1	10.03	10.16	10.29	0.395	0.400	0.405
e		1.27 BSC.			0.050 BSC.	
L	0.40	0.50	0.60	0.016	0.020	0.024
L1		0.25 BSC.			0.010 BSC.	
ZD		0.95 REF.			0.037 REF.	
θ	0	—	8°	0	—	8°

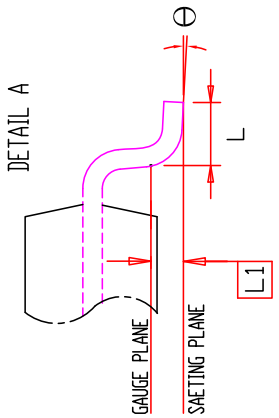




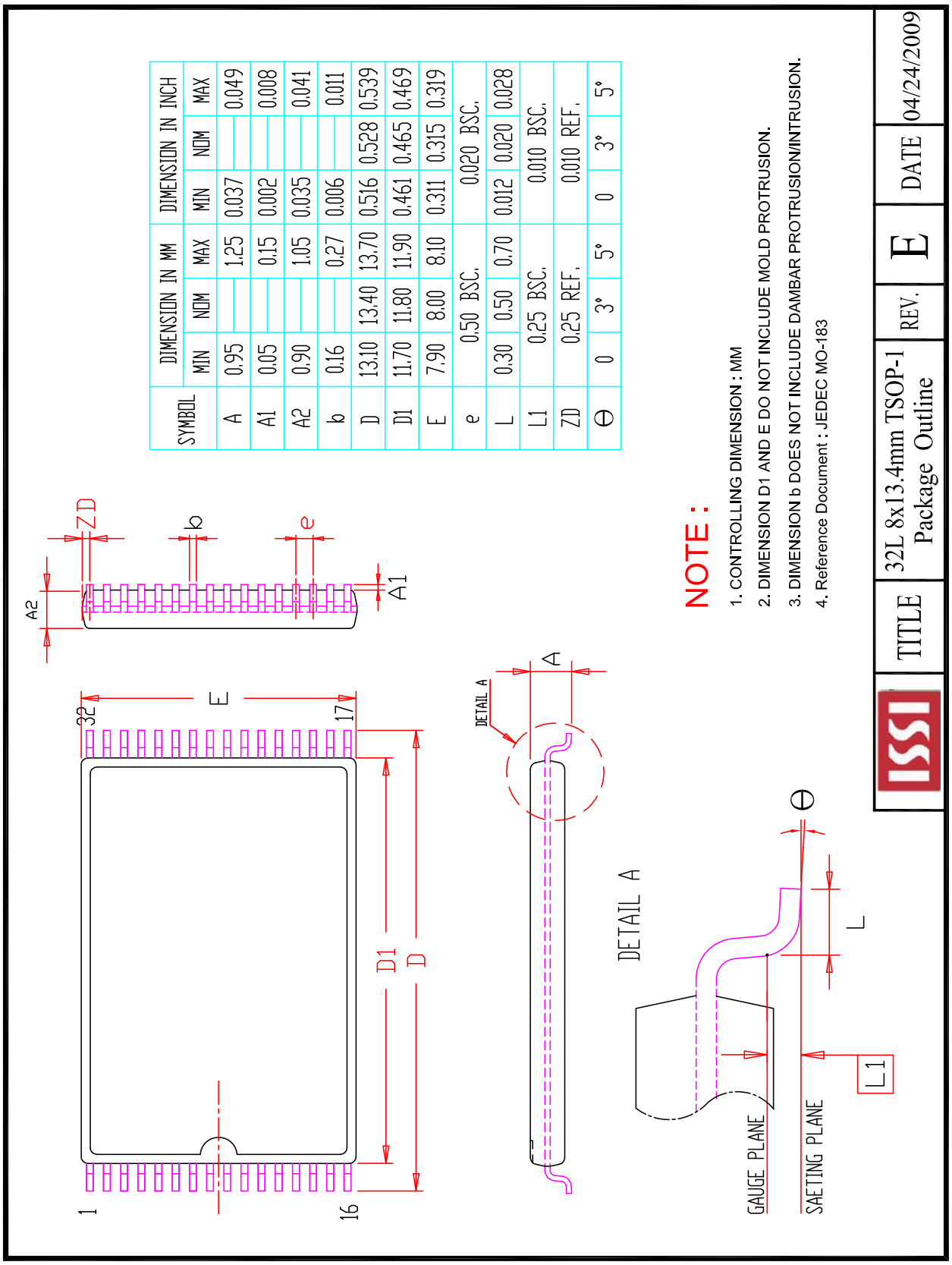


NOTE :

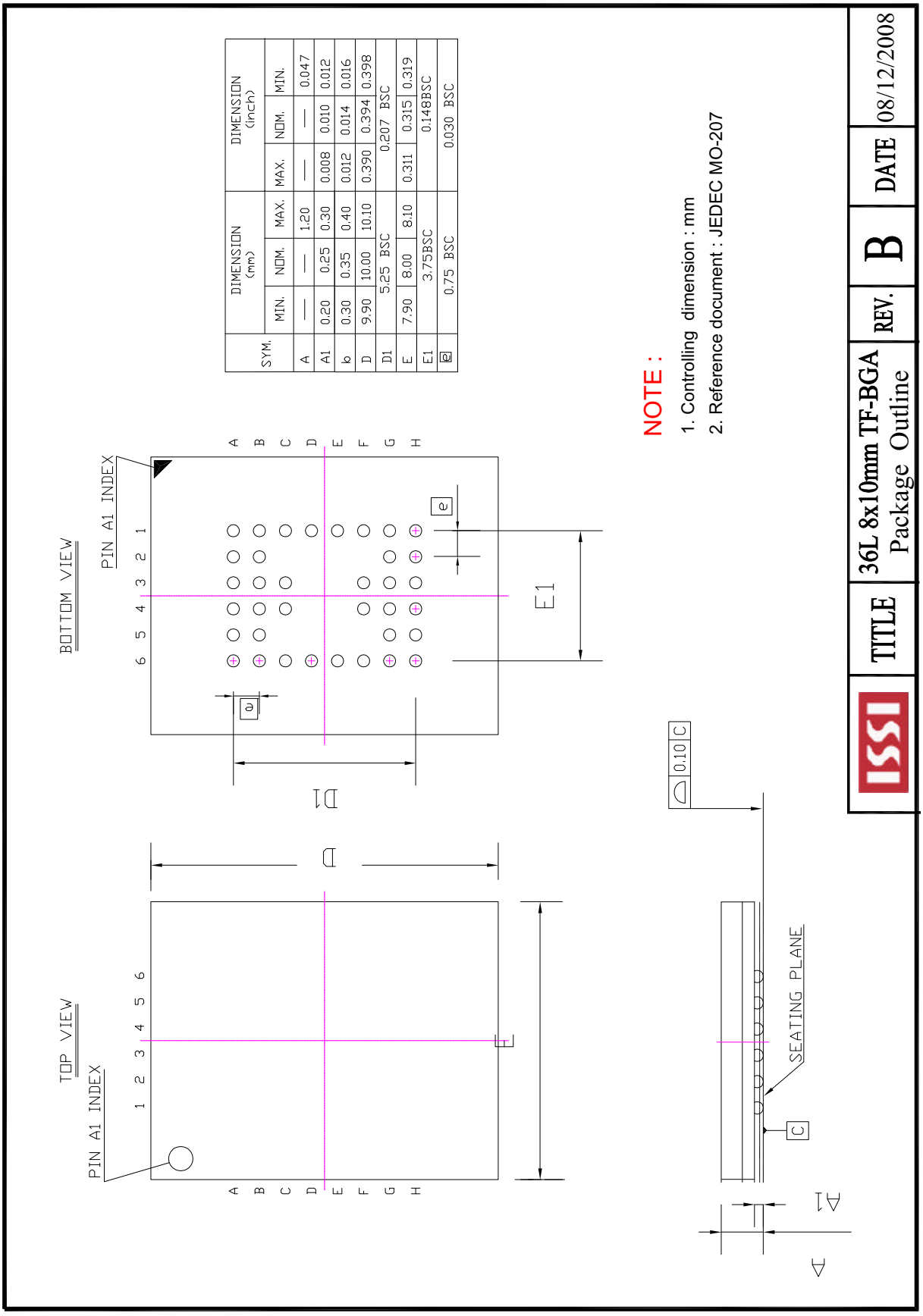
1. CONTROLLING DIMENSION : MM
2. DIMENSION D AND E1 DO NOT INCLUDE MOLD PROTRUSION.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION/INTRUSION.



ISSI	TITLE	32L 400mil TSOP-2 Package Outline	REV. E	DATE 06/23/2009



SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.95	—	1.25	0.037	—	0.049
A1	0.05	—	0.15	0.002	—	0.008
A2	0.90	—	1.05	0.035	—	0.041
b	0.16	—	0.27	0.006	—	0.011
D	13.10	13.40	13.70	0.516	0.528	0.539
D1	11.70	11.80	11.90	0.461	0.465	0.469
E	7.90	8.00	8.10	0.311	0.315	0.319
e	0.50 BSC.			0.020 BSC.		
L	0.30	0.50	0.70	0.012	0.020	0.028
L1	0.25 BSC.			0.010 BSC.		
ZD	0.25 REF.			0.010 REF.		
Θ	0	3°	5°	0	3°	5°



SYM.	DIMENSION (mm)			DIMENSION (inch)		
	MIN.	NOM.	MAX.	MAX.	NOM.	MIN.
A	—	—	1.20	—	—	0.047
A1	0.20	0.25	0.30	0.008	0.010	0.012
b	0.30	0.35	0.40	0.012	0.014	0.016
D	9.90	10.00	10.10	0.390	0.394	0.398
D1		5.25 BSC			0.207 BSC	
E	7.90	8.00	8.10	0.311	0.315	0.319
E1		3.75BSC			0.148BSC	
e		0.75 BSC			0.030 BSC	