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ATM Physical Layer Core

Features

- ATM header error correction (HEC) byte generation/checking

- HEC-based cell delineation

- Cell header single error correction/multiple error detection

- Cell payload (de)scrambling

- Direct cell mapping

- Idle cell insertion/deletion

- Out of cell delineation (OCD)/loss of cell delineation (LCD) status

- User-programmable cell filter

- UTOPIA Level 1/Level 2 with parity generation/ checking. In Level 2, all multiPHY modes are supported:
  — 1 RxClav/1 TxClav
  — Direct status
  — Multiplexed status polling

- 155.52 Mbits/s line operation

- 25 MHz UTOPIA operation (up to 50 MHz stand-alone UTOPIA)

- FIFO control/monitoring with options:
  — Internal 128 x 9 *ORCA*® FIFOs (scalable)
  — External 2^n x 9 IDT722x1FIFOs

- Flexible control inputs with options for:
  — Internal/external hard-wiring
 — Access via a parallel or serial microprocessor interface

Standards Compliance

- *ANSI* T1.646-1995: Broadband-ISDN Physical Layer Specification for User-Network Interface Including DS1/ATM*

- Asynchronous transfer mode (ATM) forum user-network interface (UNI) version 3.1

- ATM forum UTOPIA, An ATM-PHY interface specification level 1, version 2.01

- ATM forum UTOPIA Level 2, version 1.0

- ITU-T recommendation I.432: B-ISDN user-network interface physical layer specification

Benefits

- Faster development for improved time-to-market with ATM functions.

- Lower development cost through design reuse.

- VHDL source code for easy design integration.

- *ORCA*-specific optimization, tailor made for high performance.

- Ample design flexibility using built-in interface and function options.

- Verified functionality and standards compliance.
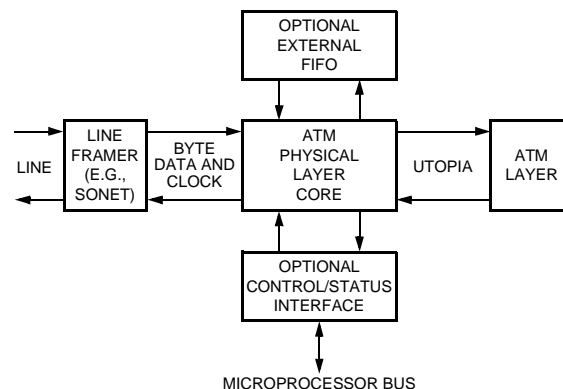
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Figure 1. ATM Physical Layer Core Application

* *ANSI* is a registered trademark of American National Standards Institute, Inc.

Description

The ATM physical layer core from *Modelware** implements, in modular VHDL, the broadband ISDN (B-ISDN) functions of the transmission convergence (TC) sublayer.

The core interfaces to the transmission line via a line framer, and to the ATM layer via a UTOPIA Level 1 or Level 2 interface (Figure 1). The core has the option of using internal or external FIFOs for cell buffering and timing transfer between the line and the ATM layer.

The core using external FIFOs synthesizes into an OR2C/2T15A and the core with two internal 128 x 9 FIFOs synthesizes into an OR2C/2T26A. When implemented using a –4 or faster speed *ORCA* FPGA, the core operates at 19.44 Mbytes/s (155.52 Mbits/s) on the line side and at 25 MHz on the UTOPIA side.

Design Package

The ATM physical layer core package contains:

■ VHDL source code

■ VHDL testbench

■ Scripts and data files for simulation (behavioral and gate-level), synthesis, and FPGA layout

■ Detailed documentation:
— Reference guide: features, architecture, interfaces, and operation
— User's guide: simulation, synthesis, and FPGA layout procedures

Required Tools

■ *MTI*[†] *ModelSim*[‡] for simulation

■ *Exemplar Logic Leonardo Spectrum*[§] for synthesis

■ Lucent Technologies *ORCA* Foundry for FPGA layout

Additional Resources

■ *ORCA ATM Physical Layer CSC Application Note* (AP97-050FPGA available from Lucent Technologies)

■ *ORCA OR2CxxA and OR2TxxA Series Field Programmable Gate Arrays* Data Sheet (DS98-140), January 1996

■ Asynchronous Transfer Mode: *ATM Architecture and Implementation*, Martin et al., Prentice Hall 1996

Ordering Information

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