

Version : 1.0

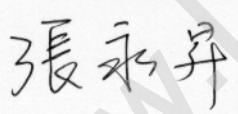
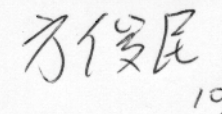
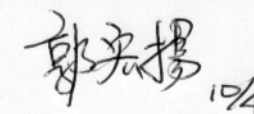
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 Http://www.lcdfriends.com

TECHNICAL SPECIFICATION

MODEL NO. : P25EN1

■ **Customer Approval** Company Name : _____

Approved By: _____ Date : _____

Approved by Product Section Manager	Checked by Product Engineer	Prepared by FAE section Manager
 張永昇 10/4 2000	 陳俊 10/4	 郭秉揚 10/4

Date : Sep. 29, 2000

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TECHNICAL SPECIFICATION**CONTENTS**

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1. Application

This technical specification applies to 2.5" color TFT-LCD panel. The 2.5" color TFT LCD panel is designed for camcorder, digital camera application and other electronic products which require high quality flat panel displays.

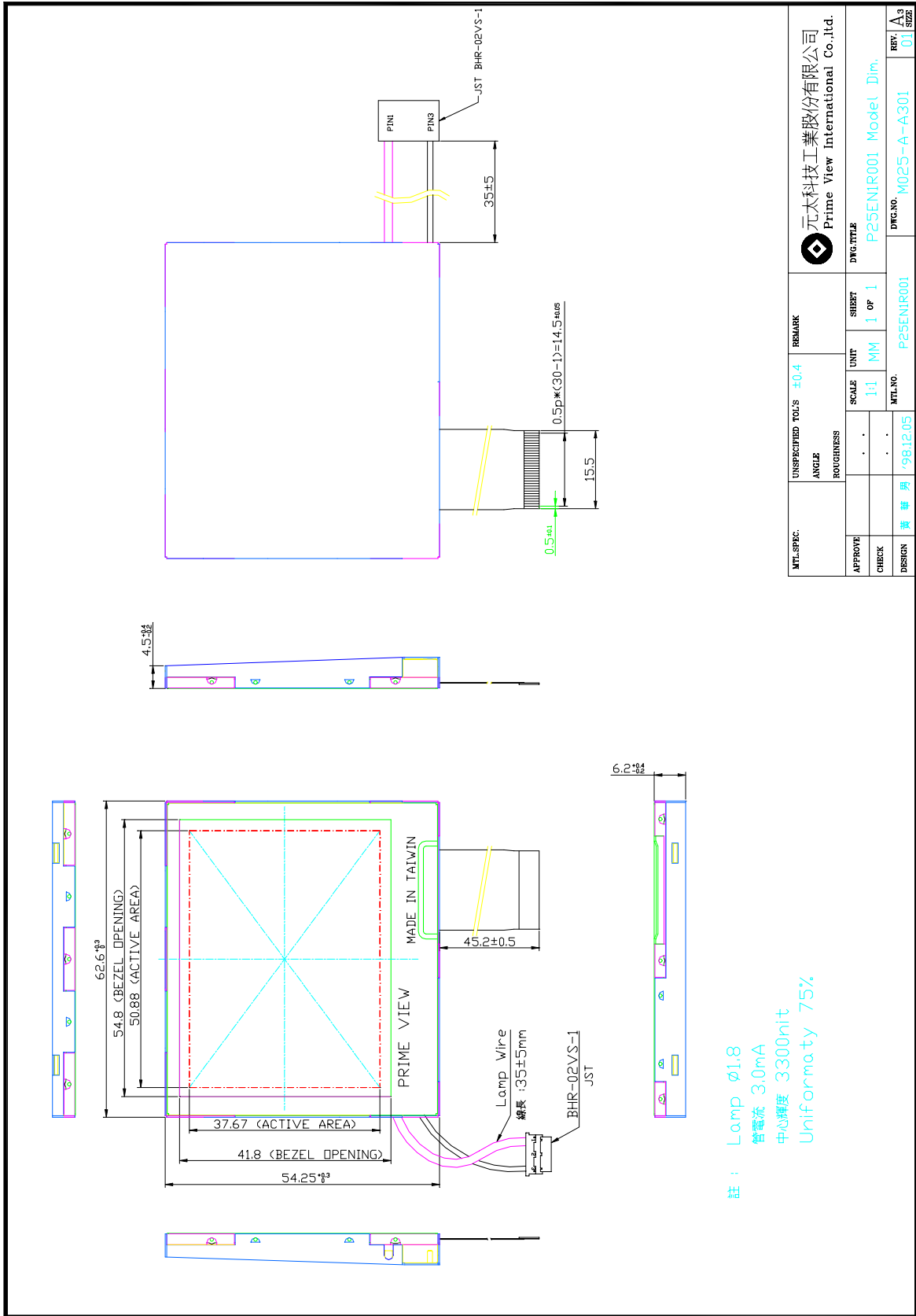
2. Features

- . Controller IC is not necessary
- . Compatible with NTSC or PAL system
- . High Resolution : 112,320 Dots
- . Optimum Viewing Direction : 6 o'clock
- . Up/Down and Left/Right Image Reversion

3. Mechanical Specifications

Parameter	Specifications	Unit
Screen Size	2.5 (diagonal)	inch
Display Format	480x 234	dot
Active Area	50.88x 37.67	mm
Dot Pitch	0.106 (W)x 0.161(H)	mm
Pixel Configuration	Delta	
Outline Dimension	See Mechanical Drawing	mm
Weight	36	g

4. Mechanical Drawing of panel:



MFG. SPEC.	UNSPECIFIED TOL'S	± 0.4	REMARK	元太科技工業股份有限公司 Prime View International Co., Ltd.	DWG. TITLE	P25ENIR001 Model Dim.	
	ANGLE				DWG. NO.	M025-A-A301	REV. Δ 01
APPROVE				SCALE	1:1	SHEET	1 OF 1
CHECK				UNIT	MM	MTL. NO.	P25ENIR001
DESIGN	黃 華 明	'98.12.05					

5.Input / Output Terminals

Pin No	Symbol	I/O	Description	Remark
1	V_{COM}	I	Common Electrode Voltage	Note 5-1
2	V_{BBA}	I	Supply Voltage for Level Shifter (Low Level)	Note 5-2
3	PV_{DD}	I	Supply voltage for panel	Note 5-3
4	V_{BBC}	I	Supply voltage for panel	Note 5-2
5	V_{SS}	I	Ground for panel	
6	V_{CC}	I	Supply Voltage for Level Shifter (High Level)	Note 5-4
7	V_{PIN}	I	Pulse high level for Level Shifter (High Level)	Note 5-5
8	V_{MIN}	I	Pulse low level for Level Shifter (Low Level)	Note 5-5
9	FRP	O	Control Signal for Video Inversion	
10	\overline{VSY}	I/O	Vertical Sync.	
11	\overline{HSY}	I/O	Horizontal Sync.	
12	C_{SYNC}	I	Composite Sync.	
13	PD	O	Phase Detector	Note 5-6
14	OSC	I	Clock Input for LC Oscillator	Note 5-6
15	V_{DD}	I	Supply Voltage for Logic Circuit	Note 5-3
16	CKC	I	Control Pin for Select I/O Signal	Note 5-12
17	UD	I	Up / Down Control	Note 5-11
18	LR	I	Left / Right Shift Control	Note 5-7
19	NP	I	NTSC / PAL Selector	Note 5-8
20	V_B	I	Video Input B	
21	V_G	I	Video Input G	
22	V_R	I	Video Input R	
23	GND	I	Ground for High voltage logic	
24	GND	I	Ground for logic	
25	DV_{EE}	I	Voltage supply for source driver high logic	Note 5-9
26	C_{COM}	I	Reference for Sample and Hold	Note 5-10
27	AV_{EE}	I	Voltage supply for sample & hold	Note 5-9
28	GND	I	Ground	
29	OV_{EE}	I	Voltage supply for operation amplifier	Note 5-9
30	VP+	I	Pre-charge high level	Note 5-9

Note 5-1 : V_{COM} should be adjusted accurately to get the best contrast ratio.

Note 5-2 : $V_{BBA}, V_{BBC} = -5V$ (Typ.)

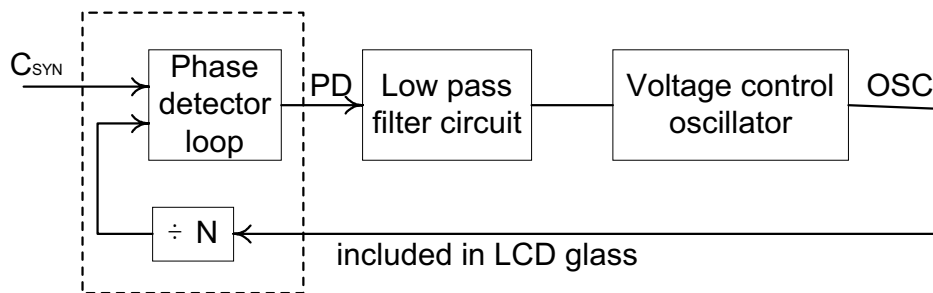
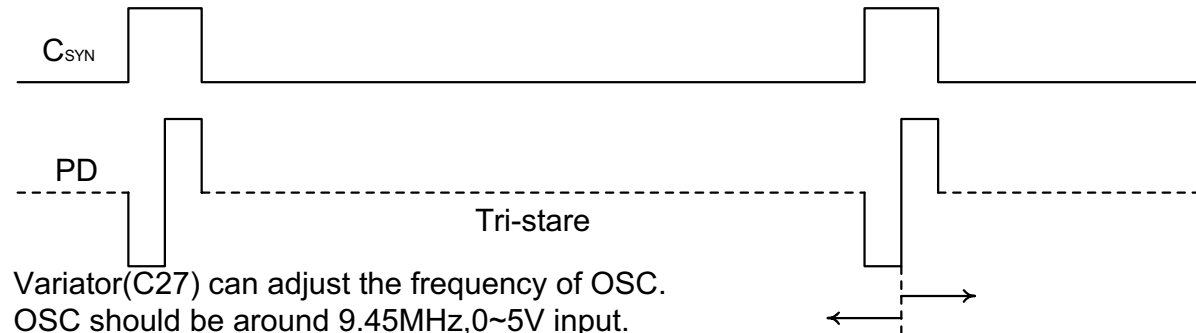
Note 5-3 : $V_{DD}, PV_{DD} = +5V$ (Typ.)

Note 5-4 : $V_{CC}=+20V(Typ.)$

Note 5-5 : V_{PIN} must be more positive than V_{MIN} .

Pin	Symbol	min	Typ.	Max.	Unit
7	V_{PIN}	12	13	14	V
8	V_{MIN}	5	6	7	V

Note 5-6 : PD output(0~5V range) from phase detector loop which is included in source driver.



Note 5-7 : Left / Right SHIFT .

Note 5-8 : Hi (+5V) for NTSC ; Low (0V) for PAL.

Note 5-9 : $DV_{EE}, AV_{EE}, OV_{EE}$ and $VP+$ all equal to +14V

Note 5-10 : $C_{COM} \doteq +5V (Typ.)$

Note 5-11 : UP / Down Shift

Note 5-12 : Pin 16(CKC) can select the function for Pin 11(\overline{HSY}) and Pin 10(\overline{VSY}).

CKC	\overline{HSY}	CSY	\overline{VSY}
Hi	\overline{HSY}	CSY Input	\overline{VSY} Output
Low	External \overline{HSY} Input	External Clock Input	External \overline{VSY} Input

6. Absolute Maximum Ratings:

GND = 0 V , Ta = 25 °C

Parameter	Symbol	MIN.	MAX.	Unit	Remark
Supply Voltage for Source Driver	DV _{EE} , AV _{EE} OV _{EE} , VP+	0	+16	V	
Supply Voltage for Gate Driver	H Level	V _{CC}	0	+26	V
	L Level	V _{BBA} , V _{BBC}	-7	+20	V
Supply voltage for controller	PV _{DD} , V _{DD}	0	+6.5	V	
DC bias voltage of common electrode	V _{com}	+2	+6	V	
Analog input signals	V _B , V _R , V _G		+12	V	

7. Electrical Characteristics
7-1) Recommended Operating Conditions:
A) Driving for TFT-LCD panel

GND = 0V , Ta = 25 °C

Parameter	Symbol	MIN.	TYP.	MAX.	Unit	Remark
Supply voltage for source driver	DV _{EE} , AV _{EE} OV _{EE} , VP+	+13.5	+14	+15	V	
Supply voltage for gate driver	H Level	V _{CC}	+19	+20	+24	V
	L level	V _{BBA} , V _{BBC}	-5.5	-5	-4	V
Supply voltage for controller	PV _{DD} , V _{DD}	+4.7	+5	+5.3	V	
Analog input voltage	Amplitude	V _B , V _R , V _G	+1.1		12	V
	DC component		+4	+6	+8	V

 ** Turn on sequence: -5V 、 +5V Input → C_{SYNC}. V_B, V_R, V_G Input → +14V 、 +20V Input

 Turn off sequence: +14V 、 +20V Input → C_{SYNC}. V_B, V_R, V_G Input → -5V 、 +5V Input

B) Driving for Backlight

Ta = 25 °C

Parameter	Min.	Typ.	Max.	Unit	Remark
Lamp voltage		220		Vrms	
Lamp current		3		mA	
Lamp frequency		35		KHz	

7-2) Power Consumption

Parameter	Conditions	TYP.	Unit	Remark
Current for V_{CC}	$V_{CC} = +20V$	1.5	mA	
Current for V_{BBA}	$V_{BBA} = -5V$	1.3	mA	
Current for V_{BBC}	$V_{BBC} = -5V$	0.05	mA	
Current for DV_{EE}	$DV_{EE} = +14V$	0.5	mA	
Current for AV_{EE}	$AV_{EE} = +14V$	3.0	mA	
Current for OV_{EE}	$OV_{EE} = +14V$	4.0	mA	
Current for PV_{DD}	$PV_{DD} = +5V$	0.2	mA	
Current for V_{DD}	$V_{DD} = +5V$	4.8	mA	
LCD Panel Power Consumption		0.18	W	
Backlight Power Consumption		0.66	W	

7-3) Input / Output Timing

Parameter		Symbol	MIN.	TYP.	MAX.	Unit	Remarks
Horizontal Sync. Output Pulse	Width	T_{HO}	4.2	4.7	5.2	μs	
	Phase Difference	T_{HP}	0	2		μs	
	Rising Time	T_{HR}	-	-	0.5	μs	
	Falling Time	T_{HF}	-	-	0.5	μs	
Vertical Sync. Output Pulse	Width	T_{VO}	-	4H	-	μs	H=1/15.75K HZ
	Phase Difference	T_{VPO}	-	1H	-	μs	odd field
	Phase Difference	T_{VPE}	-	0.5H	-	μs	even field
	Rising Time	T_{VR}	-	-	2	μs	
	Frequency	f_{FRP}	7.67	7.87	8.07	KHz	
Polarity Alternating Signal	Delay time	T_{FD}	-	-	4	μs	
	Falling Time	T_{VF}	-	-	2	μs	

7-4) Display Time Range

A) When sync. signal of NTSC system is applied.

a) Horizontally

12.6 ~ 63.39 μ s.

b) Vertical

19 ~ 253 H

B) When sync. signal of PAL system is applied.

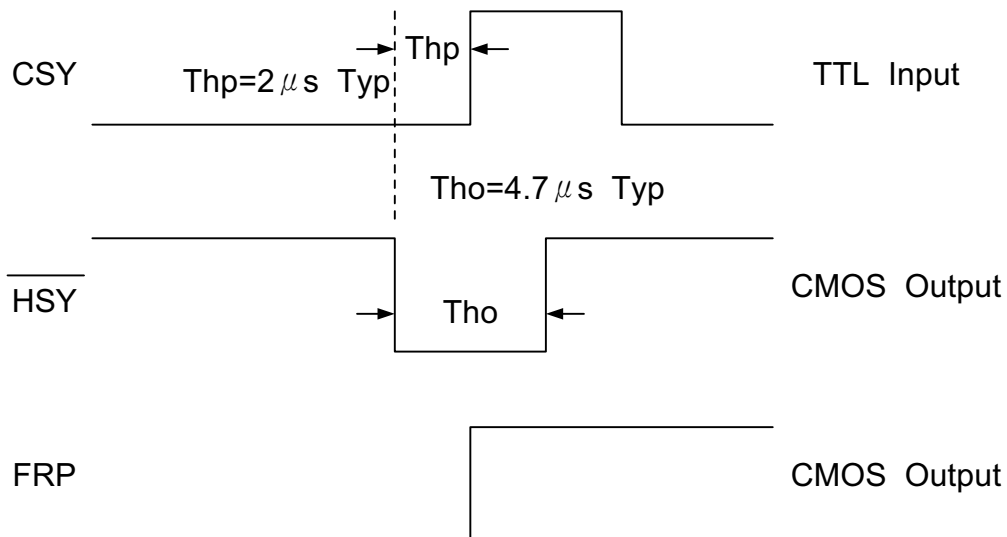
a) Horizontally

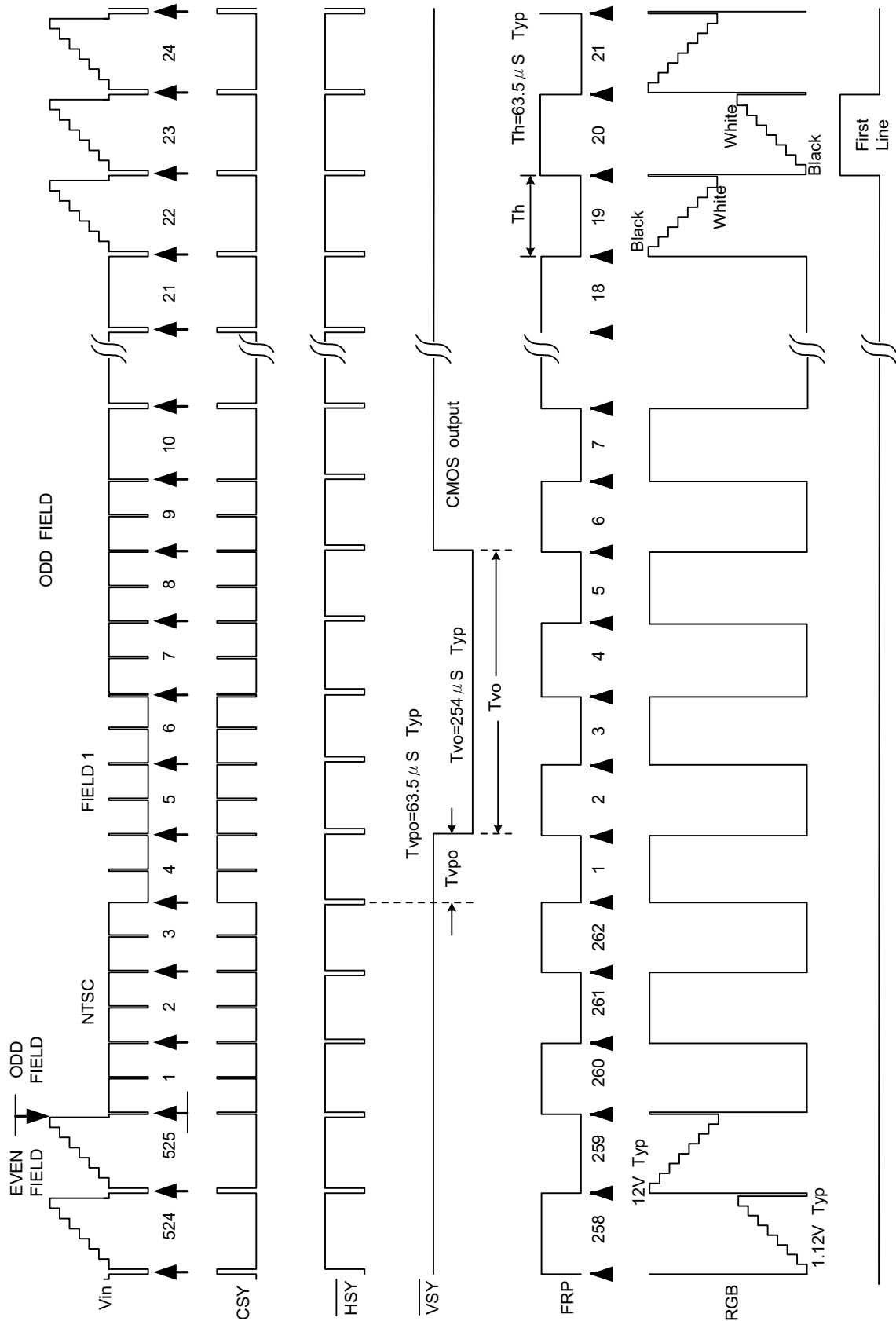
13.0 ~ 63.8 μ s .

b) Vertical

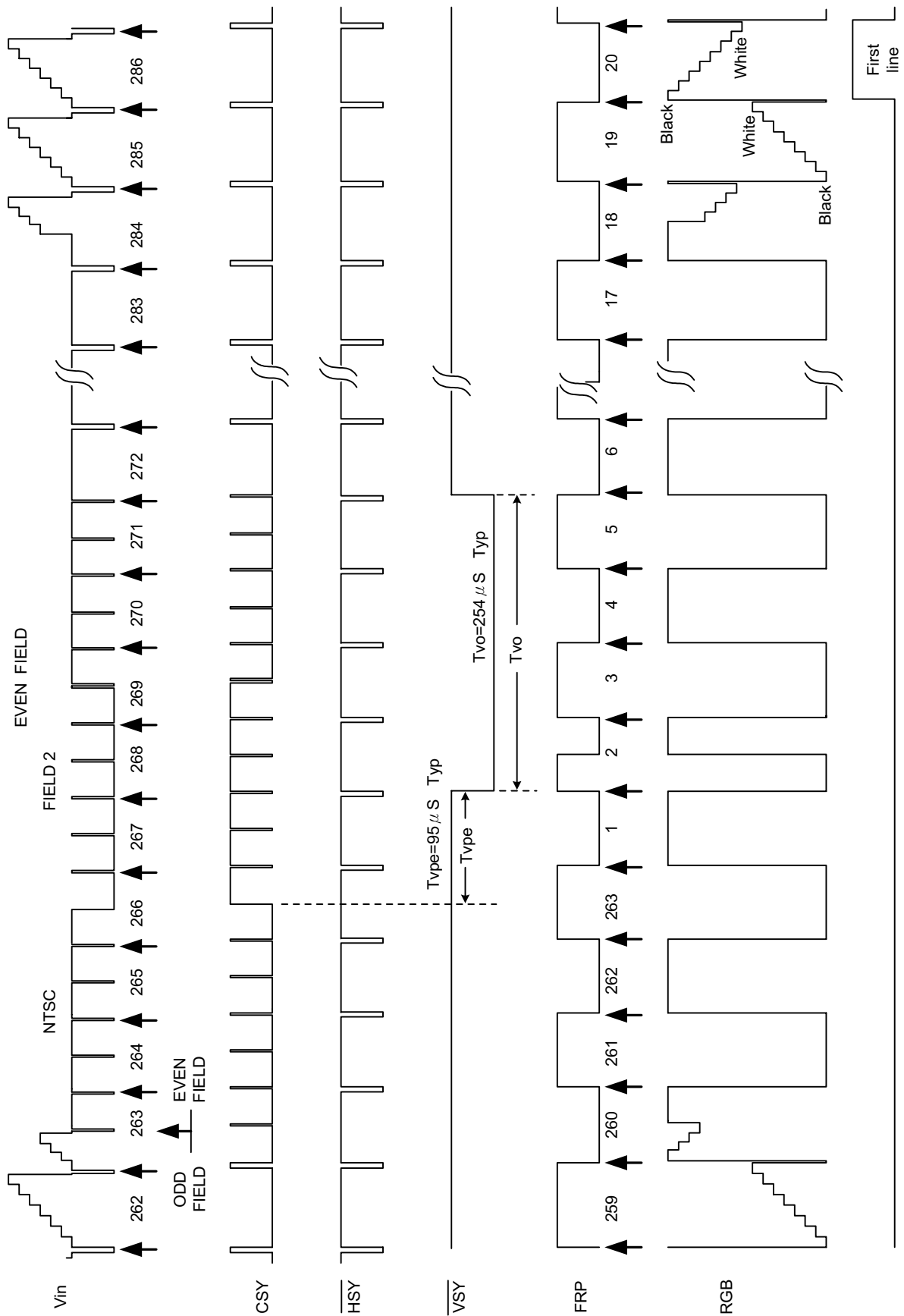
26 ~ 298 H

c) odd field : Scan lines $14n+17$ $14n+23$ ($n = 1, 2, 3..$) are not displayed.
 even field : Scan lines $14n+12$ $14n+20$ ($n = 1, 2, 3..$) are not displayed.





Timing chart of I/O and RGB signal



Timing chart of I/O and RGB signal

8.Optical Characteristics

8-1)Specification

Ta = 25°C

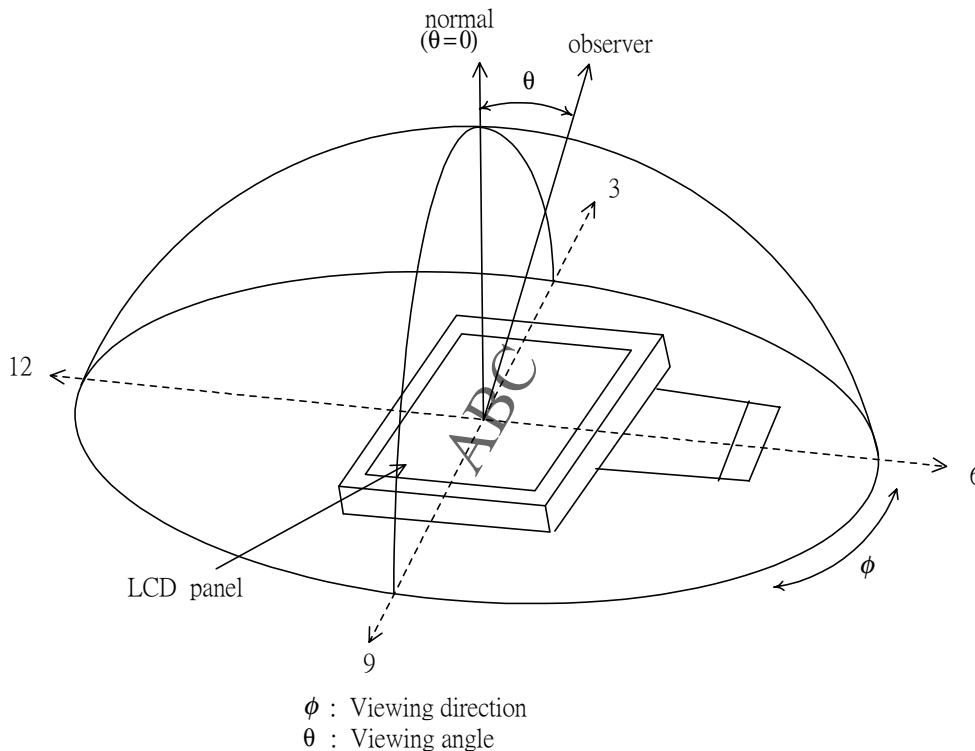
Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit	Remarks	
Viewing Angle	Horizontal	θ	± 45	± 55		deg	Note 8-3	
	Vertical	θ (to 12 o'clock)	$CR \geq 10$	10	15			deg
		θ (to 6 o'clock)		30	35			deg
Contrast Ratio	CR		80	120			Note 8-1	
Response time	Rise	Tr			30	ms	Note 8-4	
	Fall	Tf			50	ms		
Reflectance Ratio	R			2.0		%		
Brightness				200		cd/m ²	Note 8-2	
Lamp Life Time	+25°C		10,000			hr		

Note 8-1 : $CR = \frac{\text{Luminance when LCD is White}}{\text{Luminance when LCD is Black}}$

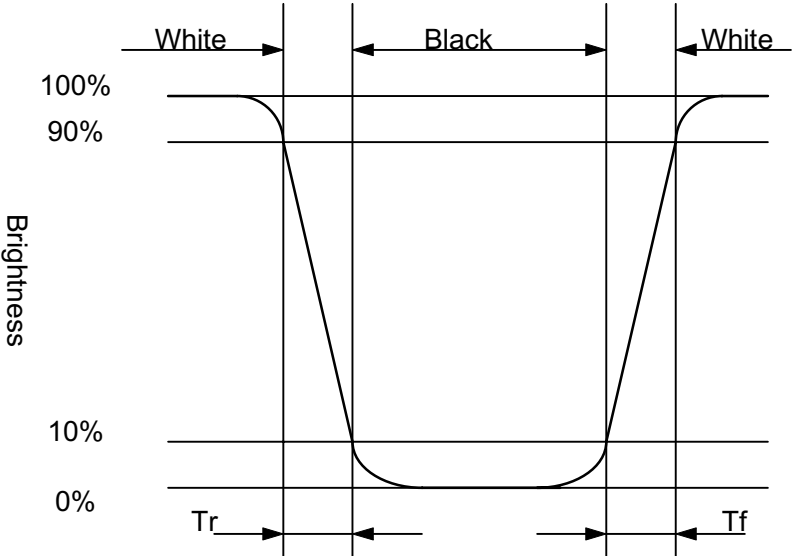
Contrast Ratio is measured in optimum common electrode voltage.
The test configurations of contrast ratio see section 8-2.

Note 8-2 : Topcon BM-7(fast) luminance meter 1° field of view is used in the testing (after 20~30 minutes operation).

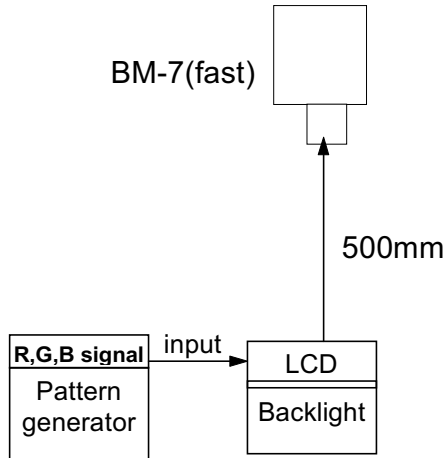
Note 8-3 : The definition of viewing angle diagrams :



Note 8-4: The definitions of response time:

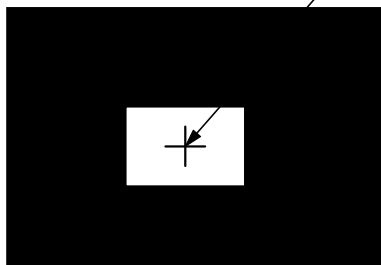


8-2) Test Configuration

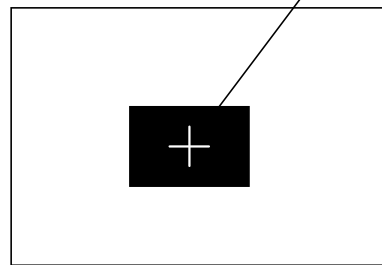


Caution: 1. Environmental illumination ≤ 1 lux
 2. Before test CR, Vcom voltage must be adjusted carefully to get the best CR.

- LCD Display Testing Point Testing Point

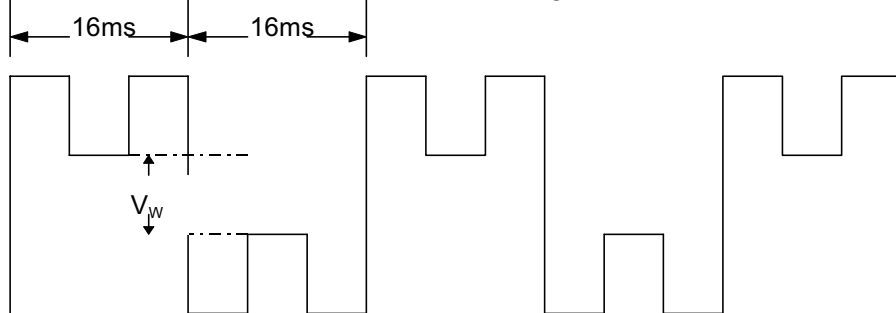


Pattern A



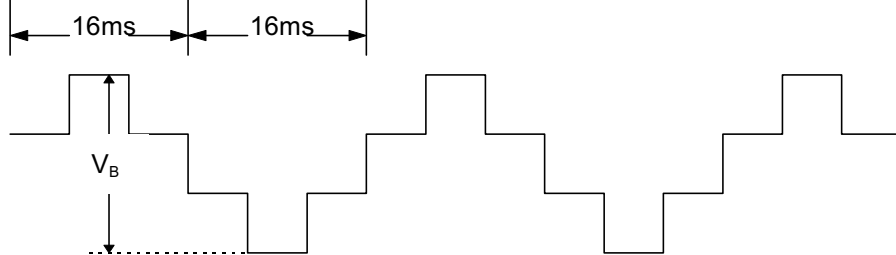
Pattern B

- R, G, B Waveform of Pattern A at Testing Point



$V_W = 2.2V \pm 0.2V$

- G, B Waveform of Pattern B at Testing Point



$V_B = 9.2V \pm 0.2V$

9. Reliability

No	Test Item	Test Condition
1	High Temperature Storage Test	Ta = +80 °C, 240 hrs
2	Low Temperature Storage Test	Ta = -30°C, 240 hrs
3	High Temperature Operation Test	Tp = +60 °C, 240 hrs
4	Low Temperature Operation Test	Tp = -10 °C, 240 hrs
5	High Temperature & High Humidity Operation Test	Tp = +60°C, 95%RH, 240 hrs
6	Thermal Cycling Test(non-operating)	-25°C → +25°C → +70°C, 200 Cycles 30 min 5min 30 min
7	Vibration Test (non-operating)	Frequency : 10 ~ 55 Hz Amplitude : 1.5 mm Sweep time: 11 mins Test period: 3 hrs for each direction of X, Y, Z
8	Shock Test (non-operating)	100G, 6ms Direction: ± X, ± Y, ± Z Cycle: 2 times
9	Electrostatic Discharge Test	150pF, 330Ω 10 times/point, 4 points/panel face

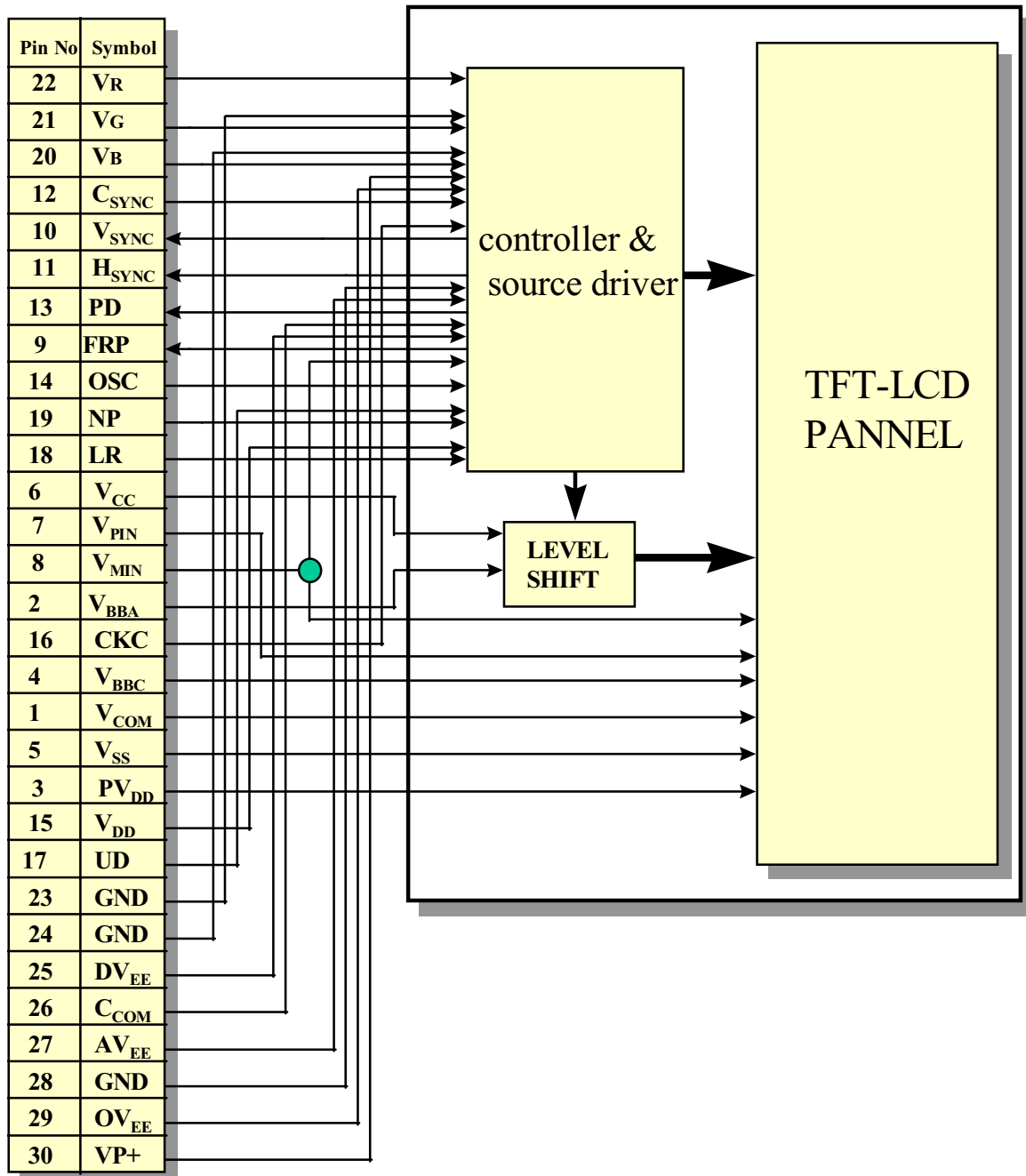
Ta: ambient temperature

Tp: panel temperature

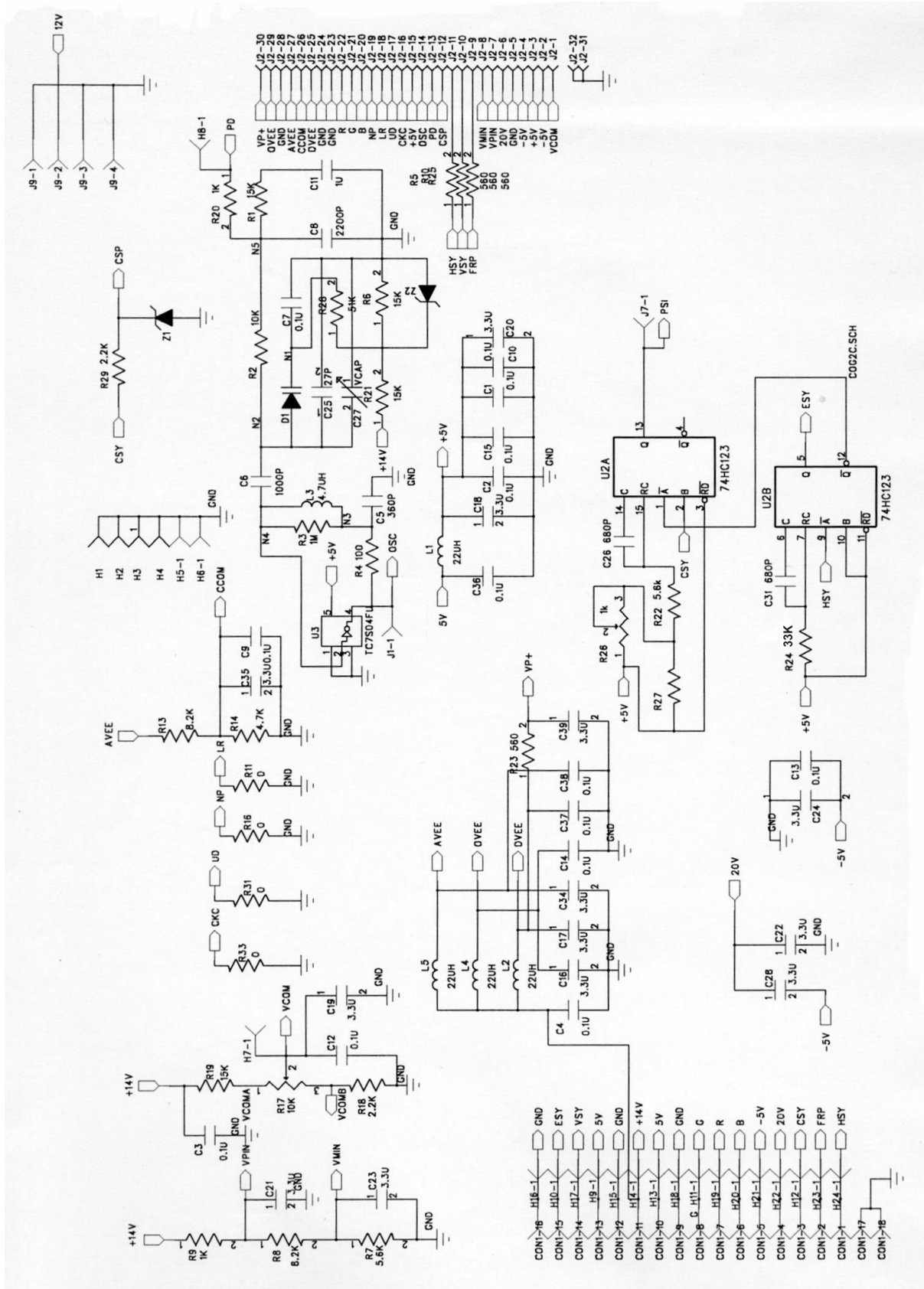
[Criteria]

Under the display quality test conditions with normal operation state, there should be no change which may affect practical display function.

10. Block Diagram



Appendix A: Interface Circuit

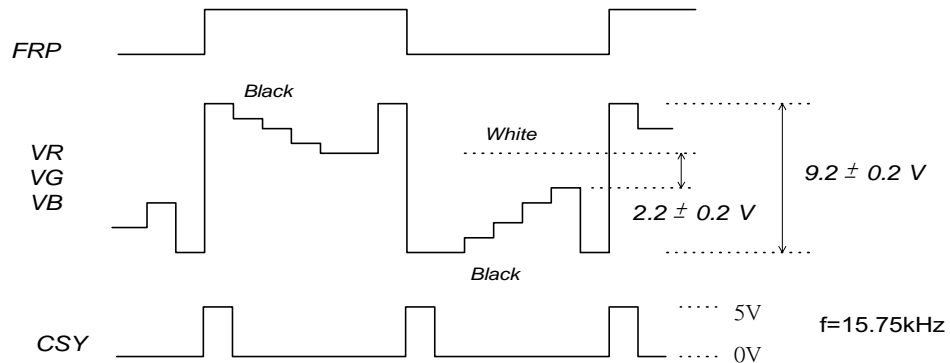


Description of the signal 16 pin connector on interface circuit

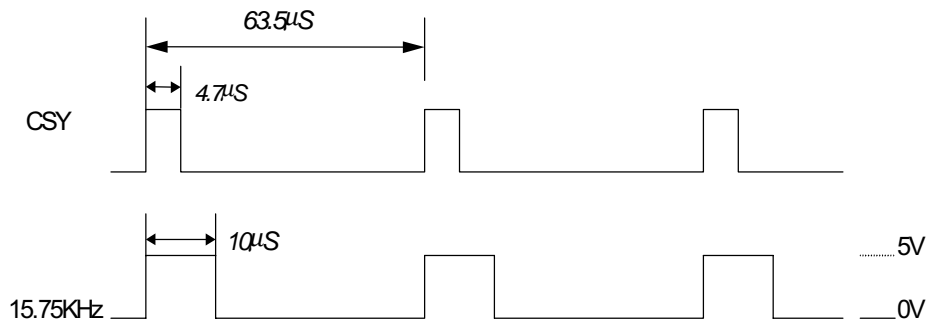
1.16 pin description:

Pin No	Symbol	I/O	Description	Remark
1	$\overline{\text{HSY}}$	I/O	Horizontal Sync. Input / Output	
2	FRP	O	Video Polarity Alternating Signal	Note 1
3	CSY	I	Composite Sync. Signal	
4	V _{GH}	I	Supply Voltage for Gate Driver (+20 V Hi level)	
5	V _{GL}	I	Supply Voltage for Gate Driver (-5V Low level)	
6	V _B	I	Specific Video Signal (Blue)	Note 1
7	V _R	I	Specific Video Signal (Red)	Note 1
8	V _G	I	Specific Video Signal (Green)	Note 1
9	GND	I	Ground	
10	V _{DD}	I	Supply voltage for controller (+5V)	
11	V _{SH}	I	Supply voltage for source driver (+14V)	
12	GND	I	Ground	
13	V _{DD}	I	Supply voltage for controller (+5 V)	
14	$\overline{\text{VSY}}$	I/O	Vertical Sync. Input/ Output	
15	PSI	O	Synchronize Pulse for Decoder	Note 2
16	GND	O	Ground	

Note 1:



Note 2: The frequency of PSI is 15.75KHz.



2. Recommended operation condition:

GND = 0V , Ta = 25 °C

Parameter	Symbol	MIN.	TYP	MAX.	Unit	Remark	
Supply voltage for source driver	V_{SH}	+13.5	+14	+14.5	V		
Supply voltage for gate driver	H Level	V_{GH}	+19	+20	+24	V	
	L Level	V_{GL}	-5.5	-5	-4	V	
Supply voltage for controller	V_{DD}	+4.7	+5	+5.3	V		
Input Signal voltage	H Level		+2.4	-	+5	V	Note 1
	L Level		-0.3	-	+0.8	V	
Output Signal voltage	H Level		+2.4	+4	+5	V	Note 2
	L Level		0		+0.5	V	

Note 1 : \overline{HSY} , CSY , \overline{VSY} ,

Note 2 : \overline{HSY} , FRP , \overline{VSY} , PSI,

3. Special components specification of the interface circuit

C27 : Variable capacitor (20pF)	Supplier : Kyocera
D1 : Variable capacitor diode (1SV214)	Supplier : Toshiba
U3 : IC TC7S04F	Supplier : Toshiba
Z1 : 5.1V Zenor diode	
Z2 : 6.2V Zenor diode	

Appendix B : Package Drawing

ZONE	REV.	DOCUMENT NO.	DESCRIPTION	DATE	REV.BY
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NOTE:

- One layer include: 1 piece of cushion sheet, 12pcs panel & 1 piece of tray.
- Q'TY: 96 pcs panel/carton.
- Dimension: 455*375*190mm
- Weight: 6.1KG

ITEM	PART NO.	DESCRIPTION	QTY	REMARK
6	50-0100091	CARTON INTERNAL	1	
5	50-0500041	開口袋450*380*700mm	1	抗靜電
4	P25EN1R001	P25EN1-...R	96	
3	50-0200003	EPE CUSHION SHEET	8	抗靜電
2	50-0300271	TRAY	9	抗靜電
1	50-0300151	FOAM	2	

MTL.SPEC.	UNSPECIFIED TOL'S ANGLE ROUGHNESS	REMARK	元太科技股份有限公司 Prime View International Co.,Ltd.
APPROVE	SCALE	UNIT	DWG.TITLE
CHECK			P25EN1-...R PACKING DWG.
DESIGN	陳萬典	07.07.99	MTL.NO. P25EN1R001 DWG.NO. M025-PA-A401 REV. 01 A4 SIZE

ZONE	REV.	DOCUMENT NO.	DESCRIPTION	DATE	REV.BY										
<p>NOTE:</p> <ul style="list-style-type: none"> 1.Q'TY:192pcs panel/carton. 2.Dimension: 480*396*405mm 3.Weight: 13.2KG 															
<table border="1" style="width:100%; border-collapse: collapse;"> <tr> <td style="width:5%;">ITEM</td> <td style="width:15%;">PART NO.</td> <td style="width:55%;">DESCRIPTION</td> <td style="width:10%;">QTY</td> <td style="width:15%;">REMARK</td> </tr> <tr> <td>7</td> <td>50-0100101</td> <td>CARTON EXTERNAL</td> <td>1</td> <td></td> </tr> </table>						ITEM	PART NO.	DESCRIPTION	QTY	REMARK	7	50-0100101	CARTON EXTERNAL	1	
ITEM	PART NO.	DESCRIPTION	QTY	REMARK											
7	50-0100101	CARTON EXTERNAL	1												
MTL.SPEC.		UNSPECIFIED TOL'S		REMARK											
		ANGLE													
		ROUGHNESS													
APPROVE		SCALE	UNIT	SHEET	DWG.TITLE										
CHECK				OF	P25EN1-...R PACKING DWG.										
DESIGN	陳萬典	MTL.NO.	P25EN1R001		DWG.NO.										
	07.07.99				M025-PA-A402										
				REV.	A4										
				01	SIZE										

元太科技股份有限公司
Prime View International Co.,Ltd.

Revision History

Rev.	Issued Date	Revised Contents
<i>Pre.</i>	<i>Feb. 22 1999'</i>	<i>Preliminary Specification</i>
<i>1.0</i>	<i>Sep. 29 2000'</i>	<i>The Interface circuit · Package drawing is added</i>